CRANFIELD UNIVERSITY

GHAITH ALI ABDUL-RAHIM

POWER CONTROL, FAULT ANALYSIS AND PROTECTION OF SERIES CONNECTED DIODE RECTIFIER AND VSC BASED MTDC TOPOLOGY FOR OFFSHORE APPLICATION

SCHOOL OF WATER, ENERGY AND ENVIRONMENT (SWEE)
HVDC Egineering

PhD
Academic Year: 2017 - 2018

Supervisor: Professor Patrick Luk
John Economou
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ABSTRACT

A multiterminal high-voltage dc (MTDC) system is a promising method for transmitting energy generated from an offshore windfarm (OWF). The creation of MTDC systems became easier by the introduction of voltage source converter (VSC) due to the flexibility and controllability it provides. This technology is newer than the line-commutated converter technology (LCC). Power systems can include any number of windfarms together with converters for both offshore and onshore power conversion. Therefore, this thesis suggests a three-terminal MTDC model of two offshore windfarms and one onshore inverter. The electric energy generated by the two windfarms is rectified into dc and transmitted to the shore using dc cable. Although a VSC or a diode rectifier (DR) can convert ac to dc, a series connection of a VSC and two DRs was proposed at the windfarm side to convert the generated power to achieve controllability of the uncontrollable diode rectifiers and reduces the high cost of additional VSCs. The proposed topology converts the ac power by dividing the windfarm power so that one-third is the share of the VSC and two-thirds is the share of the DRs. The same topology is used to convert the power produced from the other windfarm. Then, the dc power is transmitted via an undersea dc cable to the onshore location, and is then inverted into ac before it is supplied to the neighbouring ac grid using a grid-side VSC. The proposed topology has many advantages, including a significant save in windfarm VSC (WFVSC) capital cost and a significant reduction in the loss of power of the converter without losing the overall controllability. However, although this topology is suitable for windfarm applications, it might not be suitable for high-voltage direct current (HVDC) that requires bidirectional power flow unless making changes to the topology such as disconnecting the diode rectifiers.

Furthermore, fault analyses were investigated, including dc faults and ac faults. Ac faults are categorised as symmetrical or unsymmetrical faults. For comparison purposes, a Simulink model was designed, implemented, and simulated as a reference model. The reference model can operate as VSC-,

DR-based MTDC, or a mix of both in a way that any component can be added to or removed from the model at any time during the simulation run.

The contribution to the dc fault current from various parts such as dc capacitor and the adjacent feeder was investigated thoroughly, and detailed mathematical formulae were developed to compute fault current from these contributors. In addition, the results of the system response due to both fault types are illustrated and discussed. Both symmetrical and unsymmetrical ac faults were initiated on the onshore grid side, and the system response results are presented for those faults. A generalised control scheme (GCS) was proposed in this thesis, which add the ability the model to control the reactive power and is suitable for both balanced and unbalanced ac faults conditions.

A protection against faults was investigated and implemented using dc circuit breakers. The protection system was built to ensure safe operation and to fulfil the grid code requirements. Many grid codes are available and presented in the literature, such as Spanish, British, and Danish; however, a grid code by E.ON was chosen.

The protection scheme in VSC-based MTDC networks plays a vital role during dc faults. It is vital that this protection be sensitive, selective, fast, and reliable. Specifically, it must isolate the fault reliably from the system within a short time after the fault occurrence, while maintaining the remaining components of the system in a secure operational condition. For optimal performance, the protection scheme discussed in this thesis employs solid-state circuit breakers. A literature survey relevant to the tasks mentioned above was conducted.

Keywords:

HVDC, Offshore WindFarm, MTDC, VSC, Diode Rectifier. dc fault, ac fault, symmetrical fault, unsymmetrical fault, protection, DSC, DCCB, monopolar topology, VSC Control, symmetrical components, dual controller, bipolar topology, negative sequence dq

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LIST OF ABBREVIATIONS

ABB	ASEA Brown Boveri (Swiss multinational corporation)
abc	Subscript represents three-phase system, sequence a, b, and c
ac	Alternating current
ANPC	Active neutral-point clamped converter (with IGBT)
B2B	Back-to-back converter
BEIS	Department for Business, Energy, and Industrial Strategy
CB	Circuit breaker
CO_2	Carbon dioxide
CSC	Current source converter
CTL	Cascaded two-level converter
dc	Direct current
DCCB	Direct current circuit breaker
Δ	Three-phase delta connected system
DFIG	Doubly fed induction generator
dq	Direct and quadrature components, also called SRF
DR	Diode rectifier
DSC	Delayed signal cancellation
E·ON	European company; electric utility service provider
ESS	Energy storage system
Estlink	HVDC linking Estonia and Finland: $\pm 150\ kv$, 350 MW, 105 km
FB-MMC	Full-bridge multilevel modular converter
FC	Flying capacitor converter
FFT	Fast Fourier transform
FRT	Fault ride through
GCS	Generalised control scheme (strategy)
GCT	Gate-commutate thyristor
GSVSC	Grid-side voltage source converter
GTO	Gate turn off
GW	Gigawatt
HB-MMC	Half-bridge multilevel modular converter
HCB	Hybrid circuit breaker
HCS	Hill climb searching

HPF	High-pass filter
HVAC	High-voltage alternating current
HVDC	High-voltage direct current (transmission system)
HVRT	High-voltage ride through (connected with grid code requirements)
IEGT	Injection-enhanced gate transistor (semiconductor switch for VSC)
IGBT	Insulated-gate bipolar transistor (semiconductor switch for VSC or CB)
IGCT	Integrated gate-commutated thyristor (semiconductor switch for VSC or CB)
LCC	Line commutated converter
LPF	Low-pass filter
LV	Low voltage (usually distribution voltage level)
LVRT	Low-voltage ride through (connected with grid code requirements)
MAF	Moving average filter
MATLAB	Matrix Laboratory (software by MathWorks)
MeV	Medium voltage
MMC	Multilevel modular converter
MOV	Metal oxide varistor
MPPT	Maximum power point tracking
MRTB	Metallic return transfer breaker
MTDC	Multiterminal high-voltage direct current
MV	Megavolt
MVA	Mega voltampere
MW	Megawatt
MWh	Megawatt hour
NF	Notch filter
NGET	British grid code
NPC	Neutral-point clamped
OPWM	Optimised pulse-width modulation (optimised PWM)
OWF	Offshore windfarm
P	Active power
P&O	Perturb and observe
PCC	Point of common connection
PG	Pole-to-ground fault

PI	Proportional integral (controller)
PLL	Phase-locked loop (detect phase angle for VSC control)
PMSG	Permanent magnet synchronous generator
PP	Pole-to-pole fault
PPT	Point-to-point topology
PSF	Power signal feedback
PWM	Pulse-width modulation (VSC control signal with variable width of pulses)
Q	Reactive power (measured by unit var)
RLC	Resistance, inductance, and capacitance
S	Apparent Power $S = v * i^* = P + jQ$ (VA) (superscript $*$ means complex conjugate
SCR	Short-circuit ratio
SEPRI	Electric Power Research Institute
SPWM	Sinusoidal pulse-width modulation
SSB	Solid-state breaker
SRF	Synchronous reference frame (dq)
STATCOM	Static compensator (a VSC used for voltage enhancement)
SVM	Space vector modulation (used for VSC switching strategy)
SVPWM	Space vector pulse-width modulation (used for VSC switching strategy)
SWT	A model of wind turbine by Siemens
THD	Total harmonic distortion
TWh	Terawatt hour (equals $1*10^{12}$ Watt hour)
VA	Volt-ampere (apparent power unit)
VSC	Voltage-source converter based on IGBT, GTO, IEGT or IGCT
WECS	Wind energy conversion system (typically used in wind turbines such as B2B converter)
WFVSC	Windfarm voltage-source converter
WF	Windfarm power generator
WT	Wind turbine generator
XLPE	Cross-linked polyethylene cable insulator
Y	Three-phase star connected system
Y/Δ	Primary star secondary delta connected transformer

pu	Per unit quantity
rms	Root mean square value
rpm	Revolutions per minute

LIST OF SYMBOLS

abc	Subscript represents three-phase system, sequence a, b, and c
ac	Alternating current
B	Susceptance equal to $1/X$
bac	Superscript denoting backward component
C	Capacitance (F)
c	Speed of light in free space ($\approx 2.99 \times 10^8\ m \cdot s^{-1}$)
$C_i(s)$	PI controller transfer function in the s domain $= K_p + \frac{K_i}{s}$
C_{ix}	Inner current controller and subscript x=1 for d-axis, x=2 for q-axis
C_{ox}	Outer controller and subscript x=1 for P or dc voltage, x=2 for Q
d	Duty cycle
d_m	Duty cycle of MMC submodule
dc	Direct current
dq	Direct and quadrature axis reference frame
$\frac{\Delta V}{\Delta I}$	Droop voltage characteristic slope (V/A)
$erfc$	Complementary error function
f	Frequency (Hz)
$\mathcal{F}^{bac}$	Arbitrary backward constants
$\mathcal{F}^{for}$	Arbitrary forward constants
f_{max}	Highest frequency of transmission line that can be simulated (Hz)
f_o	nominal frequency of the grid (Hz)
f_{sw}	Per phase leg effective switching (total) frequency (Hz)
f_{swc}	Switching frequency of a cell (Hz)
for	Superscript denoted forward component
G	Conductance equal to $1/R$ (siemens [S] or mho)
I	Dc current (A)
i	Ac Current (A)
i_c	Dc capacitor current contributions (A)
i_f	Adjacent feeder current contributions (A)
I_d^*	Direct (d-axis) reference current (pu)

$I_o(\cdot)$	Modified 0-order Bessel function
I_q^*	Quadrature (q-axis) reference current (pu)
I_d	Direct (d-axis) measured current (pu)
I_q	Quadrature (q-axis) measured current (pu)
j	Complex number equals $\sqrt{-1} = 1\angle 90°$
$k(s)$	Propagation constant
K_1, K_2	Converters 1 and 2, dc voltage characteristic slopes, respectively
K_i	Integral gain constant of a PI controller
K_p	Proportional gain constant of a PI controller
L	Inductance (measured in H)
l	Total line length (m)
$\mathcal{L}^{-1}$	Inverse Laplace transform
m	Modulation index (unitless)
μ	Permeability for free space equals $\mu_o = 4\pi \times 10^{-7}$ H/m
μF	Measuring unit of capacitance (microfarad)
n	Transformer turn ratio
N	Total number of converters
$\mathbb{N}$	Number of sections in equivalent circuit of a transmission line
N_{mmc}	Number of submodules of MMC
$\circledast$	Convolution integral
P	Active power (Watt)
p	Number of poles (unitless)
P_t	Total time period for duty cycle calculation (time unit)
pu	Per unit system equals the actual quantity divided by a base value
Q	Reactive power (VAr)
R	Resistance (Ω)
R_c	Characteristics resistance (Ω)
R_f	Fault resistance (Ω)
rad	Angle unit equals 57.296° circle arc that equals its radius
rms	Root mean square value of voltage or current
S	Apparent Power $S = v * i^* = P + jQ$ (VA) (superscript $*$complex conjugate
s	Laplace s-domain

$\emptyset$	Skin effect factor
t	Time (s)
T	Time when the converter is on (unit time)
T_c	Transmission coefficient
T_s	Sample time
$u(t)$	Unit step function
v	Ac voltage (volt)
V	Dc Voltage (volt)
V_{dc_g}	No-load dc voltage
V_c	Amplitude of the rectangular control signal (volt)
V_{car}	Carrier signal amplitude (volt)
V_{Csm}	MMC submodule dc bus voltage (kV)
V_{dc}	Dc voltage of the converter (volt)
v_{fo}	Midpoint voltage value before filtering process (volt)
V_o	Output voltage of converter cell (volt)
V_{pcc}	Magnitude of the voltages at PCC
V_{ph}	Maximum value of the rectified phase voltage (volt)
$v_{ph}(t)$	Instantaneous value of voltage (volt)
V_{vsc}	Magnitude of the voltages at WFVSC
W_e	Stored energy in the capacitor
X	Reactance (imaginary part of impedance) $X = 2\pi fL = \frac{1}{2\pi fC}$ (Ω)
x	A point along transmission line (unit length)
Y	Admittance equals $1/Z = G + jB$ (B is the substance=$1/X$)
y	Average output of a function over a time period
γ	Damping factor of transmission line; equals $(\aleph - \beta)/2$
$*$	Superscript represents reference value
Z_c	Characteristic impedance of transmission line
$(.)^{-1}$	Inverse of function
α	Firing angle (unit angle)
β	Capacitive damping factors
γ	Propagation speed $\gamma = 1/\sqrt{LC}$
$\Gamma(s)$	Reflection coefficient in s domain

$\delta(t)$	Dirac function
δ_d	Converter voltage drop requirement (typically is less than $0.05\ pu$)
ε	Distortion factor
ε_o	Free space permittivity equals $\varepsilon_o = 8.85\ \times 10^{-12}$ F/m
ζ	Capacitor damping (typically, 0.707 affords adequate performance)
θ	Angle difference between the voltage phase of two nodes
μ	Damping factor of transmission line; equals $(\aleph + \beta)/2$
π	Pi, equals 3.1416
Π	Transmission line equivalent circuit using RL series resistance and inductance and two shunt capacitances
τ	Time constant (s)
τ_C	Dc capacitor time constant; equals CR_c
Φ	Skin effect
ω	Angular velocity (rad/s)
Ω	Resistance (ohm)
ω_c	Dc voltage controller bandwidth (typically $\approx 2\pi * 20\ rad/s$ =20 Hz)
$\aleph$	Inductive damping factors
Z	Impedance (equals $R + jX$ where X relates to L or C) Ω

1 INTRODUCTION

Electrical energy has a significant importance in the everyday lives of people and it has been used in various fields such as heating, cooling, cooking, and transportation since its introduction in the late 19th century [1, p.9]. Internationally, the energy shortage and global climate change, due to carbon dioxide (CO_2) emissions from oil, natural gas, and coal or fossil fuel, are two major challenges. Great effort has been made to add more clean energy sources to energy generation. Wind energy, which is energy that can be obtained from wind with the aid of wind turbines, arguably can be regarded as the most developed and economical technology among the renewable technologies. Wind turbines can be installed either offshore or onshore and connected together to constitute a windfarm (WF). Figure 1-1 and Figure 1-2 illustrate offshore and onshore windfarms respectively.

Figure 1-1 Sheringham Shoal Offshore Windfarm, England [2]

Figure 1-2 Onshore windfarm [3]

Power generated from the wind has witnessed rapid increase in Europe during the last decade. Figure 1-3 illustrates the total cumulative and annual installed generation power capacity in megawatts from 2001 to 2016. European countries have different percentages of installation. The UK, for example, has the biggest share (43%) among the countries in Europe, as shown in Figure 1-4 and Germany is the second with 34% [4].

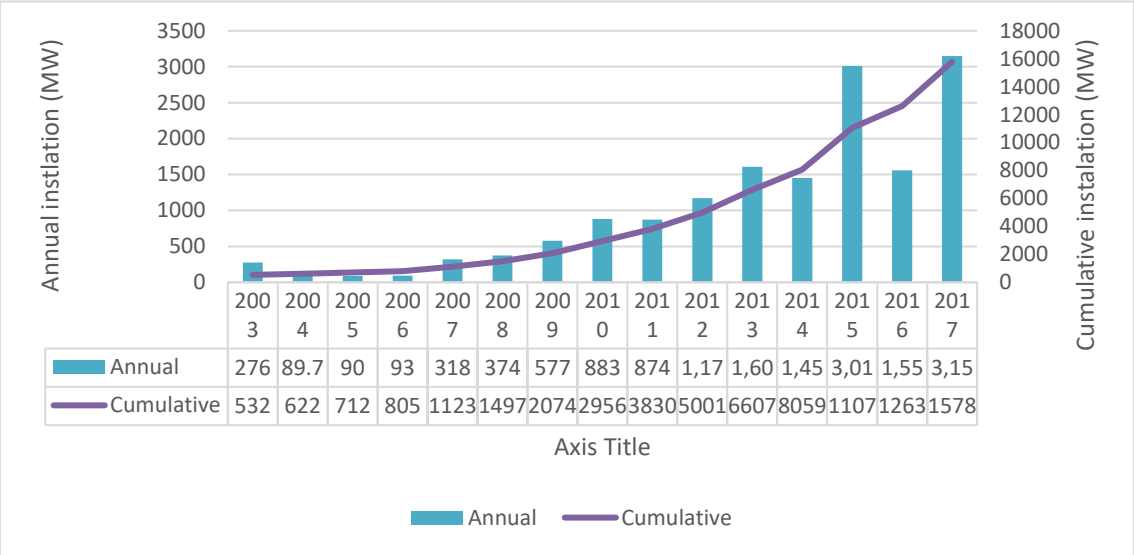


Figure 1-3 Annual and cumulative offshore wind installation (MW) [4]

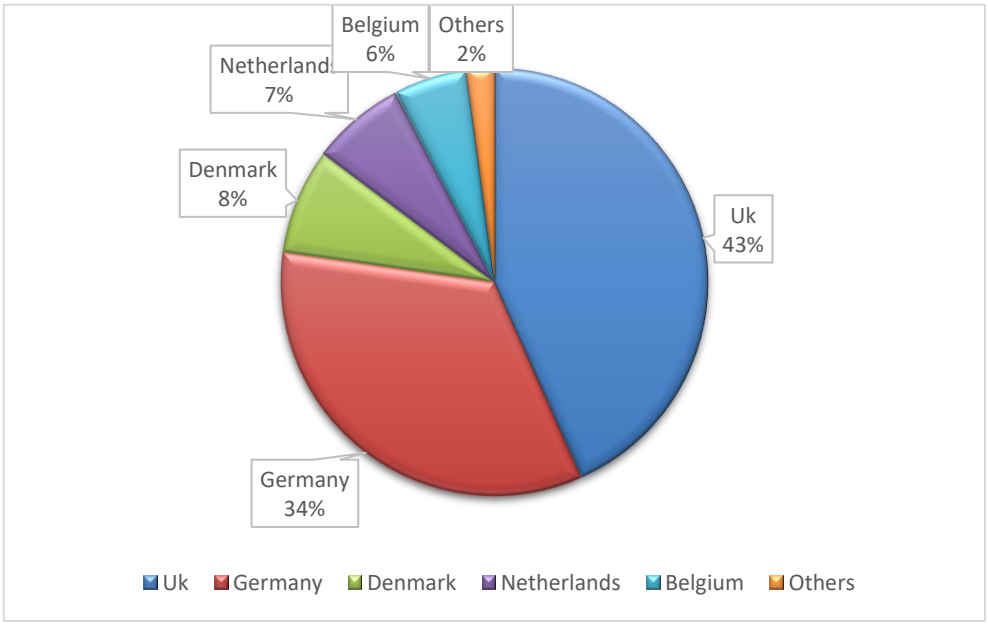


Figure 1-4 Cumulative installed offshore generation capacity (MW) by country [4]

In the UK, for example, a total energy of more than 48.64 TWh yearly (with power of 18.4 GW[1]) is being produced from the wind. This amount is enough to supply approximately 12.4 million houses[2]. However, the offshore wind energy share is 16.7 TWh, which is equivalent to 6.36 GW. This energy is calculated to save about 20 tonnes of CO_2 annually [5].

A scenario in Europe was planned to reduce the CO_2 emission by building new wind generation sources. The scenario contains a reduction of CO_2 emissions by approximately 20% in 2020 [6, p.53], 30% in 2030, and 50% in 2050; the wind energy will be an essential part in this plan [7].

Historically, the world's first commercial high-voltage dc power system, used for lighting, was implemented employing direct current (dc) by Thomas Edison in 1882 [8]. The dc voltage was 110 V and was provided to fifty-nine customers in Pearl Street in Lower Manhattan. Danes introduced the first utilisation of a wind turbine to generate electricity in 1890 [9,10, pp.17–23]. Due to the difficulties in the conversion system and stepping the voltage up and down, research was very slow. Historically, the first commercial HVDC (high-voltage direct current) was installed in Gotland, Sweden in 1954 [11,12,13, p.129]. The system featured mercury-arc valves, which were based on line commutated converters LCCs [14, p.7]. In 1972, semiconductor devices were first used as switching devices to replace the mercury-arc valves by introducing a thyristor as a switching device [15, p.1]. A converter that uses a thyristor is termed a current sourced converter (CSC) [16]. Because it employs line commutation, it can be called a line commutated converter (LCC). Using a thyristor-based converter presents various advantages, including low cost, the ability to regulate the firing angle of thyristors continuously [17], and the ability to transmit a high power of approximately 10 GW with a rated voltage of ±1.1 MV [18]. However, LCCs cannot be connected to a weak power system [1], and power reversal requires

[1] This is calculated by multiplying the installed capacity (MW) x 8760 (hours per year) x 30.1% (long-term average load factor, BEIS).

[2] For example, if installed capacity is 16.7 MW, load factor is 0.301, hours/year is 8760, and average annual consumption is 3.9 MWh, then 18.4 GW x 8760 x 0.301 *1000/ 3.9 MWh = 12.4 homes powered equivalent.

changing the voltage polarity with the aid of mechanical switches [19]. Both [20] and [21] found that proper commutation of LCC converters require an SCR (short-circuit ratio) of greater than 1.5. Weak power systems with SCR less than 1.5 require the installation of synchronous condensers to increase the system capacity (short-circuit ratio capacity) [22].

However, power systems that have an SCR between 2 and 3 are categorised as weak, while those with an $SCR < 2$ are very weak [23,24]. Thus, the weaker the power system, the lower the short-circuit ratio, and the greater the ac/dc interaction [25].

The above disadvantages can be overcome by using a newer technology called voltage-source converter (VSC) [26,27], which uses either insulated gate bipolar transistor (IGBT) or gate turn-off thyristor (GTO) as switching device [28,29]. Such semiconductor devices typically use components inside the converter themselves. Therefore, such converters use self-commutation and the converter is known as a self-commutated converter [30,31]. VSCs were first introduced on 10 March 1997 to link Hellsjon and Grängesberg, in Sweden, to transmit 3 MW over a 10 km distance, and operate at ±10 kV [32,33].

This promising technology has several advantages such as black start, which is the ability to connect and supply a weak and passive network [34,35]; good controllability [36,37]; fast transient response [38–40]; reduced footprint [41,42]; and ability to simultaneously and independently control both reactive and active power [43,44]. HVAC has been widely used for transmission and distribution of electric power [45], but advances in semiconductor technology have made HVDC less expensive [46,47]. The break-even distance for an HVDC with overhead dc lines to be less expensive than an HVAC system is about 600 km (approximately 400 mi) [48,49] and approximately 50 km for submarine or underground cable depending on transmitted power level [50,51, pp.18–27]. Figure 1-5 compares the capital cost and cost due to power losses of both dc and ac [52]. The figure clearly shows that a shorter ac line is less expensive than a dc line because of the difference of terminal equipment, where the transformers cost less than that of the converters. However, with increasing

distance, this cost will be less because dc transmission lines have a simpler shape and require much less distance between conductors, as shown in Figure 1-6 [53]. Generally, transmitting electrical power using high voltage will require smaller line cross-section and reduce the loss of the power in the transmission line (copper loss) due to the current flow. However, it will increase the required insulation cost and will necessitate bigger towers to increase the space between conductors.

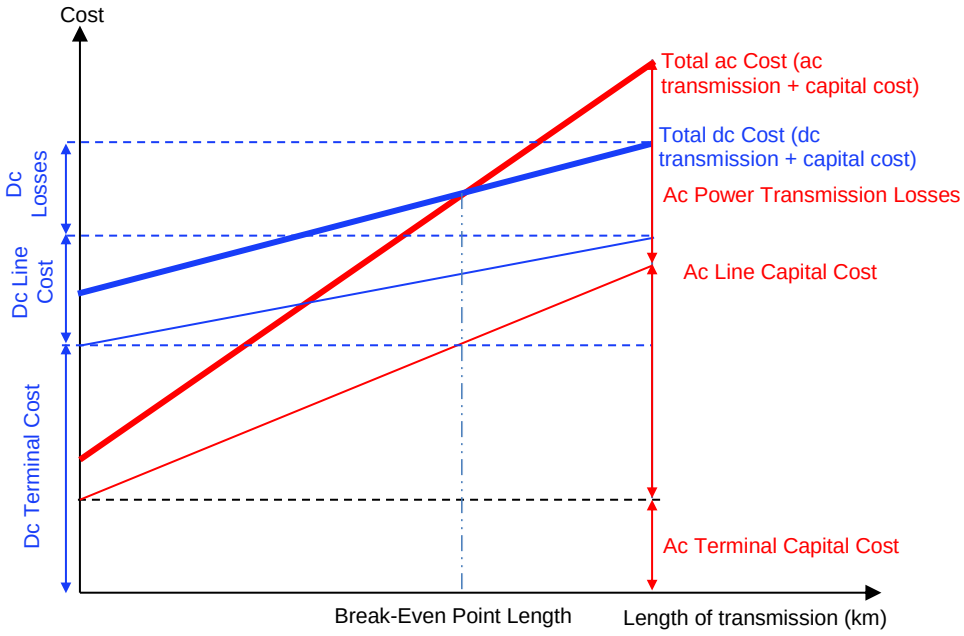


Figure 1-5 HVDC and HVAC cost comparison (both structure capital cost and power transmission cost) [52]

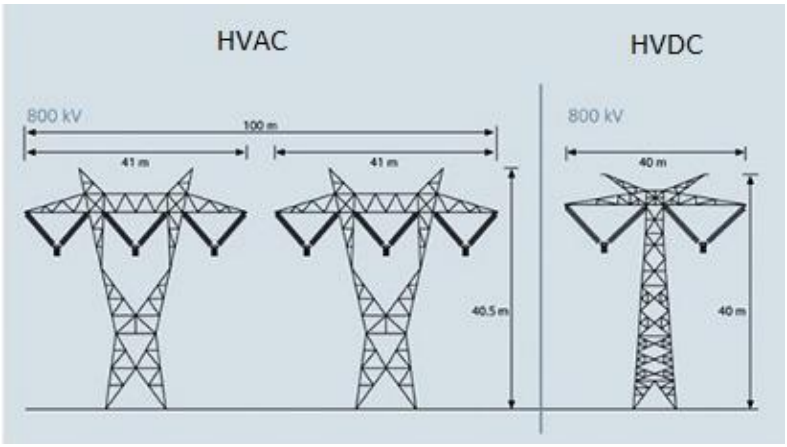


Figure 1-6 Transmission line structure comparison of HVAC and HVDC [53]

Due to the aforementioned advantages of VSCs such as flexibility and controllability, VSC technology has become the preferred technology over LCC [54,55], and HVDC construction for multiterminal high voltage dc (MTDC) networks becomes easier due to the bidirectional power control [41,56]. The MTDC network increases reliability and flexibility of power transmission systems [57]. Generally, IGBTs or GTOs are the switching devices in the VSC [28,58]. GTOs can pass higher current but less voltage for the same amount of power [28] and with a relatively slow (low-frequency) switching rate, but pulse-width modulation (PWM) still usable [59]. Although the system can be made completely from diodes [60,61], in that case the system would lose its advantage of controllability.

HVDC have many advantages over HVAC and can be summarised in the following, which encourage the use of HVDC over HVAC:

1. Large amount of power can be transmitted using HVDC system; today's HVDC technology can transmit more than 10 GW [18].
2. Power can be transmitted over long distances with dc [62].
3. Two or more power systems with different frequencies can be connected using dc link [63].
4. Power transmission loss is less for dc than for ac because of higher ac resistance due to skin effect and charging current [48,64].
5. No reactive power loss occurs due to capacitance in cables; hence, reactive power compensation is not required [65].
6. Fast change of energy direction is possible with bidirectional capability [66].
7. Ground can serve as return, and each conductor may be used as an independent circuit [48].
8. Concerning economic considerations, HVDC transmission is less expensive than ac for long distances; dc lines, cables, and towers are less expensive than for ac. The break-even distance is about 400 miles for overhead line and about 50 miles for cable (see Figure 1-5 and Figure 1-6) [67].

1.1 HVDC Technology

1.1.1 Converters

The basic and the most important element in any offshore windfarm is a converter such as VSC [68]. Wind turbines typically require two converters to convert the variable wind turbine ac voltage output into dc and invert it back into fixed ac voltage again [69]. This arrangement helps to stabilise the wind turbine ac output. Therefore, the voltage, frequency, and phase of the wind turbine is fixed [69], without the need for a gear box. The wind turbine, in this case, is called a variable speed wind turbine [70], and the machine is direct-driven [71,72] with either doubly fed induction generator (DFIG) or permanent magnet synchronous generator (PMSG) [73]. Converters are used either as ac/dc, dc/dc, dc/ac, or ac/ac (such as back-to-back “ac/dc/ac” converter or matrix converter “ac/ac” [74]). However, based on commutation technology, the available commutation processes are line commutated converters (LCC), capacitor commutated converter [75,76, p.127], self-commutated converter [30], or forced commutated converter [77].

1.1.2 Line Commutated Converter

This type of converter is generally called classic technology and is considered a mature technology. Most working HVDC systems today use this technology [76, p.122]. CSCs are usually based on line commutation (line commutated converter, LCC), which needs the ac system line voltage that is connected to the converter in its operation in the conversion process to perform the commutation from one valve to its neighbour. A LCC is constructed from a thyristor [78], which can be turned on (but not off) by a trigger pulse. Practically, before 1972, all LCC HVDC systems were mercury-arc valves. Thyristors were used for the first time in 1972 and are still used today. A current source converter, in its rectifier and inverter mode, absorbs reactive power. Hence, it needs a reactive power compensation [76, p.122]. Since the current direction cannot be changed, power flow reversal must be accomplished by inverting the dc voltage polarity of both poles of a station [79]. Figure 1-7 shows the world’s first commercial HVDC in Gotland

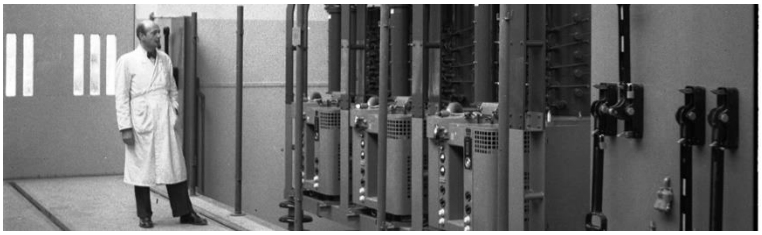


Figure 1-7 The world's first commercial HVDC Gotland [80]

1.1.3 Voltage-Source Converter

This type of converter uses semiconductor switches that have self-commutation ability. These switches can be integrated gate-commutated thyristor (IGCT), gate turn-off thyristor (GTO),or insulated gate bipolar transistor (IGBT) [81]. IGBT has more popularity in most HVDC projects than the other switching devices. Unlike a thyristor, this type of switch can be turned off and turned on as required, which gives a second degree of freedom over a thyristor, which can be turned on but not off. Several types of VSCs were investigated in the literature. The voltage level of a VSC can be a base to classify VSCs, such as 2-level (or six pulse), 3-level (or twelve pulse), and multilevel, or can be classified based on their structure, for example flying capacitor (FC) [82], neutral point clamped (NPC) [83], active-NPC (ANPC) [84], or multilevel modular cascaded converter (MMC) [85,86]. More information about multilevel converter types can be found in [87].

The following table summarises the differences between the classical converter technology and VSC technology.

Table 1-1 HVDC technologies comparison (thyristor and VSC)

Function	Classic HVDC	VSC HVDC
Switching valves	Mercury-arc, Thyristor	IGBT, GTO, IGCT
Connection to ac grid	Strong grid	Connection weak or passive grid [3] [1]
Control	Control P and consume Q	Control both P and Q independently in both directions
Power flow reversal	Require changing the voltage polarity	Easily
Ac filter	Yes	Yes
Minimum SCR	>2	0
Black start ability	No	Yes
Introduction year	1954 (and thyristor 1972)	1997
Rating (max)	± 1.1 MV, 10 GW [18]	± 326 kV, 1400 GW [88,89]

1.1.4 HVDC Topologies

Based on the dc link that transmits the electric dc power using a dc cable or an overhead transmission line which connects the rectifier and the inverter, HVDC is categorised into several topologies: monopolar, bipolar, homopolar, back-to-back, and multiterminal [76, pp.120–123]. Bipolar and homopolar systems have the same arrangement except the current direction in the second cable of the homopolar is opposite to that of the first cable, which means both cables have positive voltage, while in the bipolar transmission system one cable (pole) has positive polarity and another one with negative polarity. However, the homopolar topology is not used in practice because the return current is twice the rated current of the cable [90, p.19]. An HVDC system can be implemented as a point-to-point topology (PPT), general ring topology, star topology, or central switching ring in star topology. More details on the subject are presented in chapter 2.9.

[3] Ac systems are considered as weak based on two criteria: (1) if the impedance is high and (2) if it has low ac system inertia. This can be translated to define the term short-circuit ratio (SCR), which is dependent on the grid SCR, and can be very weak ($SCR < 2$), weak ($2 \leq SCR \leq 3$), or strong ($SCR > 3$).

1.2 Fault Analyses

Fault analysis studies have significant importance in MTDC networks because faults might cause destructive results to the entire system. There are various types of faults in the dc side, including short circuit connecting the two conductors of the poles. Such a faults is called pole-to-pole (PP), or the fault is short circuiting the pole to the ground, which is pole-to-ground (PG) fault that occurs in the cable or overhead line [91], can all present a major hazard to the system. PG faults occur when either the negative or the positive conductor (pole) is short-circuited to ground, whereas PP is a short circuit connecting the positive and negative poles. However, the transient results from a variety of sources in MTDC systems, not just PP or PG. Surges can be a result of lightning strikes, switching device operation, and dc voltage change due to terminal loss. PP faults are considered to have the most severe effects [92] on the nearby network, but generally, PG faults occur more frequently than PP faults [93].

A VSC is vulnerable to dc faults because in the case of dc faults, the capacitor will discharge and contributes to the current of the fault. Moreover, during the dc fault, the freewheeling diode will continue to conduct the entire ac current after blocking the IGBT [92]. Throughout the fault, the current increases substantially within a few milliseconds, which can damage the capacitor, freewheeling diodes of the IGBTs, and also possibly the complete VSC station [93]. Thus, the protection studies against dc faults in VSC-based MTDC networks is crucial.

Faults could occur in the ac grid—this type of fault is a major cause of power systems transients and can be disastrous for equipment connected to that network. Although ac faults are classified as either symmetrical or unsymmetrical, the latter is more common. An unsymmetrical ac fault is a fault that includes one or two phases to ground, and in this fault type there will a negative sequence. Many authors have studied the control of VSC unbalanced operating conditions, which causes the negative sequence to appear in the voltage. Therefore, a dual current control for the converter is addressed in the literature [94–103].

1.3 Fault Detection and Protection

A protection scheme [104] in VSC-based MTDC networks plays a vital role during dc faults. It is crucial that this protection be sensitive, selective, fast, and reliable. Specifically, it must isolate the fault reliably from the rest parts of the system within few milliseconds after the existence of the fault and the detection signal is received, while maintaining the remainder of the system in a secure operational condition [105].

HVDC systems that based on VSC are vulnerable to dc faults due to the large dc current of the capacitor which discharge approximately instantaneously and contribute to the fault current. Therefore, fault current interruption before it exceeds the limit values of connected equipment is important, and this action requires a rapid fault-detection algorithm and fast circuit breakers. Typically, fault detection algorithms [106] need measurement devices to detect voltage collapse, overcurrent, and frequency fluctuations. A distance-evaluating calculation is conducted simultaneously to compare the voltage [104]. However, accurate fault detection depends on a communication network that provides information about the system status at different parts which may be distant from each other. Protection system can be implemented without the need for using distant relay communication as proposed in [104]. The time for this process (i.e. from the fault occurrence to the interruption of the fault current) should be short enough to prevent equipment damage, and generally it is less than $5\ ms$ [107]. This time includes the fault detection and the circuit breaker response times. Today's technology can provide circuit breakers that respond in $2.5\ ms$ [108].

1.4 The Aim and Objectives of Thesis

1.4.1 Aim

The present work aims to propose a control of power generated from offshore windfarms based on a multiterminal HVDC using a series connection of VSC and diode rectifiers. Also, to analyse dc and ac fault characteristics and to design, implement and simulate protection algorithm that is able to detect,

locate, and isolate the faulty part to protect the proposed model against such faults.

1.4.2 Problem Description

Two technologies are available to create an HVDC: LCC and VSC. Importantly, VSC that is based on self-commutated semiconductor devices such as IGBT or GTO can overcome difficulties experienced with LCC. Although LCC can be used with bulk dc power, VSC can supply weak networks and has black start ability, and power direction reversal is an easy task. However, VSC have high cost compared to LCC. Diode rectifiers typically are more reliable and lower in cost compared with LCC and VSC and have been suggested in the literature, but they lack controllability. A model achieving the aims of controllability while reducing the cost of the system was suggested for HVDC system with a point-to-point system by Nguyen et al. in 2014 [109]. The model included a series connection of a VSC and two diode rectifiers, with each rectifier rectifying one-third of the total generated power. In this case, according to Nguyen et al., the cost of the gate drive can be reduced to 53.47% by using this configuration [109]. Moreover, this converter topology improves efficiency to 99.07%, rather than 98.4% achieved by the traditional technology [109]. Although that work was applied for a point-to-point system, the application for a multiterminal HVDC requires special attention to ensure efficient transmittal of the offshore windfarm power generated to the ac grid. Thus, the current work aims to use that topology in a three-terminal MTDC. The series connection makes the terminal voltage rise at the dc busbar in the dc side cable, similar to a series connection of batteries, which in turn will reduce the amount of insulator required for the transformer that supplies the converter and the diode rectifiers.

The proposed model was designed ─with idea of keeping it general─, implemented, and operated based on the proposed converter topology using MATLAB/Simulink to assess its operation under both normal and abnormal (fault) conditions. Several types of faults can be found on the MTDC network—they occurred either on the ac side or on the dc side. The dc side faults can occur and short-circuit the positive pole to the negative pole at any location, or a

short-circuit can connect the ground to the positive or the negative pole, which is called a pole-to-ground fault. A cable model was designed and implemented to include all these types of faults. Conversely, at the ac side, ac faults can be divided into symmetrical balanced or unsymmetrical faults. A symmetrical fault (also called balanced fault) includes all three phases. However, a symmetrical fault can include one phase or two phases to ground. A negative sequence component is present in the unsymmetrical fault. Thus, an unbalanced fault requires special attention to account for the negative sequence, and therefore, a dual current control was proposed in the literature. The dual control scheme is unable to control the reactive power. Therefore, a generalised control scheme model, such that the outer loops is able to control reactive power (Q) and dc voltage (V_{dc}), which was proposed, designed, implemented, and operated in this thesis.

Low voltage ride through (LVRT) is an important and challenging issue in dealing with the wind turbine behaviour during the fault conditions to assess the compliance of the model with the grid code requirements. Therefore, this subject must be issued in the Simulink model to protect the wind turbine while operating in severe conditions and to ensure it obeys the grid code requirements. LVRT requires a fault-detection procedure for both dc cable faults and onshore ac grid faults.

Wind turbines face variable wind conditions. Therefore, for each wind speed there is an optimal value of torque production. Thus, it is necessary to follow these changes in wind speed according to predefined optimal values of performance coefficient (C_p). This procedure is known as MPPT.

1.4.3 Objectives

To achieve the goal of finding a three multiterminal HVDC that reduces the cost while overcoming the uncontrollability of the diode rectifiers, the following objectives were proposed. The objectives are summarised as follows:

- To explore various topologies of multiterminal HVDC and HVDC transmission topologies to select the appropriate one based on its impact on the model

performance under fault and normal conditions. Other considerations, such as cost and the ability for future upgrade, will be examined.

- To design and implement converter control at windfarm side (WFVSC) and at grid side converter (GSVSC) that work under normal and abnormal conditions. The control system when the model operates as a VSC has a similar configuration to the system when diode rectifiers are connected but has different parameters of PI controllers to account for new added elements.
- To design, implement, and operate an MTDC Simulink model that contains individual blocks including two offshore wind farms, two WFVSCs, dc cable, and grid side VSC. The model will be verified using the MATLAB/Simulink environment to assess its performance.
- To investigate and analyse dc faults, such as negative to positive, positive to ground, and negative to ground fault, and evaluate their impact on MTDC. Dc faults can be implemented on various topologies, including symmetrical and asymmetrical monopole. Furthermore, grid code compliance of the model will be verified under all such operational conditions.
- To set down a mathematical expression describing the contribution to the fault current from various model components such as dc capacitor fault adjacent feeder.
- To investigate and analyse ac faults. Ac grid faults can be symmetrical faults such as three-line to ground and asymmetrical faults such as single or double line to ground, which require the use of symmetrical components to analyse the system. Unsymmetrical faults require the separation of dq components of voltage and current into positive and negative dq using, for example, delay signal cancelation (DSC)
- To design and implement a dual current control for the unsymmetrical fault to account for the presence of negative sequence components which control the reactive power by calculating it from the output of DSC.
- To test the proposed model under various operational modes, such as with or without the connection of diode rectifiers.
- To design, implement, and operate a protection system that can detect the fault, locate the faulty section, and isolate the faulty part rapidly.

- To test and validate the model for normal operating conditions, dc fault conditions, and ac fault conditions. All tests should be conducted for the case when VSC only are connected to the system as well as for the case after the diode rectifiers are connected. A comparison between these two operational modes is performed to assess the model performance.

1.5 The Contributions of the Thesis

The thesis contributions are reported and can be categorised into two main categories. These categories are related to the MTDC topology and the design, implementation and operation of the model. Three novelty areas can be highlighted in this work; these are the inclusion of reactive power control during the unbalanced operational condition, the extension of series connection into MTDC topology which requires improving the control system to take into account the power balance between the VSCs, and the implementation of reference model which enable the comparison of various operating modes. Thus, the contributions are highlighted as follows:

- Utilise a cost-effective converter topology in an MTDC. This topology employs a series connection of diode rectifiers with a VSC.
- Design, implement, and simulate a reference model that can connect or disconnect these diode rectifiers and the VSC at any time during the simulation run. Hence, it can compare the performance of different operational modes such as VSC (conventional model) and diode rectifiers.
- The VSC converter rating when the diode rectifiers are not connected will be different from that after the diode rectifiers are connected; hence, the phase reactor will be different due to this rating change, which necessitate the change of the parameters of the PI controllers.
- Propose a novel control system called the generalised control scheme (GCS), to control the reactive component in the outer control loops.
- Design a protection system suitable for the proposed MTDC topology. The protection system should detect, locate, and isolate the faulty part, and can send reclosing signal to reclose the breaker (for example send 2, 3, 4… reclosing attempts to check whether the fault is permanent or not).

1.6 List of Publications

The following papers were completed during the research based on the research outcome

- Ghaith Ali Abdul-Rahim, Patrick Chi-Kwong Luk, John Economou **Power Control and Fault Analysis of VSC-based Multiterminal HVDC in Offshore Windfarms,** Cranfield Science for a Circular Economy – how to tackle the water, energy, food nexus (CranWEF 17) conference, 2017.
- Ghaith Ali Abdul-Rahim, Patrick Chi-Kwong Luk, John Economou **Three-terminal MTDC Network Based on Series Connection of VSC and Diode Rectifier and Dc Fault Analysis.** Submitted to **IET Generation, Transmission & Distribution**.
- Ghaith Ali Abdul-Rahim, Patrick Chi-Kwong Luk, John Economou **Universal Model Implementation and Fault Analysis of a Three Terminal MTDC that Operates using VSC alone or Series Connection of VSC and Diode Rectifier.** Submitted to sustainable energy/Power electronics in renewable energy.
- Ghaith Ali Abdul-Rahim, Patrick Chi-Kwong Luk, John Economou **Implementation and Performance Evaluation of a Multi-terminal DC network based on series connected Voltage Sourced Converters and Diodes.** Submitted to section: **Sustainable Energy/Power Electronics in Renewable Energy Systems**.
- Ghaith Ali Abdul-Rahim, Patrick Chi-Kwong Luk, John Economou **Generalised Control Scheme of VSC Under Unbalanced AC Fault Conditions** submitted to **International Journal of Electrical Power and Energy Systems**.

2 LITERATURE REVIEW

2.1 Introduction

Reliability and availability are the fundamental requirements in every power system. A conventional power system based on ac transmission of electric power provides a good level of energy security. Due to the climate change challenge, other sources of electricity, such as wind power and solar power, have been developed. However, renewable energy raises the margin of unpredictability and variability. Consequently, the need for power flow reversal is increased to balance the power between two grids or networks, which in turn requires flexible control of power flow [11]. VSC-based HVDC technology can achieve the power reversal requirement and provide an attractive and feasible solution because of its fast response, good flexibility and controllability, ability to perform a black start, the ability to connect to a weak grid, and easier construction a multiterminal dc power system [110]. However, VSCs are vulnerable against dc faults because of the dc capacitor's contribution to the fault current. Furthermore, the IGBT of the VSC will be blocked during the fault, leaving the freewheeling diodes to conduct the entire current.

2.2 HVDC Overview

In 1954, the first commercial use of HVDC technology was performed by the operation of the first link connecting Gotland with the mainland of Sweden, where mercury-arc converter valves operated at 20 MW and 100 kV [80]. Two types of converter technologies are based on the commutation method: LCC- and VSC-based HVDC [111]. HVDC has gained more attention due to its ability to connect two different power systems with distinct frequencies. Moreover, it can be used in wind turbines and other renewable sources to supply fixed ac voltage and frequency output value regardless of the input value of the voltage and frequency. Today, variable-speed wind turbines are available as a result of converter use, which enables elimination of the multiple-stage gearbox that was used in the fixed-speed wind turbine generator [112]. Big turbines of 1.5 MW or more typically have a rotor rotation speed of approximately 5-24 rpm [70,112].

This means, for example, the rotation speed of the Siemens wind turbine SWT-6.0-154 is 5-11 rpm [113]. As a result of the variable rpm, the frequency of the output voltage is variable. Hence, a power converter will be an essential part to provide a constant frequency output. The relationship between frequency (f), rpm, and the number of poles (p) is ($rpm = \frac{120f}{p}$). Therefore, for a constant number of poles, the change in the output frequency is 120%.

Two types of HVDC technology are available based on the converter type. The first type of converter, which is older and considered to be a mature technology, is the line commutated converter (LCC). The LCC utilise line voltage for commutation (therefore it is termed line commutated converter, LCC [114]) and employs the thyristor as a switching device [115]. Therefore, LCC are often used whenever high power of approximately 10 GW and high voltage of more than ± 1.1 MV are required [51,116]. But the main drawback of the thyristor is the inability to be switched off unless zero current is passing through it and changes the voltage polarity [19]. Hence, commutation requires the line voltage of the connected network, which can also be supplied by a STATCOM or a synchronous compensator [117]. Typically, LCC has a large footprint, which increases the difficulty in installing it on offshore platforms [79].

In contrast, VSC is a newer technology that was first used in 1997 in Sweden in Hellsjön [118] and two years later in Gotland [119]. Since then, many VSC-based projects have been commissioned or planned. Table 2-1 shows examples of HVDC projects based on this technology. VSCs can be built using IGBTs, GTOs, or IGCTs as a switching device [81], while in practice the most commonly used valve is IGBT with PWM control to produce gate pulses. Each leg (phase) of a converter contains two IGBTs to create two levels or four IGBTs for three levels, as shown in Table 2-1.

However, many modular systems can be connected in a cascaded way to form a multilevel modular converter, or MMC [68,120–124], which is more attractive due to its nearly pure sine wave output and lower switching loss [11]. The increase in the converter level gives another advantage by reducing the filter

Table 2-1 VSC-HVDC projects

Project Name	Year	Converter rating	Ac side voltage	Dc voltage	Dc line Length	Topology	Manufacturer
Hellsjön, Sweden [33]	1997	3 MW, ±3 MVAr	10 kV (both ends)	±10 kV	10 km Overhead line	2-level	ABB
Gotland HVDC light, Sweden	1999	50 MW, -55 to +50 MVAr	80 kV (both ends)	±80 kV	2×70 km Submarine Cable	2-level	ABB
Eagle Pass, USA (B2B)	2000	36 MW, ±36 MVAr	138 kV (both ends)	±15.9 kV	Back-to-back station	3-level	ABB
Tjäreborg, Denmark	2000	8 MVA, 7.2 MW, -3 to +4 MVAr	10.5 kV (both ends)	±9 kV	2×4.3 km Submarine cable	2-level	ABB
Terrenora Interconnection (Directlink), Australia	2000	180 MW -165 to +90MVAr	110 kV – Bungalora 132 kV Mullumbimby	±80 kV	6×59 km Underground cable	2-level	ABB
MurrayLink, Australia	2002	220 MW, -150 to +140 MVAr	132 kV - Berri 220 kV – Red Cliffs	±150 kV	2×180 km Underground cable	3-level ANPC	ABB
CrossSound, USA	2002	330 MW, ±150 MVAr	345 kV NewHaven/ 138 kV Shoreham	±150 kV	2×40 km Submarine cable	3-level ANPC	ABB
Troll A offshore, Norway	2005	84 MW, -20 to +24 MVAr	132 kV - Kollsnes 56 kV - Troll	±60 kV	4×70 km Submarine cable	2-level	ABB
Estlink, Estonia-Finland	2006	350 MW, ±125 MVAr	330 kV – Estonia 400 kV – Finland	±150 kV	2×31 km Underground 2×74 km Submarine	2-level	ABB
NORD E.ON 1, Germany	2009	400 MW	380 kV – Diele 170 kV – Borkum 2	±150 kV	2×75km Underground 2×128 km Submarine	2-level	ABB
Caprivi Link, Namibia [125]	2010	300 MW	330 kV – Zambezi 400 kV – Gerus	350 kV	970 km Overhead line	3-level	ABB
Valhall offshore, Norway	2011	78 MW	300 kV – Lista 11 kV – Valhall	150 kV	292 km Submarine coaxial cable	2-level	Nexans
Trans Bay Cable, USA	2010	400 MW, ±170 MVAr	230 kV- Pittsburg 138 kV - San Francisco	±200 kV	88 km Submarine cable	MMC first time	Siemens
Nanhui Wind Farm Integration, China	2011	18 MW / 20 MVA	35 kV	±30 kV	8.4 km XLPE cable- Wind farm- Nanhui station	MMC	C-EPRI
BorWin1 Germany	2012	400 MW	170 kV (Platform BorWin alpha),380 kV (Diele)	±150 kV	2 x 75 km underground cable, 2 x 125 km subsea	MMC	ABB
East West	2013	500 MW	400 kV	±200	2x 75	2-level	ABB

Project Name	Year	Converter rating	Ac side voltage	Dc voltage	Dc line Length	Topology	Manufacturer
Interconnector [34]				kV	(underground) + 2x186(subsea) 261 km subsea		
BorWin2, Germany	2015	800 MW	150 kV-offshore, 400 kV - Diele	±300 kV	125 km offshore, 75 km onshore	MMC	Siemens
HelWin1, Germany	2015	576MW	155 kV-offshore, 400-Büttle	±250 kV	2x130 km	MMC	Siemens
INELFE [126]	2015	2×1000 MW	400 kV-Baixas, France 400 kV-Santa Llogia, Spain	±320 kV	4×(32 km Span+33km France) underground cable	MMC	Siemens
Nanao Multi-terminal VSC HVDC[4] [127,128]	2013	200 MW-100 MW-50 MW	110 kV	±160 kV	32 km	MMC[5]	DNV GL, SEPRI and CSG
Zhoushan MTDC Interconnection	2014	400/300/100/100/100 MW	220 kV and 110 kV AC	±200 kV	134 km	MMC	C-EPRI
South West link	South part 2014 West part 2016	South part: 2×600 MW	400 kV	±300 kV	South part: 4×180km underground cable + 70km overhead	MMC	Alstom
DolWin1, Germany - Heede	2015±	800 MW	155kV (Platform DolWin Alpha),380 kV (Dörpen/Wes)	±320 kV	2x75 km underground, 2x90 km subsea	MMC	ABB
ÅL-link	2015	100 MW/ 30 MVAr	110 kV at both ends	±80 kV	2x158 km		ABB
Helwin2	2015	690 MW	155 kv offshore, 400 kv onshore	±320 kV	2x85km submarine cable 2x45.5 km underground cable	MMC	Siemens
Skagerrak 4 [129]	2015	700 MW	400 kv both sides	500 kV	4x244 km	MMC	Nexans, ABB
SylWin1	2015	864 MW	155 kv, 400 kv	±320 kV	205 km 160 km sea, 45 km land)	MMC	Siemens

[4] *The world first multiterminal HVDC system, which has three terminals. Electric Power Research Institute (SEPRI) has responsibly of the project, technically. Multiple providers have taken part. For example: (1) HVDC-VSC switches were supplied by the three different suppliers. (2) two sea/land HVDC cable manufacturers, and (3) the equipment of the control and protection system were supplied by three different suppliers.*

[5] *Injection Enhanced Gate Transistor (IEGT)/ IGBT was used.*

Project Name	Year	Converter rating	Ac side voltage	Dc voltage	Dc line Length	Topology	Manufacturer
Troll A 3&4	2015	100 MW	Troll A, 66 kV Kollsnes, 132 kV	±60 kV	70 km		ABB
DolWin2	2017	916 MW	155 kV DolWin, 380 kV (Dörpen West)	±320	135 km,2x 45 km subsea,2 x 90 km underground	MMC (CTL cascaded two-level)	ABB
SydVästlänken	2016	1200 MW	400 kv	±300	260 km (197 km, 63 km)		
NordBalt	2017	700 MW ±350 MVAr	Swedish:400 kV Lithuanian: 330 kV	±300 kV	2x400 km submarine, 2x40 km land (Sweden),2x 10 km	MMC	ABB

size required to smooth out the converter output because the higher-level converter has fewer harmonics than the lower-level converter. However, this complicates the switching pattern.

Figure 2-1 Integrated control system of Nan'ao Multiterminal VSC [130]

2.3 Converters

The basic component which plays a pivotal role in any HVDC system is the converter. In renewable energy, and particularly in the wind energy industry, the converter is receiving more attention. Several types of converters are available depending on the applications that need the converters. These include ac/dc, dc/dc, dc/ac, and ac/ac "ac/dc/ac" converters. Moreover, two types of converters based on commutation type are available: line commutated converter (LCC) and self-commutated converter which is called VSC.

2.3.1 Line Commutated Converter

Since the first commercial use of HVDC in Gotland in 1954, LCC technology of converter has been in operation. Most working HVDC systems use LCC technology. This type of converter typically needs the ac line voltage of the ac system that is connected to the converter in the conversion process to perform the commutation from one valve to another valve. LCCs are, however, constructed from a thyristor, which can be turned on (but not off) by a trigger pulse. Generally, diode rectifiers can be used in HVDCs as a rectifier but not as an inverter. However, such a rectifier has no controllability for dc voltage output, which is a serious hindrance. Before the 1970s, LCC HVDC systems used mercury-arc valves; the thyristor was used for the first time in the1970s and is still used today.

The dc current direction is unchanging with time, and it flows through inductances, which may be considered approximately constant. Typically, the output of the LCC is filtered with inductances of an inductor or the inherent inductance of the transmission line [66]. On the other side, the converter can be considered as a current source, which injects both grid frequency and high-frequency harmonic currents into the ac system. Therefore, an LCC is also called a current source converter (CSC). Reversal of power flow direction can be made via inverting the dc voltage polarity of both poles of a station, which requires the use of mechanical switches [79].

To achieve the required voltage blocking level, N-submodules must be connected in series, with each submodule containing a single semiconductor device. The output voltage V_{dc} can be calculated using the thyristor firing angle [66] as follows:

$$V_{dc} = V_p \frac{3\sqrt{6}}{\pi} \cos(\alpha) \quad \textbf{(2-1)}$$

where V_p represents the maximum (peak) value of the rectified phase voltage and α refers to the firing angle.

2.3.2 Voltage Source Converter

Using another type of semiconductor switch, such as insulated gate bipolar transistor (IGBT). In an IGBT both turn-off and turn-on states can be controlled, which offers a second degree of freedom over the thyristor. Several types of VSCs were investigated in the literature. VSCs are classified based on the voltage level, such as 2-level (or six-pulse), 3-level (or twelve-pulse), and multilevel; or they can be classified based on their structure, such as flying capacitor (FC) [131,132], neutral point clamped (NPC) [133], active-NPC [134,135], multilevel modular cascaded (MMC) [136], or cascaded two-level (CTL) [137]. Thyristor-based converter (LCC) technology is available on the market in 2-level topology only [138].

The capability of VSC to operate without the need for system support for commutation (i.e. it is a self-commutated converter) is one of its advantages. The VSC has many advantages: it has the ability control both reactive power (Q) and active power (P) independently [36], has black start ability [139], can supply passive grids [29] and build multiterminal systems, and presents high dynamic performance [140].

Table 2-2 illustrates the development of the VSC technology since its first introduction commercially in a 2-level topology in 1997 in Hellsjön until 2015 when CTL topology was introduced [141, p.846].

Table 2-2 Development of VSC technology [142]

Technology	First use	Converter type	Losses of converter in %	Switching freq. (Hz)	Example
VSC first generation	1997	2-level	3	1950	Hellsjön
VSC second generation	2000	3-level NPC	2.2	1500	Eagle Pass
VSC second generation	2002	3-level ANPC	1.8	1350	Murraylink
VSC second generation	2006	2-level with OPWM	1.4	1150	Estlink
VSC Plus	2010	MMC	1	<150	Trans Bay Cable
VSC Maxsine	2014	MMC	1	<150	SuperSatation
VSC 4th generation	2015	CTL	1	=>150	DolWin 2

The dc capacitor is an essential component in the HVDC system that is based on VSC and is connected to the dc side. Dc capacitors as energy storage devices help in the commutation process in the VSC. Moreover, they provide a

low-impedance path to higher-order harmonics. Hence, these harmonic components are eliminated from the output in the dc side.

- **Two-Level Converter**

The first and the simplest three-phase converter topology consists of six IGBT semiconductor switches in total, two valves in each leg (phase), as shown in Figure 2-2. One valve is used for the positive and the other for the negative part of the waveform [28]. Positive and negative valves, in practice, encompass a number of cells. In general, high voltage, which consists of hundreds of kilovolts, is important for transmitting high-power with low-power loss. Therefore, series connection of cells is typical and necessary for VSC connection to be able to block such high voltages. For example, ±320 kV requires 38 cells in each IGBT block [137]. To ensure the VSC operation in the four quadrants, freewheeling diodes are connected to act as anti-parallel [143] components. Four-quadrant operation of a converter is associated with bidirectional control of both active and reactive components, with bidirectional direct-current flow [144,145].

Figure 2-2a illustrates a typical configuration of a 2-level converter and its output measured by Matlab/Simulink. Figure 2-2b presents the output waveform measured at the converter terminal, shown as pulses, and a sinusoidal wave measured at the load. The switching frequency was 2 kHz. Figure 2-2c shows total harmonic distortion (THD) using fast Fourier transform (FFT) via Matlab/Simulink tools. The simulation was run using a unity modulation index.

Analytically, the phase voltage of a VSC can be expressed using dc voltage and modulation index (m) as follows [66]:

$$V_{ph}(t) = \frac{1}{2} V_{dc} * m * \cos(\omega t) \quad \textbf{(2-2)}$$

where V_{ph} denotes the rms value of the phase voltage, V_{dc} represents the dc voltage of the converter, and m is the modulation index, which is typically between 0 and 1. The modulation index, m, is defined for pulse width modulation (PWM) as follows:

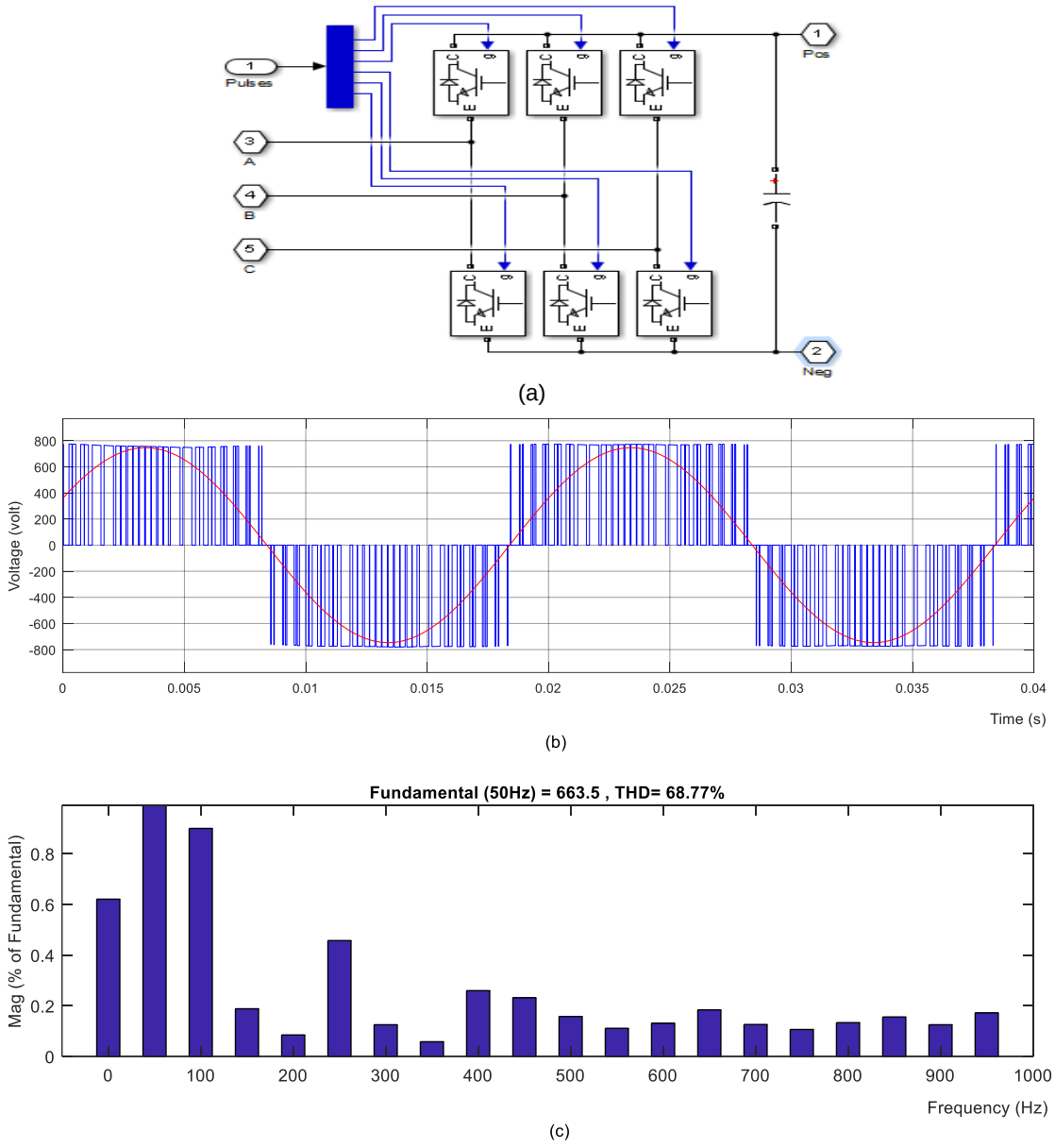


Figure 2-2 Typical configuration (a) of a 2-level, three-phase converter. (b), switching output voltage (c), and harmonics content or total harmonic distortion THD

$$m = \frac{V_c}{V_{car}} = \frac{2\sqrt{2}v_{ph}}{\sqrt{3}V_{dc}} \quad \textbf{(2-3)}$$

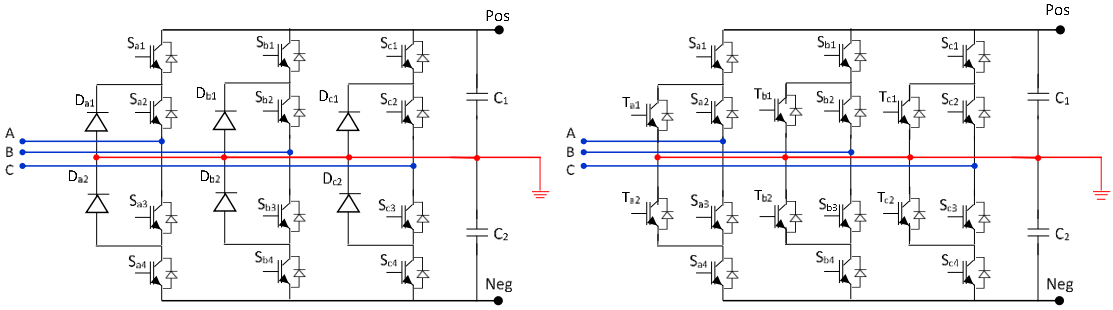
where V_c represents the amplitude of the rectangular signal of the control system, and V_{car} denotes the carrier signal amplitude.

- **Three-Level Converter**

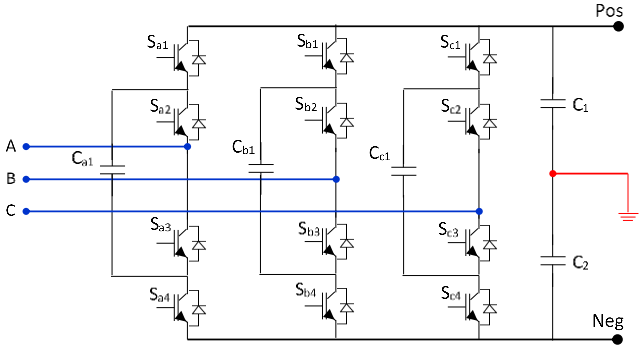
Converters that are designed as a 3-level topology typically contain twelve semiconductor switches (IGBT), and therefore they may be called twelve-pulse converters. Two categories of this topology can be found in the literature: flying capacitor (FC) converter, shown in Figure 2-3c [146], and neutral point clamped (NPC) converter, presented in Figure 2-3a. However, an active NPC converter (Figure 2-3b) is similar to an NPC converter except that the active device uses IGBTs to replace the diode clamping. The reason for proposing active NPC (ANPC) was to overcome the unequal distribution of losses between the converter valves by replacing the diodes with active switches (IGBTs).

Table 2-3 Switching logic for 3-level FC and NPC

Output dc voltage	Flying capacitor switching	NPC switching
$+\frac{V_{dc}}{2}$	S1, S3	S1, S4
0	S2, S3 or S1, S4	S4, S3
$-\frac{V_{dc}}{2}$	S2, S4	S3, S4



(a) NPC converter (b) ANPC converter



(c) Flying capacitor (FC) converter

Figure 2-3 A 3-phase converter: (a) neutral point clamped, (b) active neutral point clamped, and (c) flying capacitor recreated from [147]

The waveforms of the voltage produced by these two topologies are similar, but the switching logic is different. Table 2-3 shows the differences between the switching logic of NPC and FC converters of one leg [146, p.26].

This type of converter offers several advantages over 2-level converters because it has smaller output voltage steps, which reduces the higher-order harmonics in the output waveform. Thus, the total harmonic distortion (THD) in the output is lower, as shown in Figure 2-2c and Figure 2-4b. Consequently, a smaller filter is required to eliminate the harmonics from the output compared to an equivalent rating 2-level inverter. Thus, the NPC converter can be used for higher voltage conversion because the switches are exposed to half of the bus voltage only, or lower voltage IGBT modules can be used to produce the same output voltage.

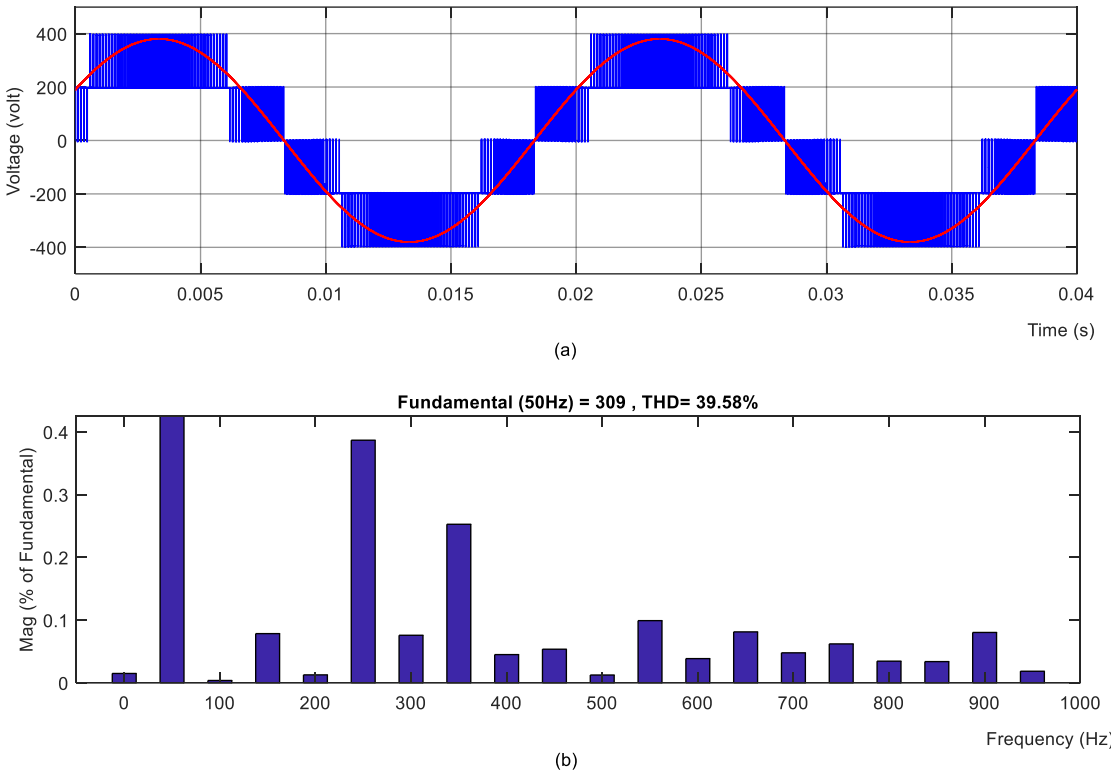
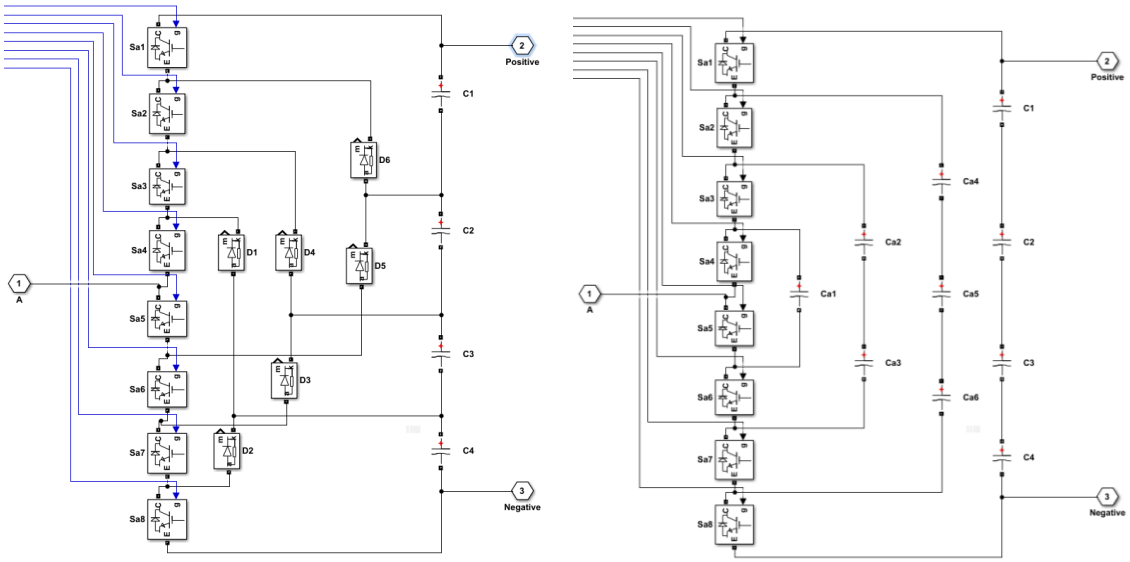


Figure 2-4 Output waveform of a 3-level converter: (a) switching pattern and output voltage, and (b) harmonic contents, THD

- **Multilevel Converter**

Multilevel converter topology has received increased attention in the power industry. This type of converter was reported in [82] thoroughly. Increasing converter level will decrease the switching times (or the on-off states) of the valves and enhance the converter output, which makes the output closer to a sine wave and consequently reduces the need for big filters. Figure 2-5 shows multilevel (5-level) flying capacitor and neutral point clamped converters. The principle of operation for a classical 5-level neutral point clamped converters and the switching states are explained as follows [82].



(a) 5-level NPC [148] (b) 5-level FC [83]

Figure 2-5 Five-level one-leg diode clamped converter: (a) NPC and (b) FC

- Voltage level $V_o = V_{dc}$, all the upper switches (S_a1 - S_a4) are turned on.
- Voltage level $V_o = \frac{3V_{dc}}{4}$, the upper three switches and the upper switch in the second arm (S_a2 - S_a5) are turned on.
- Voltage level $V_o = \frac{V_{dc}}{2}$, the lower two switches in the upper arm and the upper two switches in the lower arm (S_a3 - S_a6) are turned on.
- Voltage level $V_o = \frac{V_{dc}}{4}$, the lower two switches in the upper arm and the upper two switches in the lower arm (S_a4 - S_a7) are turned on.
- Voltage level $V_o = 0$, the switches in the lower arm (S_a5- S_a8) are turned on.

Table 2-4 summarises the switching technique.

Table 2-4 States of switching strategy for 5-level diode clamped converter

Output voltage V_o	Switching states							
	S_a1	S_a2	S_a3	S_a4	S_a5	S_a6	S_a7	S_a8
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = \frac{3V_{dc}}{4}$	0	1	1	1	1	0	0	0
$V_3 = \frac{V_{dc}}{2}$	0	0	1	1	1	1	0	0
$V_2 = \frac{V_{dc}}{4}$	0	0	0	1	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

As in 3-level converters, the switching logic of 5-level flying capacitor converters is different from that of NPC. Table 2-5 illustrates the switching strategy for the 5-level FC converter.

Table 2-5 Switching logic of 5-level flying capacitor converter

Output voltage V_o	Switching states							
	S_a1	S_a2	S_a3	S_a4	S_a5	S_a6	S_a7	S_a8
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = \frac{3V_{dc}}{4}$	1	1	1	0	1	0	0	0
$V_3 = \frac{V_{dc}}{2}$	1	1	0	0	1	1	0	0
$V_2 = \frac{V_{dc}}{4}$	1	0	0	0	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

An m-level NPC converter generally comprises m-1 dc capacitors. For example, a 5-level converter has four capacitors connected to its dc bus in each leg to produce m levels of the voltage. Each capacitor contributes the amount of $\frac{V_{dc}}{4}$ [82]. A typical output of a 5-level converter and the harmonics contents (THD) are shown Figure 2-6.

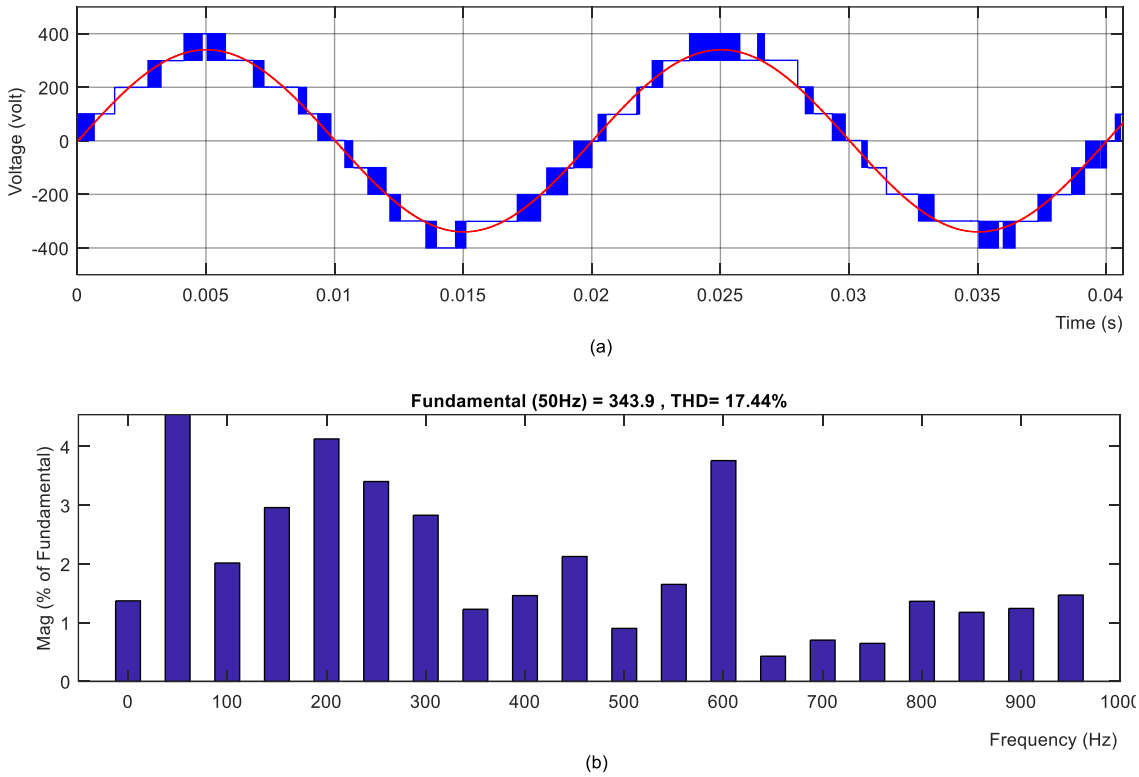
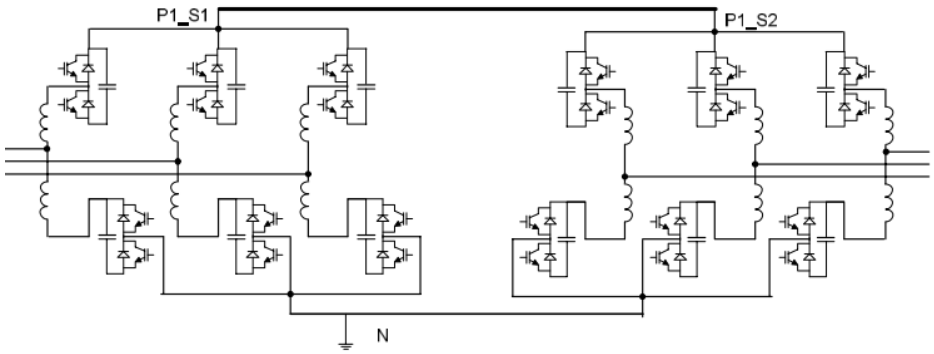


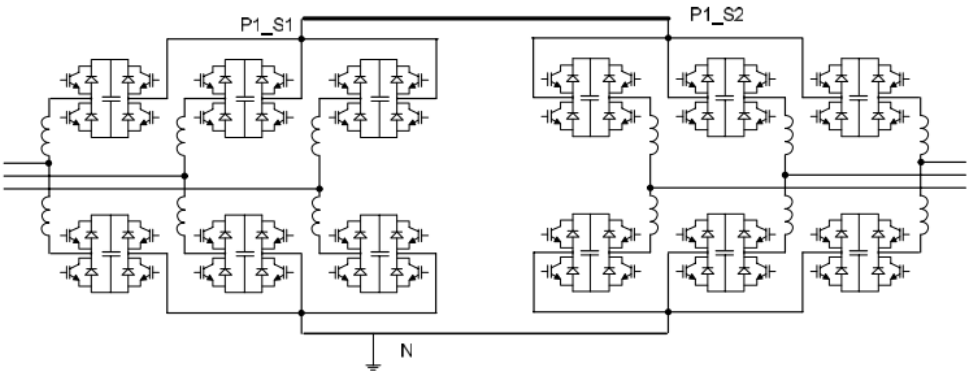
Figure 2-6 Output of a 5-level converter and THD: (a) output voltage and switching pattern and (b) harmonic content, THD

- **Modular Multilevel Converter**

A newer multilevel configuration, called the multilevel modular cascaded (MMC) converter, was proposed by Lesnicar and Marquardt in 2003 [149]. Their converter is considered to be a next-generation converter and suitable for high-voltage, high-power applications. This type of VSC uses standalone submodules, either half-bridge (HB-MMC) or full-bridge (FB-MMC). Figure 2-7 illustrates both FB-MMC and HB-MMC, and was recreated from [150]. The first use of this converter topology was in 2010 in the HVDC Cable project of Trans Bay, USA. Any number of these submodules can be connected in series to provide the required blocking voltage and power rating. Figure 2-8 shows a typical converter arrangement and converter arm segments for 400 MW; each converter's arm consists of 216 power modules [151].



(a) HB-MMC



(b) FB-MMC

Figure 2-7 Modular multilevel converter: (a) HB-MMC and (b) FB-MMC [150]

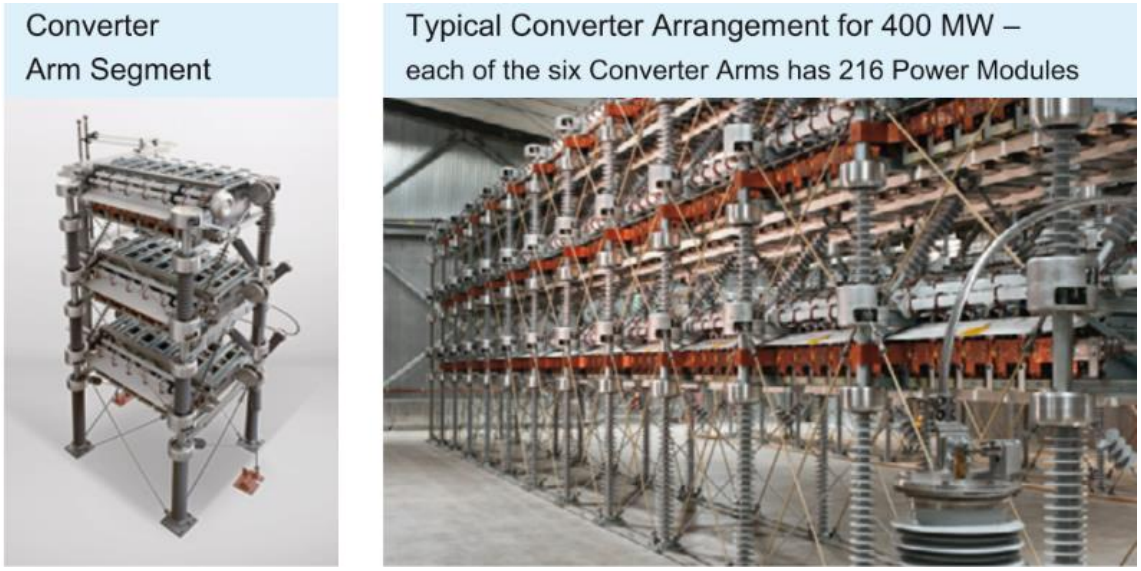


Figure 2-8 Voltage source converter [151]

Jonsson et al. (2013) [150] introduced a detailed analysis and comparison between VSC types, including HB-MMC and FB-MMC, to determine the performance and losses and the capability to withstand different fault conditions and the corresponding fault ride through. Their goal was to determine VSC rating in terms of current and voltage, semiconductor and cell capacitor, and dc breaker to evaluate the cost and losses.

A typical output of a 20-level converter and the harmonics contents (THD) is shown Figure 2-9. It can be seen that the THD in this case is much less than that of the previous converters. THD For 20-level converter is 5.15 % while for 5-level converter THD equals 17.44 %, for 3-level THD is 39.58 % and for 2-level converter THD is 68.77 %.

The duty cycle is a key term that describes the output power of the converter. For a submodule arm, the duty cycle is calculated by

$$d_m(t) = \frac{\frac{V_{dc}}{2} - V_{ph}(t)}{N_{mmc} - V_{Csm}} \tag{2-4}$$

where d_m is the MMC submodule duty cycle, V_{dc} is the output voltage of HVDC (kV), V_{ph} is the converter rms phase voltage (kV), N_{mmc} is the number of submodules of MMC, and V_{Csm} is MMC submodule dc bus voltage (kV). In general, duty cycle is the measure of the output power and is defined as the proportion of on-time (active) to the total period (cycle). Mathematically, duty cycle (d) is

$$d = \frac{T}{P_t} * 100\% \tag{2-5}$$

where T represents the time where the signal is active (time unit), and P_t denotes the total period of time (time unit). Hence, low duty cycle leads to low power output of the converter, and vice versa.

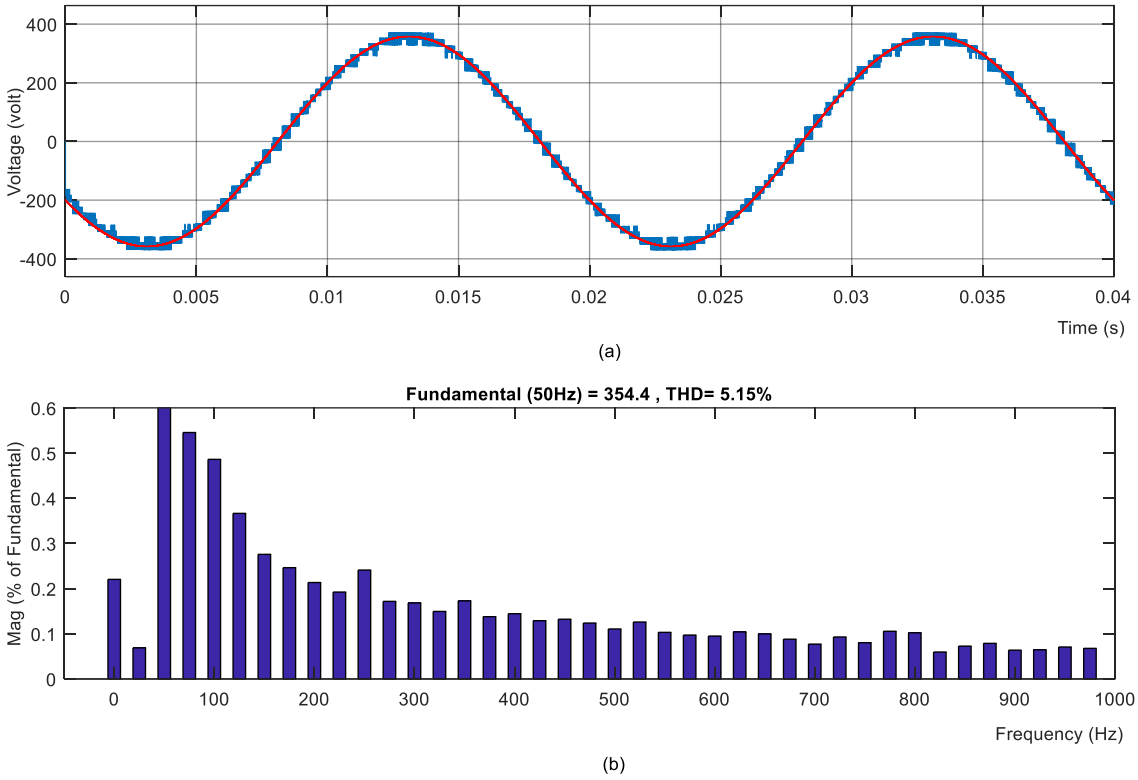


Figure 2-9 20-level VSC (a) output voltage (b) THD analysis

The average output y over the time period T of any function $f(t)$ is calculated:

$$y = \frac{1}{T}\int_0^T f(t)\,\mathrm{dt} \tag{2-6}$$

For the waveform shown in Figure 2-10, $f(t)$ equals y_{max} when $0 < t < dT$ and y_{min} when $dT < t < T$. Then, (2-6) will be

$$y = \frac{1}{T}\left(\int_0^{dT} y_{max}\,\mathrm{dt} + \int_{dT}^{T} y_{min}\,dt\right)$$

$$= \frac{dT.y_{max} + T.(1-d).y_{min}}{T}$$

$$= d.y_{max} + (1-d).y_{min} \tag{2-7}$$

which can be simplified when $y_{min} = 0$, which is the situation in many cases such as the for the on/off state of the gate drive. Then:

$$y = d.y_{max} \tag{2-8}$$

This signifies that 100% duty cycle means fully on.

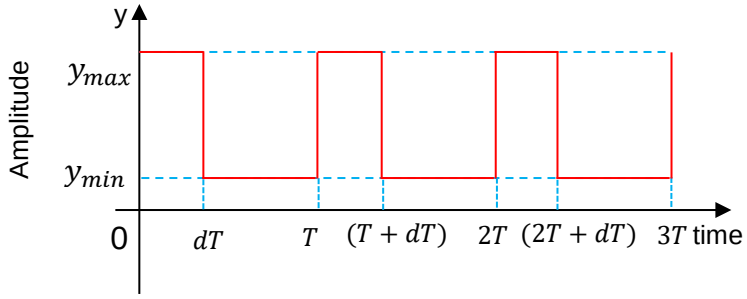


Figure 2-10 Pulse wave to illustrate y_{min}, y_{max} , and duty cycle

- **Cascaded 2-Level (CTL) Converter**

This converter topology is similar to MMC topology, which uses 2-Level converter blocks (cells) that are cascaded connected together to provide a nearly sinusoidal voltage at the output bus of the converter, as shown in Figure 2-11 (figure was redrawn from [137]).

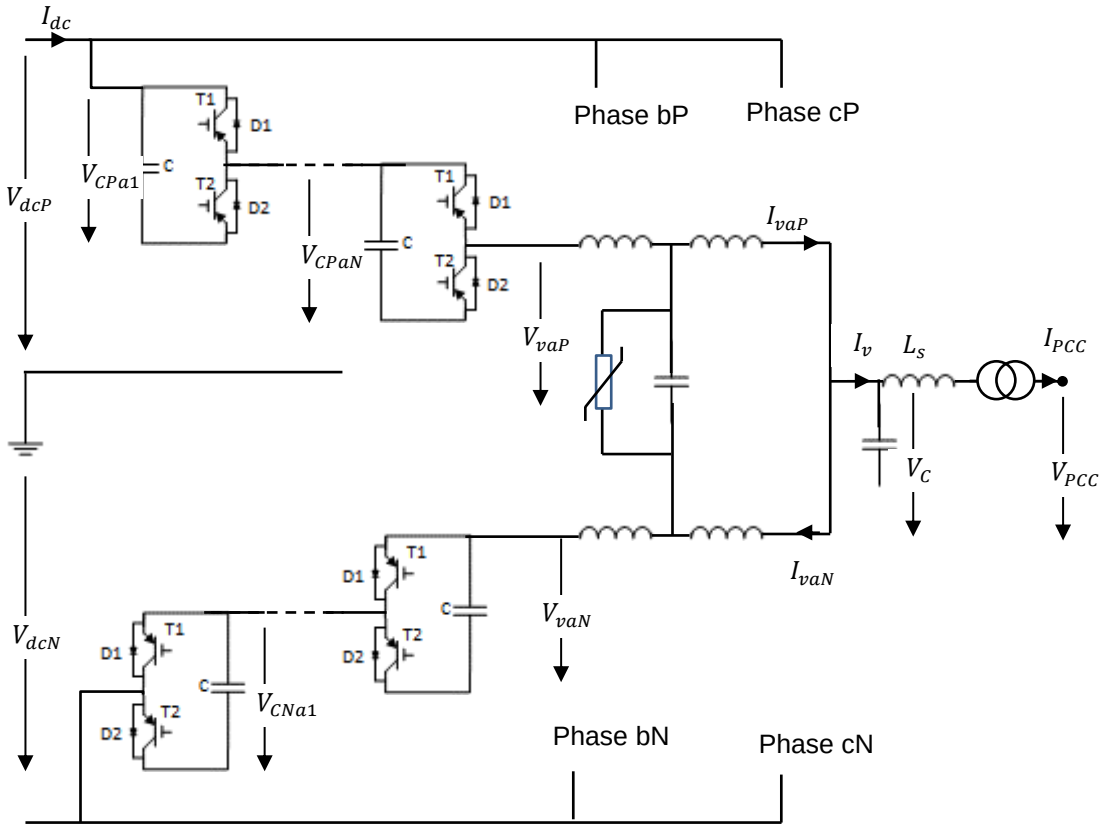


Figure 2-11 Cascaded 2-level converter layout recreated from [137]

CTL converter cells operate at lower switching frequency ($f_{swc} = 150\ Hz$). However, the overall switching frequency (or effective switching frequency) of a leg consisting of 38 cells is 11.4 kHz. The effective switching frequency is given by:

$$f_{sw} = 2\mathrm{N} f_{swc} \tag{2-9}$$

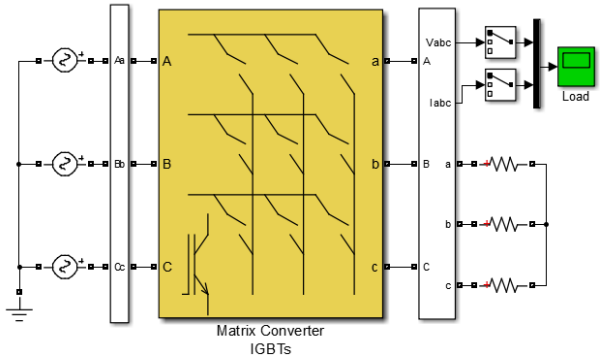
where f_{swc} represents the switching frequency of a cell, N is the number of cells per arm, and f_{sw} denotes the per-phase leg-effective switching frequency.

Jacobson et al. (2010) [137] presented the concept of a low-loss cascaded two-level (CTL) converter and addressed the reliability concerns by the previous multilevel models. The CTL converter reduced the losses of the converter to approximately 1%.

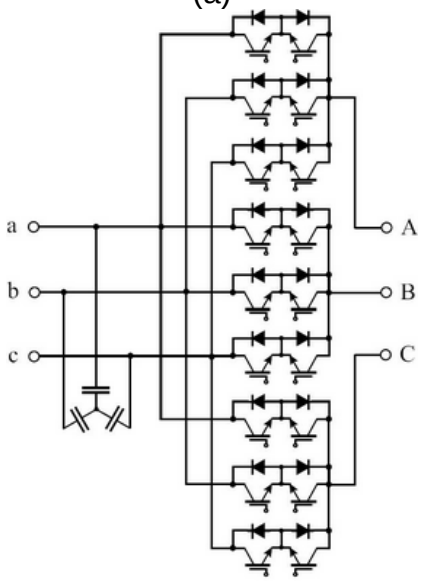
2.3.3 AC to AC Converter

This type of converter transforms ac voltage to ac either in one step or two steps. A matrix converter is an example of an ac-to-ac converter; one is shown in Figure 2-12. Figure 2-12a depicts a Matlab model with a three-phase three-line input and three-phase three-line output and was built using nine switches (cells). Figure 2-12b shows a schematic diagram of the entire matrix block. This type of converter, as indicated by the name, converts the ac voltage to another ac voltage in a single stage without intermediate dc link or energy storage such as capacitor. The matrix converter has achieved only low penetration in the power conversion application, but it is seen as the future concept of ac/ac conversion and motor drive applications.

For instance, Altun & Sunter[152] proposed in 2012 a variable speed control technique for a doubly fed induction generator (DFIG) using a matrix converter connected to its rotor. Maximum power point tracking (MPPT) of the wind turbine was achieved by controlling the shaft speed. The converter capacity was about one third of the rated power.



(a)



(b)

Figure 2-12 Matrix converter: (a) Simulink model and (b) Schematic diagram (from Simulink)

The common converter technology to convert ac voltage into ac voltage is the back-to-back (B2B) converter. This topology uses the dc link as an intermediate stage. Typically, a dc capacitor is connected to the dc link. The dc link cable is kept as short as possible, as illustrated in Figure 2-13.

B2B has been heavily presented in literature, including [58,144,153]. The B2B arrangement is commonly used inside wind turbines to help the variable-speed operation [154] of the wind turbine. Variable-speed operation means that the wind turbine is direct driven (i.e. the gear box is eliminated, and the wind turbine is connected directly to the grid) [155].

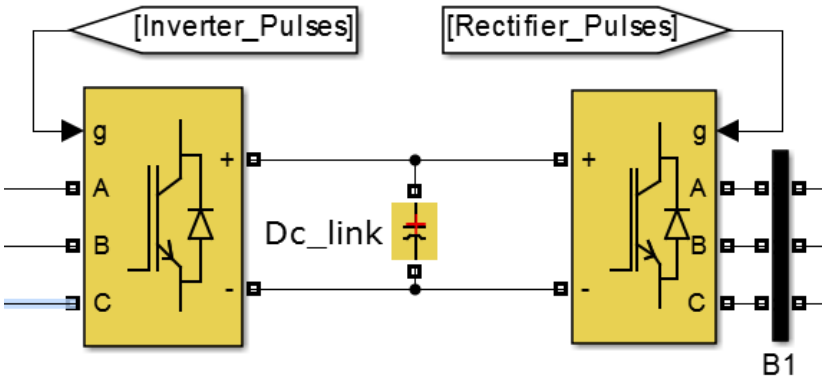


Figure 2-13 Back-to-back (B2B) converter Simulink model

2.3.4 Total Harmonic Distortion

Total harmonic distortion (THD) is a measure of the distortion in a waveform due to the higher-order harmonics in the signal. The THD level is inversely proportional to the level of the converter. The higher the level of the converter, the lower the THD contents in the waveform. It is measured as a percentage of the fundamental wave and can be defined mathematically as follows [156]:

$$THD = \sqrt{\frac{sum\ of\ all\ amplitude\ squares\ of\ all\ harmonic\ voltages}{square\ of\ the\ amplitude\ of\ the\ fundamental\ voltage}} * 100\%$$

or

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_1} * 100\% \quad (2\text{-}10)$$

The THD output in Figure 2-2 in page 25, Figure 2-4 in page 27, Figure 2-6 in page 30, and Figure 2-9 in page 33 was calculated at the output voltage of the converters, before the filter. A typical THD output of a 20-level converter and the harmonics contents (THD) is shown Figure 2-9. It can be seen that the THD in this case is much less than that of the previous converters. THD For 20-level converter is 5.15 % while for 5-level converter THD equals 17.44 %, for 3-level THD is 39.58 % and for 2- level converter THD is 68.77 %.

2.3.5 Modulation

Semiconductor switches (valves) such as IGBT are switched on or off by pulses provided by a gate drive. These devices typically have a response time (i.e.

turn-on and turn-off delay times) of a few microseconds. Thus, the switching frequency of a VSC converter, which is generally constructed using an IGBT, depends mainly on the turn-on and -off delay times and the junction temperature. This temperature is a function of the operating current and voltage. Therefore, high-frequency operation of converters allows the use of a modulation technique. Modulation is a method of converting a signal into varying-width pulses. These pulses switch the valves on or off and, hence, the converter output is determined by the switching technique. Several techniques can be used to generate pulses, including pulse width modulation (PWM) [157], space vector modulation (SVM or SVPWM) [158], sinusoidal pulse width modulation (SPWM) [159], and optimised PWM (OPWM).

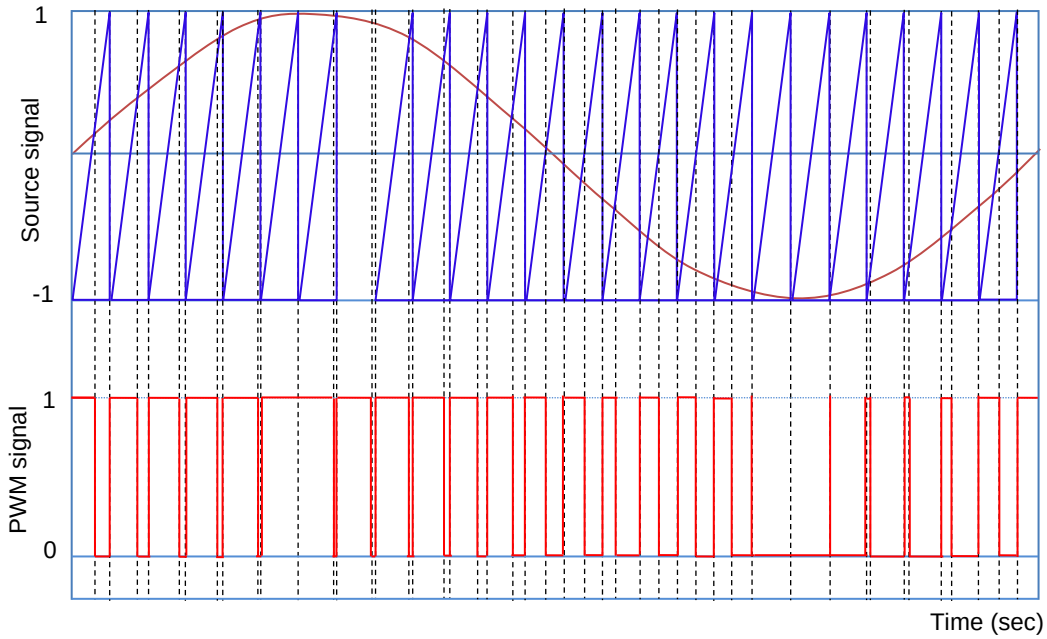


Figure 2-14 PWM generation technique

Whatever technique is used, the principle of operation is to supply these pulses to the gate of the semiconductor devices, inside the converter, to control their on-, and off-state. For this project, a 3-level converter and, consequently, 12-pulse PWM was the chosen switching strategy to convert the power generated by the offshore windfarms into dc. The PWM signal is generated via the intersection method. The intersection method compares a high-frequency sawtooth (or a triangular) waveform, which is called the carrier signal, with a reference sinusoidal signal. When the carrier signal (sawtooth in Figure 2-14) is

less than the reference signal (sine wave), the PWM signal (pulses) is in the high state; otherwise, it is in the low state.

For a 12-pulse generator, a raw vector of 12-element dimension is produced, and each element is sent to an IGBT in the converter according to a predetermined switching state.

Authors in the literature have proposed various techniques suggesting the use of a variety of switching strategies. For example, Song & Nam [94] used a dual-current control topology to control a PWM converter that can supply grids under an unbalanced voltage condition. Jang et. al. [160] proposed a control method for PWM converters to operate in the case when the VSC is supplied by a non-ideal voltage source. Two of the four current control loops were used to eliminate the 5^{th} and 7^{th} harmonics.

2.3.6 Diode Rectifier

The simplest ac-to-dc rectifier can be made using diode rectifiers, which are available as single- or three-phase and half or full wave [161, pp.143–144]. Diode rectifiers have many advantages, such as smaller size, increased reliability because there is no need to use gate drivers or tap changing transformers, and relatively low cost [61]. However, the output voltage of such rectifiers is constant and lacks controllability. Therefore, converters that have controlled semiconductor switching devices such as thyristors and IGBTs have replaced the diode rectifiers in the power system applications [161, pp.143–144]. Uncontrolled rectifiers have been proposed in literature by many authors for use in the HVDC to convert the output power of the wind turbine despite the uncontrollability by adding new elements such as a dc chopper.

For instance, diode rectifiers were proposed in [60,61,110] as the only part of the conversion process in windfarm applications. The use of diode rectifiers is less expensive, has a lower installation cost, results in lower power loss, and presents higher reliability in comparison to VSC, and the use of such rectifiers can be advantageous in HVDC systems. However, diode rectifiers will produce higher harmonics, which in turn require a larger filter to eliminate the harmonics

from the output. Additionally, for wind turbine applications, this proposal can control either the offshore ac voltage or the maximum power point tracking control of the wind turbine by connecting additional components such as dc choppers.

Nguyen et al. [109] proposed a series connection of two diode rectifiers and VSC, where the VSC is responsible for controlling the voltage and frequency in the PCC (point of common coupling). However, the proposed conversion process was applied to a PPT (point-to-point topology). Therefore, the current work aims to extend this topology to be applied to an offshore MTDC network. Therefore, the goal for this thesis to extend the topology to multiterminal HVDC (MTDC) required special attention to change the proposed control system, which focused on harmonics elimination, to a more advanced one to account for the addition of more windfarms. Furthermore, another arrangement regarding the sequence of connection was suggested in this thesis. The previous proposal suggested the method of connecting the VSC in the bottom of the two diode rectifiers. This connection enables the converter to measure its own voltage. The connection of the VSC in the middle between the two diodes rectifiers enables control by measuring the total voltage of the negative and positive poles of the dc cable. Both arrangements were implemented and tested, and the simulation results are presented for them in this thesis.

2.4 Hybrid HVDC Based on VSC and Thyristor Topologies

Some researchers were trying to combine VSCs and thyristor-based converters to obtain the benefits of both. For example, the authors in [139] proposed a system that contains both thyristor-based converter and VSC as static compensator (STATCOM) to connect an island system lacking generation capability. A description of the operation and the control strategy is given under normal and fault conditions.

2.5 Modelling and Control

Modelling and control is presented by a large number of publications including [19,27,168–171,43,155,162–167] for various types of converters for 2-level, 3-

level, and multilevel converter systems. Many aspects were considered. Some control strategies can be used to control wind turbines; these include maximum power point tracking (MPPT) or HVDC systems. All control strategies have the same principles and use the vector control scheme. The vector control scheme generally depends on two PI controllers in the inner two loops. These two controllers regulate the dq currents which are provided by the reference current from the outer controllers. Depending on the use of the converter, the outer loops may control $P - Q$, or $V_{dc} - Q$.

However, control strategies that are suitable for multiterminal HVDC systems are droop control, voltage margin, priority control, and power ratio control. These strategies are designed to ensure that power is balanced between terminals and the delivered power to the grid meets the demands requirements.

2.5.1 Control of Voltage and Frequency

Many publications proposed strategies to control voltage and frequency. To guarantee favourable balancing of P and Q, the classical voltage droop control technique may be used to regulate both the voltage and frequency in a network that does not use STATCOM. For example, Blasco-gimenez et al. [60] used distributed voltage and frequency control to change the voltage using the reactive power and frequency via active power, with an HVDC using a diode rectifier. The diode rectifier was connected to convert the ac voltage and current of the PCC, and a thyristor-based converter was used to convert this dc back into ac. However, this control strategy relies mainly on the firing angle of the rectifier to control, directly or indirectly, voltage and frequency of the OWF network.

Fazeli et al. [73] connected a DFIG to the HVDC grid. For this purpose, classical voltage droop control was used to control the machine and supply the grid by constant voltage and frequency, regardless the speed of the shaft, according to the flow of power in each. However, the use of DFIGs is becoming less common as the use of PMSGs is rising. PMSGs are employed increasingly by companies in projects all over the world.

Furthermore, voltage control mode and current control mode are possible with a combination DR and VSC in WT operation [50].

A hierarchical control scheme is another control methodology, and it was studied by Egea-Alvarez et al. [41] for use in MTDC networks. The structure of hierarchy methodology in that work is to separate different time domains of various control actions.

2.5.2 Power Control

To increase the reliability and to maximise the ability of power transmission of the HVDC network, MTDC offers a good solution to control the power inside the system [90]. The controllers of OWF inverters are constructed by applying coordinated control to regulate both active (P) and reactive (Q) components sufficiently to achieve the above purpose. The power (both P and Q) can be controlled based on the principles of power and angle as follows [1]:

$$P = \frac{V_{pcc}V_{vsc}}{X}.n\sin(\theta) \tag{2-11}$$

$$Q = \frac{n\,V_{pcc}V_{vsc}\cos(\theta) - n^2\,V_{pcc}^2}{X} \tag{2-12}$$

where V_{pcc} and V_{vsc} are the voltage magnitudes at PCC and WFVSC, respectively, θ refers to the angle difference between the voltage phases of the two nodes, X is the reactance of the line (and the filters and transformer, if available) connecting the two nodes, and n is the transformer turn ratio.

For voltage-based control, the $q-axis$ reference frame is aligned with the PCC voltage, and the magnitude of V_{pcc} is equal to the $q-axis$ of V_{pcc}. Figure 2-15 shows the vector diagram of the voltages.

Then, from equations (2-11) and (2-12) and Figure 2-15, the active and reactive power of WFVSC is rewritten in $dq-\ axis$ as follows [109]:

$$P = \frac{n\,V_{pcc}V_{d-vsc}}{X} \tag{2-13}$$

$$Q = \frac{n\, V_{pcc} V_{q-vsc} - n^2\, V_{pcc}^2}{X} \tag{2-14}$$

In the above equations, V_{q-vsc}, V_{d-vsc} represent the $q-$ and $d-axis$ of WFVSC voltages, respectively. The equations indicate that P is controlled by the d-component, and Q is controlled by the q-component of WFVSC in a dq reference frame (SRF). Additionally, this means that the $d-axis$ of the WFVSC component controls the dc link voltage, while the $q-axis$ controls the PCC voltage [109].

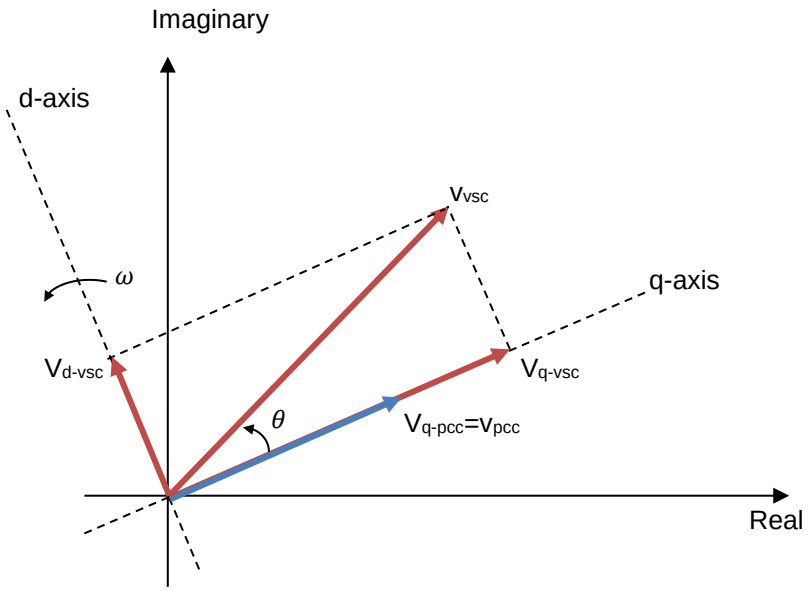


Figure 2-15 Vector diagram WFVSC and PCC voltages

W. Wang et al. [172] derived a dynamic model to identify the controllability and robustness for VSC in an MTDC model containing four terminals. In addition, control equations of nonlinear power flow were studied. Integrating power flow of the MTDC with a classical power flow of ac systems was presented.

2.5.3 Maximum Power Point Tracking

Power generation from wind turbines in typical operational conditions depends on the wind speed. Consequently, power curve characteristics vary for different wind speeds, as illustrated in Figure 2-16, which is taken from [173]. Therefore,

it is important to keep tracking the optimal operating point. Several algorithms to determine the optimal power point are found in the literature [174]:

- Perturb and Observe (P&O) method, also known as Hill Climb Searching (HCS) method
- Tip Speed Ratio method
- Power Signal Feedback (PSF) technique
- Optimal Torque Control
- Fuzzy Logic Controller method

Koutroulis & Kalaitzakis [175] proposed an MPPT method comprised of a buck dc converter and a microcontroller unit using HCS. Their proposed method could control the wind turbine without knowing its optimal power values or measuring the wind speed, and the wind turbine was able to operate at variable speed.

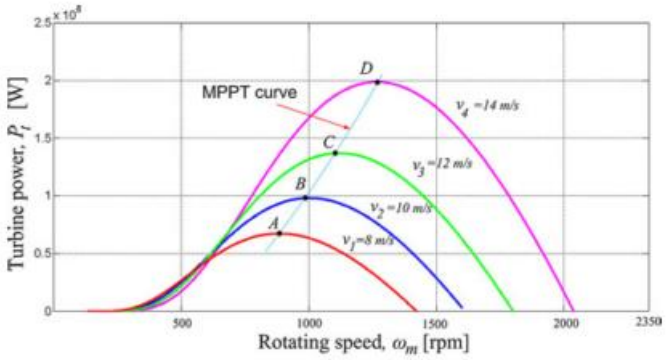


Figure 2-16 Typical wind turbine power characteristics [173]

2.6 HVDC Topologies

2.6.1 Multiterminal HVDC (MTDC) Topologies

In the past, a few wind turbines with a small amount of generation led the electric power utilities to treat wind turbine generation as negative loads subtracted from the actual load rather than as generators in their analysis—with this scenario, net load is treated in a conventional way. Furthermore, a simple topology, called point-to-point topology, is used. The last two decades have witnessed the introduction of VSCs and an increase in the volume of wind

energy generation. This has led to the development of multiterminal HVDC. MTDC-VSC systems, generally are structured by connecting more than one converter to a common HVDC point. For instance, Gomis-Bellmunt et al. [26] presented a variety of topologies, including point-to-point configuration (PPT), general ring, star, and star with a central switching ring topology. At one time, PPT, which is not an MTDC, was the common topology to use because of the low amount of wind energy available. However, due to the increased number of wind turbine installations and the introduction of VSC, MTDC topology is becoming a more convenient way of connecting windfarms because it is more reliable and flexible. MTDC network construction is much easier with VSC because of its flexibility and controllability, which is the ability to control both active and reactive power.

A comparison of offshore windfarm topologies is presented in [176]. The calculations revealed that series dc and series parallel combined connection of OWF could be an option for future designs in spite of its low reliability, which can be enhanced by adding redundancies.

2.6.2 DC Grid

HVDC Networks can be developed further to include dc networks in the transmission system. However, the author [64] showed that dc grids can be different from MTDC because of the ability to use multiple levels of dc voltage. A dc transformer or a dc-dc high power converter was used to empower the dc transmission networks. The dc transformer can serve as: dc voltage stepping, control dc voltage or power, and fault isolation. The efficiency and feasibility of LV and MeV dc grids were investigated in [177]. A resonant converter in an offshore windfarm using a medium-voltage dc grid was designed and analysed by Robinson et al. [178]. Furthermore, HVDC grids are an attractive solution to connect wind turbines in an offshore windfarm.

2.7 Fault Analysis

Fault can occur in any part of the power system for a variety of reasons. The common causes can be external such as human errors or physical damage due

to digging or other constructional duties, or they can be internal such as flashover and failure of insulations. Hence, power system fault analysis studies are a required subject to provide information necessary to select switchgear, conduct relay setting, and determine system stability. However, power systems, in general, are dynamic and change over time during the operation due to switching generators or transmission lines on or off, or during planning, such as adding transmission lines and generators to the system. Therefore, fault analysis studies need to be performed routinely by utility engineers. In any case, MTDC faults can occur in the ac or dc side.

Fault analysis studies have significant importance in the MTDC network because a fault might cause destructive results to the whole system. Among all types, faults in the dc side, such as short circuit of dc cable, pole-to-pole (PP), or pole-to-ground (PG) faults that occur in the cable, present the major hazard to the system. Throughout the fault, the current increases substantially in few milliseconds, which may damage either the dc cables nearby, freewheeling diodes of the IGBTs, or even the entire VSC station and the MTDC network. Thus, the study of the faults in the dc cable and the protection in VSC-based MTDC networks is important and necessary.

Faults in power systems are the main cause for transients that could be very hazardous for equipment connected to that network. However, transient results from a variety of sources in an MTDC system, not just PP and PG, and surges can be a result of lightning strikes, switching device operation, and dc voltage change due to terminal loss. PP faults are considered to be the most severe effects [92] on the nearby network, but generally, PG faults occur more frequently than PP faults [93].

2.7.1 Grid Code

Conventional power stations operate mainly by synchronous generators. These generators typically can support the transmission system stability due to its high inertia response, oscillation damping, power synchronization, and voltage backup in faults [179]. These features are used in conventional power plants to meet the requirements of the grid code. Hence, transmission system operators

have a relatively reliable and stable operation of power systems worldwide [179].

In contrast, technical characteristics of wind turbines that are used today are primarily fixed- or variable-speed, such as induction generators, DFIG, and PMSG with back-to-back converters. These, however, differ from conventional generators, and have a major effect on the characteristics of the power system. Thus, grid code demands that the windfarm act in a way similar to that of a conventional power station to maintain reliability and stability of the power system. At the same time, grid codes have challenged the manufacturers of wind turbines as they obligatorily adapt their technology to fulfil the grid codes. As a result, transmission system operators and wind power developers worked together to review the grid codes to stabilise the transmission system assistance [180].

- **Fault Ride Through**

Among the sources of renewable energy in the world, wind energy application is gaining increasing attention. Because of this growing proportion of wind power generation, its connection to the grid should be considered by utilities. Recently, many countries have adopted their own rules and processes to connect large-scale windfarms [181]. Grid codes developed by different countries are more or less similar [6, p.17]. Fault ride through (FRT) is the main challenge among the grid code requirements. The general requirements for wind turbines in the case of fault occurrence are summarised as:

- The wind turbines should be kept connected during grid voltage over- and under-voltage, which is also called low voltage ride through (LVRT) and high voltage ride through (HVRT), respectively.
- The wind turbine should have the ability to support the system recovery by suppling reactive power during the fault.
- The wind turbine should resume the active power production at a limited rate.

Many authors have studied the grid codes and presented their findings in the literature. For example, Erlich and Bachmann [182] discussed German grid code and stated that the wind turbine should be disconnected when the voltage exceeds the nominal value by 15%, and the allowable frequency ranges between 47.5 and 51.5. According to the grid code, wind turbines are expected to fulfil the grid code requirements in their operation (regarding the drop in voltage level and voltage-time profile) during faults and stay connected to the network [183]. Many grid code requirements can be found in the literature and have been described by Tsili and Papathanassiou [184] such as E.ON grid code [185], British grid code NGET [186, p.chapter cc 1-95], and Spanish grid code. Figure 2-17 depicts the grid code by E.ON and shows the LVRT and HVRT (redrawn from [187] and [179]).

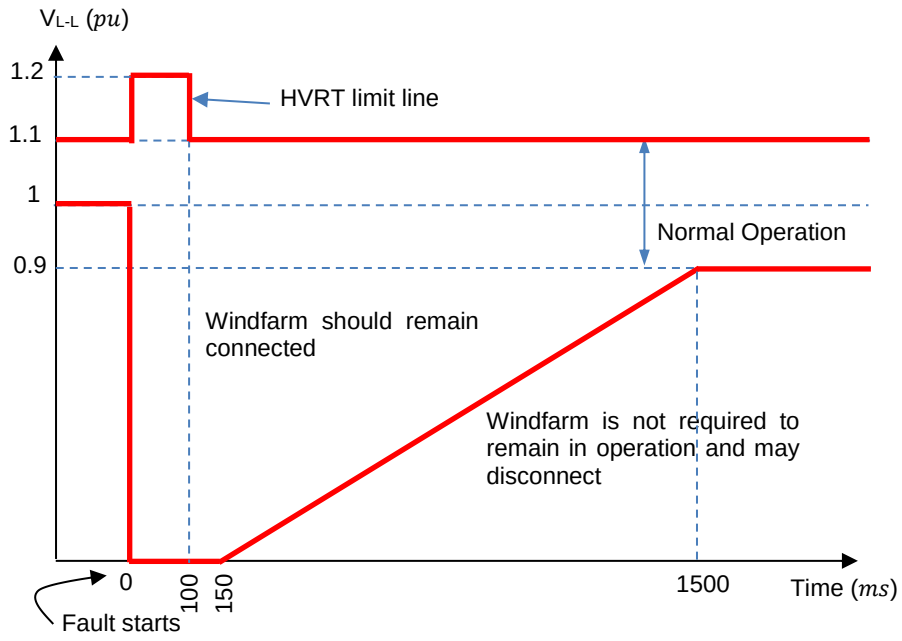


Figure 2-17 LVRT and HVRT grid code requirement during fault by E.ON.

Moreover, authors may use a grid code to assess the proposal complement with the grid code, such as was done by Nguyen and Lee [183], who proposed a combination of energy storage system (ESS) and braking chopper to account for LVRT in a system with PMSG to reduce the cost. The dc link voltage was controlled by ESS, and the GSVSC are allowed to follow the grid code requirement regarding the reactive current.

- **Reactive Current Compensation Requirement during Grid Faults**

During fault conditions, wind turbines should supply reactive power (reactive current) to comply with the grid code requirements, to recover the voltage to its normal value [188]. However, modern power electronic devices such as VSCs can control both active power (P) and reactive power (Q) independently, in a way similar to that of conventional power stations [189]. The injection of reactive power helps to maintain stability of voltage and compensate for the reactive power from cables and transmission line.

For instance, wind energy conversion systems (WECS) are able to fulfil the grid code requirements by proper design of their control system of power converters [190]. Moreover, the power factor should be kept controlled in the range between 0.95 lead to 0.95 lag, for the case when the WECS supplies 1.0 pu active power and ±0.33 pu reactive power [179,188].

The function of FRT should start when the voltage of the system falls below $0.9\,pu$. For voltage ranging from $0.9\ pu$ to $0.5\,pu$, the compensation system should inject 2% reactive current for every 1% fall in voltage, as shown in Figure 2-18 (taken from [185]). If the voltage falls below $0.5\,pu$, the system must supply $1.0\,pu$ reactive current. Thus, the wind turbine supplies $1\,pu$ reactive power and $0\,pu$ active power. The transition from the normal state to the abnormal should be within $20\,ms$ [188].

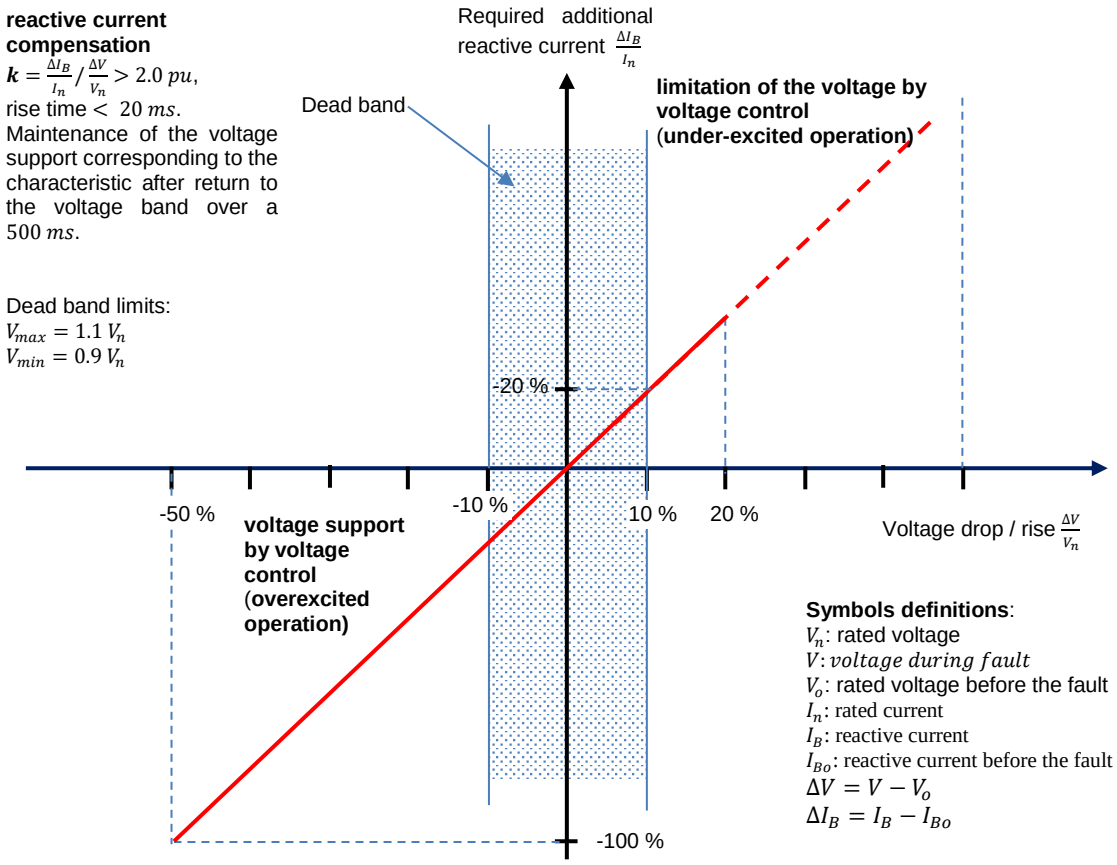


Figure 2-18 Reactive current injection requirement [185]

2.7.2 DC Faults

Several factors affect the dc system including HVDC line (cable) topology, such as symmetrical and asymmetrical monopolar. Typically, a dc fault causes a transient, which presents as a surge traveling along the cable, starting from the fault point location. MTDC network protection, however, still constitutes a major challenge. Unlike conventional point-to-point HVDC, a practical dc system needs circuit breakers (CBs) at both line ends to isolate faults selectively to maintain normal operating conditions of all other healthy system parts. To specify CB specifications in the HVDC, knowledge of full transient overvoltage and overcurrent of the fault should be understood well.

Many authors have presented dc faults in their papers. Among these, Bucher et. al. [191] provided a thorough analyses of pole-to-ground fault current and its effect on an MTDC network for a three-terminal network. Influence of various

system components on the fault current transient development and the collaboration between these modules and the circuit breaker was presented. However, this work was limited to PG faults, and it did not include the onshore grid effect on the fault. Also, their work was limited to the transient conditions, which means it is limited to several milliseconds after the fault occurrence.

Analyses of pole-to-pole and pole-to-ground in HVDC VSC-based systems can be found in [192], which suggested a recovery demand of overhead line short faults by designing system grounding, transformer modification, and monopolar topology adaptation. However, a point-to-point topology system was investigated in that work, and hence the effect of adjacent cable was not included, and no focus was placed on the ac side in terms of analyses, particularly in the first tens of milliseconds.

Yousefpoor and Kim [193] studied dc faults in MTDC and suggested a control method to manage VSCs based on voltage droop and a dead-band controller. They aimed to avoid the use of CBs by isolating the converter. However, VSCs are provided by an anti-parallel diode, which continues conducting during the transient, and includes the contribution of capacitive sources such as dc capacitor and cable capacitance. Furthermore, their second publication [194], with a similar droop control strategy and either master slave or dead band control, deals with the loss of the terminal station. Unlike master slave, dead band control enables the MTDC to operate satisfactorily with the loss of the master station.

2.7.3 AC Faults

Two types of faults can be studied in MTDC systems and can be found in the literature: ac and dc faults. Fault analysis in the ac power system and the protection/isolation devices is now considered as a mature technology [105,195, p.60]. However, the rise rate of dc faults is much higher than that for ac faults, which is limited by the circuit impedance. Therefore, protection against dc faults should be faster—approximately $1\ ms$ [90, pp.234–241]. Ac grid faults generally are divided into balanced and unbalanced faults. Moreover, to obtain VSC transmission advantages, several technology advances are necessary. This

requirement is the ability of VSC to operate in severe conditions such as dc fault and unbalanced grid fault [196].

The output of the converter has no ripple in the case of balanced and sinusoidal input waveform, except the harmonics that are caused by the switching of valves. However, if the voltage is unbalanced, then low-frequency harmonics exist in both input and output waveforms, causing a distorted signal, and this may affect some sensitive devices such as medical instruments [160]. The controller needs to deal with this unbalance, therefore many authors has proposed a control strategy to operate in such conditions.

For example, in [103], a dual control strategy was employed to control the dc voltage in the outer control loop and to control the current in the inner control loop for both negative and positive dq currents in the SRF [94]. However, there was no control on the reactive power. Therefore, this thesis proposed adding reactive power control alongside the dc voltage in the outer control loop to account for the unbalanced conditions. Thus, the outer controllers control both dc voltage and reactive power in the grid-side VSC. This control scheme may be considered as a generalised control strategy (GCS), which can be used for both balanced and unbalanced conditions and deals controls the reactive power. This is beneficial specially for unbalanced load that can be found for example in residential distribution network or during unbalanced ac faults.

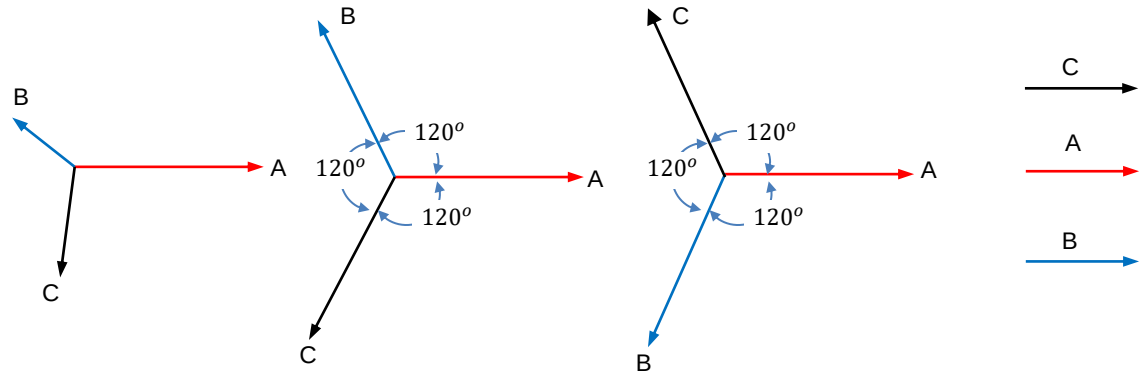
- **Symmetrical Three-Phase Fault**

A three-phase symmetrical fault (also called a balanced fault) occurs when a short circuit involves all three line-conductors and also may involve the ground. The fault impedances Z_f can be any value, but when $Z_f = 0$, the fault is called a solid fault. Therefore, such faults can be either (I) three line-to-ground fault or (II) three-line fault (without ground connection). These types of faults are called balanced faults because all three phases are affected equally. In addition, the analysis of the fault could be done on a per-phase basis, the same way as the normal operation. However, the behaviour of both fault types is identical as a result of the balanced nature of the fault, although the fault is severe, especially

when $Z_f = 0$. This type of fault is less frequent than the other fault types, and it accounts for about 5% of the total system faults.

- **Unsymmetrical Faults**

Most network faults generally cause voltage dips and present symmetrical components in the system. Symmetrical components are a representation of an unbalanced n-phase system by n-group of symmetrical phases. For example, a three-phase unbalanced system is converted into three groups of 3-phase balanced systems. These three groups are negative-, positive-, and zero-sequence components, which rotate clockwise (same as the source rotation), counter clockwise (opposite to the source rotation), and unrotated, respectively, as shown in Figure 2-19. Therefore, it is reasonable to include these symmetrical components in the control system of voltage source converters which are connected to that system [197].



(a) Source phasor diagram (b) Positive sequence (c) Negative sequence (d) Zero sequence

Figure 2-19 Symmetrical component phasor representation

Hence, control under the unbalanced ac fault will require dealing with symmetrical components. Symmetrical components are typically used to simplify the complexity of the study under such faults. However, a control system is typically constituted by using a dq reference frame. Therefore, the controller requires these symmetrical components to be separated into negative dq and positive dq accordingly.

Due to the separated symmetrical components, the controller needs to be separated, in turn, for each group of dq components, which means that the controller needs to be constructed for the two groups: one for positive dq and one for negative dq to account for unbalanced current due to abnormal operating conditions. Therefore, a dual-current controller was proposed in 1999 by Song and Nam [94] to deal with the ripple components that appear in the dc link voltage to account for the unbalanced source of voltage. Thus, a separate control for each of the negative and positive sequence components was used in the model.

The negative [198] and positive sequence can be separated using two methodologies [199]. The first one is determined by taking into consideration the fact that the negative sequence component of the current appears as a double frequency (2ω) in the positive sequence synchronous frame, which should be controlled and eliminated by the controller. In other words, i_{dq}^{p} is dc while i_{dq}^{n} is ac with 2ω frequency in the positive synchronous frame. Alternatively, in the negative synchronous frame, the situation is reversed (i.e. i_{dq}^{n} is dc and i_{dq}^{p} is ac with 2ω frequency) [200]. Hence, connecting a notch filter (NF) eliminated the negative sequence and left the positive dq sequence [98]. The same can be done to eliminate the positive sequence to obtain the negative sequence.

The second method of separating the positive dq component and the negative sequence component is carried out by delayed signal cancellation (DSC) [201,202]. Many algorithms were used to implement DSC. All of these algorithms were implemented by using a delay of one-fourth of the signal and adding the delayed signal to the input signal to obtain the results.

2.8 Fault Protection

Protection of an MTDC system has significant importance in VSC-based HVDC since VSCs are vulnerable to dc faults due to large discharge currents of the dc capacitor. Hence, fault current interruption is necessary before exceeding the thermal limit values of the semiconductor devices connected to the system.

Typically, dc fault current increases to a large value within a short time, which requires a fast fault detection algorithm and fast circuit breakers. Thus, Bucher and Frank showed that the capacitance discharge of the filter (which is measured by $5\ ms$) and cable are the dominant current during the first $10\ ms$. In addition, the in-feed from the ac side contributes and dominants to the fault current after $10\ ms$ [203]. However, the first peak of fault current is reduced by reducing the dc capacitor size, which means changing the converter topology. Furthermore, the reduction of in-feed current from the ac grid side is accomplished by increasing the phase reactor impedance between the transformer and the converter [203].

The fault current interruption generally needs a detection algorithm, which may or may not depend on a communication network to provide information about the system status at different parts of the network. The detection algorithm should to be able to determine that a fault occurs in a certain part within a short time. After the fault detection, the circuit breakers should respond to the fault quickly. However, today's technology can provide circuit breakers that respond within approximately $0.2\ ms$. Table 2-6 summarises dc circuit breaker characteristics [204].

Table 2-6 Dc circuit breaker summary survey

	Traditional CB with arrester	Hybrid circuit breaker	Solid state CB without auxiliary circuit
Arc / PE	Arc chamber	PE	PE
Breaker time	$40\ ms$ ($20\ ms$ for oscillation + $20\ ms$ arcing)	About $2\ ms$	About $0.2\ ms$
On-state resistance	negligible	<5 mΩ	100 mΩ estimated
Maximum current	4-5 kA	5-10 kA	~ 6 kA

Circuit breakers that are used in MTDC adopt active or passive oscillating structure, which contains an oscillating circuit to produce oscillating current to achieve zero crossing point current [204]. However, in ac systems, the zero current is naturally occurring where the current is interrupted. In a dc system,

there are no naturalzero crossing points; therefore, it is necessary to produce such points artificially by forcing the current to zero. Two methods can be used to achieve zero current. The first is by imposing an oscillatory current on top of the dc current that has greater amplitude than the dc current. The second is by inserting a series voltage source to opposite the supply voltage; hence, the current becomes zero [205].

2.9 HVDC TOPOLOGY

An HVDC power system is an efficient and flexible way to transmit a bulk amount of electrical energy over long distances. Since its introduction, the use of HVDC was limited due to the difficulty in connecting two areas by a single converter and single inverter linked by a dc cable. Today, a significant amount of renewable energy sources, such as windfarms, are connected to the power systems. Because of this, the concept of connecting more than one windfarm together to create a multiterminal HVDC (MTDC) was introduced. The first MTDC was initiated in 2013 in Nanao, China, with the Nanao multi-terminal VSC-HVDC project [127,128].

This chapter contains two sections after the introduction: the first section addresses HVDC transmission topologies, and the second section describes MTDC topologies, specifically. However, both sections will provide information about HVDC topologies and the effect of each topology on the system behaviour in normal and fault operation conditions to help in selecting suitable topology.

2.10 HVDC Transmission Topologies

Many topologies are suitable for the use in HVDC systems. Due to dc voltage characteristics, such as unidirectional voltage and fixed polarity of the line voltage, several topologies are possible. These topologies can be found in the following configurations, and are based on the type of transmission line that links the rectifier and inverter, such as monopolar, bipolar, back-to-back, and multiterminal. Several configurations are available for the topology of the overall HVDC systems, such as point-to-point (PPT), general ring, star, and central switching ring in a star topology.

2.10.1 Monopolar

The simplest HVDC topology is the monopolar topology. Monopolar topology can use one conductor line or cable. Monopolar generally can be either symmetrical or unsymmetrical monopole, as shown in Figure 2-20 [206] and Figure 2-21, which illustrate a single conductor transmission line that is used to

connect the Cahora-Bassa – Apollo HVDC link, which transmits 1920 MW at ±533 kV over 1,420 km (880 mi) [207].

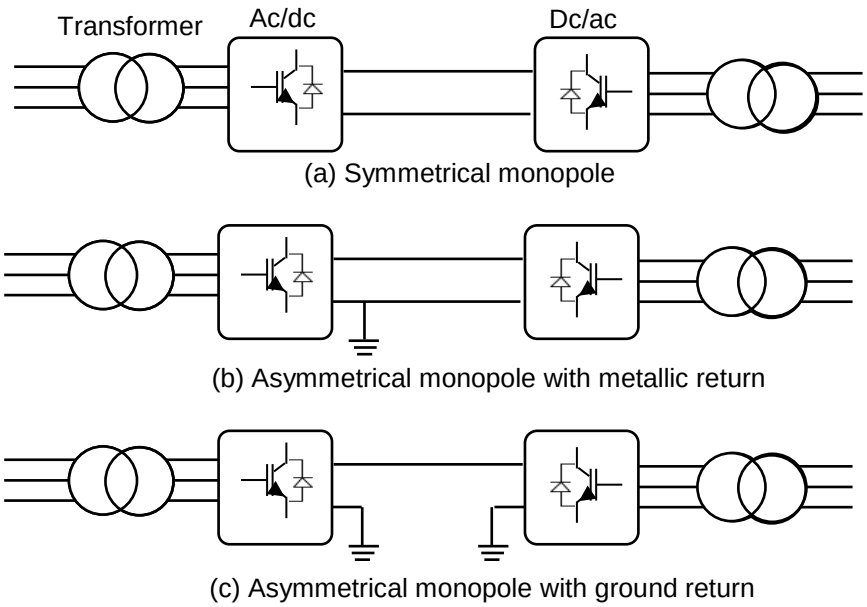


Figure 2-20 Monopole HVDC transmission types

Figure 2-21 Apollo monopolar converter station [208]

The monopolar topology is found in the following types:

- **Symmetric Monopolar**

This topology typically consists of two conductors: one for the positive voltage and one for the negative voltage. Figure 2-20a depicts a symmetric monopole topology. This topology has several advantages, including: no in-feed of the fault currents from the ac side network in the case of dc PG faults, transformers are not subjected to dc stresses, and ground dc current is not present.

However, the monopole topology also has disadvantages: its redundancy is limited in comparison with a bipolar structure, and it requires two dc lines that should be insulated completely.

- **Asymmetric Monopole with Metallic Return**

This topology uses the same configuration as the symmetric monopole except the return path is grounded in the former; hence, it is called asymmetric monopole with metallic return conductor which is grounded. In this configuration, one terminal is used to transfer the power between the rectifier and the inverter, while the other pole is connected to the earth. Therefore, there is no need to insulate the return conductor. Figure 2-20b shows a simple asymmetric monopole with metallic return. Several advantages can be gained using this topology:

- The metallic return, when used, does not require full insulation to the dc conductor return path.
- Future expansion to a bipolar scheme is possible.
- There is no ground dc current.

- **Asymmetric Monopole with Ground Return**

A schematic diagram of this structure is illustrated in Figure 2-20c. Unlike the previous structure, no metallic return is used here; instead, this topology uses the ground as return path. Beside its simplicity, it has two advantages: losses and cost are minimised because of the use of a single dc line, and the expansion to a bipolar scheme is possible for future expansion if required.

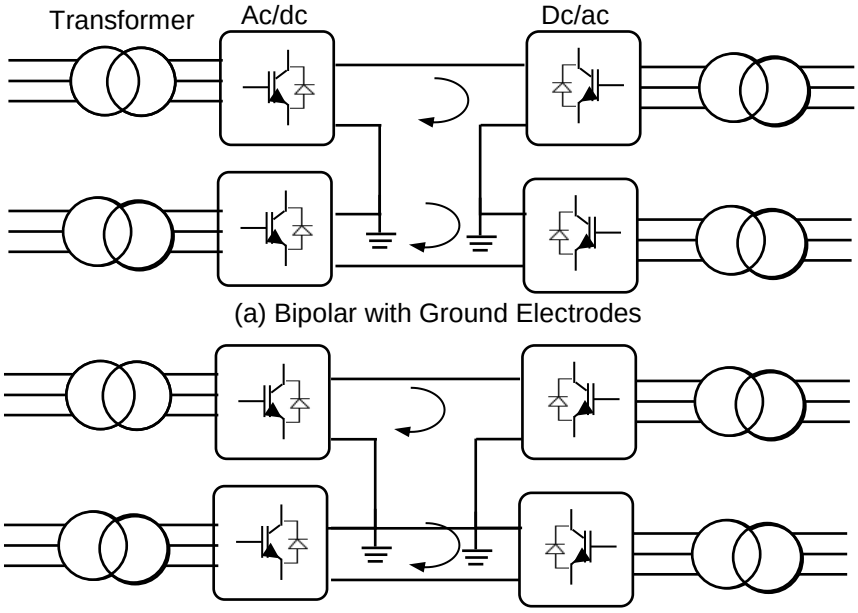
However, the use of this structure leads to several disadvantages, which can be summarised in the following points:

- Permission for continuous operation is required because of ground dc current.
- Permission for ground electrodes is required due to environmental impacts.
- The neighbouring ac network in-feeds the dc PG fault current.
- Structure has limited redundancy compared with bipolar topology.

- Transformers must be designed to withstand dc stresses.

2.10.2 Bipolar

A schematic diagram of a bipolar transmission topology is shown in Figure 2-22, which presents two bipolar configurations: bipolar with ground electrodes (or asymmetric bipolar), and bipolar with metallic neutral (or symmetric bipolar) [206]. Figure 2-23 shows a bipolar transmission line.



(a) Bipolar with Ground Electrodes

(b) Bipolar with Metallic neutral

Figure 2-22 Bipolar HVDC transmission

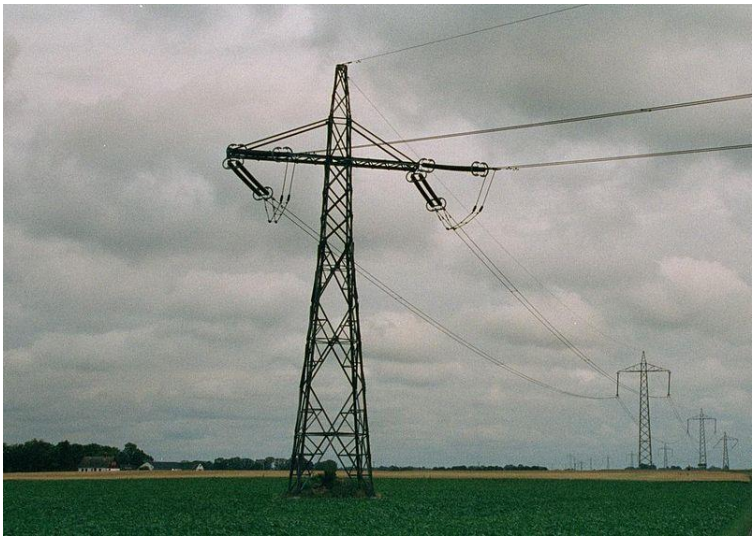


Figure 2-23 Bipolar system pylons of the Baltic-Cable-HVDC in Sweden [209, p.49]

In this configuration, two conductors operate at high potential compared to ground. In normal operating conditions, the positive pole current is equal to that of the negative pole, and no current will pass through the ground return.

- **Bipolar with Ground Electrodes**

Figure 2-22a illustrates a simple system of a bipolar conductor with ground return. The advantage that gives a 50% redundancy of the total system rating is offered by this topology. The disadvantages are summarised as follows:

- Costs more than monopolar configurations with same rating.
- Continuous operation requires permission for ground dc current.
- Permission is required because of potential environmental impacts of electrodes.
- The neighbouring ac network in-feeds the dc PG fault current.
- Transformers must be designed to withstand dc stresses.

- **Bipolar with Metallic Electrodes**

Figure 2-22b shows this type of bipolar configuration, which costs more than the metallic return. This topology has the advantage that it provides 50% of the total system rating redundancy. The disadvantages of this topology are:

- It costs more than monopolar configurations for the same rating.
- Neutral dc conductor needs insulation for low voltage.
- Transformers must be designed to withstand dc stresses.

However, bipolar topology can be modified to be homopolar dc link topology by reversing the polarity of the bottom pairs [210, p.13], as shown in Figure 2-24.

However, in homopolar configuration, the two poles have the same return path. Therefore, the return path current is double the current of the line pole current ($2I_d$). Therefore, this topology has not been used in any actual HVDC system installation, and most installations used in point-to-point systems are bipolar and operated as monopolar topology under contingency situations [90, p.19].

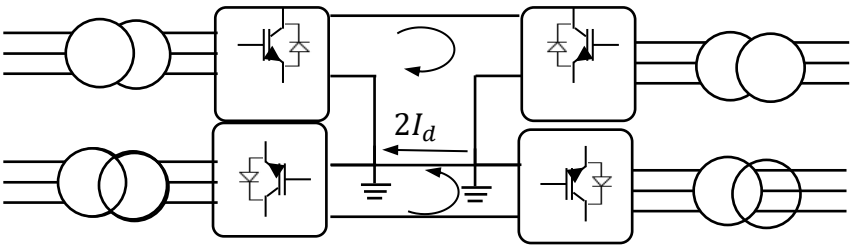


Figure 2-24 Homopolar HVDC transmission topology

2.10.3 Back-to-back

When both the rectifier and the inverter are sited in the same place or station, this topology is back-to-back (B2B) topology. Usually the rectifier and inverter is connected by a dc link cable, and the length of the dc cable is kept as short as possible. B2B topology has two stages: the first stage is the rectification of the ac input into a dc voltage, and the second stage is the inversion of the dc voltage back into constant amplitude and frequency ac voltage output. This configuration is typically used in wind turbines to produce fixed amplitude and frequency ac voltage output even if the ac input is not constant because of changing wind speed. Therefore, the wind turbines give constant output, and the gear box can be eliminated; the wind turbine is called variable speed wind turbine with direct driven generator. Moreover, this topology is also used to connect ac power systems of two different frequencies (for example, two networks that operate at two different frequencies). Thus, B2B enables the wind turbines to operate as variable-speed wind turbines, in contrast to fix-speed wind turbines which require a gear box to keep the generator speed constant. Therefore, this configuration is considered to be an ac/ac converter.

A B2B station generally has somewhat simpler construction than the transmission projects. The dc voltage level may be selected at any voltage level, but it is typically set at approximately 320 kV. However, the optimum voltage level value may be decided according to capital cost, transmission losses, and the amount of power to be transmitted. As in ac systems, dc power can be transmitted using cables or overhead transmission line, whereas for B2B converters, power is usually transmitted via dc cable. The smoothing reactor is

the primary equipment at the ac side. The control system may be simplified as well; because of the short distance between the rectifier and inverter, no telecommunication equipment is required between the inverter and rectifier.

2.10.4 **Multiterminal**

With the increasing number of windfarms, multiterminal HVDC topology could be used. In this configuration, two or more converter stations, such as two windfarms, are connected together via a submarine cable or an overhead transmission line. Instead of connecting a windfarm to the onshore grid using point-to-point connection (as shown in Figure 2-26), which means connecting one rectifier to one inverter, MTDC is used to gather the power generated from two or more windfarms and transmitting the resulting power to the onshore grid. An example of a three-terminal MTDC based on symmetrical monopole is illustrated in Figure 2-25.

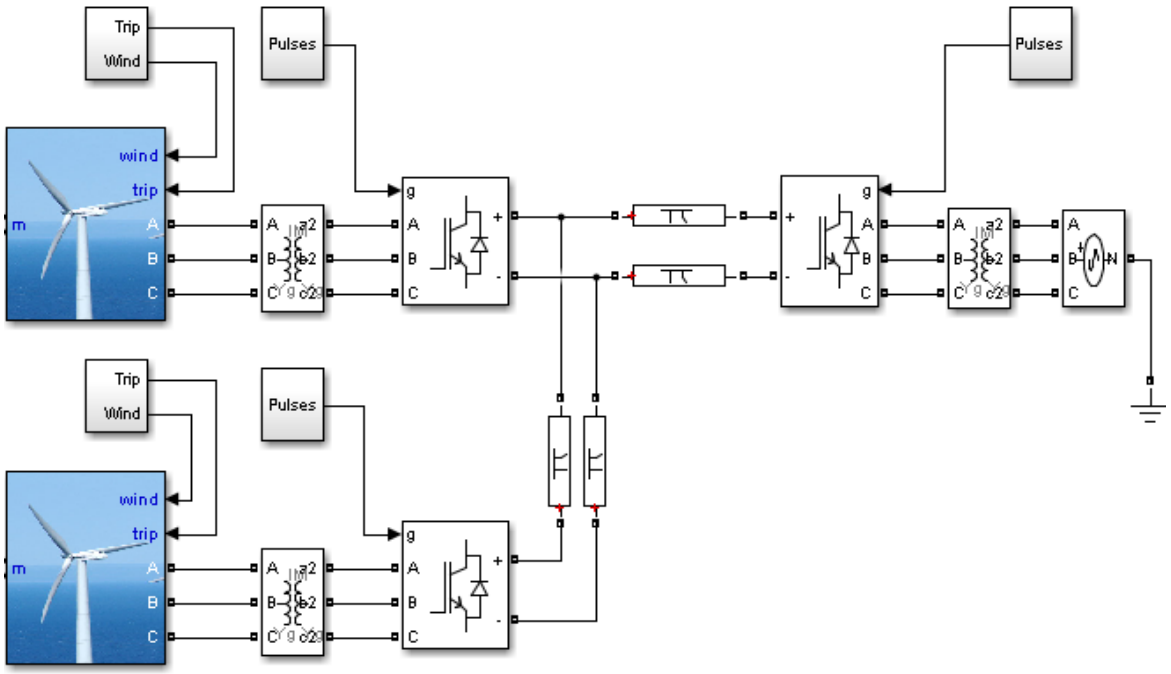


Figure 2-25 Example of a multiterminal HVDC network

2.11 Multiterminal Direct Current Topologies

Various topologies of multiterminal HVDC systems might be used to send electric energy from offshore windfarms to the onshore grid. The basic

requirements to assess these topologies are reliability, security, and installation and transmission costs. Some configurations have been used in ac networks for many years [26]. The HVDC grid topology selection is connected to the converter and dc faults characteristics.

2.11.1 Point-to-Point Configuration

The first and simplest configuration is the point-to-point configuration (PPT). This topology is illustrated in Figure 2-26 [26], which is a schematic diagram showing a four-PPT connections. In the case of failure in the converter or HVDC circuit breaker, faulty part (or faulty line) isolation is the proper action and could be done by opening the onshore ac CB of the grid and allow the wind turbine trip-off to go on to increase the rotational speed (over-speed) or enable dc link over-voltages [26].

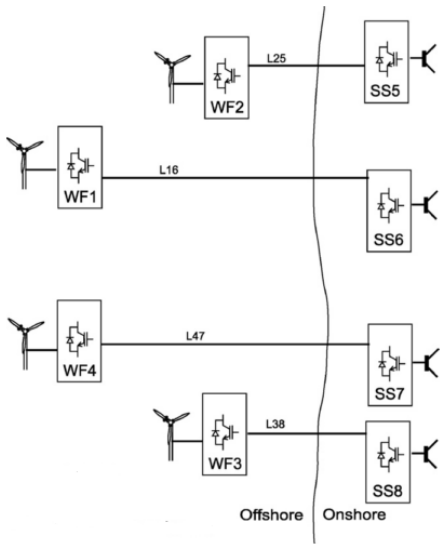


Figure 2-26 Four-point-to-point topology [26]

If maximum power criteria loss is encountered, then there is no need to use HVDC CBs. A line fault leads to the loss of the windfarm connected to that line. Consequently, this topology is inflexible.

2.11.2 General Ring Topology

This configuration is a multiterminal HVDC network topology (see Figure 2-27) because it connects more than one windfarm (converter). The dc lines, which

are generally cables in offshore windfarm applications, are connected to all buses in the system constituting a loop. Thus, there is a line or more which must transmit the total power generated by all offshore windfarms of the grid if the loop is disconnected from one side. The ring topology could operate as a closed ring, which is the normal operation mode, by closing all the isolators and circuit breakers, or it can operate as an open loop by opening one isolator or circuit breaker in the ring.

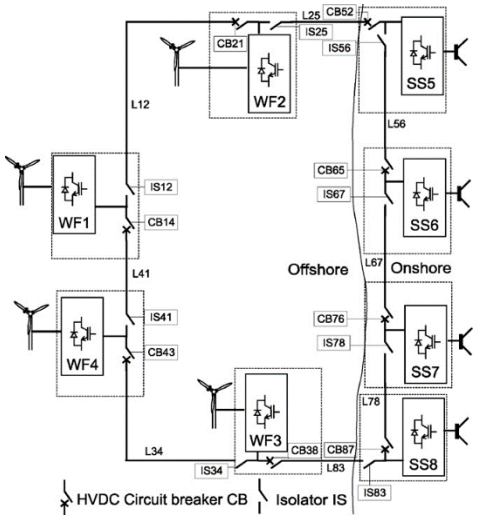


Figure 2-27 General ring topology showing four windfarms [26]

If a dc grid fault or a converter fault is detected, the first action is isolating the faulty part by opening the dc CBs that are connected to the two-faulted line end, and making the system operate as an open loop. Then, when the current of the fault becomes zero, the isolators will isolate the faulty part and the proper CBs will be reconnected. Figure 2-28 shows an example to illustrate this operation. This configuration is flexible, but due to the need for some lines to operate at full power rating, it results in some extra cost. If a maintenance or long-term HVDC faults occur, the network can operate as open loop. Furthermore, communications are required to enable the CBs to organise and isolate only the faulty areas.

Clearly, the isolators could be replaced by solid-state HVDC CBs. Although this will increase the cost, the power supplied from WF1 will be delivered continuously.

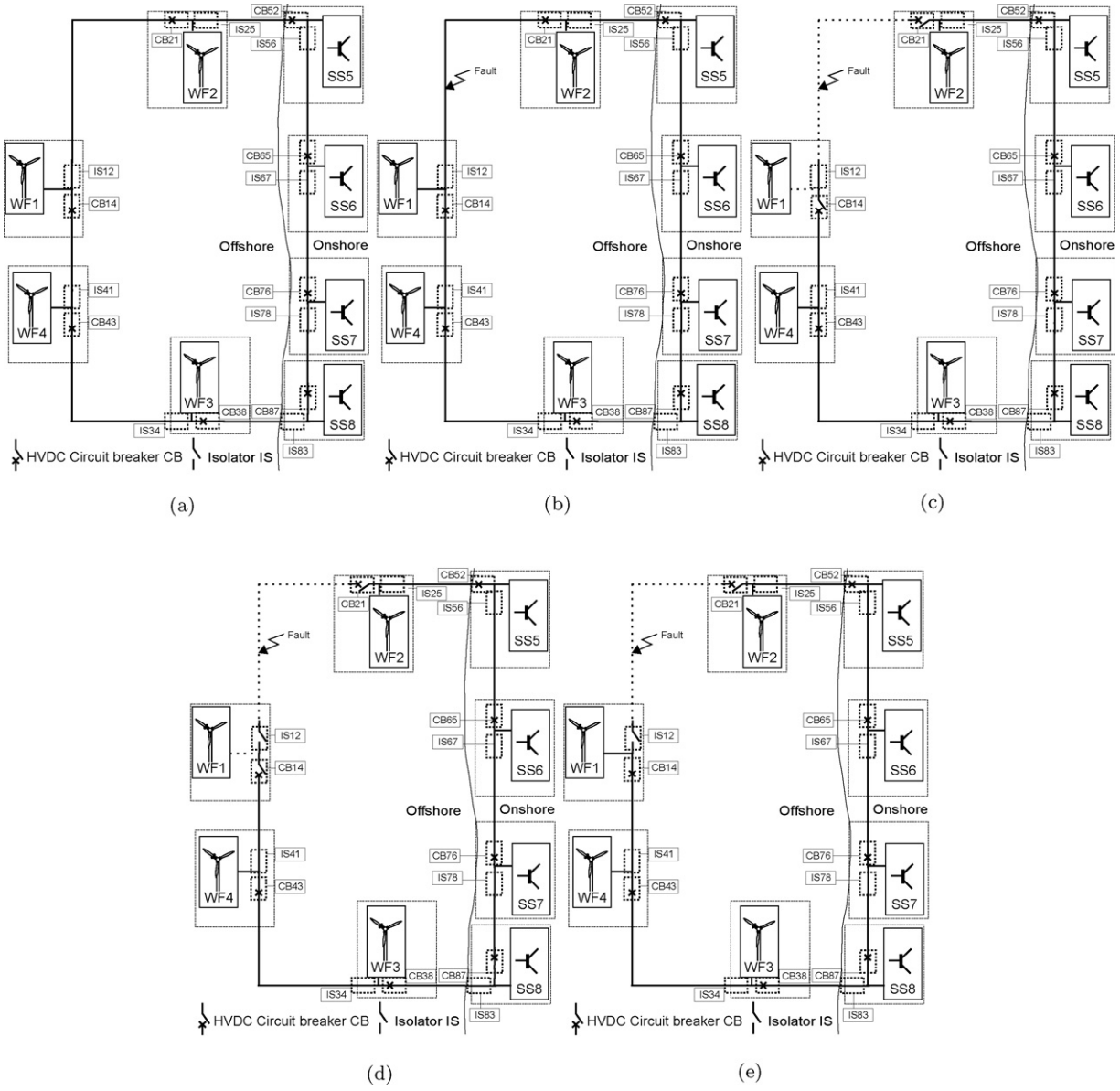


Figure 2-28 Line fault operation of a ring topology: (a) normal operation, (b) line 12 fault at t_0, (c) open circuit breakers CB21 and CB14 at t_1, (d) isolator IS12 opens at t_2, (e) t_3 closing CB14 to re-establish the windfarm 1 connection [26]

The following steps show the operation of the system illustrated in Figure 2-28.

1. Figure 2-28a is a closed ring showing normal operation.
2. At $t = t_0$, a fault occurs in L_{12} (Figure 2-28b).
3. At $t = t_1$, the ring is opened, losing WF1 (Figure 2-28c).
4. At $t = t_2$, isolator IS12 is opened (Figure 2-28d).
5. At $t = t_3$, CB14 is closed to connect WF1 (Figure 2-28e).

2.11.3 Star Topology

Figure 2-29 shows a schematic diagram of a star topology. This topology is an MTDC system in which all windfarms are connected directly to a central node. In such configurations, all ratings of the lines or cables match the windfarm-generated power rating that connects it, which reduces the cost. The main disadvantage of star topology is that the loss of the central point will lead to the loss of the entire system. Therefore, despite the many advantages offered by star topology, it can be considered an infeasible multiterminal configuration for wind farm connections [26].

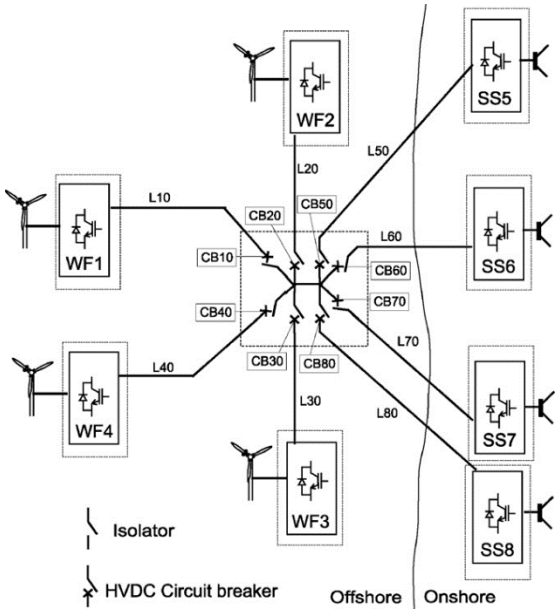


Figure 2-29 Star topology [26]

A converter and dc faults can be disconnected by opening the related link with the help of the HVDC CB. The star configuration requires an offshore platform to be built and located in the central point to incorporate all CBs and the connections of the star node. This configuration is not as flexible as ring topology because of the permanent loss of the entire system in the case of a central point loss.

2.11.4 Central Switching Ring in a Star Topology

This type of topology is a combination of the previous two topologies, the general ring and the star topology, to constitute a hybrid configuration. This

topology is shown in Figure 2-30. The configuration is actually a star topology, and the connection of the central point is via a switching ring. Such a topology overcomes all the disadvantages of the general ring and the star topologies. The full rating of power is needed only in the central ring; the circular line length is kept to the minimum possible value, and the system separates faults while keeping the criteria of minimum power loss seen. The main negative point of this topology is its need for an offshore platform to place all CBs in the central ring.

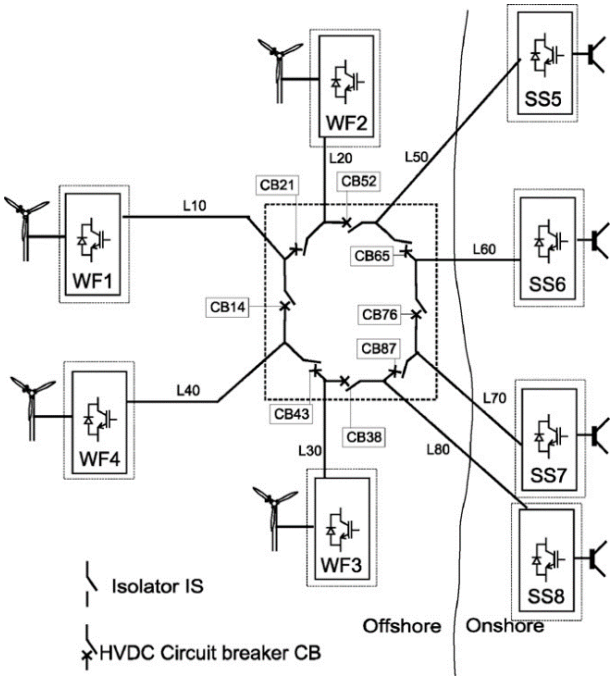


Figure 2-30 Central switching ring in a star configuration [26]

Line capacities of the central ring must be equivalent to the total amount of power that is generated by all subsystems (offshore windfarms). Furthermore, the central switching ring shows flexible operation for long- and short-term faults of HVDC. Similar to star topology, this topology has the same problem regarding a long-lasting fault in the line resulting in a full windfarm loss connected through that line from the central point.

2.12 Summary

This chapter introduced the literature survey about the contents of future chapters. After a simple introduction about the chapter, VSC was described as

an answer to avoid the difficulties of other technologies. Then, an HVDC overview was included to give a general idea about HVDC, which includes two technologies and gives a summary of the existing projects that use VSC since its first introduction. Both types of HVDC technologies were included in the next section, and a variety of VSC topologies were introduced. A 3-level converter topology was chosen, designed, and implemented; this topology satisfies the requirements for the model; however, any other topology can be used. A vector control strategy was used because of its ability to control active power (P) and reactive power (Q), or control the reactive power and dc voltage (V_{dc}). In the proposed model, one converter, the grid side converter, was used to control V_{dc} ; the other two converters controlled the P and Q to ensure delivery of the power produced by the windfarms. Different topologies was considered in the last two sections. A star topology was used in this thesis as a proposed model.

The grid code was studied because it is necessary to know the boundaries and the limits for safe operation when dealing with faults and protection. Despite the variety of grid codes available, the grid code by E.ON was chosen due to its simplicity and the fact that it provide a good level of safe operation.

HVDC transmission topologies was introduced and discussed from the point of view of cost, expandability and fault behaviour. Various MTDC networks topologies was presented and discussed based on cost, reliability, and fault isolation techniques. However, the choice of a topology is affected by many factors including the environment impact, geography, and the availability and the distance to the grid connection.

The proposed model in this thesis was based on a novel converter topology of two diode rectifiers connected in series with a VSC to implement MTDC. Fault analyses studies (both dc and ac) are presented for the proposed model. A generalised control scheme is also presented to control the reactive power in the outer loop to deal with unbalanced ac conditions such as single line to ground fault in the ac grid side of the converter.

3 MTDC DESIGN AND CONTROL

3.1 Introduction

Offshore windfarm (OWF) constructions have already begun. Approximately 100 GW of wind power is expected to be built by 2030 in the north sea [211]. Of the total number of 80 OWF installations around the globe, 33 (approximately 41%) were installed in the North Sea.

Power flow control of a multiterminal HVDC transmission system is considered one of the most essential tasks performed by the VSC-HVDC, as direct voltage control of an HVDC link is crucial to ensure balancing of power flow amongst all connected nodes [1].

Point-to-point HVDC system control is generally set in a way such that one terminal is designed to control the dc voltage of the dc cable and the other terminal controls the current or the power. This strategy of control (i.e. having one converter to control the dc voltage only) can be drawn-out to multiterminal systems. However, by allowing only one terminal to be responsible for voltage regulation, power balance cannot be guaranteed and will be progressively more difficult when the MTDC system grows. Therefore, for large MTDC grids, having one terminal control the voltage is not preferred. Thus, MTDC grids necessitate a good control strategy for sharing the control of the dc voltage of the network amongst the other nodes, in order to develop and operate the system successfully and securely.

Many control strategies were submitted in the literature for proper operation of multiterminal system. Four different direct voltage control approaches that suit multiterminal operation were analysed and compared according to their capability of performing different market dispatch schemes in [212, pp.44–56].

This chapter introduces the proposed system model overview and the control methodologies for wind farm and grid-side VSC control. In addition, control techniques such as droop and priority control that are suitable for MTDC are presented.

3.2 Proposed System Overview

The schematic diagram in Figure 3-1 illustrates the proposed system. The model includes two offshore windfarms that generate 360 MW power each. Power of each OWF is converted by a windfarm-side VSC (WFVSC). The VSC model is constructed by a series connection of two diode rectifiers and a VSC, and each rectifier is responsible for converting one-third of the total power and one-third of the voltage. This means that 120 MW is converted by each rectifier. However, series connection enables the dc voltages from rectifiers to be summed. One-third of voltage is rectified by the VSC to ensure controllability of the total voltage of the dc cable. Then, dc power is transmitted to the onshore side via submarine dc cable, which is represented by a Π section equivalent circuit and modelled as a symmetrical monopole. Then, at the receiving end, which is located at the onshore side, a grid side inverter (GSVSC) is used to convert the dc power into ac before connection to the ac grid to supply the generated power to the onshore grid. A swing bus is the final step of the model to represent the onshore grid.

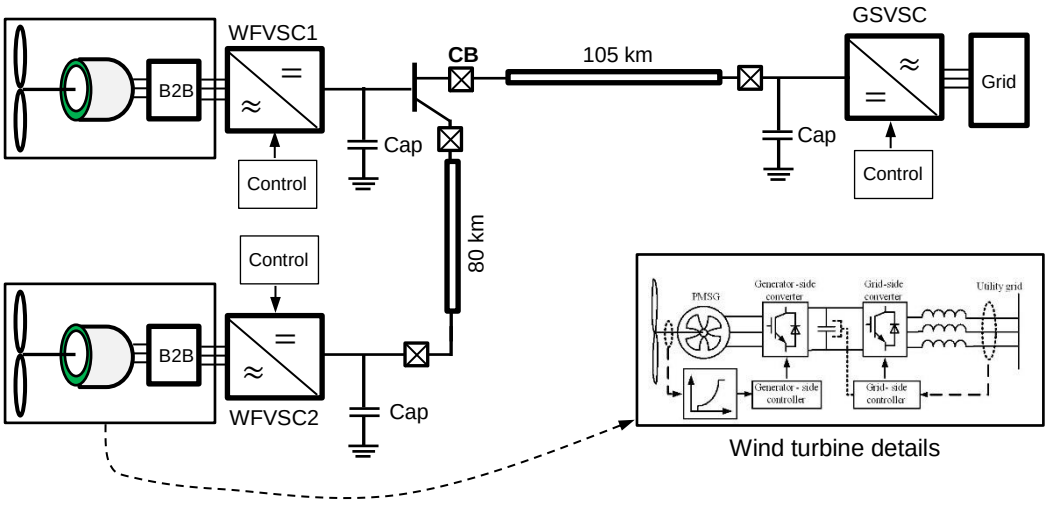


Figure 3-1 Power transmitted from WFVSC-DR to GSVSC by cable

Figure 3-2 shows a detailed schematic diagram for the WFVSC1 and WFVSC2 models, which have a similar design. The transformers are connected as Y/Δ with grounded neutral for the VSC and Y/Y-Δ for the diode rectifiers to benefit

from the $30°$ phase-shift angle between the Y and Δ secondary coils to eliminate the fifth and seventh harmonics.

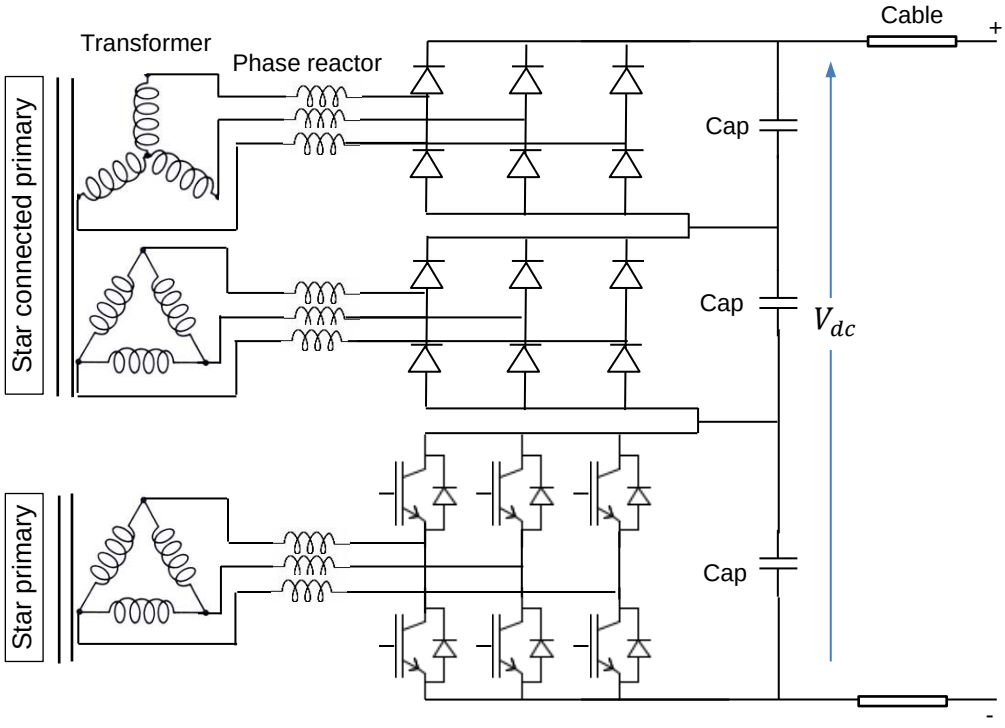


Figure 3-2 Detailed model for VSC-DR connection

The subsea dc cable model that was used in the simulations is based on a MATLAB/Simulink block. For instance, the cable parameters, including cable

Table 3-1 Dc cable parameters

Parameters	Value	
	Coper	Aluminium
Cross sectional area	1000 mm^2	2000 mm^2
Continuous power rating	315.23 MW	370 MW
Dc resistance at 20ºC	0.0176 Ω/km	0.0149 Ω/km
Ac resistance at 20ºC	0.024 Ω/km	0.020 Ω/km
Outer diameter	103 mm	114 mm
Material	Coper	Aluminium
Capacitance	0.22 µF/km	0.29 µF/km
Reactance (metallic sheath closed) 0.15 m spacing (50 Hz frequency)	0.159 Ω/km	0.131 Ω/km
Reactance (metallic sheath open) 0.15 m spacing (50 Hz frequency)	0.164 Ω/km	0.136 Ω/km

radius and operating voltage level, were taken from an actual XLPE (cross-linked polyethylene), $\pm 362\ kv$, 315 MW VSC-HVDC submarine cable [213,214].

The cable parameters are summarised in Table 3-1. This 105-km-long cable is a submarine cable that links Estonia and Finland (Estlink) [140,215,216, pp.1–16]. The cable parameters can be scaled up to the required operating voltage for a $\pm 320\ kV$ cable without changing the electric field intensity. The cable main insulation is typically extruded by thin layers of semiconducting material on both outer and inner surfaces to prevent electric field concentration between the insulation and the conductor and to provide a smooth interface for the electric field [217, p.12].

3.3 VSC Control – Steady-State Conditions

3.3.1 VSC Theory of Operation

Unlike LCC technology, VSCs use self-commutated valves such as IGBT or GTO. Self-commutation enables VSCs to be turned on or off, as required, at relatively high frequency, while LCC, which is based on a thyristor, can be turned on one time per cycle only. Due to the ability to operate at high frequency, VSCs are able to modulate the output to produce nearly sinusoidal output voltage (current) and also control the power factor by the ability to control active and reactive power [210, pp.27–28]. A general schematic diagram of a VSC is illustrated in Figure 3-3. Point x in this figure refers to the PCC of the ac network. This point is considered as a measuring point reference for ac quantities such as voltage, current frequency, and angle. The point is measured by phase locked loops (PLL) and therefore is considered as a reference point of VSC.

The application of Kirchhoff's voltage law between points x and c gives

$$v_{x\_ac} - v_{c\_abc} = R i_{abc} + \frac{L\, i_{abc}}{dt} \qquad \textbf{(3-1)}$$

where R and L represent the total resistance and the total inductance of both the transformer and the phase reactor, respectively.

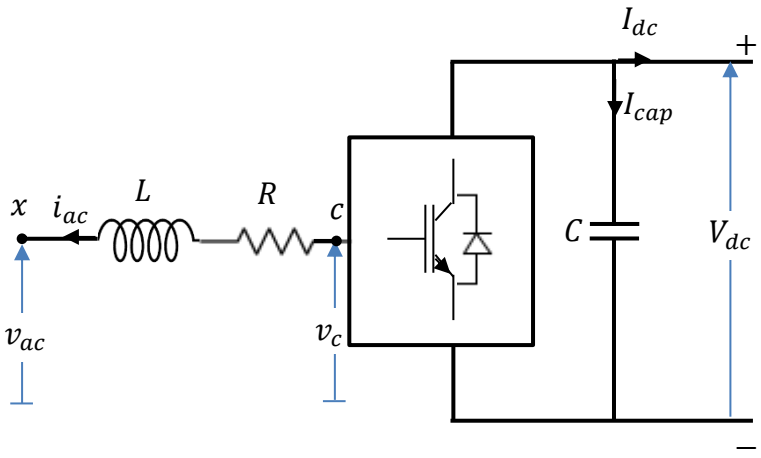


Figure 3-3 VSC circuit

Performing a Park transformation of equation (3-1) to SRF rotating reference frame ($dq-axis$) gives

$$v_{x\_dq} - v_{c\_dq} = R i_{dq} + j\omega i_{dq} + \frac{L\, i_{dq}}{dt} \tag{3-2}$$

and rearrangement and separation of (3-2) into d and q gives

$$\frac{L\, d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} v_{x\_d} \\ v_{x\_q} \end{bmatrix} - \begin{bmatrix} v_{c_d} \\ v_{c_q} \end{bmatrix} - R \begin{bmatrix} i_d \\ i_q \end{bmatrix} - j\omega \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{3-3}$$

In equation (3-3), the square matrix $\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$ is equivalent to j, which rotates the phasor by $90°$. Hence, the equivalent circuit can be given based on (3-3) in dq reference frame is shown in Figure 3-4.

The power balance between ac and dc as seen from point x in the $dq-axis$ is given by the following equation:

$$\begin{aligned} S_{x\_dq} &= \frac{3}{2}.v_{x\_dq} i_{dq}^{*} = \frac{3}{2}\left(v_{x\_d} + j v_{x\_q}\right)\left(i_d - j i_q\right) \\ &= \frac{3}{2}\left[\left(v_{x\_d} i_d + v_{x\_q} i_q\right) + j\left(v_{x\_q} i_d - v_{x\_d} i_q\right)\right] \end{aligned} \tag{3-4}$$

where S represents the apparent power and equals $S = P + jQ$; during the normal operational condition in the steady state, the exchange of the active

power between the ac- and dc-side is equal. This is written mathematically in equation (3-5) [218].

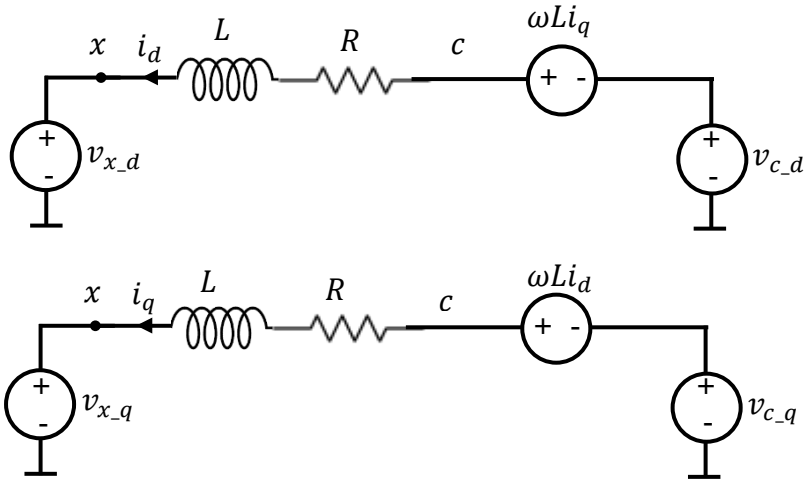


Figure 3-4 Equivalent circuit of a VSC in dq reference frame

$$P_{dq} = P_{dc} \tag{3-5}$$

$$\frac{3}{2}\left(v_{x\_d} i_d + v_{x\_q} i_q\right) = V_{dc} I_{dc} \tag{3-6}$$

which leads to

$$I_{dc} = \frac{P_{dq}}{V_{dc}} = \frac{3}{2}\frac{(v_{x\_d} i_d + v_{x\_q} i_q)}{V_{dc}} \tag{3-7}$$

The dc side output current is also related to the dc capacitor as follows:

$$I_{dc} = C.\frac{dv_{dc}}{dt} + i_L \tag{3-8}$$

If the $d-axis$ of the synchronous reference frame is chosen to be aligned with the vector of the ac voltage, then $v_q = 0$ and the instantaneous values of P and Q, which are injected or absorbed from the grid, are as follows [218]:

$$p = \frac{3}{2} v_d i_d \tag{3-9}$$

$$Q = \frac{3}{2} v_d i_q \tag{3-10}$$

Then, the converter is considered as a constant-source current supply I_{dc}, and the relationship between dc voltage and phase voltage is given by

$$v_{ph}(t) = \frac{1}{2} V_{dc} * m * \sin(\omega t + \theta) \quad \textbf{(3-11)}$$

where v_{ph} is the instantaneous phase voltage, ω is the frequency, δ is the voltage angle between points x and c, and m is the modulation index. Its value is between 0 and 1, and it is calculated for the VSC-PWM converter by [219]

$$m = \frac{2\sqrt{2} v_{ph}}{\sqrt{3} V_{dc}} \quad \textbf{(3-12)}$$

Equation (3-11) shows that the phase, frequency, and amplitude each can be independently controlled. The voltage-drop across R and L can be regulated by the voltage at point c (v_c). Hence, both P and Q can be controlled according to the following formulae [10]:

$$P = \frac{v_x v_c sin\theta}{\omega L} \quad \textbf{(3-13)}$$

$$Q = \frac{v_x (v_x - v_c cos\theta)}{\omega L} \quad \textbf{(3-14)}$$

The above equations consider the phase reactor as ideal. Figure 3-5 shows the phasor diagram for VSCs in rectifier and inverter mode. This figure explains the VSC modes of operation. For example, if v_c lags the ac system voltage v_x, the converter will operate as a rectifier and the power will flow from the ac side to the dc, and vice versa when v_c leads v_x.

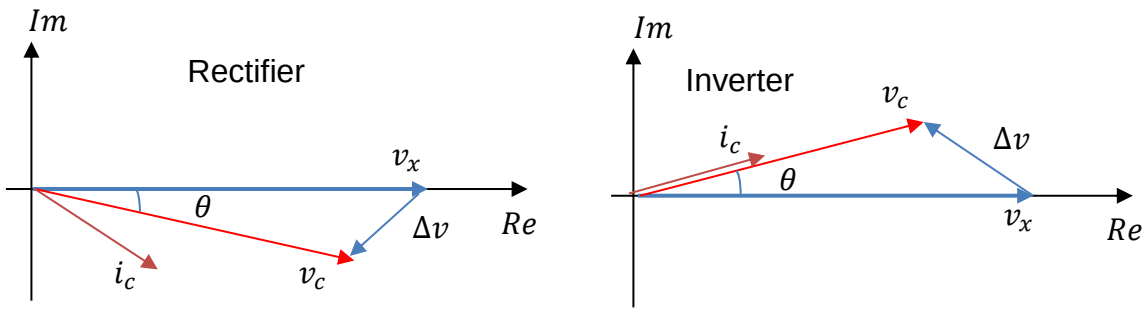


Figure 3-5 Inverter and rectifier mode phasor diagram of VSC

Moreover, if $v_x > v_c$, the VSC will consume reactive power, while for the case when $v_x < v_c$, reactive power will be generated by the converter. Figure 3-6 illustrates the $P - Q$ relationship of a VSC, where ideally VSCs can operate anywhere inside the dashed circle, which has boundaries representing $1\ pu$.

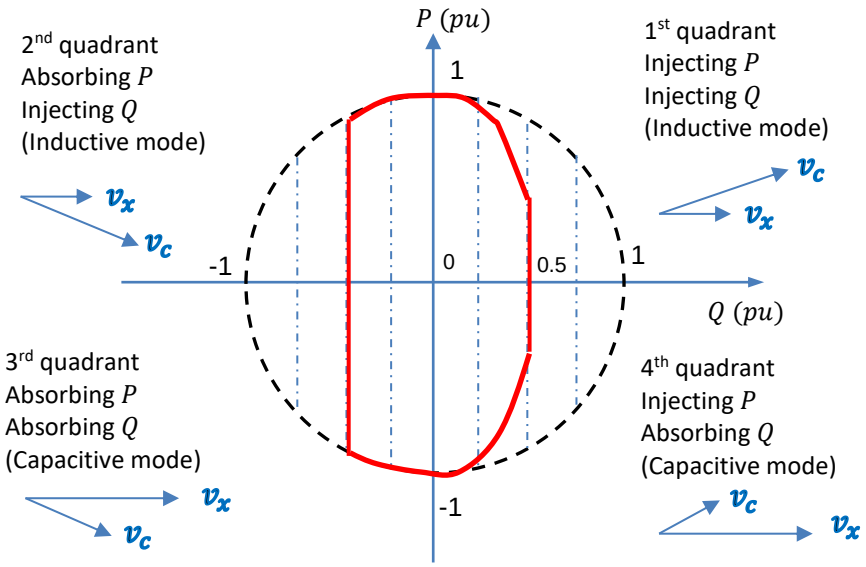


Figure 3-6 P-Q relationship in a VSC

However, in practice, real VSC operation is limited inside the red area with solid lines [206]. In a two-terminal HVDC (i.e. point-to-point connection), one terminal can be used to control the active power, while the second terminal is used to control the dc voltage. Thus, balanced conditions in terms of active power exchange will take place. Additionally, Q is used to control ac side voltage.

The operation circle can also be limited by the maximum dc voltage limitation. The reactive power depends on the voltage difference between the grid and the VSC as shown in equation (3-14). Thus, the VSC voltage dependency on the voltage of the dc link leads to limit the reactive power (Q). The Q limit varies with the grid voltage variation. High grid voltage results in a decrease in the difference of the VSC and the grid voltages, which decreases the reactive power generation.

3.3.2 Phase Reactor

VSCs are not linked to the ac grids directly, but generally are connected through a series of phase reactors, as shown in Figure 3-3. The phase reactor serves as a kind of low-pass filter, and as coupling inductive reactance for VSC network connection. Phase reactors have significant importance to the operation of VSCs due to the following purposes [10]:

- Limit fault current
- Reduce harmonic current content due to VSC switching
- Enable $P-$ and $Q-$ control by stabilising the ac current

The required phase reactor parameters must be known before the configuration of the control system of the VSC, which should be able to control both P and Q precisely. Then the combination of the transformer and the phase reactor inductances is calculated according to the impedance of the ac side of the converter as follows [10]:

$$L = L_{ph} + L_{tr} = \frac{Z_{base} x_{ph}}{\omega_o} = \frac{v_{ac}^2 x_{ph}}{2\pi f_o . S_{VSC}} \quad \textbf{(3-15)}$$

where L denotes the total inductance sum of both the phase reactor L_{ph} and the transformer L_{tr}; x_{ph} is the pu value (the effective VSC reactance value as seen by the grid is generally equal to 0.15 to $0.2\,pu$) [220], f_o is the grid frequency, S_{VSC} is the VSC active power rating, and v_{ac} is the ac rms nominal voltage. The transformer and phase reactor typically are designed to withstand stresses of high-frequency VSC voltage that appear due to IGBT switching actions.

3.3.3 AC Filter

The output ac voltage of the converter contains higher-order frequency harmonics due to the PWM switching process. However, the output voltage waveform should have a sinusoidal or nearly sinusoidal shape as a requirement; therefore, a shunt

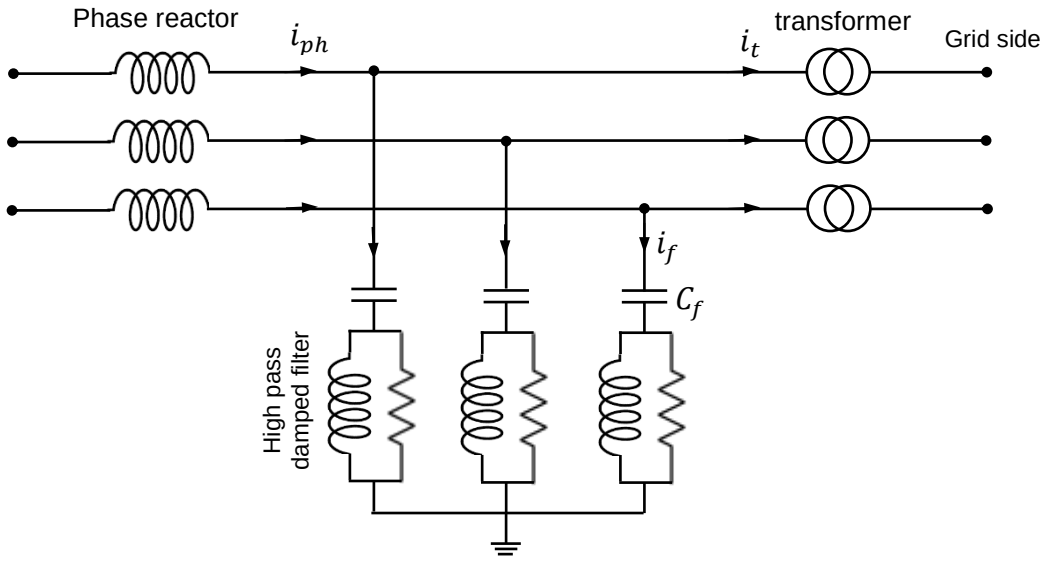


Figure 3-7 Line section showing phase reactor HPF

ac filter must be added to the VSC circuit to filter out these harmonics. Figure 3-7 shows a damping high-pass filter (HPF) situated between the transformer and the midpoint of the phase reactors. HPFs normally have low impedance to high frequency current. Therefore, a high-frequency current component (higher-order harmonics) will pass through this shunt capacitive path, which will leads filter out the harmonics from the output current [221]. The quality waveform of the voltage can be improved according to the following expression:

$$C_{filter}\frac{dv_{filter}}{dt} = i_{ph} - i_{tr} = i_{filter} \quad \textbf{(3-16)}$$

where C_{filter} represents the capacitance of the filter; v_{filter} is the midpoint voltage between transformer and reactor; i_{ph} is the phase current of the reactor; i_{tr} refers to the transformer current; and i_{filter} is the current of the filter. Rearranging equation (3-16) yields:

$$dv_{filter} = \frac{1}{C_{filter}} i_{filter} dt \quad \textbf{(3-17)}$$

The solution of the above equation in the s domain gives the following expression:

$$v_{filter} = v_{fo} + \frac{1}{C_{filter}} \int i_{filter} dt = v_{fo} + \frac{i_{filter}}{C_{filter} s} \quad \textbf{(3-18)}$$

where v_{fo} refers to the original voltage at the midpoint between the transformer and the phase reactor before the filtering process. This equation can be used to calculate the filtered voltage by knowing the exchanged current of the filter.

Figure 3-7 shows a shunt RLC three-phase filter, which generally is used in VSC. Depending on the VSC applications, the PWM carrier frequencies of the VSC relatively high frequency range and typically are about 1 kHz and new generations of VSC operate at lower frequencies of 150 Hz. Therefore, the objective is to filter out PWM frequencies associated with the carrier frequency that appears in the output. Thus, ac filter selection depends upon the converter switching frequency and the base impedance of the VSC, according to the following equation:

$$Z_{filter} = x_{filter}.Z_{base} = \frac{v_{filter}^2\, x_{filter}}{2\pi f_o S_{VSC}} \quad \textbf{(3-19)}$$

$$L_{filter} = \frac{Z_{filter}}{2\pi f_{sw}} = \frac{L_{filter}}{Z_{filter}^2} \quad \textbf{(3-20)}$$

where Z_{filter} and x_{filter} are the filter impedance and reactance (Ω), respectively, and have a typical value of $0.15\,pu$ [220]; f_o represents the nominal frequency of the grid (Hz); S_{VSC} is the rating power of VSC; and f_{sw} is the converter switching frequency (Hz). Switching frequency in any VSC contains high-order harmonics; therefore, the filter design of VSCs is not a straightforward task that requires many factors to be considered.

3.3.4 DC Capacitor

The commutation process in the VSC (i.e. the process of switching the valves on and off to commutate the current between the valves) depends on the dc capacitor, which provides a low reactive bath to the current commutation [206]. Furthermore, the dc capacitor serves as a harmonic filter of the voltage on the dc side and consequently reduces the voltage ripple [222] by using its stored energy. Likewise, dc capacitors have a damping effect that decreases the disturbances produced by the dc side or the ac side (during faults), which causes the dc voltage to change rapidly. The dc capacitor can limit the rate of

change of the voltage, and its damping ability is affected by the size of the dc capacitor, which determines the capacitor time constant. The time constant and capacitance relate to each other, as shown in the following equation:

$$\tau = \frac{W_e}{S_{VSC}} = \frac{1}{2}\frac{C v_{dc}^2}{S_{VSC}} \quad \textbf{(3-21)}$$

where W_e symbolises the stored energy in the capacitor, C refer to the capacitance (F), and τ denotes the capacitor time constant (sec). The time constant of a capacitor represents the time required for the capacitor to reach the rated voltage when the rated power is supplied. Clearly, the time constant can be amplified by increasing the capacitance value of the capacitor, which in turn is reflected on the dc ripple of the voltage and thus prevents instability in the dc voltage:

$$C = \frac{S_{VSC}}{v_{dc}^2} \cdot \frac{2\zeta}{\omega_c} \cdot \frac{1}{\delta_d(1-\delta_d)} \quad \textbf{(3-22)}$$

where ζ denotes the capacitor damping (generally, 0.707 affords adequate performance), ω_c represents the bandwidth of the dc voltage controller (typically approximately $2\pi * 20$ rad/s or 20 Hz [61]), and δ_d is the pu voltage drop requirement across the converter (normal value is less than $0.05\,pu$). However, the outer loop must have lower bandwidth than that of the inner loop [223].

3.3.5 Windfarm Converter Control

Windfarm side converters were selected to control both active and reactive power. The windfarm control system converter, WFVSC, is depicted in Figure 3-8.

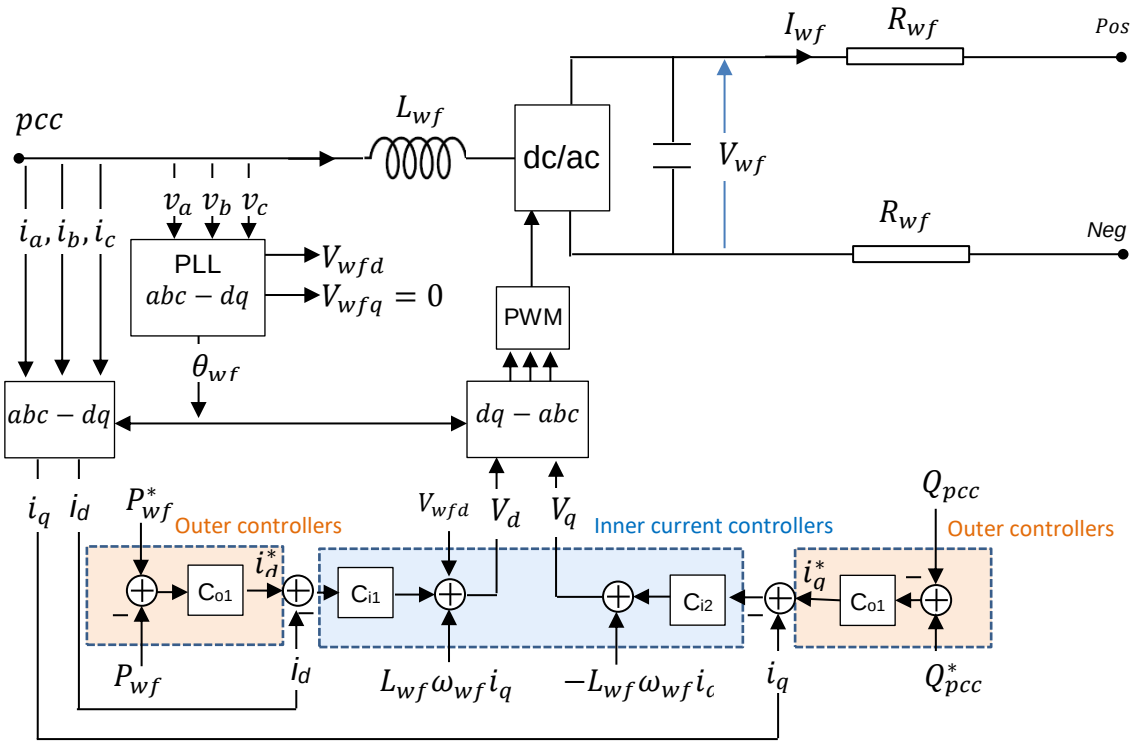


Figure 3-8 WFVSC control system

The system contains four PI controllers; two PI controllers constitute the outer loops. The outer control l9oops compare the active and reactive powers measured at the point of common coupling (PCC) using predetermined reference values (set-point). The resulting error signals are provided to the two PI controllers, which produce the direct (I_d^*) and quadrature (I_q^*) reference current values. The outputs of the outer loops ($I_d^*$and I_q^*) are the reference values for the inner current controller loops. The inner current loops compare the measured with the reference values (i.e. compare I_d with I_d^*, and I_q with I_q^*), and the error signal is also passed through the other two PI controllers to obtain the reference values V_d and V_q [65]. The inner loops have much faster step responses than the outer loops (approximately 1:10). The two PI controllers of the outer loops have the same step response with the same proportional and integral gains, and the other two in the inner controller have the same gains. However, to find these gains, the PI controllers must be tuned.

Several tuning methods are available, including modulus optimum [218], Ziegler–Nichols [224], Tyreus-Luyben [225], or software tools such as Control System Designer (such as sisotool) [226], which was used here. The criteria that were used for PI tuning were based on the rising and settling times. The converter itself was included in the control model as a delay of period of one sampling time. Table 3-2 summarises the parameters of the PI controllers.

Table 3-2 PI controller parameters of WFVSC

Parameter	Values
K_p and K_i (outer loops)	3.0, 3.0
K_p and K_i (inner loops)	0.6, 6
K_{p2} and K_{i2} (K_p for the second case, outer loops)	5.0, 5.0
K_{p2} and K_{i2} (K_p for the second case, outer loops)	0.7, 7
Damping ratio (ξ)	$\frac{1}{\sqrt{2}}$

Two cases were designed, implemented, and operated in the model: the case when the VSC alone was connected to the model and the case when the diode rectifiers were connected in series with the VSC. Although a third case is possible, when the diode rectifier only is connected to the system model, this case was not designed. However, the third case was studied in literature.

3.3.6 Grid Side Converter Control

The control system for this converter is illustrated in Figure 3-9. This converter control has the same construction as the windfarm side converter. The block that generates pulses to control the converter on the onshore side, which often is called the grid side converter (GSVSC), is shown in Figure 3-9.

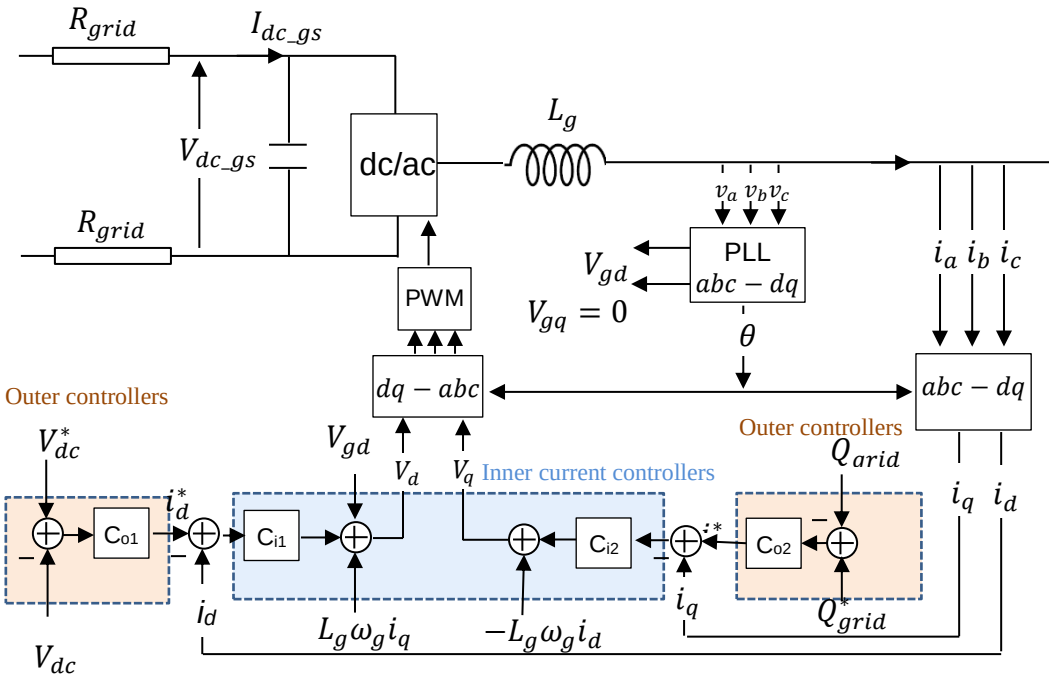


Figure 3-9 A control system block diagram for grid side converter

The gate drive control block, which produces pulses to trigger the VSC on the onshore side (GSVSC) to switch the IGBTs on or off, is shown in Figure 3-9. This converter is responsible for converting the dc power to the ac grid and for keeping the generated power balanced on the ac and dc sides. The system depends primarily on four control loops, where the outer loops are responsible for regulating the dc voltage and reactive power [40] and the inner loops regulate the current dq components. The current control set-point is provided through the dc voltage and reactive power regulator, and the input can vary based on the applications [68].

The design and implementation of the control block was made general, which means the same block diagram can be used on the windfarm side or the grid side after changing one option. The option is to choose between either controlling the P and Q, which are used on the windfarm side, or P and V_{dc}, which control the grid side. Figure 3-10 shows a schematic diagram of the GSVSC control. The parameters of the PI controllers are given in Table 3-3

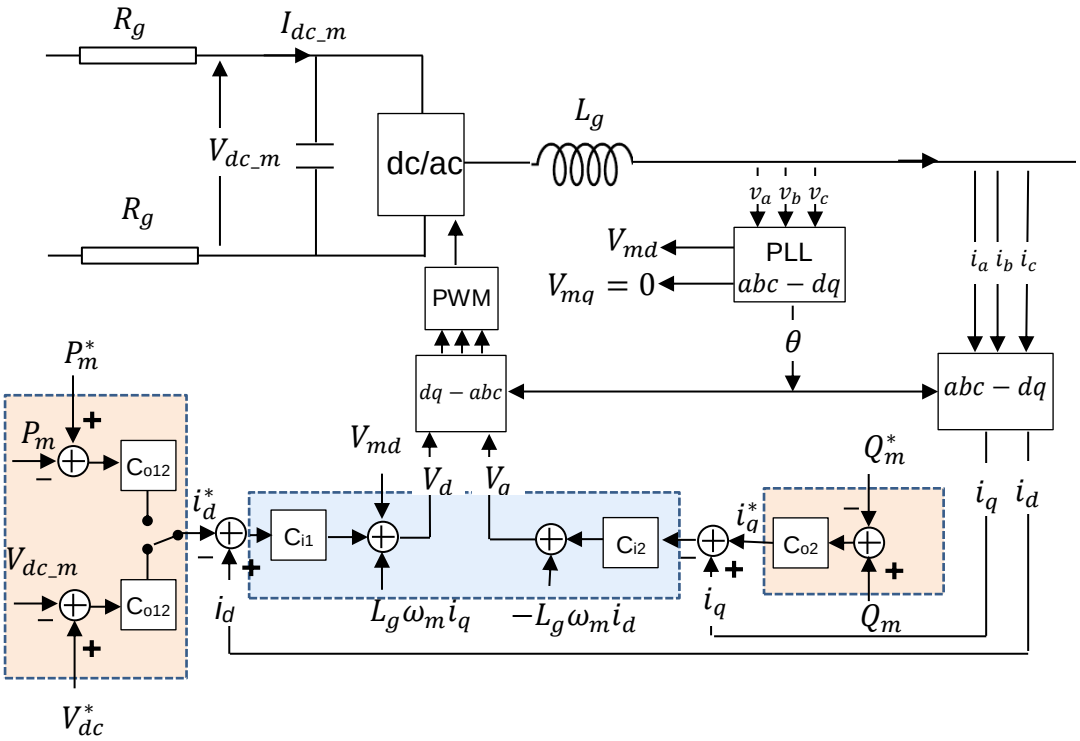


Figure 3-10 Control system block diagram with manual switch

Furthermore, two control systems with the same scheme were implemented in the same block to account for the addition of the diode rectifiers. This was to enable comparison between the two cases of diode rectifiers connected or disconnected. The two control systems have an identical design but different parameters of PI controllers. Thus, the model performance can be assessed on the same basis, and the model can be considered as a reference model to compare the operation in both normal and abnormal operating conditions.

Parameters for a second case are not required for GSVSC because the same amount of power is converted and delivered by the GSVSC in both cases. This is because the amount of power and dc voltage for the case when just VSC is connected and the case when the diode rectifiers are connected are equal.

Table 3-3 PI parameters of GSVSC

Parameter	Values
K_p and K_i (reactive power)	3.0, 3.0
K_p and K_i (dc voltage)	2.0, 40
K_p and K_i (inner loops)	0.6, 6
Damping ratio (ξ)	$\frac{1}{\sqrt{2}}$

3.4 Vector Control Strategy

A vector control strategy provides the ability of decoupling the control for both active and reactive power. This control scheme relies on two independent cascaded controllers. The outer current controllers provide the reference signal to the inner current controllers. The current controllers provide the switching information to a PWM, which triggers the IGBTs according to the measured values. Accurate switching signals also depend on the gains, K_p and K_i, of the PI controllers, which is not an easy task and requires a tuning technique. Several methods are available to tune a PI controller to find the gain coefficients K_p and K_i. these gains are known as the proportional and integral gains, respectively.

3.4.1 Inner Current Controller

The switching frequency in a VSC determines the required converter speed to react the operating point change from one point to another. Moreover, the bandwidth of the controller also determines how fast the system will respond to the signal change. Therefore, the switching frequency relates to the bandwidth of the controller in a similar way [146, p.75].

To calculate the controller bandwidth, the Laplace transformation is required to equation (3-3); then:

$$sL\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} v_{x\_d} \\ v_{x\_q} \end{bmatrix} - \begin{bmatrix} v_{c_d} \\ v_{c_q} \end{bmatrix} - R\begin{bmatrix} i_d \\ i_q \end{bmatrix} - j\omega\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad \textbf{(3-23)}$$

where s represents the Laplace s-domain, and L and R stands for the total inductance (H) and resistance (Ω) of the transformer and phase reactor respectively. The matrix $\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$ provides $90°$ phasor rotation. Equation (3-23) can be implemented as block diagram as illustrated in Figure 3-11. The system is linear and time invariant (autonomous), which means it is not explicitly dependent on time. From Figure 3-11, the transfer function can be written for the $q-axis$ as follows.

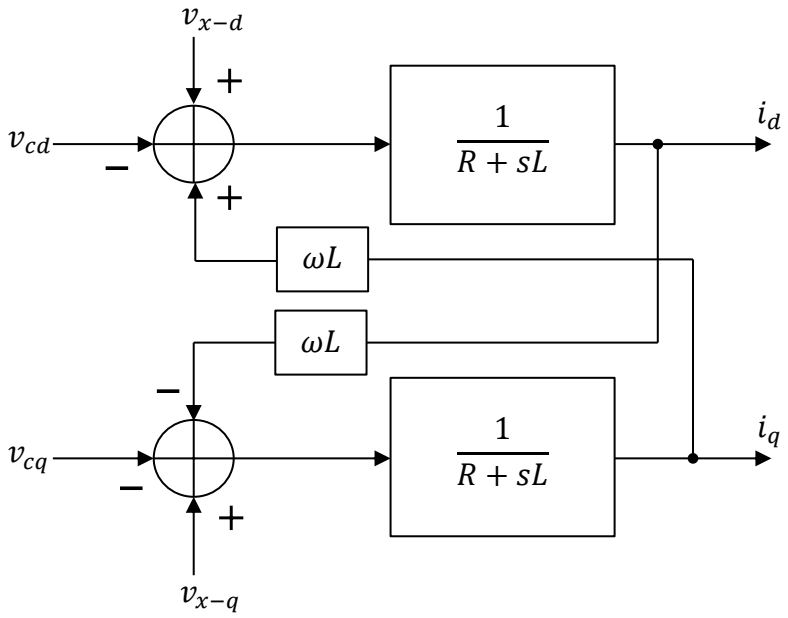


Figure 3-11 Inner current controller transfer function

$$\frac{i_q}{-v_{cq}} = \frac{\frac{1}{R+sL}}{1+\frac{(\omega L)^2}{(R+sL)^2}} = \frac{R+sL}{\left(s+\frac{R}{L}\right)^2+\omega^2} \qquad \textbf{(3-24)}$$

where i_q denotes the $q-component$ of current, and v_{cq} denotes the $q-component$ of voltage. Exactly the same transfer function is employed for the $d-axis$ by interchanging q and d subscripts. The open-loop system is oscillatory and poorly damped; therefore, closing the loop is necessary by feedback from the converter [146, p.76]. Then, the system in Figure 3-12 can improve the system response by shifting the transfer function poles of the open-

loop system toward the real axis. The transfer function of the closed loop is given as follows:

$$\frac{i_q}{i_q^*} = \frac{C_i(s) \cdot \frac{1}{R + sL}}{1 + C_i(s) \cdot \frac{1}{R + sL}} = \frac{C_i(s)}{C_i(s) + R + sL} \quad \textbf{(3-25)}$$

where $C_i(s)$ represents the PI controller transfer function in the s domain, and i_q^* denotes the reference current, which represents the output of the outer loop. The transfer function of the PI controller includes two coefficients: the proportional and the integral $K_p + \frac{K_i}{s}$ [227]. Then, (3-25) becomes:

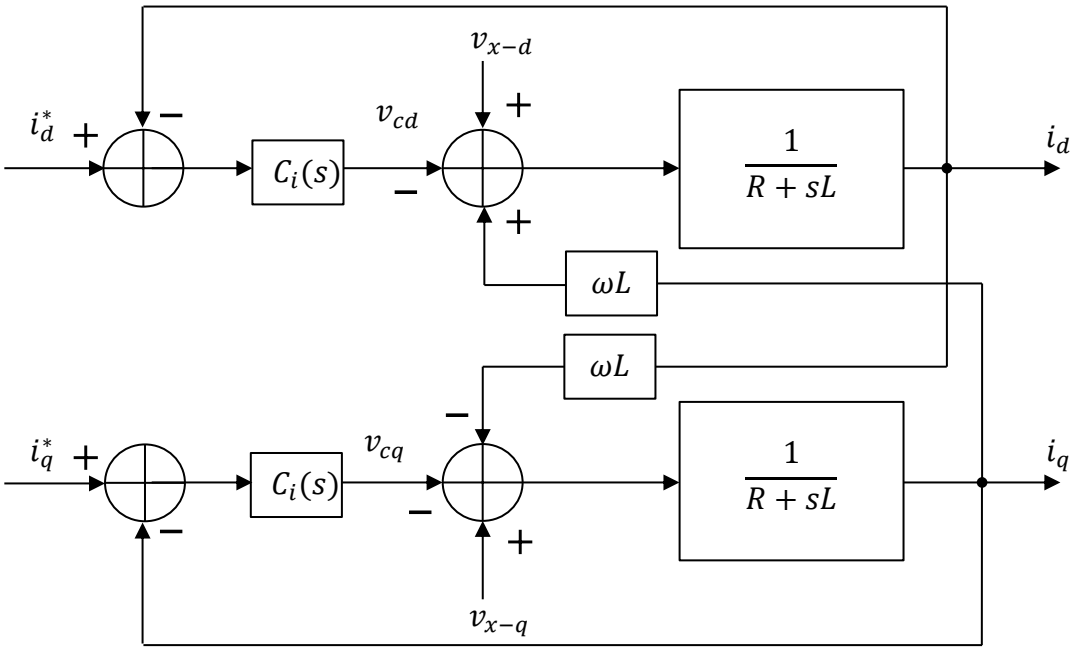


Figure 3-12 Feedback control of the inner current controller

$$\frac{i_q}{i_q^*} = \frac{K_p + \frac{K_i}{s} \cdot \frac{1}{R + sL}}{1 + K_p + \frac{K_i}{s} \cdot \frac{1}{R + sL}} = \frac{\frac{K_p}{L}s + \frac{K_i}{L}}{s^2 + \frac{R + K_p}{L}s + \frac{K_i}{L}} \quad \textbf{(3-26)}$$

Equation (3-26) is a second-order transfer function and has two poles. The denominator representing the characteristic equation of the closed-loop transfer function is

$$s^2 + s\frac{R + K_p}{L} + \frac{k_p}{L} = 0 \quad \textbf{(3-27)}$$

which can be compared to the standard second-order characteristic polynomial:

$$s^2 + 2\xi\omega_n s + \omega_n^2 = 0 \quad \textbf{(3-28)}$$

where ξ represents the damping ratio, which typically equals 0.707; and ω_n is the natural frequency in rad/sec. The two poles can be found as [183]

$$poles = -\xi\omega_n \pm j\omega_n\sqrt{\xi^2 - 1} \quad \textbf{(3-29)}$$

However, PI parameters can be found using pole-zero cancellation (3-26) [160]. Then, the PI parameters can be calculated by $K_p = 2\xi\omega_n L - R$ and $K_i = {\omega_c}^2 L$ [76, p.138].

3.4.2 Outer Controllers

Depending on the controller position, the outer controllers were used to control either the dc voltage or the active or reactive power, as illustrated in Figure 3-10. For instance, the converters at the windfarm side control both P and Q, which are the purpose of the outer control loop. The converter at the grid side is responsible for controlling reactive power and dc voltage. These controllers should have a slower step response than the inner-loop controllers. Furthermore, they are responsible for producing the reference currents (I_{dq}^*) for the inner controllers.

- **Active and Reactive Power Controllers**

In traditional ac power system applications, at the generator terminals, typically a phase shift occurs between the voltage and current waveforms. This phase difference depends on inductance, capacitance, and resistance of the generator itself and the grid connected to that generator. Therefore, the product of the rms values of voltage and current are not equal to the amount of power from the generator. However, in an HVDC system, the product is equal to the power due to the unidirectional voltage and current in the dc system [228, p.416]. Then, the active (P) and reactive (Q) power in a three-phase system are related to the apparent power according to the following equations [228, p.622]:

$$S = P + jQ = \sqrt{P^2 + Q^2} \quad \textbf{(3-30)}$$

$$S = v_a i_a + v_b i_b + v_c i_c + j\frac{1}{\sqrt{3}}\left[(v_b - v_c)i_a + (v_c - v_a)i_b + v_a - v_b)i_c\right] \quad \textbf{(3-31)}$$

Then

$$P = v_a i_a + v_b i_b + v_c i_c, \qquad \text{and } Q = \frac{1}{\sqrt{3}}(v_{ab} i_c + v_{bc} i_a + v_{ca} i_b) \tag{3-32}$$

where S denotes the apparent power measured in (VA); P stands for the active power measured (W); Q represents the reactive power measured in (var); i_a, i_b, and i_c are line currents in (A); and v_a, v_b, and v_c are line-to-ground voltages in (v). One of the advantages of the VSC is that it controls both active and reactive power independently in the four quadrants (i.e. it can produce or consume active and reactive power). The reactive power control was used in both ends (windfarm side and grid side).

The P and Q in the SRF coordinate system (dq) at the PCC are calculated by the following equation [76, p.138]:

$$P = \frac{3}{2}\left(v_d i_d + v_q i_q\right) \tag{3-33}$$

$$Q = \frac{3}{2}\left(v_q i_d - v_d i_q\right) \tag{3-34}$$

In typical operational conditions (i.e. steady state), the three-phase voltages are balanced, which results in $v_q = 0$. Then, (3-33) and (3-34) are reduced to

$$P = \frac{3}{2} v_d i_d \tag{3-35}$$

$$Q = \frac{-3}{2} v_d i_q \tag{3-36}$$

Therefore, the values of the dq current references are

$$i_d^* = \frac{2P^*}{3v_d}, i_q^* = \frac{-2Q^*}{3v_d} \tag{3-37}$$

The schematic diagram of active and reactive power controllers is shown in Figure 3-13. PI controllers were added to this figure to cancel the steady-state errors.

Figure 3-13 can be represented mathematically as follows [146, p.79]:

$$i_d^* = \left(P_{ref}^* - P_{measured}\right).K_p + \frac{K_i}{s} \tag{3-38}$$

$$i_q^* = \left(Q_{ref}^* - Q_{measured}\right).K_p + \frac{K_i}{s} \tag{3-39}$$

where $P_{measured}$ and $Q_{measured}$ are the measured active and reactive ac power at the PCC, respectively, and P^*_{ref} and Q^*_{ref} represent the reference values for active and reactive power, respectively.

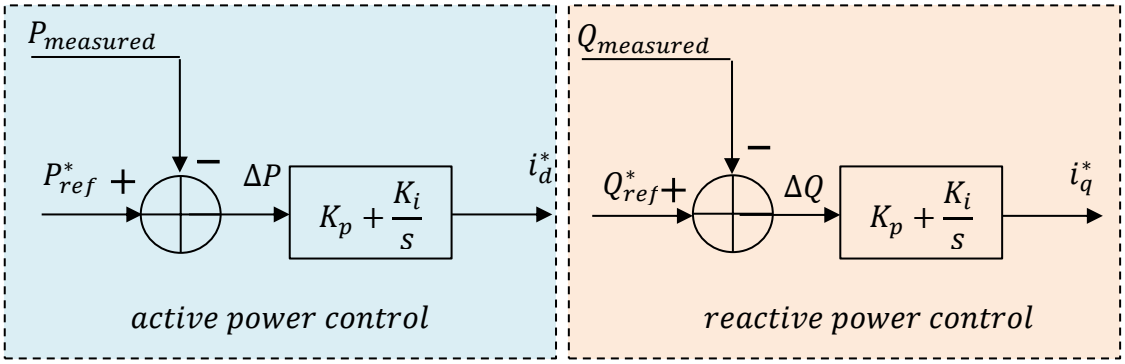


Figure 3-13 Block diagram for active and reactive power control

- **Direct Voltage Control**

In multiterminal networks, the dc voltage of the dc cable is controlled by one terminal, which is usually on the grid side. Under steady-state condition, neglecting the converter losses, then the power at the dc side equals the power at the ac side, as in (3-5), which results in

$$I_{dc} = \frac{P_{dq}}{V_{dc}} = \frac{3}{2}\frac{v_d i_d}{V_{dc}} \tag{3-40}$$

Then, imbalance between the dc and ac side power results in changing of the dc link capacitor voltage according to the following equation [40], and substituting (3-40) into (3-8) gives [218]:

$$C_{dc}\frac{dV_{dc}}{dt} = \frac{3}{2}\frac{v_d}{V_{dc}} i_d - I_L \tag{3-41}$$

The relationship between the voltage magnitude of the ac and dc sides is given by

$$V_{dc} = 2.\sqrt{\frac{2}{3}}.v_{LL\_rms} = 2.v_{ph\_peack} \tag{3-42}$$

where v_{ph_peack} denotes the ac peak phase voltage and v_{LL_rms} is the rms line-to-line voltage. The nonlinear equation (3-41) describes the dynamic behaviour of the dc link. However, the PI parameters must be determined based on the linearized model. Therefore, upon linearization of (3-41) and specification of dc voltage reference value (V_{dc}^{*}), (3-41) becomes [218] the following:

$$\frac{\Delta V_{dc}}{\Delta i_d} = \frac{3}{2}\frac{v_d}{V_{dc}^{*}}\frac{1}{C\ s} \qquad \textbf{(3-43)}$$

Similar to the active and reactive power controllers, the dc voltage controller compares the measured dc voltage with a reference voltage. The error ($\Delta V_{dc} = V_{dc}^{*} - V_{dc}$) is sent to PI to produce a reference current to the inner current controller as follows:

$$i_d^{*} = (V_{dc}^{*} - V_{dc}).K_p + \frac{K_i}{s} \qquad \textbf{(3-44)}$$

where V_{dc} denotes the measured dc voltage of the dc cable. The dc voltage controller, based on equation (3-44), is shown in Figure 3-14.

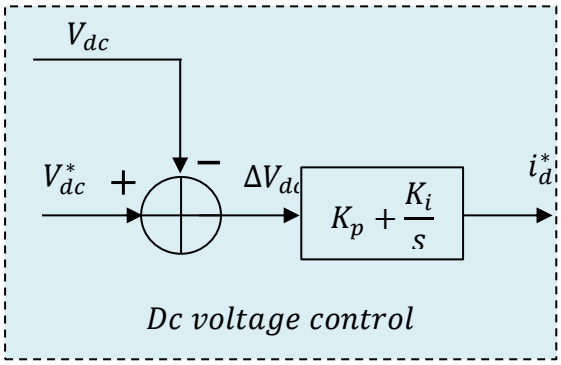


Figure 3-14 DC voltage controller block diagram

3.5 MTDC Control Strategies

In a VSC-based MTDC, dc voltage control is a vital task to be given to a VSC station because of the requirement of balancing the dc voltage across the dc cable, which results in a balance of the power flow between the interconnected nodes. Moreover, if the dc voltage increases to high values, then protective equipment may be triggered. Conversely, drop of dc voltage may result in difficulties to the control system [146, p.98].

In a two-terminal transmission system, one terminal generally is assigned to control the dc voltage and the other terminal to control the power. However, this control strategy (i.e. leaving one terminal to control dc voltage) may be adopted in an MTDC system. However, it should be noted that the current provided from all power-controlling stations should not exceed at any time the limits of the station that controls the dc voltage. This limit is mathematically expressed as

$$P_{Vdc}^{capacity}(t) \geq \sum_{i=1}^{N-1} P_{Idc}^{i}(t) \quad \textbf{(3-45)}$$

where $P_{Vdc}^{capacity}(t)$ represents the instantaneous active power capacity of the station that controls the dc voltage [VA], $P_{Idc}^{i}(t)$is the capacity of the $i-th$ VSC station [VA], and N is the total number of VSC terminals.

Therefore, it is evident from (3-45) that ensuring power balance between all MTDC terminals by having one VSC control the dc voltage becomes increasingly difficult to accomplish by increasing the number of terminals. Hence, for an MTDC network with a large number of terminals, having only one terminal control the dc voltage is not favourable. Thus, a control strategy that enables the MTDC network to have more than one terminal controlling the dc voltage is essential for successful expansion and operation of a large MTDC network.

Therefore, this section introduces the available control strategies that suit the controllability of the MTDC such as droop control, power ratio control, priority control, and voltage margin.

3.5.1 Voltage Droop-Control Strategy

This control strategy was originally introduced to control thyristor-based MTDC systems, although it was also used for VSC-based MTDC systems. The droop-control structure for MTDC systems works in a similar way to the control structure in conventional ac networks, where the frequency variation, which depends on load change, is used as a control signal for the control scheme to regulate the produced power to supply demand. In MTDC grids, the droop mechanism is employed to regulate the dc voltage within predetermined limits

by changing the converter current to ensure power balance among all terminals at all times.

The droop-control strategy is able to synchronise several VSC terminals, and fast communication among VSC terminals is not required [54]. In the case of dc voltage increase in the dc side of the MTDC, then surplus power is available in the system, which means the regulating station must increase power inversion to keep the system balanced. Conversely, if a voltage reduction occurs, that means power is lacking in the network and the controlling VSC should increase power rectification.

Similar to ac systems, which operate and should comply with grid code, dc systems also require rules. For example, the parameters of droop control, such as level of dc voltage (V_{dc}^{max}, V_{dc}^{min}) during normal steady state or transient operation, might be formalized by a standard [229], as shown in Figure 3-15.

This method uses a proportional controller to assure the power balance. This proportional controller represents the droop characteristic to describe the relationship between the current of the converter and the dc voltage in a unique way, as shown in Figure 3-15. However, this droop characteristic is valid only for the network topologies that were built with the droop characteristics from the first [212]. Consequently, if the topology of a network is changed, the control strategy will not operate properly without changing the droop characteristic.

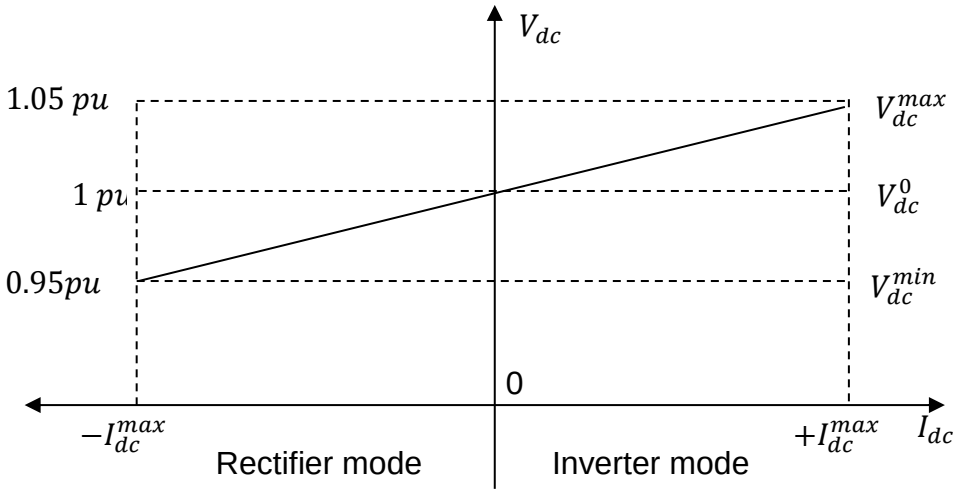


Figure 3-15 DC voltage droop characteristics of converter

A voltage margin of, say 5%, might be set between the maximum and minimum values of droop characteristic of the HVDC voltage to prevent the proportional gain of the PI controller (K_p) from overvalues. This is due to the inverse proportionality of controller gain and the characteristic of the droop voltage control. If an excessive value is reached, the dc voltage may experience instability.

However, this method is unable to maintain the dc voltage at predetermined values. If an increase in the value of the dc voltage begins in the network, this means that the network has surplus power, and the stations that are regulating the dc voltage must start to escalate inversion of power to re-establish the power balance. Conversely, if the dc voltage starts to drop down, the power generated in the grid is insufficient and the station that controls the dc voltage must increase rectification.

The droop controllers should be designed and constructed such that the minimum and maximum dc voltage values occur at the converter maximum current. The droop constant selection could optimise power transfer between terminals [54].

Thus, the droop characteristics can be represented mathematically by the following equation [35]:

$$V_{dc\_g}^{*} = V_{dc\_g} + K_d I_g \quad \textbf{(3-46)}$$

where $V_{dc\_g}^{*}$ denotes the reference dc voltage (V), V_{dc_g} equals the no-load dc voltage (V) (i.e. the voltage with zero current), I_g denotes the dc current (A), and K_d represents the droop characteristics slope $\frac{\Delta V}{\Delta I}$ (V/A). Figure 3-16 shows the droop controller block diagram, based on equation (3-46).

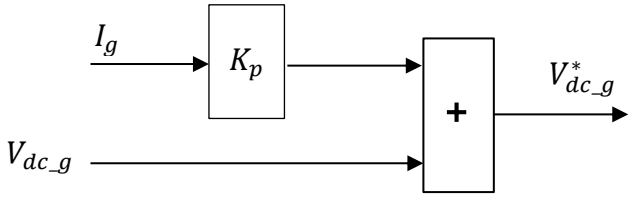


Figure 3-16 Droop-control block diagram

3.5.2 Power Ratio Control Strategy

The idea behind this control method is to establish a certain power ratio among VSC stations. The system operator can set the ratio of transmitted power between the stations and change it periodically according to the load requirement [230]. Power-ratio control strategy is different from voltage droop-control strategy because the angle of one-droop characteristics changes, whereas the second characteristics slope is fixed. The operator of the network can alter the proportion of power between these two terminals that controls dc voltage, as shown in Figure 3-17, which illustrates the dc voltage droop characteristics of two stations. Dc power is obtained from

$$P_{dc} = V_{dc} I_{dc} \quad \textbf{(3-47)}$$

Under typical operating conditions, the nominal values of voltage are approximately equal to V_{dc} for both stations. Hence, the dc power is directly proportionate to the dc current: i.e. ($P_{dc} \propto I_{dc}$). Thus, the transmitted power shared between each of the two VSC converter stations is

$$\frac{P_1}{P_2} \approx \frac{I_{dc1}}{I_{dc2}} = n \quad \textbf{(3-48)}$$

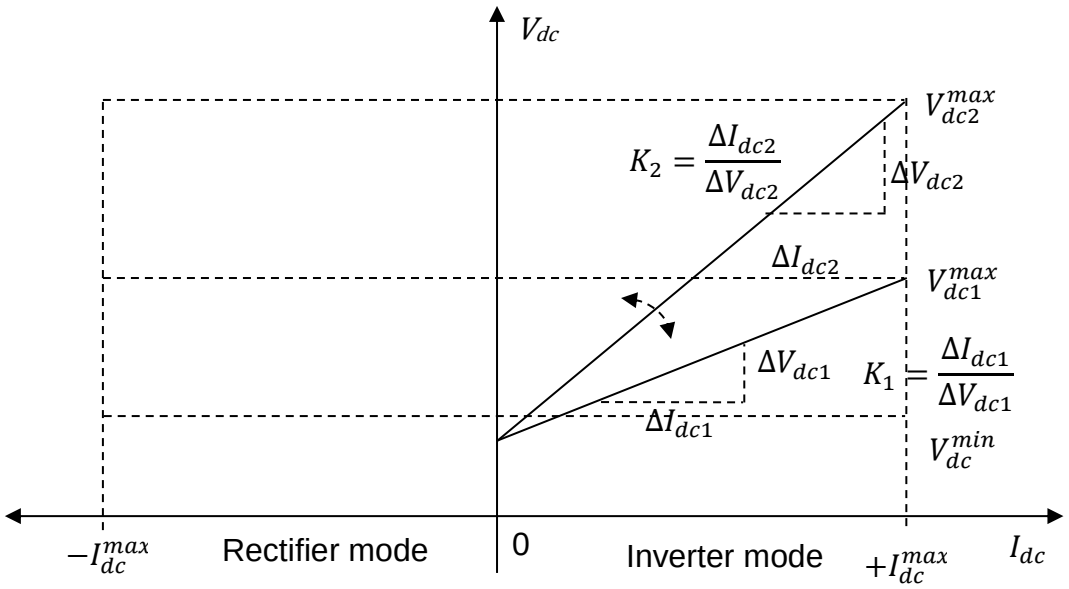


Figure 3-17 Converter dc voltage droop characteristics of terminals 1 and 2.

For operation in steady-state conditions, the relationship that relates the dc voltages of the two onshore converters is

$$V_{dc2} = V_{dc1} + R_1 I_{dc1} - R_2 I_{dc2} \tag{3-49}$$

where R_1 and R_2 symbolises the resistances of the cables that connect the first and second onshore converter, respectively. Nevertheless, these values of R_1 and R_2 can vary because of temperature changes of cable. Therefore, the power distribution precision may be affected. From Figure 3-17, the droop characteristics of the dc current are:

$$\begin{aligned} I_{dc1} &= K_1 \Delta V_{dc1} = K_1 (V_{dc1} - V_{dc1}^{min}) \\ I_{dc2} &= K_2 \Delta V_{dc2} = K_2 (V_{dc2} - V_{dc2}^{min}) \end{aligned} \tag{3-50}$$

Here K_1 and K_2 refer to the characteristics slopes of the dc voltage. By assuming that the minimum dc voltages of the two converters are equal, i.e. $V_{dc}^{min} = V_{dc1}^{min} = V_{dc2}^{min}$, then from (3-50) and (3-49), the following equation is possible to be written to obtain

$$\left(V_{dc2} - V_{dc}^{min}\right) - \left(V_{dc1} - V_{dc}^{min}\right) = R_1 I_{dc1} - R_2 I_{dc2} \tag{3-51}$$

Substituting the dc voltages from (3-49) into (3-50) gives

$$\frac{I_{dc2}}{K_2} - \frac{I_{dc1}}{K_1} = R_1 I_{dc1} - R_2 I_{dc2} \quad \textbf{(3-52)}$$

To ensure the necessary ratio of the transmitted power (n), which is set by the operator in the case of steady-state operation, the two-droop characteristics relationship is

$$\frac{I_{dc1}}{I_{dc2}} = \frac{R_2 + \frac{1}{K_2}}{R_1 + \frac{1}{K_1}} = n \Longrightarrow K_2 = \frac{1}{\frac{n}{K_1} + nR_1 - R_2} \quad \textbf{(3-53)}$$

This method involves communication to achieve the required power ratio among the dc converters, which is a drawback. To achieve the power ratio, the manager of the system will need the power generated by offshore windfarms at all times to be able to set the droop features of each station to control dc voltage. The expandability is another disadvantage because of the difficulty to find the analytical expression for the power ratio [146, p.101].

3.5.3 Priority Control Strategy

This method of control considers that one converter station on the land has priority over the others, from the viewpoint of delivering power generated by the OWF. Hence, the remaining onshore converters will wait, without receiving any power, until the capacity of the highest-priority station is reached [231]. The priority control method can be considered as a modification of the dc voltage droop method to set the prior converter power sharing. The terminal that has the highest priority will be allowed to control the dc voltage, with the aid of a PI controller, until the rated capacity, which is set by the system operators, of the terminal is reached. Conversely, other terminals simply will receive the extra power that is transmitted from the highest-priority converter, as shown in Figure 3-18.

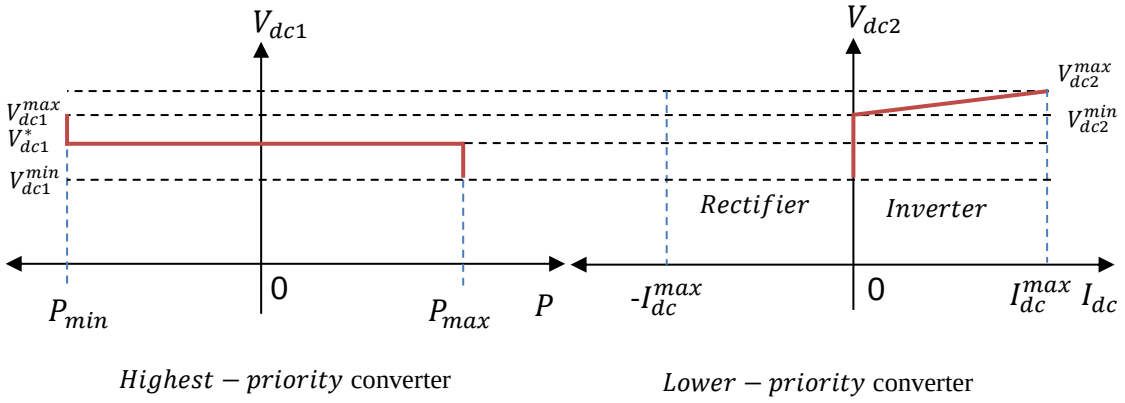


Figure 3-18 DC voltage characteristics and dc voltage droop characteristics

For the case in which the total generated power by the OWFs is less than the rated capacity of the highest priority converter, the dc voltage is regulated at a predetermined value. Hence, no power is converted at the other converters until its capacity is reached.

To achieve such a dispatch scheme, the system operator needs to predefine (V_{dc2}^{min}) with a value that is greater than or equal to the highest value of the first converter to account for operating point change. The values of dc droop voltage control should take into consideration the characteristics of the system, such as variation of dc cable resistance and dynamic upper values of dc voltage, to guarantee the operation of the second converter only when the limit of the first converter is reached.

3.5.4 Voltage Margin Control Strategy

The converter in this control scheme operates effectively in a constant power control mode to keep the voltage at the local dc bus within pre-set limits $V_{dc\_low} < V_{dc} < V_{dc\_high}$ [232]. In this strategy, all converters in the multiterminal grid should have a marginal reference dc voltage offset to generate the voltage margin. The method was initially proposed to control a 3-terminal B2B HVDC network in Japan [233]. The elementary control approach of this method contains a limiter with a dc voltage controller at the output Figure 3-19 . The dc voltage regulator uses a proportional integral controller (PI). The limiter is used to constrain the $d - axis$ reference current to the highest and lowest values to

avoid overcurrent in the valves of the converter [232]. Consequently, the active power passes through the VSC and is bounded by the higher and lower limits. By this approach, the controller of the dc voltage can maintain the dc voltage to match the reference value, providing that the active power passes through the station within predetermined limits.

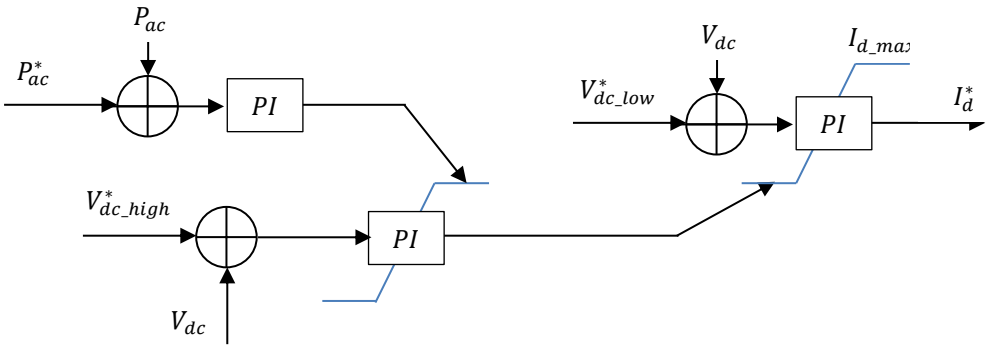


Figure 3-19 A limiter and dc voltage controller in the voltage margin method

In a multiterminal HVDC system, the dc voltage characteristic could be used in V_{dc} control of two converters or more. The reference value of V_{dc} can be set for each converter with a different value from the rest by a certain voltage margin. Thus, the dc voltage control will be moved from one station to another sequentially. The converter that has the lowest reference dc voltage first will regulate the V_{dc}; the highest dc voltage reference converter will regulate last. Figure 3-20 illustrates the V_{dc} characteristics of two converters with a voltage margin operation. Initially, converter 2 will regulate the dc voltage, and converter 1 will receive energy (P_{dc}^{lower}) inside the system. Thus, point P in the figure will be the operating point. This is a fixed power-sharing equivalence, where converter 1 receives a constant value of active power.

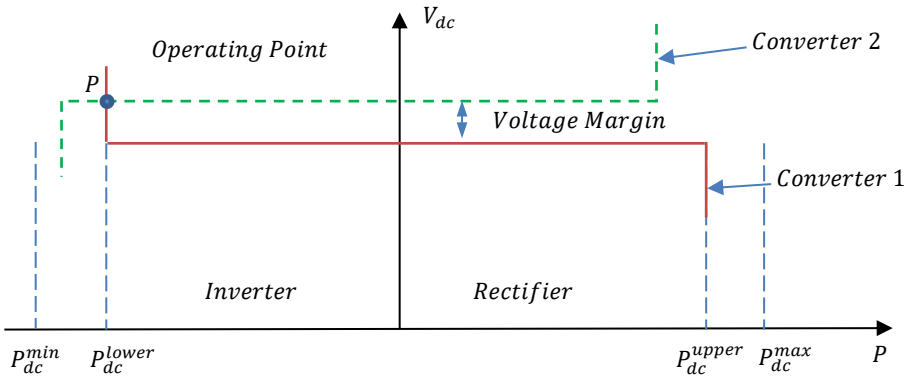


Figure 3-20 Voltage margin controller characteristics

When the offshore windfarm produces more power than the capacity of station 1, the extra power will be received by station 2. Then, a new operating point to the left of point P will be the operating point. When the inversion reaches the maximum value in converter 2, control of the dc voltage is no longer available because both converters have reached their limits of power. In this case, the OWF output power must be reduced by dissipating the surplus power in breaking resistors with the aid of a dc chopper or by reducing the output power of the wind turbines rapidly.

3.6 Steady-State Results and Case Studies

The aim of this section is to present the simulation results of the proposed model under steady-state operational conditions (no fault). Three case studies were performed: first, the case with VSC only connected to the system; second, the case with the diode rectifiers (DRs) connected to the system at time $t = 2.5\ s$, for the VSC-DR-DR arrangement; and third, similar to the second case except that the arrangement is DR-VSC-VSC (i.e. VSC is in the middle). Noting that, the sign of the active power indicates the direction of power flow. For example, a positive sign means the flow of the power is from the windfarm to the dc side through the converter; vice versa, on the grid side, a positive sign means that the power flows from the converter toward the grid. In the dc cable, a positive sign indicates that power flows direction is from the WFVSC toward

the GSVSC through the dc cable in all cases (summarised in Table 3-4). The case studies are summarised in Table 3-5.

Table 3-4 Power flow sign indication

Sign	Power flow direction	Sign	Power flow direction
+	Windfarm→ WFVSC	-	WFVSC → Windfarm
+	GSVSC → Grid	-	Grid → GSVSC
+	WFVSC → GSVSC	-	GSVSC → WFVSC

Table 3-5 Case study summary

	VSC	Diode Rectifiers	Arrangement
Case 1	√	-	VSC
Case 2	√	√	VSC-DR-DR
Case 3	√	√	DR-VSC-DR

- **Case 1 (Voltage Source Converter Only)**

The proposed offshore multiterminal model was designed, implemented, and operated using a 3-terminal multiterminal. The arrangement, which is shown in Figure 3-1, includes two offshore windfarms with WFVSC converters and one onshore VSC converter station. The two offshore windfarms were considered as lumped models, by using a single equivalent WT and generator to represent the windfarm. However, this thesis does not include the windfarm simulation and considers it as a fixed generation source. The converters at the windfarm side were designed and implemented using two diode rectifiers and a VSC. The elements of the group are connected in series and work as rectifiers. Each rectifier converts one-third of the total power and one-third of the total voltage. The output voltage and the active power (P) and reactive power (Q) of the PCC of windfarm 1 are depicted in Figure 3-21. The base for pu calculations was chosen equal to the rated values; rated power is 360 MW, rated dc voltage equals to 320 kV.

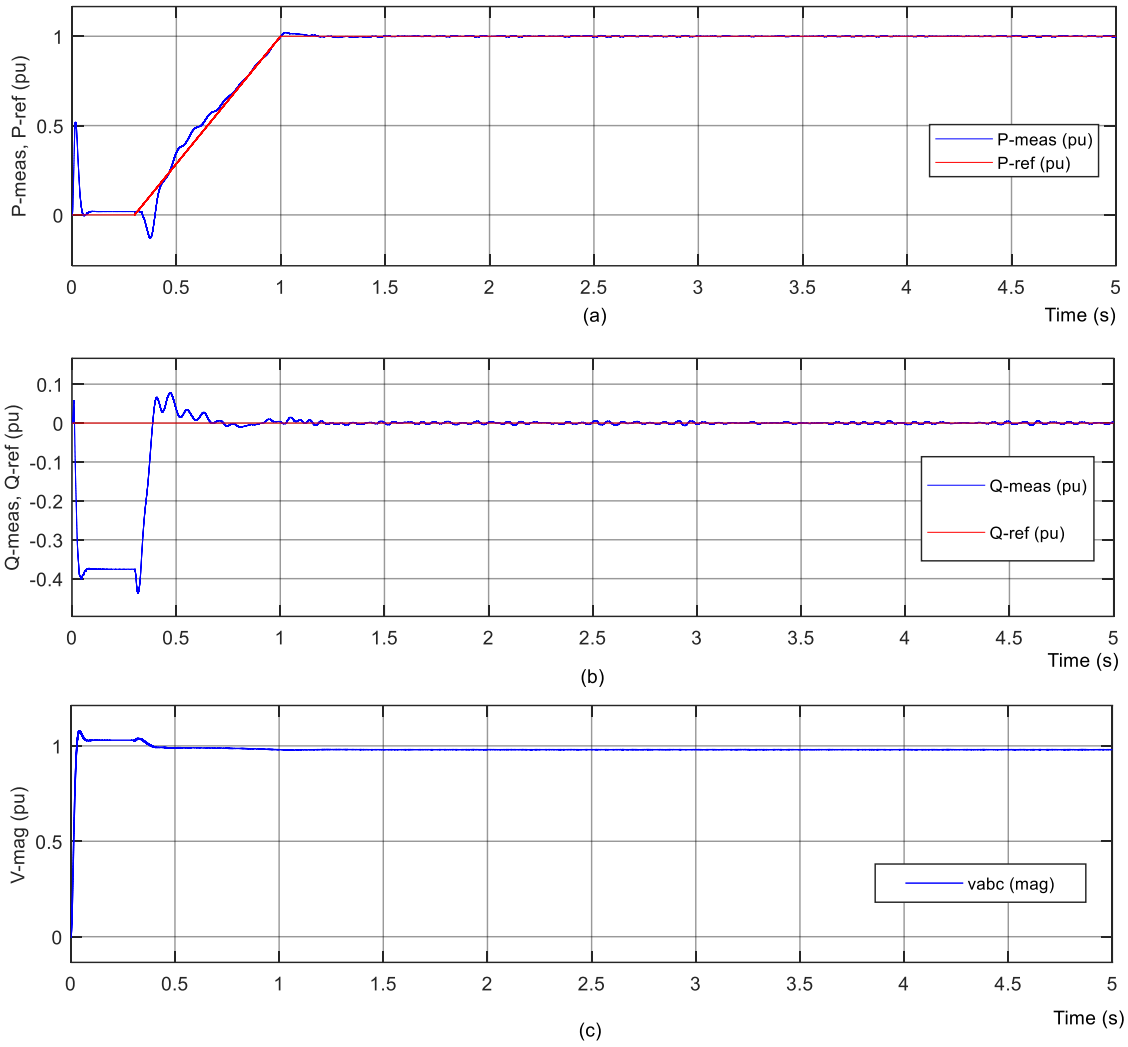


Figure 3-21 Active reactive power at PCC windfarm 1: (a) measured (blue) and reference (red) active power, (b) measured (blue) and reference (red) reactive power, and (c) voltage magnitude (Case 1)

The model was run without the connection of the DRs (i.e. the model is simply VSC-based MTDC). It can be seen that the measured power (blue line) follows the reference (red line). The simulation started at time $t = 0\,s$, and all converters were blocked. GSVSC was turned on at $t = 0.1\,s$, and the WFVSCs were both turned on at $t = 0.3\,s$. At the same time, the reference power signals began ramping and within $0.7\,s$ reached the rated value at $1\,pu$. A similar curve can be seen for windfarm 2. The parameters that were used in the simulation are summarised in Table 3-6.

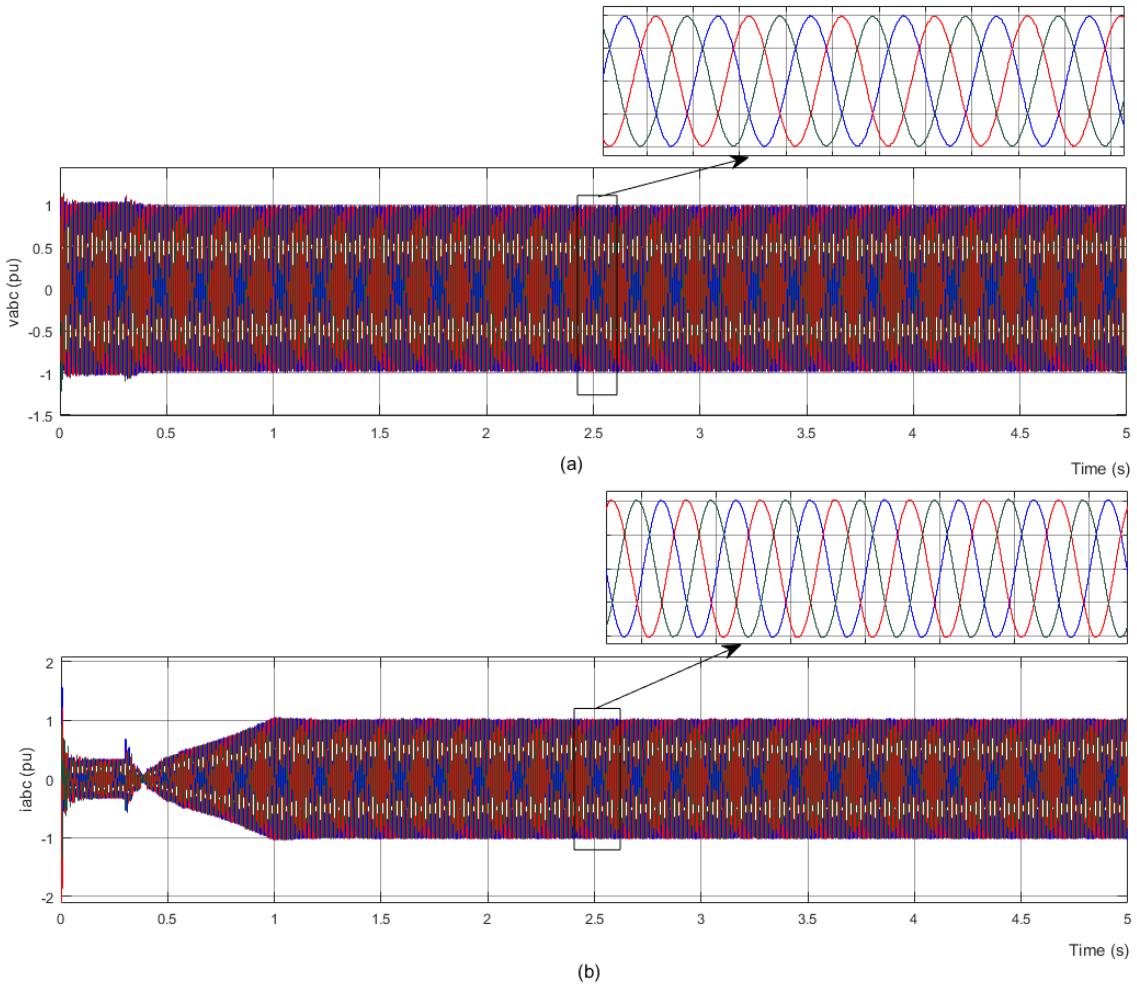


Figure 3-22 Three-phase ac voltage and current measured at PCC in pu: (a) three-phase voltage and (b) three-phase current (Case 1)

Figure 3-22 illustrates the measured three-phase ac voltage and current in (pu) at PCC. It can be seen that both voltage and current waveforms are sinusoidal. Zoomed views are also shown in the figure. The voltage is slightly more than $1\ pu$ until the time $t = 0.3\ s$, after which the voltage becomes $1\ pu$, which is the typical value, after the connection of the VSC and started to control the power. However, the current followed a different pattern: before $0.3\ s$, only the reactive current appears in the system, as indicated in Figure 3-21b in the reactive power curve. Then, the current began to increase and reached $1\ pu$ within approximately $0.7\ s$. The three-phase voltage and current of the second windfarm measured at PCC2 were similar to those for windfarm 1.

Table 3-6 Model parameters

Component	Parameter	Copper value	
Cable	Conductor type	Cu subsea cable	Al
	Length	74 Km	31 km
	Resistance	0.0149 Ω/km	0.0176 Ω/km
	Inductance	5.0637e-4 H/km	5.223e-4 H/km
	Capacitance	0.22 µF/km	0.29 µF/km
	Cross-sectional area	1000 mm^2	2000 mm^2
WFVSC	Power	360 MW	-
	Ac voltage at PCC	160 kV	-
	Dc filter capacitance	70 µF	-
	Transformer turn ratio	1.4375	-
Diode rectifiers	Power rating (each)	120 MW	-
	Dc filter capacitance	70 µF	-
	Transformer Y/Y/Δ	1.4375	-

Figure 3-23 illustrates the pu value of the dc voltage measured at the VSC of the first windfarm (WFVSC 1). The dc voltage was measured at both the positive and the negative poles. Before the time $t = 300\,ms$, the voltage began at zero and reached a value of approximately $1.2\,pu$.

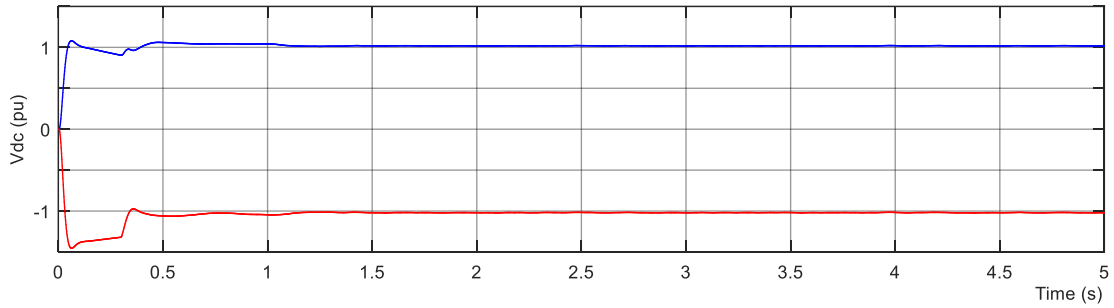


Figure 3-23 DC voltage at the dc cable (case 1)

This was due to the charging current of the reactance in the system. After that, the voltage settled down at $\pm 1\,pu$. The actual value for the voltage was $320\,kV$, which is the nominal value and equal to the base value.

Figure 3-24 shows the inner current controllers in per unit for both active and reactive currents in the inner current controllers. The figure shows clearly the measured values (blue) follow the reference values (red) within short time. The control algorithm calculates the reference in the outer loop. This calculation was about $0.2\,s$, which depends on the speed of the controller characteristics such

as the disturbance rejection and reference tracking. These characteristics is changed based on the gain values (K_p and K_i) presented in Table 3-2.

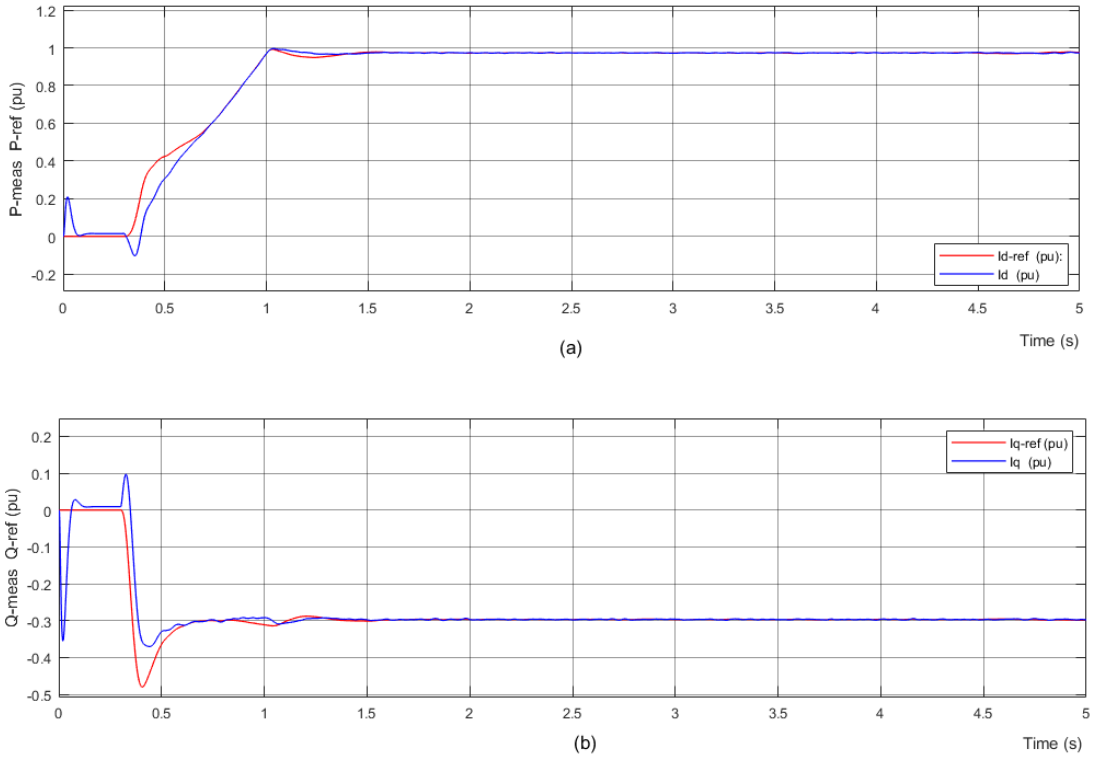


Figure 3-24 Per unit dq currents of the inner current controllers (a) compares i_d and i_d^*, (b) compares i_q and i_q^*

- **Case 2 (Voltage Source Converter and Diode Rectifiers)**

The following section illustrates the proposed model with the connection of the diode rectifiers during the simulation. The simulation was performed with the diode rectifiers connected in series with the VSC in both windfarms, and the VSC was connected to the bottom of the diode rectifiers, as shown in Table 3-5 and Figure 3-2 (i.e. VSC-DR-DR connection). The scenario for the second case was started at time $t = 0\ s$; initially, all converters were in the off-state (blocked), while at time $t = 0.1\ s$, the grid side converter was connected. At time $t = 0.3\ s$, WFVSC1 and WFVSC2 were connected simultaneously and began converting the power. The reference power line started to increase to reach $1\ pu$ within $0.7\ s$ and the measured followed the reference value. Until $t = 2.5\ s$, the model works in a similar way to the first case. At this point, the diode

rectifiers (DR) were connected in series with the VSC, and the arrangement was VSC–DR–DR, as shown in Figure 3-2.

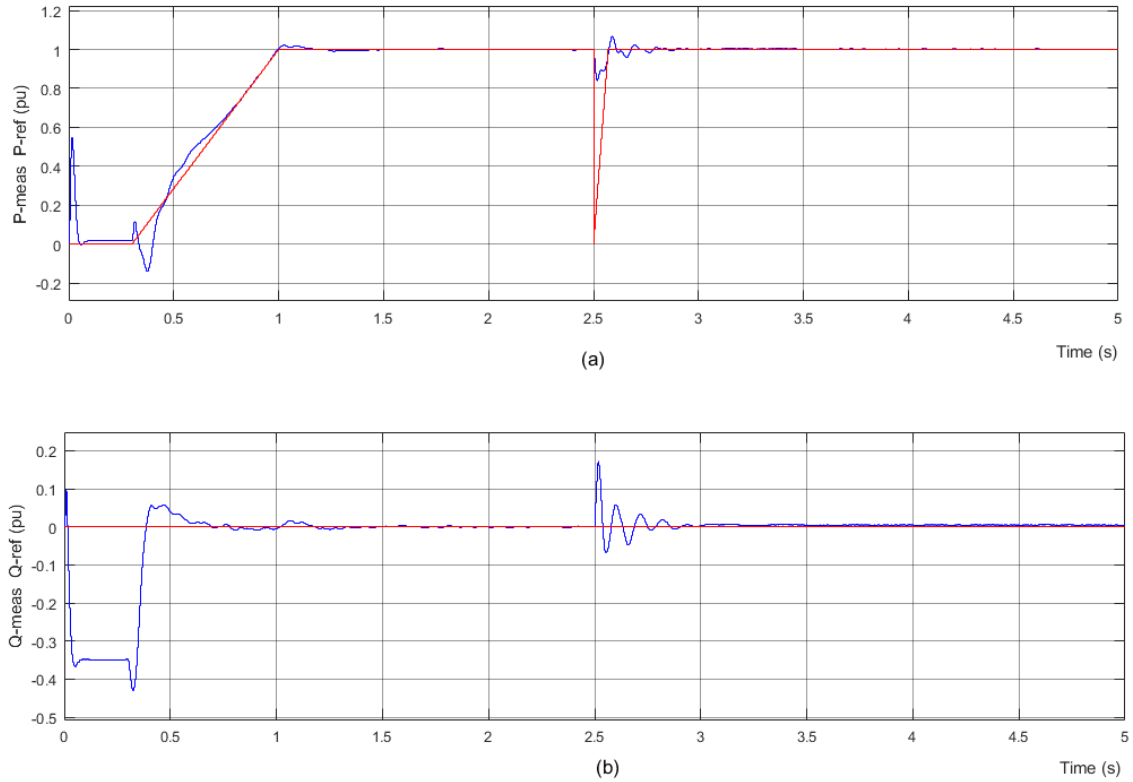


Figure 3-25 Active and reactive power at PCC: (a) active power and (b) reactive power (case 2)

The active power begun by the charging current peaked at $0.5\,pu$ for approximately $40\,ms$ and then settled down to approximately $0\,pu$ until $0.3\,s$, when the converters connected to the model as shown in Figure 3-25. Then, the active power followed the reference line to reach the rated value of $1\,pu$ at time $t = 1\,s$, and stayed at the same level. At time $t = 2.5\,s$, the two diode rectifiers were connected in both windfarms. At this point, the controllers of both windfarms were switched to another controller. The second controller of each windfarm has the same structure as the first except for the parameters of the PI controllers to account for the new connected diode rectifiers, which changes the rated power and voltage by one-third of the total generated power of each windfarm. The new controllers of both windfarms have a faster ramping reference line (1:10) to minimise the disturbance due to the switching process, as shown in Figure 3-25a.

The reactive power behaves slightly differently from the active power. The measured reactive power (blue curve) in Figure 3-25b started from zero and a negative value of approximately $0.35\,pu$ due to the reactive element in the model until the time $t = 0.3\,s$, when the converters were connected and started to control P and Q at $0\,pu$ and followed the reference line (red line). After some fluctuations, the reactive power settled at approximately zero. When the diode rectifiers were connected, the measured value shows some fluctuations for about $0.23\,s$, where it reached a value of less than 2% [6] of the rated value.

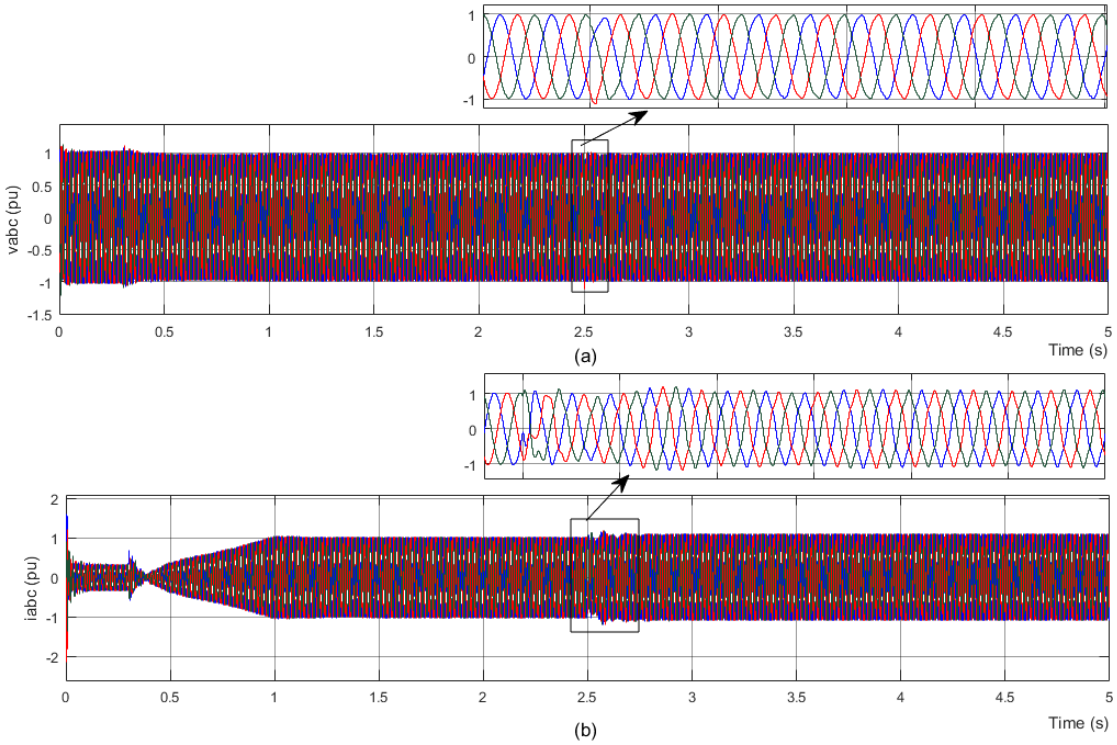


Figure 3-26 Three-phase voltage (a) and (b) three-phase current (case 2)

The final value was $0.005\,pu$, which is acceptable according to the grid code requirements. The three-phase ac voltage and current at the point of common coupling (PCC) are shown in Figure 3-26. The ac voltage started at slightly more than $1\,pu$, while the converter was at its blocked mode. After $0.3\,s$, the converter connected to the system and started to control the output, and the voltage became $1\,pu$, which is the rated value. At $t = 2.5\,s$, when the DRs

[6] The settling time typically is defined as the required time for the signal to stay within 2% of final (rated) control value.

connected with the VSC, a slight fluctuation occurred for less than a half cycle, as shown in the zoomed-in view. However, the three-phase ac current has a different waveform. For the first half-cycle, the current had an overshoot due to the charging current of the reactive elements. Until $0.3\,s$, the current was at approximately $0.34\,pu$, which is a reactive current. Then, the current started to increase gradually to $1\,pu$. At time $t = 2.5\,s$, the DRs were switched on and showed a minimal disturbance. The current after switching on the DRs was slightly more than $1\,pu$, which is due to the reactive current and is shown clearly in Figure 3-25.

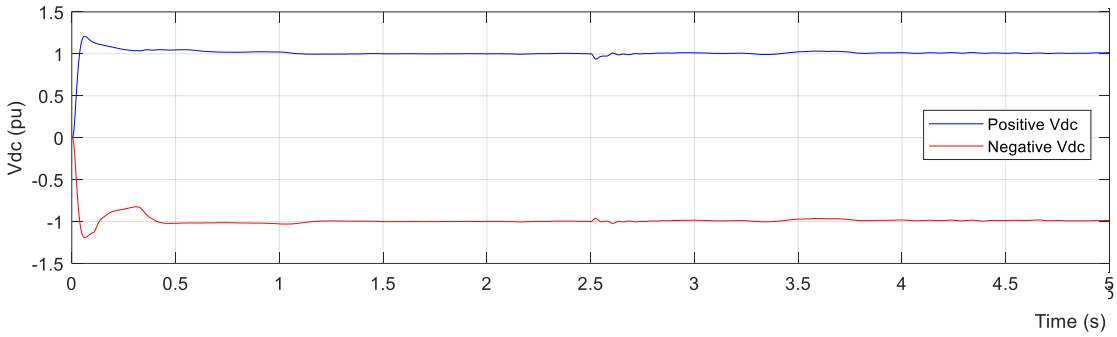


Figure 3-27 DC voltage with DRs connected (case 2)

The dc voltage for the second case is shown in Figure 3-27. The characteristics shown in this figure are the same as in the first case in Figure 3-23, which is at its rated value of $\pm 1\,pu$ ($\pm 320\,k\,V$) except for a small drop at $2.5\,s$ due to the added elements.

The output at the grid side was also measured, and the following results were obtained, as shown in Figure 3-28. The grid-side inverter is a voltage source converter (VSC) only, and no diode rectifiers were added.

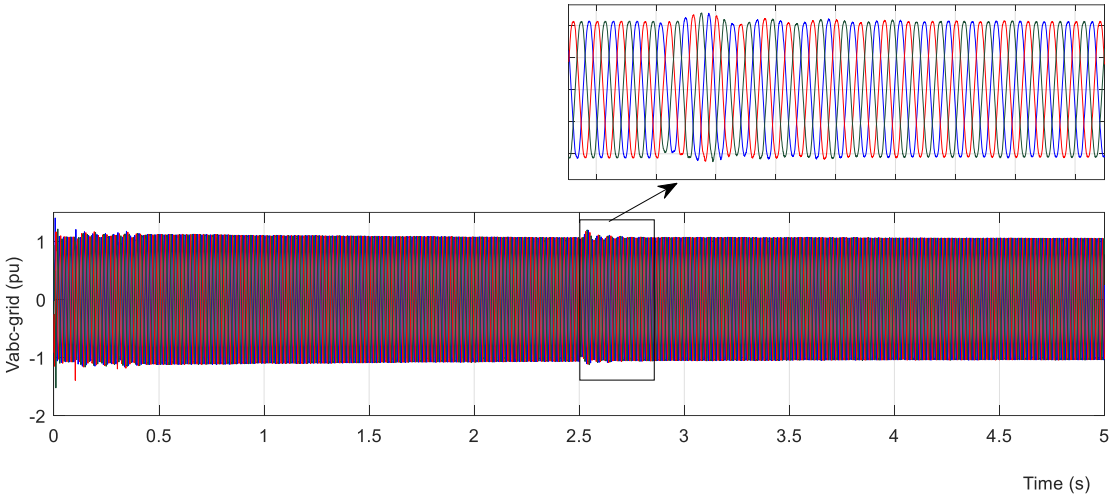


Figure 3-28 Grid-side output ac voltage – second case

- **Case 3 - VSC and DRs with the VSC in the middle**

A third case study, which is the same as case 2 except for a different rectifiers arrangement, was designed, implemented, and simulated. In this case, the arrangement is DR-VSC-DR (i.e. the VSC is connected in the middle, as shown in Figure 3-29).

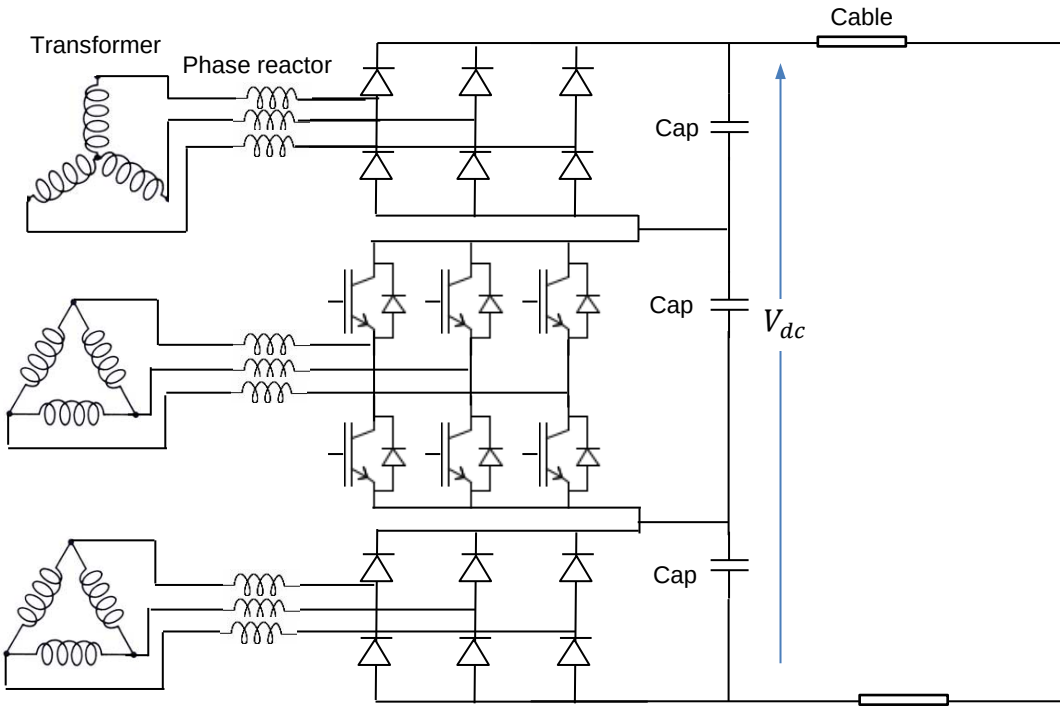


Figure 3-29 Converter topology with the VSC in the middle

Unlike the second case, the VSC controls the total voltage of the dc cable instead of its own voltage. However, the simulation results showed that this case gives the same results as in the second case (case 2). Figure 3-30 presents the results for this case. This figure reveals the active, reactive and three-phase voltage produced by windfarm 1.

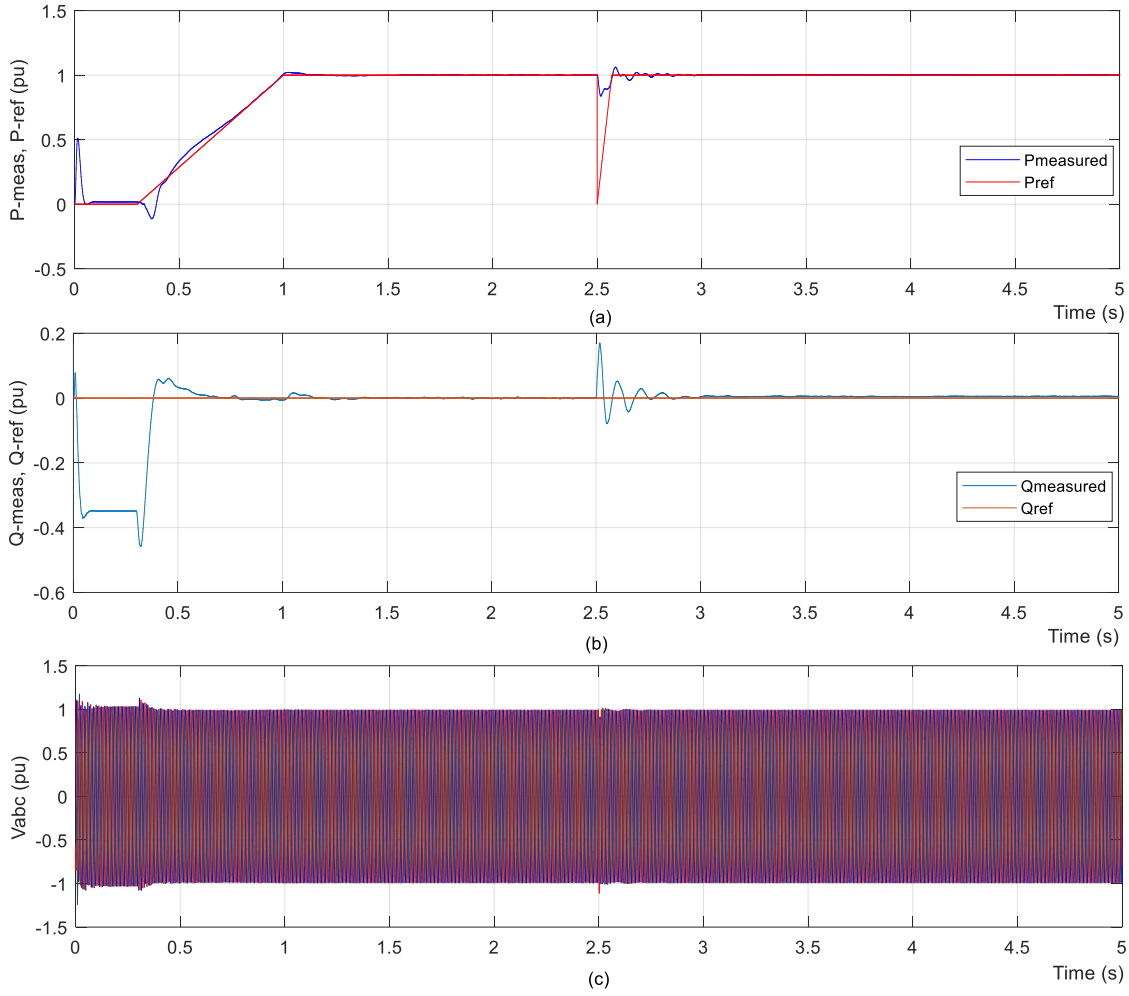


Figure 3-30 Third case for VSC in the middle in pu: (a) measured and reference active power, (b) measured and reference reactive power, and (c) three-phase ac voltage at windfarm 1 (case 3).

3.7 Summary

This chapter introduced an MTDC model based on the series connection of a VSC and two diode rectifiers. The design principles of the model equipment (block) was presented. The control strategies for the converters and the MTDC

system were presented and discussed. The model enables the comparison between two connections such as the case when the diode rectifiers are connected to the model with the case when the diode rectifiers are disconnected. Therefore, the model is a reference model, which can run various operational modes including a VSC system only or VSC and diode rectifier system. This model was designed and implemented using MATLAB/Simulink. Finally, the results for three case studies was presented.

The analyses and the simulation results shows that this topology can be used to implement MTDC model.

4 DC FAULT ANALYSES

4.1 Introduction

Fault analysis studies have significant importance in MTDC networks because faults can present destructive results to the overall system. Among all, faults in the dc side, such as short circuit of the dc cable—such as pole-to-pole (PP) or pole-to-ground (PG) faults that can occur in the cable—can cause major damage to the system. PG faults occur when either the positive pole or negative pole is short-circuited to ground; PP faults involve a short circuit connecting the positive to the negative pole. Throughout the fault, the current increases substantially and rapidly and can damage the nearby dc cables, freewheeling diodes of the IGBTs, and possibly the entire VSC station and MTDC network can be at risk. Thus, the study of dc cable faults and protection in VSC-based MTDC networks is crucial.

Faults in power systems are the main cause for transients that could be hazardous for connected equipment to that network. However, transients are caused by a variety of sources in MTDC systems. Surges can be a result of lightning strikes, switching device operation, and dc voltage change due to terminal loss. PP faults are considered to present the most severe effects on the nearby network [92], but generally, PG faults occur more frequently than PP faults [93].

In any case, the protection scheme of MTDC systems should be sensitive, selective, fast, and reliable. Specifically, they must be designed to isolate the faulty part reliably from the rest healthy parts of the system within a short time after the fault occurrence, while maintaining the remaining parts of the system in a secure operational condition.

The time development of PG faults in a system is described in the next sections by presenting the example of a short circuit in the system at the dc cable.

4.2 The Model of DC Cable

The dc cable model that was used in the model was designed and implemented using MATALB/Simulink. The cable model can be based on lumped parameters or on distributed parameters. However, a lumped-parameter cable model was selected, designed, and implemented. The cable parameters, including cable radius and operating voltage level, were taken from an actual XLPE (cross-linked polyethylene), $\pm 150\,kV$, $350\,MW$ VSC-HVDC subsea cable [213,214]. This $105-km$-long subsea cable links Estonia and Finland (Estlink) [140,215,216].

Table 4-1 Dc cable parameters

Layer	Material	Radius or thickness $[mm]$	Resistivity (ρ) $[\Omega \cdot m]$	Permittivity (ε) [F/m]	Permeability (μ) [H/m]
Cable core	Cu	25.2	1.72 e^{-8}	1	1
Insulation	XLPE	15	-	2.3	1
Sheath	Lead	2.8	$2.2e^{-7}$	1	1
Insulation	XLPE	5	-	2.3	1
Armor	Steel	5	$1.8e^{-7}$	1	10
Insulation	PP	4	-	2.1	1

The cross-sectional area can be scaled up to the operating voltage of a $\pm 320\ kV$ cable without changing the electric field intensity. A summary of cable material properties is shown in Table 4-1; cable cross-sectional area layout is depicted in Figure 4-1 [234].

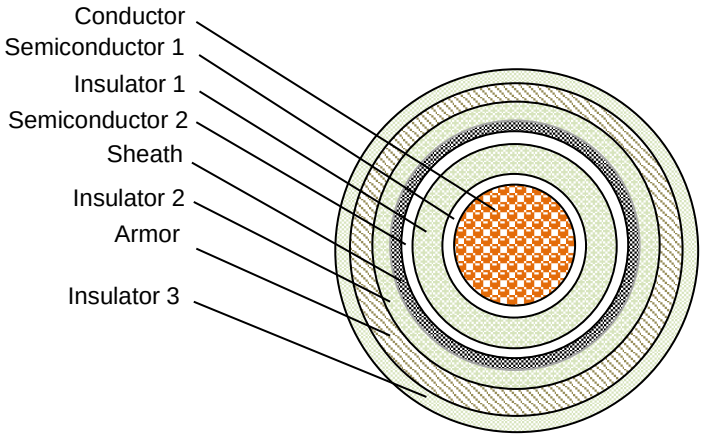


Figure 4-1 DC cable based on XLPE

The cable main insulation is typically extruded by thin layers of semiconducting material on both outer and inner surfaces to prevent electric field concentration between the insulation and the conductor and to provide a smooth interface for the electric field [217]. Generally, the sheath of the cable is grounded at approximately $900\ m$ (i.e. at cable joint) to provide a path to ground when the sheath encounters overvoltage in the case of sheath-to-pole faults. Each joint is grounded by a bare copper [235]. In this thesis, it was assumed that the sheath had ground potential. The parallel resistive branch of the insulation of the XLPE cable was set to $1 \times 10^{-12}\ [s \cdot km^{-1}]$.

The Simulink model of the subsea cable was designed and implemented so that it could simulate the fault at any given point using four sections. Parameters of the cable can be given for any section and can be different from other sections. For example, the four sections can have different material types, line lengths, RLC line parameters, and fault resistances. Moreover, all fault types, including PG fault and PP fault, can be initiated in the cable, as shown in Figure 4-2.

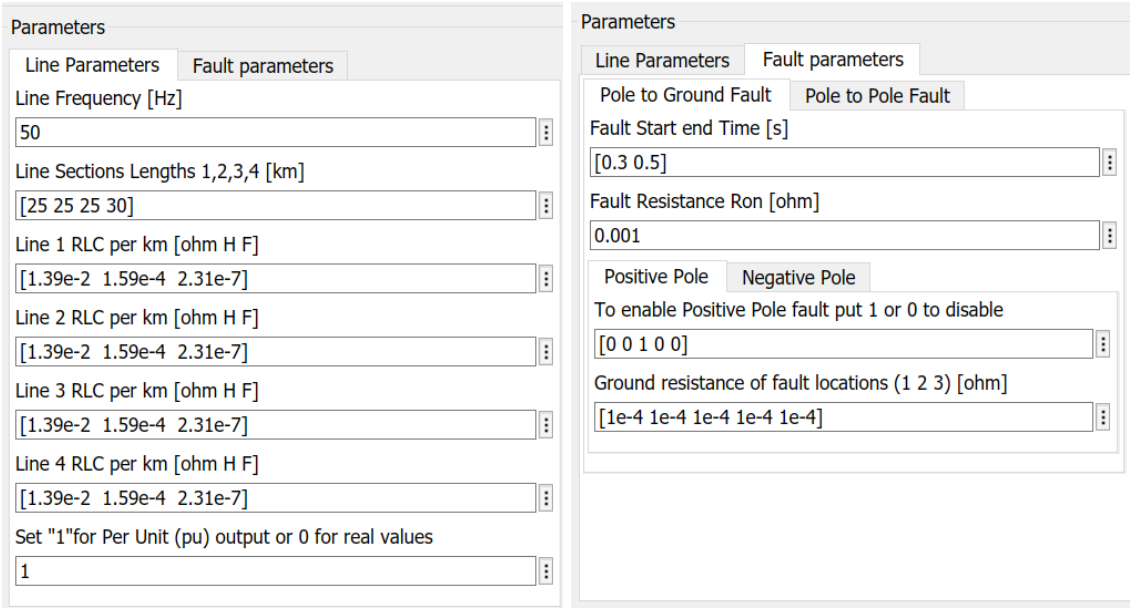


Figure 4-2 Mask of cable model

The block consists of four sections, which have four-line section lengths and four RLC values. The measurements for voltage and current can be made either as absolute values or as per-unit values (pu). The right-hand side of Figure 4-2 shows the fault information. To enable a certain type of fault, one zero should be replaced by a 1 for five different locations (i.e. the first zero represents a fault at the WFVSC1 dc busbar, the second zero produces a fault between sections 1 and 2, and the fifth zero initiates a fault at the receiving end busbar, GSVSC). The fault resistance for these locations can be specified separately. The parameters in Figure 4-2 are for a positive PG fault. The negative PG and PP faults can have similar information. The fault timing can specify the start and end times of the fault, which are the same for both negative and positive PG.

4.2.1 Frequency-Independent

The model of the dc cable may not consider the frequency dependency of the line parameters. However, some parameters, such as the resistance due to the skin effect, are frequency dependant. In this section, the frequency dependency of the line parameters was neglected to simplify the solution. During steady-state operation, frequency-dependant parameters can be ignored.

- **Series Impedance**

The easiest way to model the cable is by representing it using series impedance (RL). Such a model gives accurate results only for short lines due to negligible cable capacitance. Also, this assumption is acceptable under steady-state operation studies such as load flow analyses, and the operating voltage is dc voltage (or low-frequency voltage) within a medium range of voltage. Therefore, a cable model based on detailed frequency-dependant parameters is unnecessary [236]. For long cables, this model is inappropriate.

- **Cascaded Lumped Pi-Sections**

For short cables, the series impedance representation of the cable model is sufficient. However, neglecting the shunt capacitance gives inaccurate results for longer cables. Thus, a cascaded multi $\Pi - sections$ yields more accurate results by including the capacitance of the cable. This model uses a definite number of $\Pi - sections$.

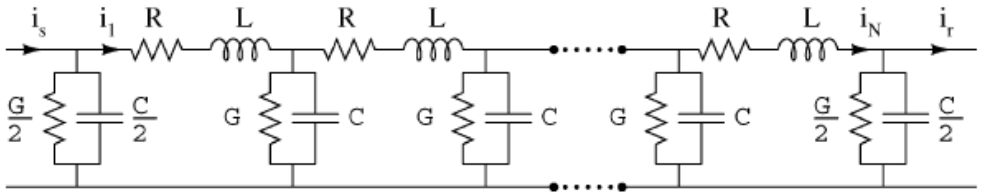


Figure 4-3 N pi-section cascaded line model

Each section is modelled by admittances and impedances, which are frequency independent, and lumped, as shown in Figure 4-3. the number of sections that required for better accuracy, depends upon the operating frequency range. Thus, the highest possible frequency, which can give a reasonable accuracy by the cascaded $\Pi - sections$ can be approximated using the following equation [237], which shows that the relationship between the number of sections and the highest frequency approximately

$$f_{max} = \frac{\mathbb{N}.\gamma}{\pi.l} \qquad \textbf{(4-1)}$$

where f_{max} is the highest frequency (Hz), l is the total line length (m), $\mathbb{N}$ is the number of $\Pi - sections$, andγ is the traveling wave speed, which is calculated by the following expression:

$$\gamma = \frac{1}{\sqrt{LC}} \quad \textbf{(4-2)}$$

For example, if the traveling wave equals the speed of light ($c = 2.99 \times 10^8\ m/s$) in a $100\ km$ long overhead line, then a single $\Pi - section$ line gives accurate results for approximately 950 Hz. A single-section model could be sufficient to study the interaction between the control system and the power system. However, if the model is to represent a cable involving high-frequency studies in the range of kilohertz, such as transient switching surge, then much shorter $\Pi - sections$ are needed. However, a line model using distributed parameters gives the most accuracy.

If the simulation time step is larger than the wave traveling time in the dc cable modelled by lumped parameters, then the simulation will give accurate simulation results. Otherwise, accuracy would be lost.

- **Bergeron Model**

This model is based on a constant frequency. It uses the distributed inductance and capacitance (LC) line parameters. However, the line resistance is lumped at the ends of the line and placed in the middle of the model. Hence, the Bergeron Model gives the least accuracy among the distributed parameter models. This model is suitable only if fundamental frequency is important and line length is long enough [238]. Therefore, the model can be used when computational speed is more important than accuracy. The result is reasonable and the accuracy can be achieved if ($\frac{R}{4} \ll R_c$), where $R_c = \sqrt{\frac{L}{C}}$ is the line characteristic impedance or the surge impedance [239, p.124].

- **Distributed Parameters of Lossless line**

The parameters R, L, C, and G are actually distributed along the line. The analytic expressions in this section are based on the traveling wave theory. Unlike Bergeron's, this model considers the resistance, reactance, and admittance, which will be represented as distributed elements. The analytic expressions derived for fault surges based the following partial differential equation (PDE) at point x along a lossless cable:

$$\frac{\partial v(x,t)}{\partial x} = -L\frac{\partial i(x,t)}{\partial t} \quad \textbf{(4-3)}$$

$$\frac{\partial i(x,t)}{\partial x} = -C\frac{\partial v(x,t)}{\partial t} \quad \textbf{(4-4)}$$

where L, C are inductance, capacitance of the line respectively, derivation and substitution of (4-3) and (4-4) gives the following equations into decoupled form:

$$-\frac{\partial^2 v(x,t)}{\partial x^2} - L.C\frac{\partial^2 v(x,t)}{\partial t^2} = 0 \quad \textbf{(4-5)}$$

$$-\frac{\partial^2 i(x,t)}{\partial x^2} - L.C\frac{\partial^2 i(x,t)}{\partial t^2} = 0 \quad \textbf{(4-6)}$$

The general solution could be given using D'Alembert as follows:

$$v(x,t) = v^{for}\left(t - \frac{x}{\gamma} + \mathcal{F}^{for}\right) + v^{bac}\left(t + \frac{x}{\gamma} + \mathcal{F}^{bac}\right) \quad \textbf{(4-7)}$$

$$i(x,t) = i^{for}\left(t - \frac{x}{\gamma} + \mathcal{F}^{for}\right) + i^{bac}\left(t + \frac{x}{\gamma} + \mathcal{F}^{bac}\right) \quad \textbf{(4-8)}$$

where $\mathcal{F}^{for}$, $\mathcal{F}^{bac}$ are arbitrary forward and backward constants, respectively, and $\gamma = 1/\sqrt{LC}$ is the propagation speed. The term $v^{for}\left(t - \frac{x}{\gamma} + \mathcal{F}^{for}\right)$ is a traveling voltage wave that propagates with constant velocity in the positive direction along the $x - axis$. The same analogy holds true for v^{bac}, i^{for}, and i^{bac}. These terms are the forward voltage, backward voltage, forward current, and backward current, respectively. Substituting (4-7) and (4-8) into (4-3) [240, p.51] yields the following:

$$i^{for} = \frac{v^{for}}{R_c} \quad \textbf{(4-9)}$$

$$i^{bac} = -\frac{v^{bac}}{R_c} \quad \textbf{(4-10)}$$

Then, substituting the above equations into (4-8) gives

$$v(x,t) = v^{for}\left(t - \frac{x}{\gamma} + \mathcal{F}^{for}\right) + v^{bac}\left(t + \frac{x}{\gamma} + \mathcal{F}^{bac}\right) \quad \textbf{(4-11)}$$

$$i(x,t) = \frac{1}{R_c}\left[v^{for}\left(t - \frac{x}{\gamma} + \mathcal{F}^{for}\right) - v^{bac}\left(t + \frac{x}{\gamma} + \mathcal{F}^{bac}\right)\right] \quad \textbf{(4-12)}$$

For infinite-length line, $\mathcal{F}^{for} = \mathcal{F}^{bac} = 0$. For finite-length line, $\mathcal{F}^{for} = T$, $\mathcal{F}^{bac} = 0$, and $T = \frac{l}{\gamma}$; l is the line length.

- **Distributed Parameters for Lossy Line**

Unlike ideal (lossless) cable, the general solution for practical cable cannot be formulated using the time domain directly by d'Alembert method because of the dispersion caused by line losses [240, p.129]. Hence, the PDE in the time domain is

$$-\frac{\partial v(x,t)}{\partial x} = Ri + L\frac{\partial i(x,t)}{\partial t} \quad \textbf{(4-13)}$$

$$-\frac{\partial i(x,t)}{\partial x} = \mathrm{G}v + \mathrm{C}\frac{\partial v(x,t)}{\partial t} \quad \textbf{(4-14)}$$

where R and G represent cable resistance and conductance, respectively. Transformation of these equations to the s domain gives

$$\frac{dV}{dx} = -Z(s)I \quad \textbf{(4-15)}$$

$$\frac{dI}{dx} = -Y(s)V \quad \textbf{(4-16)}$$

where $Z(s)$ and $Y(s)$ are the respective impedance and admittance of the cable per-unit length in Ω and $siemens$, respectively, as shown in (4-17) and (4-18):

$$Z(s) = sL + R \quad \textbf{(4-17)}$$

$$Y(s) = sC + G \quad \textbf{(4-18)}$$

Derivation and substitution of (4-15) and (4-16) and rearranging the results gives independent decoupled formulae describing V and I, as follows:

$$\frac{\partial^2 V}{\partial x^2} - V.k^2(s) = 0 \quad \textbf{(4-19)}$$

$$\frac{\partial^2 \mathrm{I}}{\partial x^2} - I.k^2(s) = 0 \quad \textbf{(4-20)}$$

where $k(s)$ denotes the propagation constant, expressed as

$$k(s) = \sqrt{Z(s).Y(s)} = \sqrt{(R+sL)(G+sC)} \quad \textbf{(4-21)}$$

The solution of equations (4-19) and (4-20) in the s domain gives

$$V(x,s) = V^{for}(s) \cdot e^{-k(s)\cdot\left(x-\mathcal{F}^{for}\right)} + V^{bac}(s) \cdot e^{-k(s)\cdot\left(x-\mathcal{F}^{bac}\right)} \quad \textbf{(4-22)}$$

$$I(x,s) = \frac{1}{Z_c(s)}\left[V^{for}(s) \cdot e^{-k(s)\cdot\left(x-\mathcal{F}^{for}\right)} - V^{bac}(s) \cdot e^{k(s)\cdot\left(x-\mathcal{F}^{bac}\right)}\right] \quad \textbf{(4-23)}$$

where V^{for}, V^{bac}, $\mathcal{F}^{for}$, and $\mathcal{F}^{bac}$ are arbitrary forward and backward functions, and $Z_c(s) = \sqrt{\frac{Z(s)}{Y(s)}} = \sqrt{\frac{R+sL}{G+sC}}$ is the characteristic impedance of the cable.

The solution equations (4-22) and (4-23) in the time domain are not direct. However, Miano & Maffucci [240, p.137] used the convolution theorem approach to obtain impulse response of the line $q(x,t)$ and the step of the voltages $V^{for}(t)$ and $V^{bac}(t)$ timely and locally. This approach gives the values of the voltage and current in any location in a two-dimensional time - space plane:

$$v(x,t) = [q_v(x,t) \circledast v^{for}(t)] + [q_v(l-x,t) \circledast v^{bac}(t)] \quad \textbf{(4-24)}$$

$$i(x,t) = [q_i(x,t) \circledast i^{for}(t)] + [q_i(l-x,t) \circledast i^{bac}(t)] \quad \textbf{(4-25)}$$

where l stands for the cable length (m), ($\circledast$) denotes a convolution integral, and $q_v(x,t)$ is the response of the voltage impulse in the time domain, defined as follows:

$$q_v(x,t) = e^{-\mu\frac{x}{\gamma}}.\delta\left(t-\frac{x}{\gamma}\right) + \mathcal{y}^2 e^{-\mu t}\frac{x}{\gamma}\frac{I_1\left(\mathcal{y}.\sqrt{t^2-\left(\frac{x}{\gamma}\right)^2}\right)}{\mathcal{y}.\sqrt{t^2-\left(\frac{x}{\gamma}\right)^2}}u\left(t-\frac{x}{\gamma}\right) \quad \textbf{(4-26)}$$

where $I_1(\ldots)$ is a first-order modified Bessel function [241, p.559], $\delta(t)$ is a Dirac function, $u(t)$ represents a unit step function, $\mathcal{y} = (\aleph - \beta)/2$ and $\mu = (\aleph + \beta)/2$ are coefficients where $\aleph = R/L$ and $\beta = G/C$ are inductive and capacitive damping factors, respectively.

The impulse response has two terms: the first is the main term, which is responsible for the attenuation and given by the losses that are distributed over the line; and second term accounts for the waveform distortion due to the dispersion of the cable. The first term can be solved easily since it involves a

Dirac delayed pulse only, while the second term is more complex and requires more complex calculations and effort. The trapezoidal numerical integral approximation rule is used to solve the convolution integral [240]. However, neglecting the second term does not affect the results in most cases. A similar derivation is used for the impulse response of the current $q_i(x,t)$:

$$q_i(x,t) = \frac{\beta+1}{R_c} e^{-\mu\frac{x}{\gamma}} \delta\left(t-\frac{x}{\gamma}\right) + e^{-\mu t} I_1\left(v.\sqrt{t^2-\left(\frac{x}{\gamma}\right)^2}\right) u\left(t-\frac{x}{\gamma}\right) + \frac{\beta-\mu R_c}{R_c} I_o\left(v.\sqrt{t^2-\left(\frac{x}{\gamma}\right)^2}\right) u\left(t-\frac{x}{\gamma}\right) \quad \textbf{(4-27)}$$

with $R_c = \sqrt{\frac{L}{C}}$, $I_o(\cdot)$ is a modified 0-order Bessel function [242, pp.355–358], and $u(.)$ denotes a unit step function.

4.2.2 Frequency Dependence of Parameters

The previous section considered cable parameters as frequency independent. However, cable parameters are not constant when frequency changes. For example, cable resistance shows the highest frequency dependency over an entire range of frequency from very low frequency of 1 Hz to 1 MHz, as shown in Figure 4-4 (blue dotted curve) [243, p.86]. The high frequency-dependant resistance is primarily because of the skin effect. The current tends to pass closer to the surface when the frequency is higher, making the skin depth thinner.

Figure 4-4 shows the inductance of the cable $L(f)$ (red solid line). Inductance $L(f) = 0$ at $f = 0\ Hz$ (i.e. dc current) and reaches a peak value frequency

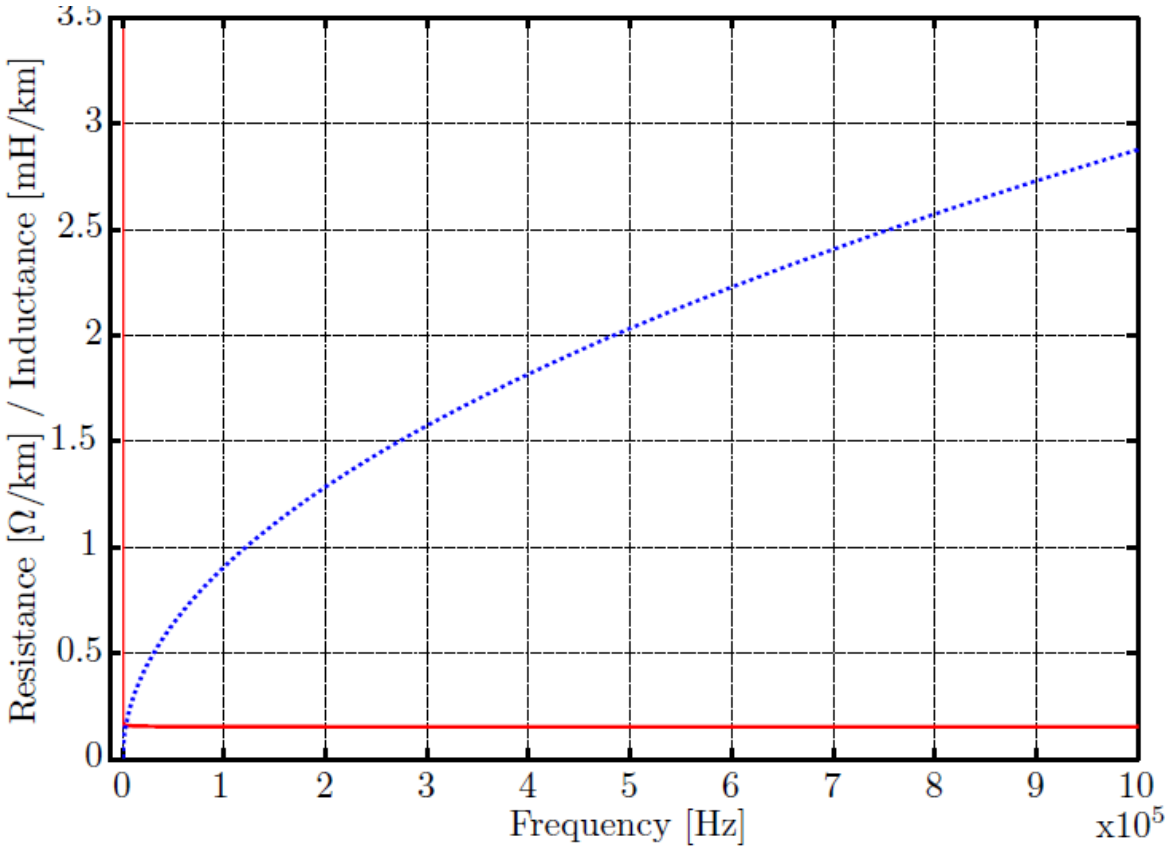


Figure 4-4 Cable frequency dependency parameters: resistance Ω/km (blue) and inductance mH/km (red)

below $1\ Hz$ range. The inductance shows almost constant values for frequencies higher than $1\,Hz$, where it decreases slightly as the frequency increases. Therefore, during typical operating conditions, fault inductance could be assumed as constant. If frequency-dependant parameters are considered, then equation (4-24) and (4-25) should include this dependency as follows [244]:

$$v(x,t) = V_o.erfc\left(\frac{\varepsilon}{2\sqrt{t-\frac{x}{\gamma}}}.\frac{x}{\gamma}\right).u\left(t-\frac{x}{\gamma}\right) \quad \textbf{(4-28)}$$

$$i(x,t) = \frac{V_{dc}}{Z_c}.e^{\varepsilon^2 t}.erfc\left(\varepsilon\sqrt{t-\frac{x}{\gamma}}+\frac{\varepsilon}{2\sqrt{t-\frac{x}{\gamma}}}.\frac{x}{\gamma}\right).u\left(t-\frac{x}{\gamma}\right) \quad \textbf{(4-29)}$$

where $\varepsilon = \frac{\Phi}{2L}$ designates the distortion factor, Φ is the skin effect factor, and $erfc$ symbolises the complimentary error function, which is defined as follows: $erfc = \frac{2}{\sqrt{\pi}} \cdot \int_x^{\infty} e^{-t^2} dt$.

4.3 AC Network

The adjacent ac networks to which the offshore HVDC system is connected may be modelled using an equivalent R_{ac} and X_{ac} impedance of the short-circuit ratio and a voltage source v_{ac}. Determination of the ac network parameter values is accomplished using the power network short-circuit ratio (SCR) in the ac grid at the PCC. The SCR can also be defined as the division of the fault power and the converter rated power and is mathematically expressed as follows [203]:

$$SCR = \frac{P_{PCC}^{sc}}{P_{conv}^{rated}} \quad \textbf{(4-30)}$$

where the superscript (sc) signifies short circuit, and the subscript ($conv$) refers to the converter. Then, the ac resistance and inductance are calculated as follows:

$$R_{ac} = \frac{V_{ac}^2}{SCR.P_{conv}^{rated}} \cdot cos\left(\tan^{-1}\frac{X_{ac}}{R_{ac}}\right) \quad \textbf{(4-31)}$$

$$L_{ac} = \frac{V_{ac}^2}{SCR.P_{conv}^{rated}} \cdot sin\left(tan^{-1}\frac{X_{ac}}{R_{ac}}\right) \cdot \frac{1}{2\pi f} \quad \textbf{(4-32)}$$

The term $\frac{X_{ac}}{R_{ac}}$ represents the ratio of the ac system reactance to its resistance; f is the nominal frequency of the ac system, and the subscript $conv$ denotes converter.

4.4 Network and Converter Model

The model shown in Figure 4-5 is based on the model illustrated in Figure 3-1, which was used here for the dc fault studies. The two converters at the offshore side are based on the series connection of a VSC and two diode rectifiers, as shown in Figure 3-2. A PP fault was established that has fault resistance R_f of

0.001 at a location $50\ km$ from WFVSC1. The distance of the fault was chosen randomly and is not the most severe case regarding the converter station. The impact of distance on fault current is beyond the scope of this thesis; the topic can be studied by changing the fault resistance. Fault resistance has a much greater influence on fault current than the (smaller) faulty cable section resistance; the closer the fault to the busbar, the greater the fault current. However, faults at, or close to, the busbar are uncommon.

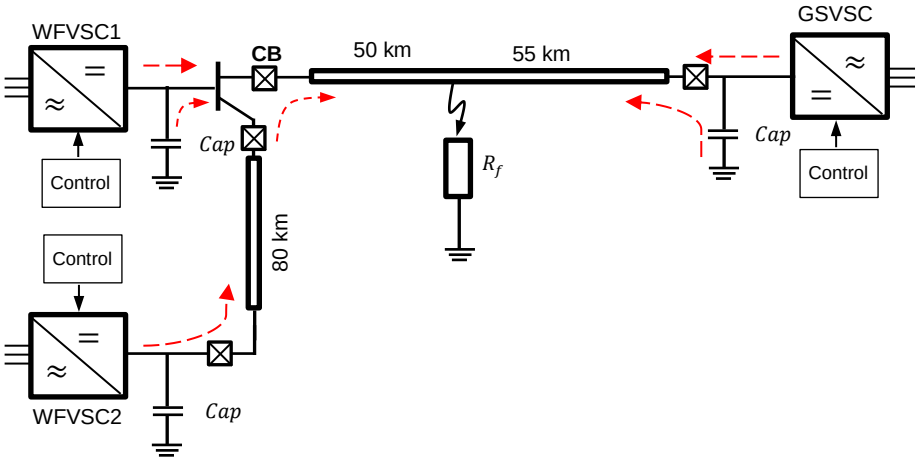


Figure 4-5 The proposed model showing fault currents

The VSC converter used in this study is 3-level NPC (also called 12 pulse) $\pm 106.67\ kV$ with rated power of $120\ MW$. The converter is connected in series with two diode rectifiers with the same voltage and power ratings presented earlier in section 3.2. A monopolar-based VSC topology with lumped dc capacitors (Cap) with grounded-midpoint at each terminal. However, other topologies such as bipolar are possible.

Figure 4-6 depicts the cable equivalent circuit that connects and transmits the dc power from WFVSCs to GSVSC. The parameters of the ac grid were determined according to the ac system SCR at the PCC that connected to the converter.

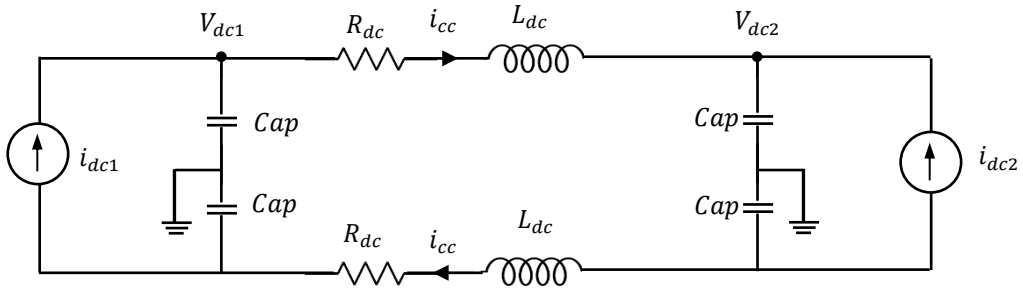


Figure 4-6 Equivalent circuit HVDC-VSC (between WFVSC and GSVSC)

The SCR is found by dividing the capacity of the system during the fault at the PCC to the converter rated power [203], as shown in equation (4-30). More details in section 4.3.

4.5 Fault Currents Transient Analysis

4.5.1 Fault Current Contribution Sources

To explain the fault current and its transient development through a dc circuit breaker (CB) when a dc fault occurs in a cable of the MTDC system, the schematic diagram is presented in Figure 4-7. This figure also displays the parts of the system that contribute to the fault current. Hence, the fault current is caused by a collection of individual components (contributors) such as cables, dc capacitors, and the neighbouring feeders. This allows the influence of each component on the fault current to be studied and analysed individually. Consequently, the total current of the fault in the CB is calculated using the superposition. Knowing the fault current and the transient conditions enables the system designer to design a fault detection algorithm and to determine the dc CB specifications.

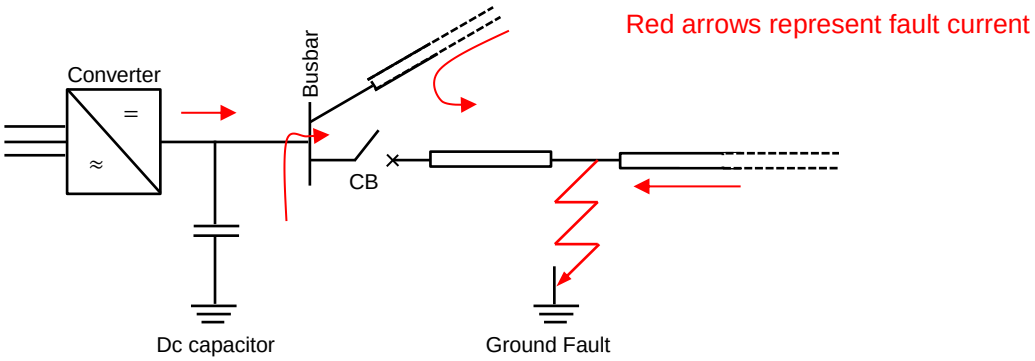


Figure 4-7 A section dc network layout; red arrows are the fault current

In this section, PP faults will be analysed in a monopolar cable of the proposed MTDC model with two dc cable branches, including all fault current component contributors in the dc CB. Although faults of overhead lines are more frequent than cable faults, cable faults are usually permanent [93], and dc systems should be able to cope with. PG faults generally occur more frequently compared to PP faults, but PP faults result in more severe impacts on the system [92].

4.5.1.1 Short-Circuited, Infinitely Long Cable

To start analysing cable transmission lines, the analytical expression is considered for an infinitely long line. The derivation is to find out wave shape distortion by short circuiting one end of the cable, as shown in Figure 4-8. Then, voltage $v_x(x,t)$ and current $i_x(x,t)$, which are calculated at any time and at any point, can be derived.

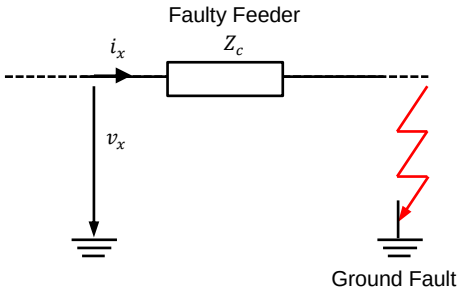


Figure 4-8 infinitely long cable discharge

A negative voltage wave will be initiated during the occurrence of the dc fault, and will lead to a high-frequency waveform due to the very steep surge front.

During the propagation of the wave through the cable and after the reflection at the terminal capacitor, the wave front may flatten, but the frequency content is still high. In such a case, the inductance of the cable contributes to a high level of independence. As shown in Figure 4-4, the resistance parameter is dealt with as a dependent of frequency only. The penetration depth of the traveling surges is much less than the conductor diameter of the cable because of the high frequency content. Hence, the current is assumed to pass through a conductor surface of an indeterminately thin film, and the cable impedance is directly proportional to the square root of the frequency [245]. Generally, the inner conductor dc resistance of XLPE cables is low, and dielectric losses are also negligible, as illustrated in section 4.2. Thus, shunt conductance and dc resistance have negligible effect and can be neglected. So, the Laplace s −domain of the admittance and impedance of the cable is described as

$$Z(s) = \Phi \cdot \sqrt{s} + L.s \tag{4-33}$$

$$Y(s) = C \cdot s \tag{4-34}$$

where Φ represents the skin effect. By applying a binomial expansion to $k(s)$ and $Z_c(s)$, and taking the first two terms, the following approximations is obtained [245]:

$$k(s) = \sqrt{\left(L \cdot s + \Phi \cdot \sqrt{s}\right) \cdot C \cdot s} \approx \frac{s}{\gamma}\left(1 + \frac{\Phi}{2L} \cdot s^{-\frac{1}{2}}\right) \tag{4-35}$$

$$Z_c(s) = \sqrt{\frac{\left(L \cdot s + \Phi \cdot \sqrt{s}\right)}{C.s}} \approx R_c\left(1 + \frac{\Phi}{2L} \cdot s^{-\frac{1}{2}}\right) \tag{4-36}$$

with high-frequency characteristic impedance of the cable, $R_c = \sqrt{\frac{L^{HF}}{C^{HF}}}$, and the speed of propagation $\gamma = \frac{1}{\sqrt{L^{HF}C^{HF}}}$. Current and voltage surge equations are computed using (4-24) and (4-25), respectively, in the s domain. However, the forward traveling wave ($V^{for}(s)$) is considered only, and the magnitude of the initial voltage step at the fault location is assumed as V_o:

$$V^{for}(s) = \frac{V_o}{s}$$

$$V^{bac}(s) = 0$$

$$V(x,s) = \frac{V_o}{s} e^{-\frac{x}{\gamma}s - \frac{x}{\gamma}\varepsilon s^{1/2}} \quad \textbf{(4-37)}$$

$$I(x,s) = \frac{V_o}{R_c s(1+\varepsilon s^{1/2})} e^{-\frac{x}{\gamma}s - \frac{x}{\gamma}\varepsilon s^{1/2}} \quad \textbf{(4-38)}$$

The solutions in the time domain were derived by Wigington & Nahman, and Magnusson [244,245], respectively:

$$v(x,t) = V_o \cdot erfc\left(\frac{\varepsilon}{2\sqrt{t-\tau}} \cdot \tau\right) \cdot u(t-\tau) \quad \textbf{(4-39)}$$

$$i(x,t) = \frac{V_o}{R_c} \cdot e^{\alpha^2 t} \cdot erfc\left(\alpha\sqrt{t-\tau} + \frac{\varepsilon}{2\sqrt{t-\tau}} \cdot \tau\right) \cdot u(t-\tau) \quad \textbf{(4-40)}$$

where the delay of the traveling wave is $\tau = \frac{x}{\gamma}$, a complementary error function is $erfc$, the distortion factor is $\varepsilon = \frac{\Phi}{2L}$, and $u(t)$ is a unit step function [242, p.1029].

The above equations give a good estimate of coaxial cable high-frequency behaviour.

4.6 Fault Current Contributors

4.6.1 DC Capacitor Contribution

During the dc fault, the total dc voltage V_{cap} in the Laplace domain at distance l from the CB, across the capacitor, equals the forward plus backward (reflected) traveling wave, as shown in following expression:

$$V_{cap}(s) = V^{for}(l,s) + V^{bac}(l,s) = V^{for}(l,s) + \Gamma(s) \cdot V^{for}(l,s) \quad \textbf{(4-41)}$$

where $\Gamma(s)$ is the reflection coefficient in the s domain, which is defined as

$$\Gamma(s) = \frac{Z_{cap}(s)||Z_c - Z_c}{Z_{cap}(s)||Z_c + Z_c} = -\frac{s}{s + \frac{2}{CR_c}} \quad \textbf{(4-42)}$$

Clearly, $\Gamma(s)$ is a function of the capacitor C, which is given by $Z_{cap}(s) = \frac{1}{sC}$ and the characteristic impedance R_c.

- **Exact Transformation**

A time domain solution is determined by using displacement law and transformation pairs [246]:

$$V_{cap}(t) = V_o.erfc\left(\frac{\varepsilon}{2\sqrt{t-\tau}}.\tau\right) - V_o\frac{1}{2}e^{-\frac{2}{CZ_c}(t-\tau)}.\left[e^{-i\alpha\tau\sqrt{\frac{2}{CZ_c}}}.erfc\left(\frac{\varepsilon\tau}{2\sqrt{t-\tau}} - i\,.\sqrt{\frac{2}{CZ_c}(t-\tau)}\right) + e^{i\varepsilon\tau\sqrt{\frac{2}{CZ_c}}}.erfc\left(\frac{\varepsilon\tau}{2\sqrt{t-\tau}} + i\cdot\sqrt{\frac{2}{CZ_c}(t-\tau)}\right)\right].u(t-\tau) \quad \textbf{(4-43)}$$

In the above equation, a complex argument is found in the error function; Faddeeva-Function ($\omega(z)$) is used to compute it [242, p.297].

Then, the capacitor current contribution i_c is calculated:

$$i_c(t) = -C_{cap}.\frac{dV_{cap}}{dt} \quad \textbf{(4-44)}$$

The negative sign is used in (4-44) because the V_c polarity opposes the direction of capacitor current, as shown in Figure 4-9.

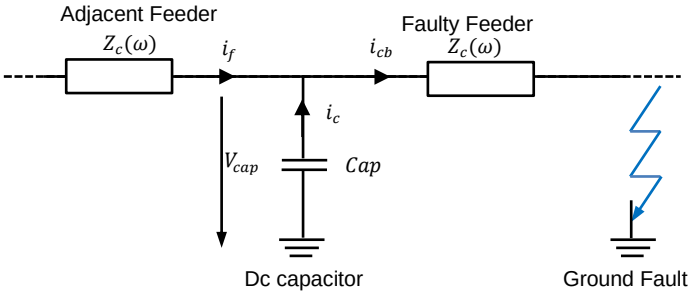


Figure 4-9 Current Contribution of adjacent feeder and dc capacitor

- **Approximation**

Equation (4-44) gives the exact solution in the time domain, which is long and requires greater computational effort. However, the exponential function

argument can be modified to give an approximation in the s domain in (4-41) for the reflected wave of the voltage. This can be obtained by shifting the frequency s in the numerator by $\frac{2}{CZ_c}$ as follows:

$$V^{for}(l,s)\cdot\Gamma(s) = -\frac{V_o}{Z_c}.e^{\left(-\tau s-\tau\varepsilon s^{\frac{1}{2}}\right)}\cdot\frac{1}{s+\frac{2}{CZ_c}}$$
$$\approx -V_o.e^{-\tau\left(s+\frac{2}{CZ_c}\right)}\cdot e^{\tau\frac{2}{CZ_c}}\cdot\frac{e^{-\tau\varepsilon\sqrt{s+\frac{2}{CZ_c}}}}{s+\frac{2}{CZ_c}} \quad \textbf{(4-45)}$$

The factor $e^{\tau\frac{2}{CZ_c}}$ will compensate for the error shift $\frac{2}{CZ_c}$ of the frequency in the exponential function term, but for the second term, this gives an incorrect result because of the frequency square root. However, this approximation is valid only if s is larger than $\frac{2}{\tau_C}$. The term τ_C is the dc capacitor time constant and equals CZ_c. When equation (4-45) is transformed back to the time domain, this will allow the application of displacement law, which results in the following equation:

$$V_{cap}(t) = V_o\cdot erfc\left(\frac{\varepsilon\tau}{2\sqrt{t-\tau}}\right)\cdot\left(e^{-\frac{2}{CZ_c}(t-\tau)}-1\right)\cdot u(t-\tau) \quad \textbf{(4-46)}$$

The capacitor voltage time derivative gives the current contribution of the capacitor as

$$i_c(t) = -C.\frac{dv_{cap}}{dt}$$
$$= -V_o.\left[e^{-\frac{\varepsilon^2\tau^2}{4(t-\tau)}}\cdot(t-\tau)^{-\frac{3}{2}}\cdot\left(e^{-\frac{2}{CZ_c}(t-\tau)}-1\right)\right.$$
$$\left.-\frac{2}{CZ_c}e^{-\frac{2}{CZ_c}(t-\tau)}\cdot erfc\left(\frac{\varepsilon\tau}{2\sqrt{t-\tau}}\right)\right]\cdot \mathrm{u(t-\tau)} \quad \textbf{(4-47)}$$

4.6.2 Contribution of Adjacent Feeder

The feeder that is connected to the same busbar of the faulty cable is termed the adjacent feeder and is shown in Figure 4-7 and Figure 4-9. The current contribution derivation of the adjacent feeder to the fault current i_f is calculated

using a similar approach to the previous section for the calculation of capacitor contribution. The incident surge of negative voltage that begins at the location of the ground fault is partially propagated through the busbar to the neighbouring cable; hence, it has a contribution to the total CB fault current due to its discharge. Therefore, the ground fault current of adjacent feeder of length l from the dc CB is calculated in the s plane by

$$I_f(s) = I^{for}(l,s) \cdot T_c(s) = I^{for}(l,s) \cdot [\Gamma(s) + 1] \quad \textbf{(4-48)}$$

where $I^{for}(l,s)$ stands for the forward surge of current and $T_c(s)$ is the transmission coefficient. An infinitely long adjacent feeder was assumed. Thus, unlike equation (4-41) for the voltage of the capacitor, a backward traveling wave is not considered in the above equation.

- **Exact Transformation**

To calculate the exact current contribution of the adjacent feeder in the time domain, the partial fraction decomposition is used in the denominator of the previous equation.

$$I_f(s) = I^{for}(l,s) - \frac{V(l,s)}{\left(s + \frac{2}{CZ_c}\right) \cdot (\varepsilon s^{-1/2} + 1)}$$

$$= I^{for}(l,s) - \frac{V(l,s)}{\varepsilon^2 + \frac{2}{CZ_c}} \left(\frac{\frac{2}{CR_c}}{\frac{2}{CZ_c} + s} + \frac{\varepsilon s^{1/2}}{\frac{2}{CZ_c} + s} - \frac{\varepsilon}{\varepsilon + s^{1/2}} \right) \quad \textbf{(4-49)}$$

By means of the transformation pairs found in [247, p.461], direct transformation of both the first and last terms in (4-49) to the time domain can be found. However, to transform the second term, both the denominator and numerator should be first multiplied by $s^{1/2}$, which infers the resulting solution derivative of the time domain:

$$\frac{\varepsilon s}{\frac{2}{CZ_c} s^{1/2} + s^{3/2}} = \frac{d}{dt} \mathcal{L}^{-1} \left\{ \frac{\varepsilon}{\frac{2}{CZ_c} s^{1/2} + s^{3/2}} \right\} \quad \textbf{(4-50)}$$

The exact solution in the time domain can be done using mathematical software such as Mathematica and is not present here.

- **Approximation**

Similarly, adding a frequency shift to $I^{for}(l,s)+\frac{2}{CZ_c}$ gives an approximation that simplifies the solution and corresponding adjustment factors by excluding the terms in the square root and uses the displacement law. Therefore, the resulting equation in the time domain is

$$i_f(\mathrm{t}) = \frac{V_o}{Z_c}\, \mathrm{e}^{\varepsilon^2 t}\, erfc\left(\varepsilon\sqrt{t-\tau}+\frac{\varepsilon\tau}{2\sqrt{t-\tau}}\right)\left(1-e^{-\frac{2}{CZ_c}(t-\tau)}\right)\mathrm{u}(\mathrm{t}-\tau) \quad \textbf{(4-51)}$$

However, this is accurate only if $s \gg \frac{2}{CZ_c}$.

4.6.3 Total CB Current

By applying the superposition to all fault current contributions, the total current resulting from the first surge is obtained. Hence, the sum of the dc capacitor current i_c and the neighbouring feeder currents i_f is the current in the dc CB:

$$i_{cb}(\mathrm{t}) = i_c(\mathrm{t}) + i_f(\mathrm{t}) \quad \textbf{(4-52)}$$

Additionally, to consider the following surges that are reflected by the fault, the travel delay for i_c and i_f should be incremented by 2τ. Therefore, the total CB current due to subsequent N surges is

$$i_{CB}(\mathrm{t}) = \sum_{m=0}^{N-1}\left[i_c(\mathrm{t}-2\tau\mathrm{m}) + i_f(\mathrm{t}-2\tau\mathrm{m})\right] \quad \textbf{(4-53)}$$

Note that that the adjacent feeder cable was assumed to be infinitely long. Therefore, backward traveling surges are not considered in the above equation. This is because there are no reflections from the adjacent feeder.

4.7 DC Cable Fault Characteristics

Classical HVDC (LCC) systems are considered robust to the faults in dc side due to the connection of large smoothing reactance which is typically series connected with dc cable. Therefore, there is no overcurrent in the dc cable. On

the other hand, VSC-based HVDC are robust to ac side disturbances due to the controllability of the VSCs. However, VSCs are vulnerable to dc faults due to the freewheeling diodes and the discharge current from the reactive elements. Thus, once a fault happens in the dc cable, the response of the system to the fault presents three stages based on the time of each stage, as shown in Figure 4-10 [107]. These stages are expressed as follows:

- Stage 1: The equivalent circuit of this stage is shown in Figure 4-10a. This stage is due to the dc capacitor discharge, which means that the dc capacitor contributes to the fault through its discharge. This stage occurs immediately after the fault.
- Stage 2: This stage is represented by Figure 4-10b, which is the freewheeling diode period. In this stage, the IGBTs of the VSC are in their blocking mode due to self-protection. The antiparallel diodes continue working as uncontrolled rectifiers. This stage starts after the dc capacitor discharge and its voltage becomes zero.

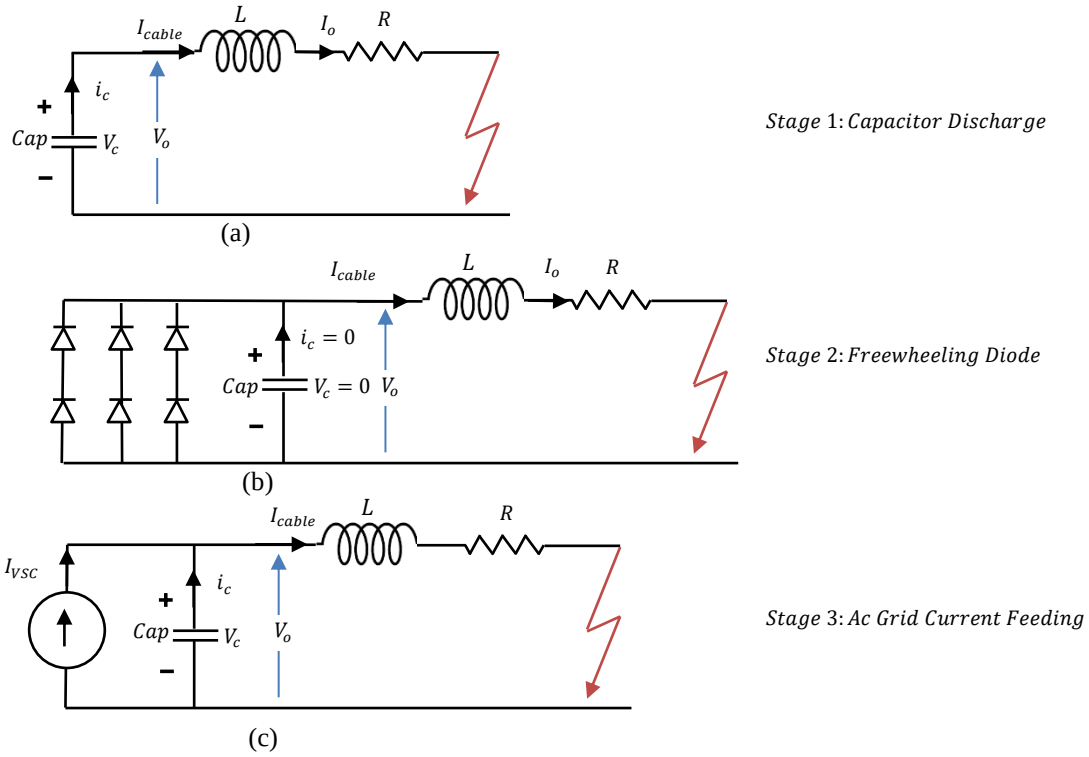


Figure 4-10 Equivalent circuits for short-circuited cable fault showing the three phases

- Stage 3: Figure 4-10c illustrates the equivalent circuit of this stage. The ac current of the grid feeds the dc fault during this stage; the ac grid feeds the fault via the diode path

4.8 Pole-to-Ground Fault Analyses

PG faults are caused primarily internally by aging of the insulators or externally by digging (or by anchoring in the case of subsea cables) [214, pp.211–221]. These factors may lead to a cable insulation breakdown and ultimately to a PG fault. In the case of cable insulation failure, an electric current will pass to the ground through the nearest grounding point initiated from that faulty insulation point between the pole and sheath. The arc current rises rapidly, and a breakdown and damage likely occurs to the cable at that location, resulting in a low resistive path between the ground and the pole. Low resistive path of the fault current reduces the voltage of the dc cable to a low value within microseconds. The voltage value is determined by fault resistance, fault current magnitude, and soil characteristics (soil resistivity, and time constants of soil ionization and deionization) [248]. Due to the fault path inductance, cable capacitance, and voltage supporting devices, there is no instantaneous voltage drop, although it occurs rapidly. However, the lower the fault resistance, the more severe the fault conditions and the higher the line voltage drop. Hence, the path of discharge characteristics plays a vital role in fault conditions. Just after the fault, voltage surges begin traveling (traveling wave phenomena) toward the terminals in both directions, and the cable capacitance starts to discharge into the fault progressively. The negative wave of the traveling voltage will be reflected by the terminal as a positive wave because of the terminal capacitor and the traveling time τ [249]. The dc capacitors at the VSC terminals are designed to filter out ripples of the dc voltage. In the case of a multilevel converter, a smaller filtering capacitor is required, but for a 3-level NPC VSC, a higher capacitor volume is needed (approximately three times greater) than that of a 2-level VSC to maintain the ripple of the DC line voltage within about 5% [250]. However, filter capacitances might be unrequired in MMC topologies with a sufficiently high number of levels (submodules) [251];

during dc faults, the storage capacitors are prevented from discharge by the blocked valves of the converter [252, p.173]. Typically, dc capacitors at the midpoint of bipolar HVDC systems are grounded to offer the pole voltages a reference voltage [250,253].

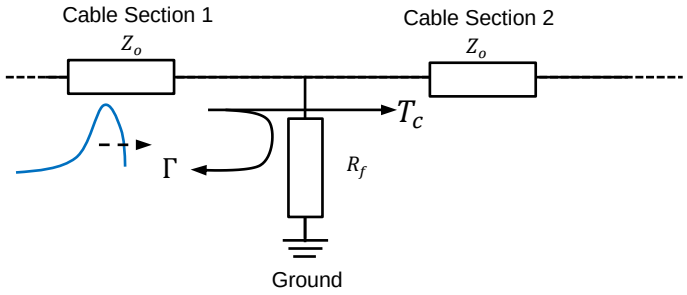


Figure 4-11 Transmission and reflection of waves at the location of the fault

When the bipolar system is required to operate as a monopole, the midpoint is generally grounded using a low resistive or reactive impedance, or it can be left ungrounded. A closed loop will be produced from the grounded midpoint of the capacitor and the PG fault that provokes the capacitor's discharge [191]. This discharge current and reflected traveling wave coincide with each other. The backward traveling wave is calculated using the incident wave convolution form and the dc capacitor response of the impulse [240] (assuming the parameters of the cable have pure capacitance):

$$v_{refl}(t) = \left[-\delta(t) + \frac{2}{Z_c * C} e^{-\frac{l}{Z_c C}} * \sigma(t)\right] * v_{incid}(t) \quad \textbf{(4-54)}$$

where $\delta(t)$ is a unit impulse (Dirac pulse); C is dc capacitance; Z_c is lumped, approximate cable resistance; and $\sigma(t)$is a step function.

At the location of the fault, part of the wave will be reflected, and the rest of the wave will travel to the opposite section through the fault along the cable. The value of the reflected wave depends upon the reflection coefficient (Γ) and the coefficient of the transmission (T_c). This is illustrated in Figure 4-11. The traveling surges, both the backward and forward, produce multiple peaks in the waveform of the current [203]. The reflection coefficient is defined mathematically as follows:

$$\Gamma = -\frac{1}{1 + \frac{2R_f}{Z_c}} \quad \textbf{(4-55)}$$

R_f refers the resistance of the fault and Z_c is the cable characteristic impedance during the fault, which is defined as follows:

$$\mathrm{Z}_c = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad \textbf{(4-56)}$$

The relationship between the reflection coefficient and transmission coefficient is as follows:

$$\mathrm{T} = 1 + \Gamma \quad \textbf{(4-57)}$$

Figure 4-12 shows the relationship between the reflection coefficient and the fault resistance magnitude, to gives an indication about the parameters affect the reflection coefficient which helps in determining the reflected surge.

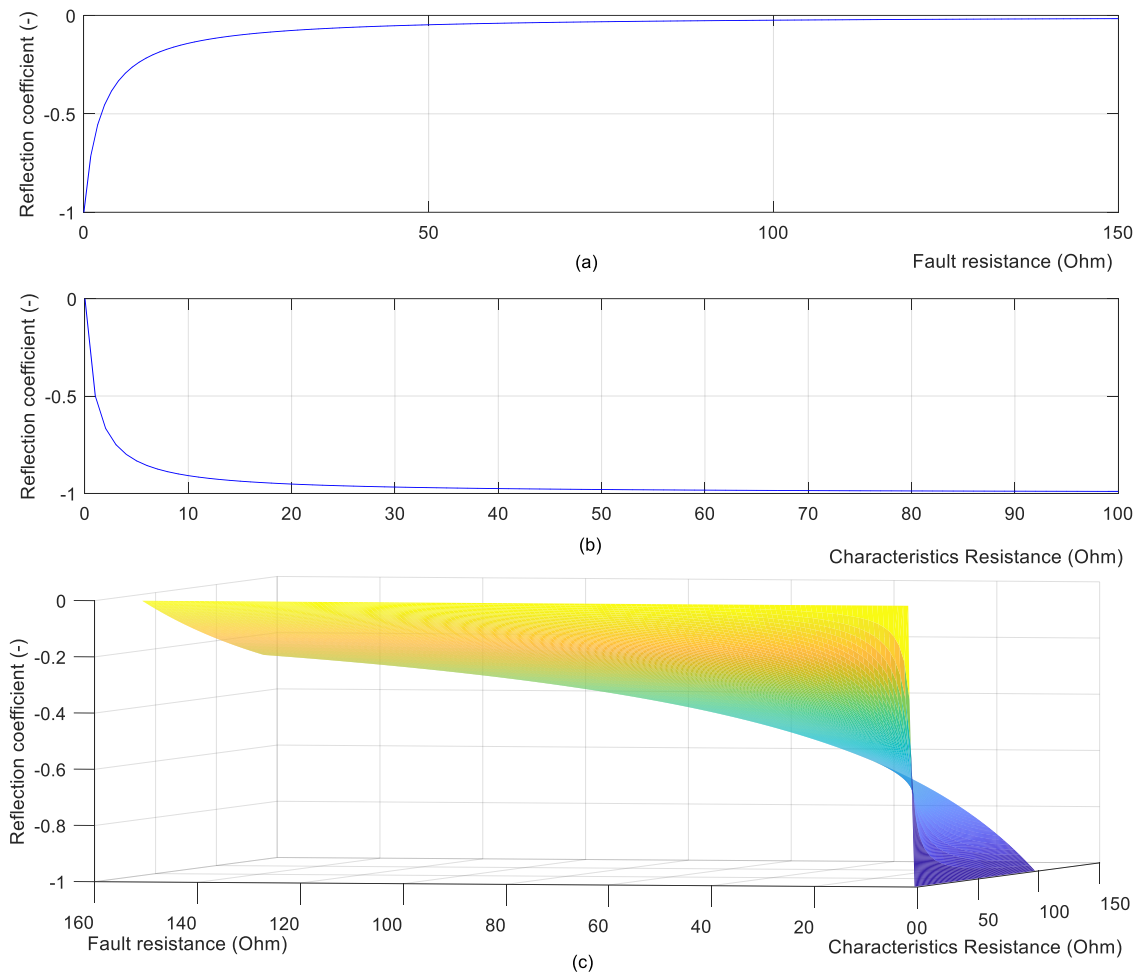


Figure 4-12 Reflection coefficient as a function of (a) fault resistance at fault location, (b) characteristic resistance, and (c) fault resistance and characteristic resistance

4.9 Simulation Results and Discussion

While classical HVDC technology depends upon a thyristor because reactors can successfully suppress the dc fault current, VSCs show high dc fault vulnerability. Faults in dc cables, however, are more frequent than faults in the other sections of the system, which are caused primarily by insulation breakdown due to deterioration, aging, electrical stresses, physical damage, and environmental conditions.

In such fault types, a short circuit can occur between positive and negative poles. Therefore, severe fault conditions with hazardous impacts can be seen in

the system. Hence, this section investigates the system performance under pole-to-pole faults. Moreover, the protection system was disabled to observe the characteristics of the fault under such condition. During the fault, the freewheeling diodes across the IGBTs and the series-connected rectifiers continue conducting and providing a path current to follow to the fault.

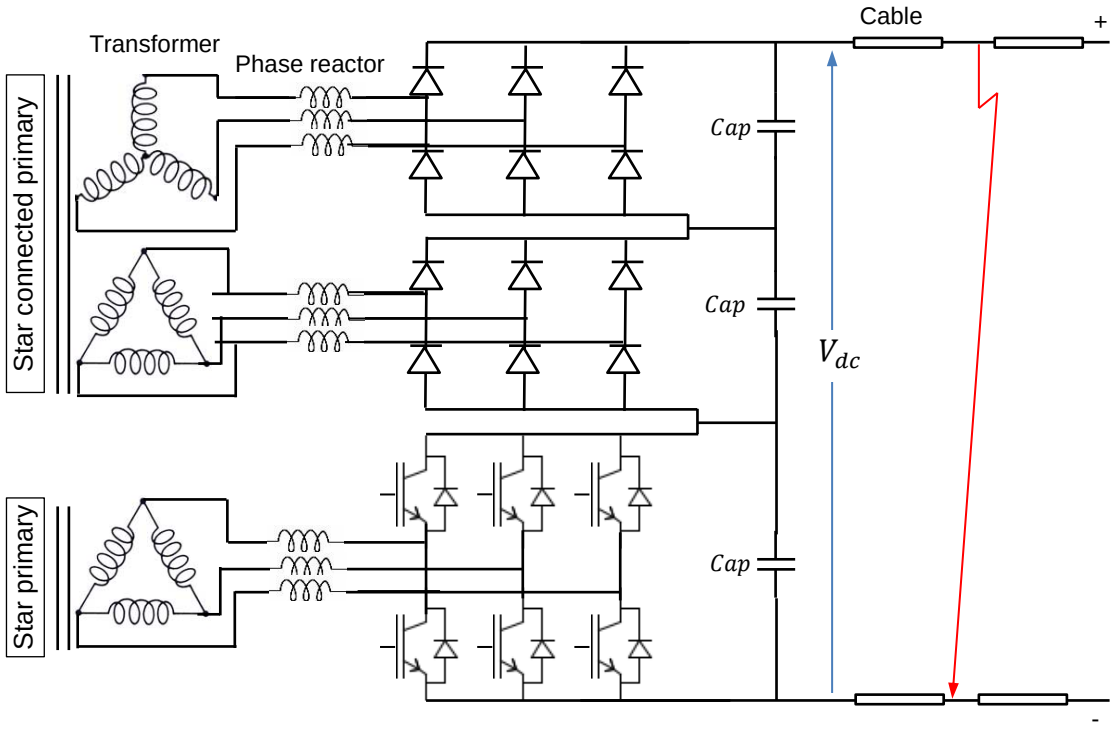


Figure 4-13 System configuration under PP faults

A section of the model with dc cable pole-to-pole fault is illustrated in Figure 4-13. However, in fault analyses, IGBTs generally are blocked by self-protection. This leaves the anti-parallel diode to conduct the fault current, which is usually overcurrent [92]. Therefore, IGBTs can be omitted in fault studies. Note that the transformer for the diode rectifier has two secondary terminals and is configured as Y/Y/Δ. However, various stages for contribution of different system components are presented in section 4.7. The MATLAB/Simulink model was introduced in section 3.2, and the proposed model's performance under dc fault is presented in this section, in case a comparison of faults under two different operational modes is required.

4.9.1 Simulation Case Studies

The proposed model was tested using MATLAB/Simulink software. The model was used as VSC only, which is called Connection 1 (refer to section 3.6). Table 4-2 summarises these cases and the connections in each case. However, a case with diode rectifiers only was not tested. The simulation started at ($t = 0\ s$) for $5\ s$. Then, at $t = 2.5\ s$, the diode rectifiers were connected to the model. Doing this enables the model to compare the two operational Modes I and II in the same model in a single simulation run. To assess the model, a dc fault was initiated in Mode I, and the same dc fault was used in Mode II. Therefore, the system performance can be evaluated in the same simulation run. The simulation was run two times, the first one using Connections 1 and 2, and a second run using Connections 3 and 4. The model parameters are found in Table 3-1, Table 3-2, and Table 3-6.

Table 4-2 Case study summary

Operational model	Connection name	VSC	Diode Rectifiers	Arrangement
Mode I (VSC only)	Connection 1	√	-	VSC-DR-DR
Mode II (With diodes)	Connection 2	√	√	VSC-DR-DR
Mode I (VSC only)	Connection 3	√	-	DR-VSC-DR
Mode II (With diodes)	Connection 4	√	√	DR-VSC-DR

- **Case 1 (Connections 1, 2)**

The configuration converter and the rectifiers were arranged as VSC-DR-DR, as shown in Figure 4-13. The total simulation time was $5\ s$; the simulation was started with the VSC only connected to the model. At time $t = 0\ s$, all of the converters were in their block mode or disconnected (Figure 4-14). Therefore, no current (active power) flowed to the dc system.

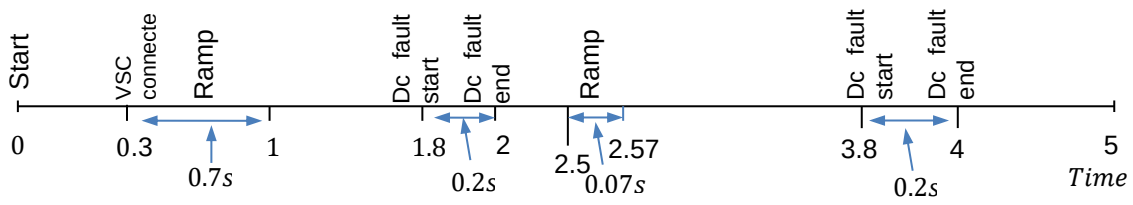


Figure 4-14 Simulation timing

At $t = 0.3\ s$, the VSCs of windfarms 1 and 2 were connected to the system, as shown in Figure 4-15a, which illustrates both active and reactive power at PCC of windfarm 1. Similar results can be obtained from windfarm 2. Hence, the measured active power at windfarm 1 ramped from zero to reach the rated value

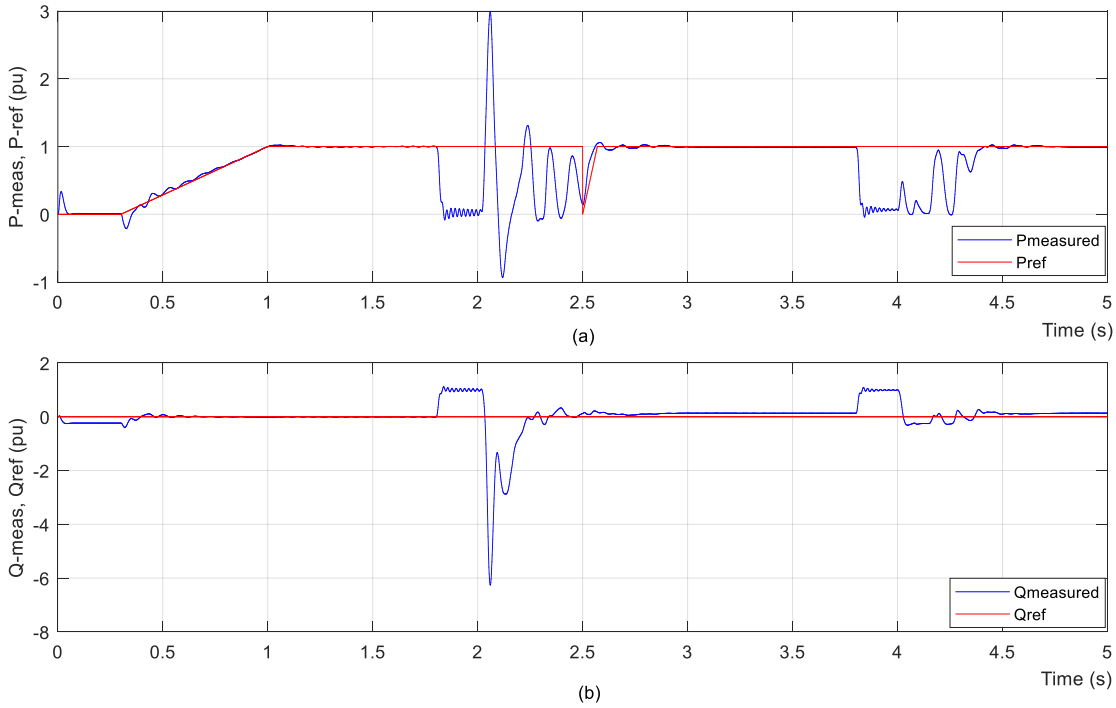


Figure 4-15 Active and reactive power at PCC: (a) active power and (b) reactive power

($1\ pu$) within $0.7\ s$. It can be seen that the measured active power (blue line) followed the reference value (red line). At $t = 1.8\ s$, the PP dc fault was started. It lasted for $200\ ms$ and caused the active power to fall down to zero within $50\ ms$ then become approximately $0.1\ pu$. After the fault clearance, an overshoot of $2.5\ pu$ was measured, and fluctuations followed the overshoot. At $t = 2.5\ s$, the diode rectifiers were switched on and connected to the system. The active power also followed the reference value. Another fault was started at $t = 3.8\ s$ and lasted for $200\ ms$; the same response was seen as the previous fault, where the active power fell down to zero within $50\ ms$ and then settled down at approximately $0.1\ pu$. The difference between Modes I and II was that with Mode II, after the fault clearance, the overshoot disappeared and the

fluctuations were supressed more rapid. The fluctuation took approximately $0.35\,s$, which means that the proposed configuration improved the system response against dc faults in terms of the overshoot elimination and the time required for the system to return to its steady-state operation. Note that the system in this case works without a protection system, which was disabled.

The reactive power measurement was $0\,pu$ at the simulation start. Then, there was a negative reactive power due to the reactive elements, including the harmonic filter and phase reactor. After switching on the converters, they started to control the reactive power at $0\,pu$. The negative sign means that the reactive power direction is from the converter toward the windfarm. At the fault occurrence time ($1.8\,s$), the reactive power increased to $2\,pu$ within $40\,ms$, as shown in Figure 4-15b.

After the fault clearance, a negative reactive power peaked at $-4\,pu$ and returned gradually to its steady-state value ($0\,pu$). This was the case until $3.8\,s$, when the second fault started. This time, the reactive power increased to $1.5\,pu$, which is slightly less than the previous one by 25%. After the fault clearance, as in the active power, the overshoot did not appear and the negative reactive power settled down after $0.3\,s$ at the steady-state value. Thus, the system response was improved after the connection of the diode rectifiers for both active and reactive power.

Figure 4-16 illustrates the three-phase voltage and current measured at the PCC. The voltage in Figure 4-16a started with slightly more than $1\,pu$. Then, at $0.3\,s$, the converters were connected and started to control the active and reactive power, which leads to control of the ac voltage to $1\,pu$. When the fault started, the voltage dropped to about $0.78\,pu$. However, after the fault clearance, the voltage witnessed overvoltage. Each phase of the voltage had a different overvoltage value due to the different instantaneous phase magnitude and angle values. At $3.8\,s$, the voltage dropped to about $0.85\,pu$. After the fault which lasted for $200\,ms$, the voltage increased to $1.05\,pu$ to be $1\,pu$ within $17\,ms$.

The three-phase current shown in Figure 4-16b started from $0\ pu$ and increased gradually in an analogous way to the active power, which followed the reference line to reach $1\ pu$. At $t = 1.8\ s$, the current increased to about $3.5\ pu$; however, each phase had a different overcurrent peak. The overcurrent of each phase depends on the instantaneous phase magnitude and current value. The current became approximately $2.5\ pu$ until about $t = 2\ s$. Then, after the fault clearance, another overcurrent can be seen, which had a peak of about $4.5\ pu$. The current fluctuation lasted for more than $0.5\ s$.

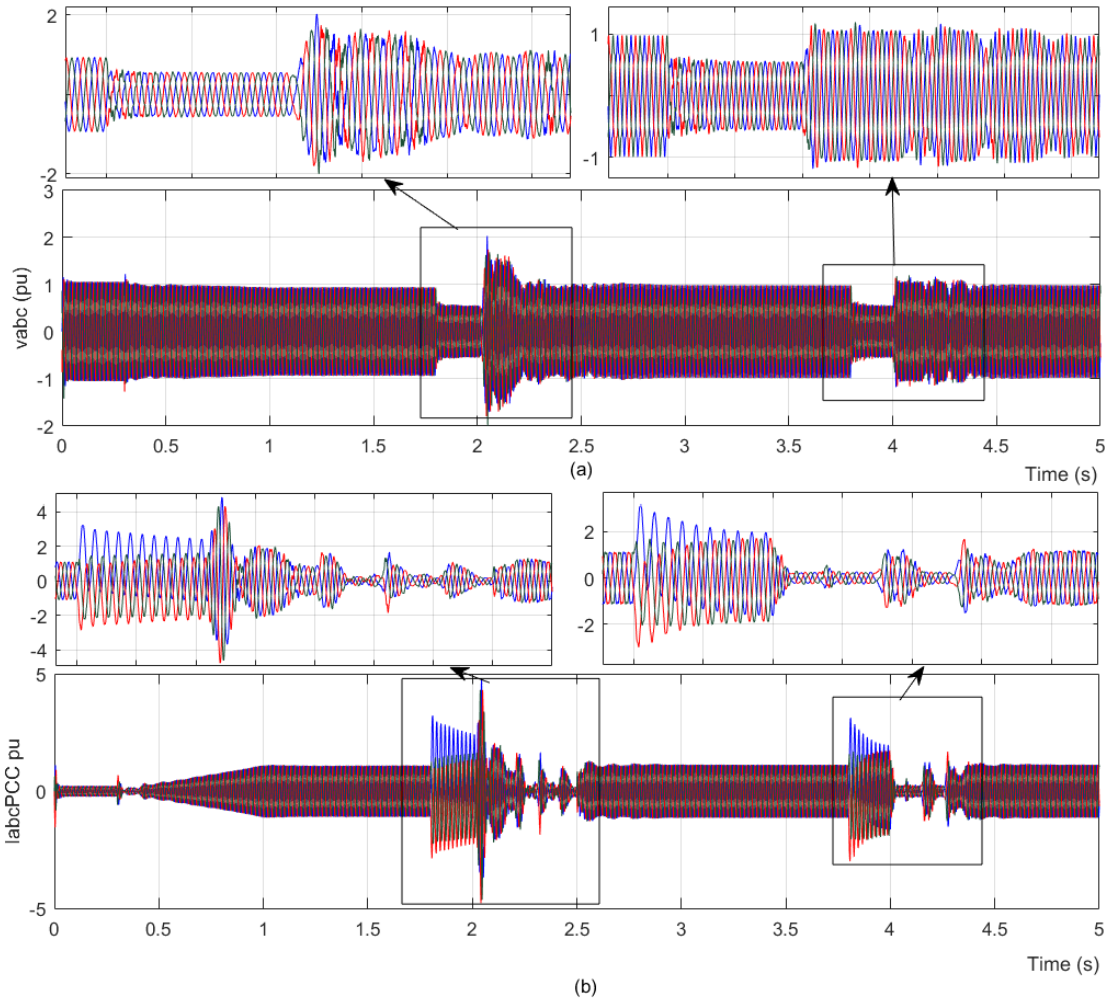


Figure 4-16 Three phase voltage (a) and current (b) at PCC (connections 1, 2)

The ac current at $t = 3.8\ s$ had an overcurrent in the same way as the first fault, but this time it was approximately $3.35\ pu$. In addition, it was different among the three phases due to the different magnitude and phase angle. After the fault

clearance, the current returned to its normal value within $0.3\,s$. Similar to the result with the active power, the fault response of the model was improved due to the connection of diode rectifiers in terms of the overcurrent and the time required for the current to return to its steady-state operation conditions.

Figure 4-17 depicts the positive and negative dc voltage measured in per-unit at the WFVSC1 dc busbar. The dc voltage close to windfarm 2 had the same characteristics. The voltage curve in this figure has similar characteristics as that in Figure 3-23 until the time $t = 1.8\,s$ when the voltage (both negative and positive) dropped to $0\,pu$ within $50\,ms$. The voltage after $t = 2\,s$ witnessed positive and negative overvoltage of approximately $3\,pu$ and peaked within about $80\,ms$ before settling down to $1\,pu$ within about $0.5\,s$.

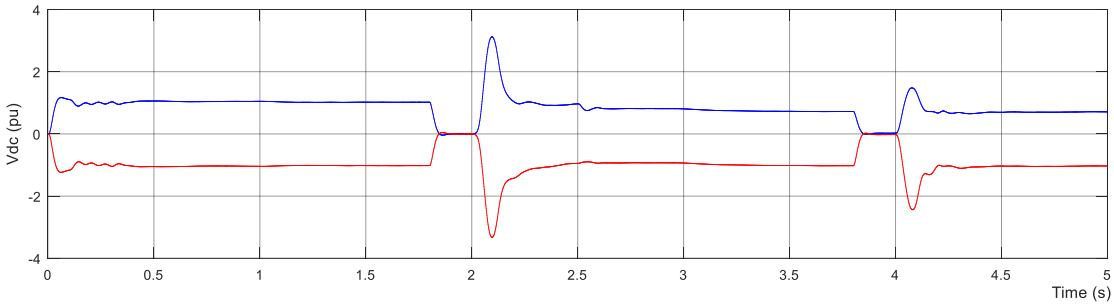


Figure 4-17 Positive and negative dc voltage (cases 1, 2)

The diode rectifiers were connected at $t = 2.5\,s$. Then, at $t = 3.8\,s$, a dc voltage sag was measured, which was similar to the one due to the first fault, and it dropped to zero. After the fault clearance, the voltage had an overvoltage that peaked at $1.5\,pu$, which is less than that of Mode I. This reduction in the amplitude of the overvoltage is considered an improvement, which means that the proposed model has a better fault performance in terms of overvoltage and overcurrent reduction and in terms of time required for the model to return to the steady-state operation. The negative pole and positive pole peaks had different magnitudes. The negative pole overvoltage peak was slightly more than the positive peak. This can be eliminated using the second case (Case 2) when connecting the VSC in the middle.

- **Case 2 (Connections 3,4)**

The configuration with converter and rectifiers was arranged as DR-VSC-DR, as shown in Figure 3-29. The simulation time in this case was also $5\,s$. The simulation began with the VSC only connected to the model at time $t = 0\,s$, and all of the converters were in their block mode (disconnected). At $t = 0.3\,s$, the WFVSC 1 and 2 were connected to the system as shown in Figure 4-14. Similar results can be obtained in Case 2 as for Case 1 except some minor differences. The measured results at windfarm 2 are not presented. The results measured at windfarm 1 are summarised in Figure 4-18 and Figure 4-19.

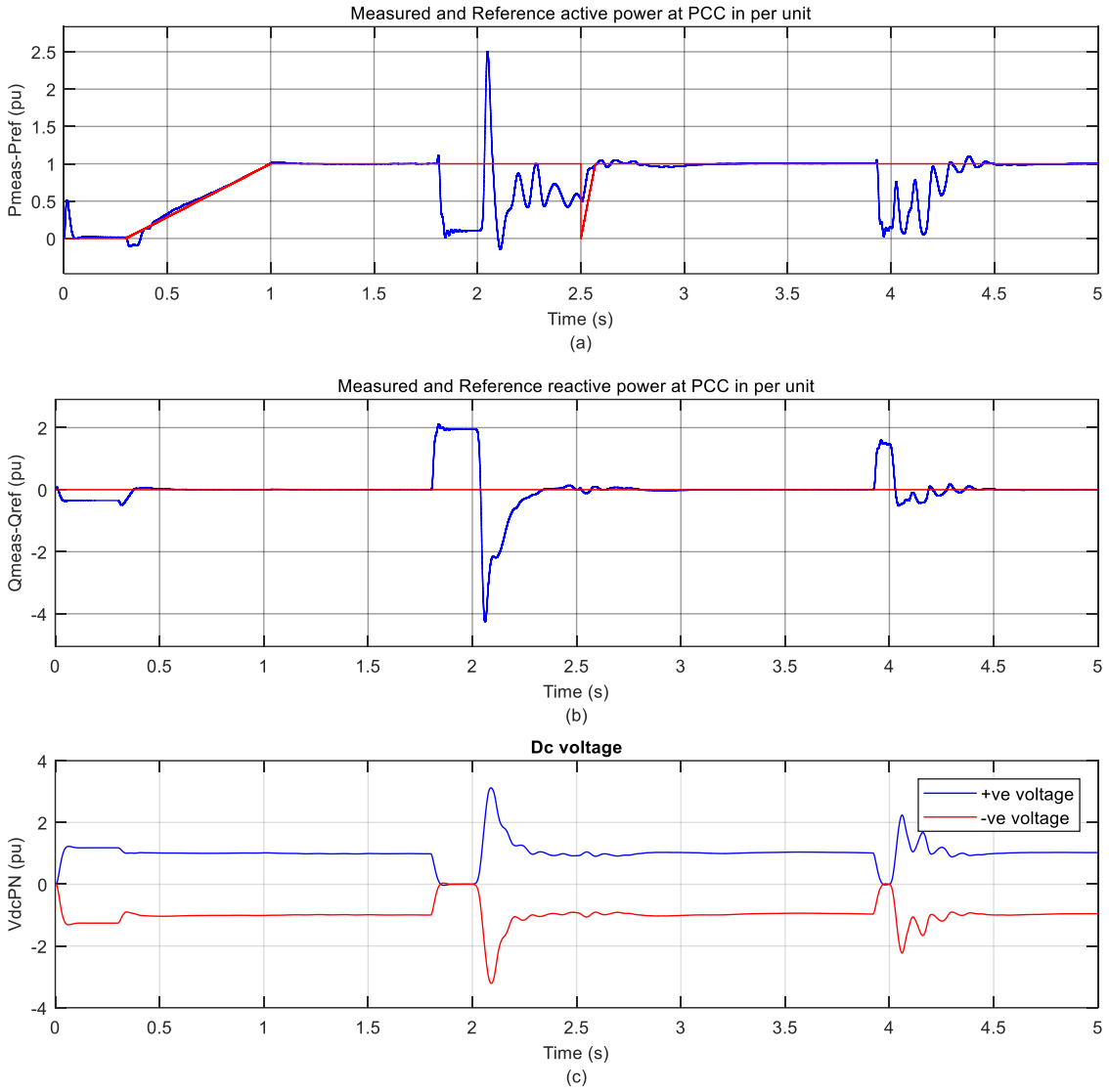


Figure 4-18 Active (a) and reactive (b) power and dc voltage (c) of WF1 (connections 3, 4)

Comparing the results of Figure 4-18 with similar results from the previous case, the same fault characteristics and the same peak values for active power and reactive power after the fault clearance were obtained, as shown in Figure 4-18a, b. However, as expected, the dc voltage had a different overvoltage, as revealed in Figure 4-18c. For the first case (Case 1), the positive and negative peaks were not equal, and the negative voltage amplitude was slightly greater than the positive amplitude. In the second connection (Case 2), the amplitudes of the overvoltage were the same. This difference is due to the balanced

measurement of the dc voltage when the VSC in the middle. The VSC in Case 2 measured the total positive to negative voltage instead of its own voltage.

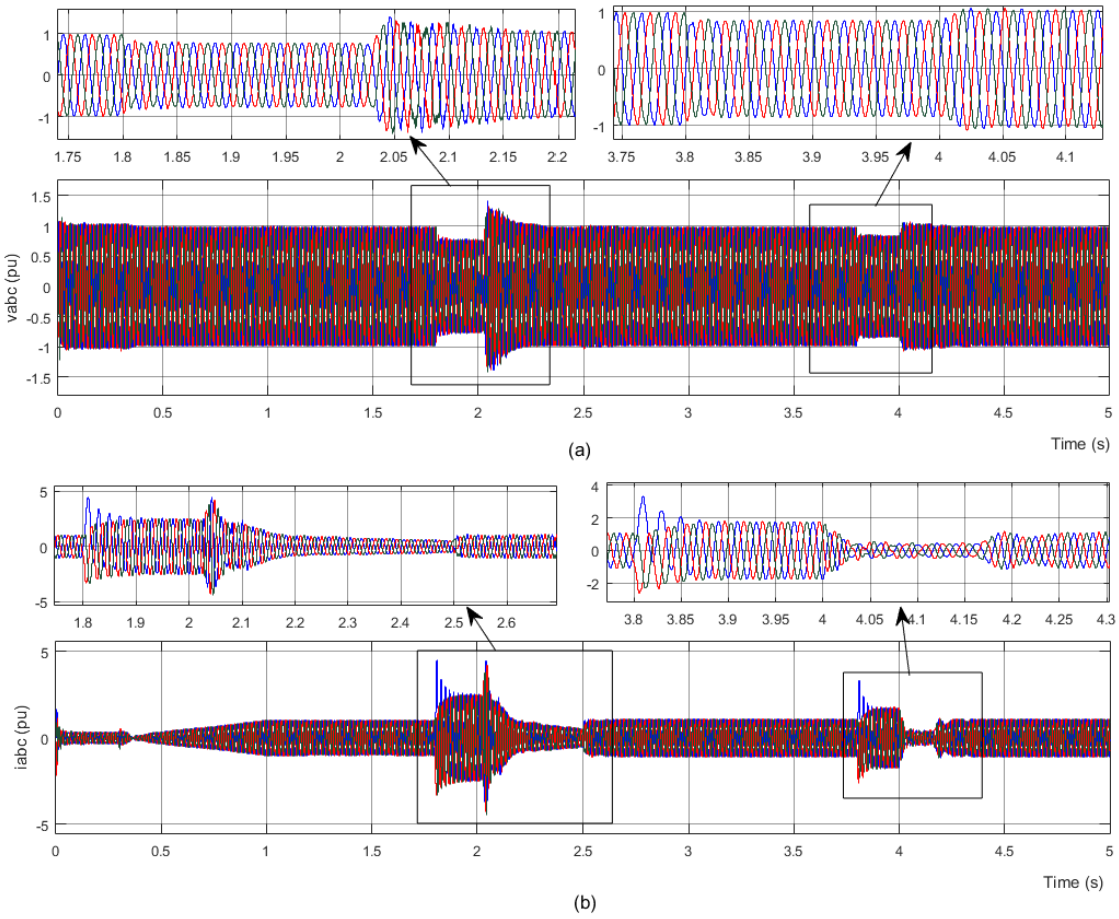
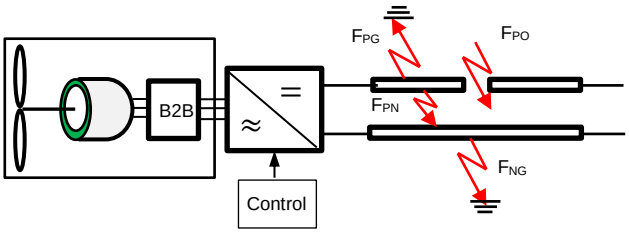


Figure 4-19 Three-phase voltage (a) and current (b) (connections 3, 4)

4.10 DC Cable Open-Circuit Fault

The previous fault analyses consider the fault as a short circuit. However, dc faults can be found as open-circuit faults. Figure 4-20 illustrates four possible types of dc cable faults in the HVDC system. The open conductor fault influences generator-side VSCs only and not GSVSC, although such a fault may affect the ac grid power system due to the generation loss [107]. This energy interruption of the transmission path leads to overvoltage behind the VSC and acceleration of the generator as a result of the redundant power generated by the wind turbine.



F_{PG} Positive-to-ground fault, F_{NG} Negative-to-ground fault, F_{PN} Positive-to-negative fault, F_{PO} Positive open circuit fault

Figure 4-20 DC fault types

The solution may be proposed by connecting a dc chopper or energy storage at the dc cable to limit or absorb the rectified dc overvoltage or by connecting a dumping load at the ac side of the generator. Energy storage systems may be used as well at the converter dc link, although the author [183] has proposed a hybrid of dc chopper and ESS to account for high voltage. The later solution is possible for small-scale power systems such as wind turbines but not for large-scale power systems with power of multi-hundreds of megawatts.

4.11 Summary

The fault analyses studies are presented in the chapter for MTDC networks. The analyses started by finding the dc cable model which necessary when calculating cable characteristics using the traveling wave theory. The model can use approximate equivalent circuit based on lumped impedance or more accurate model based on distributed line parameters. The effect of frequency change on the cable parameters can be determined using frequency dependent parameters. The contributions of fault current from various model components such as the dc capacitor and the adjacent feeder was present.

The simulation was also carried out based on two case studies give the necessary information to compare various connections during the dc fault. The two cases include the connection of diode rectifiers. The simulation results show that connection of the diode rectifiers improve the model performance after the fault in terms of the overcurrent elimination and the time required for the model to return to its study state operation.

5 AC GRID FAULT ANALYSES

5.1 Introduction

Power system fault analysis studies are a required subject to provide information that is necessary to select switchgear, relay settings, and system stability factors. Power systems, in general, are dynamic and change over time during the normal operation due to the act of switching equipment such as generators or transmission lines on or off. Power systems also change during planning, such as when adding transmission lines and generators to the system. Therefore, fault analysis studies need to be performed routinely by utility engineers to account for these changes. The most common causes that lead to occurrence of faults in power systems are flashover, failure of insulations, human errors, or physical damage due to digging or other construction duties. However, these sources of faults may lead to a fault that involves all three phases. These faults may be symmetrical faults (balanced faults), or unsymmetrical faults which involve one or two phases only can occur. Nevertheless, faults can be either line-to-ground short-circuit, short circuit between lines, or may be produced by open line or two lines. Generally, balanced three-phase faults represent only 5% of the initial faults in power systems, with and without earth connection. Single line-to-ground faults constitute 80%, of which double line faults represents 15% of the unbalanced faults. The latter fault can often worsen to a three-phase fault. The remainder of the faults are open conductor faults.

Regardless of the fault type, faults, in general, can be classified into two categories: balanced (symmetrical) or unbalanced (asymmetrical) faults. Symmetrical three-phase faults can be studied by a single-phase equivalent circuit, while unbalanced faults can be solved using symmetrical components, which serve in reducing the calculation complexity. Faults in ac power networks are considered to be a well-developed knowledge [195]. Hence, to achieve full benefits of VSC transmission, several advances of technology are necessary. These necessary requirements come from the ability to operate in severe conditions such as unbalanced grid fault conditions [196].

5.2 Fault-Level Calculations

The fault level in power systems is the maximum current (or MVA) that can pass through the line conductors when zero impedance is connected (during the fault) to the system. Knowing this value is important to determine the switch gear capacity. Generally, MVA (or pu) is used to express the fault level, and nominal rating of voltage is employed to determine the maximum current of the fault, which is expressed as follows:

$$\mathrm{MVA}_{fault} = \sqrt{3} \cdot V_{nom} \cdot I_{sc} \quad \textbf{(5-1)}$$

where MVA_{fault} is fault level (in MVA) at a given point, V_{nom} is nominal voltage in kv, and I_{sc} is line short-circuit current (in kA) passing through the fault. The fault level in pu is given by:

$$fault\ level(pu) = I_{sc\_pu} = \frac{V_{nom\_pu}}{Z_{pu}} = \frac{1}{Z_{pu}} \quad \textbf{(5-2)}$$

The right-hand side is simplified because the pu value of V_{nom} equals 1; Z_{pu} is the per-unit impedance. Also,

$$\mathrm{MVA}_{fault} = fault\ level(pu) \cdot \mathrm{MVA}_{base} = \frac{\mathrm{MVA}_{base}}{Z_{pu}} \quad \textbf{(5-3)}$$

The busbar fault level is a measure of short-circuit ratio of the busbar (SCR). The ability of the busbar to maintain its voltage depends on SCR strength. Therefore, an infinite busbar that has infinite SCR can maintain the voltage across it under any condition, including faults [254, p.596]. More information about SCR is found in section 4.3.

Short-circuit current magnitude is not constant over time (i.e. it is time dependant because of synchronous generators) and is bigger at the beginning of the fault and then starts decaying to the steady value. Therefore, circuit breakers (CB) should have reactors to limit the current when necessary.

MVA level gives a better indication of stress than the current of the fault on CBs to know the recovery voltage and to design the CB to withstand the interruption arc after the fault. Many factors affect the fault current and include the

machines' $emfs$ (electromotive force), the internal impedances of the network machines, line impedances of the system between the machines, and the fault itself.

5.3 Symmetrical Faults

As mentioned before, three-phase faults can be either a short circuit that includes all of the three-system lines or a three-line to ground fault. However, the case where all three lines are open is not included, since in such a case there is no load and the VSCs can operate under no load or in weak networks [1,23]. To analyse balanced three-phase faults, positive-sequence components are needed to be known only. Moreover, the solution needs only a single-line diagram, since currents in all three lines are shifted by $120°$ from each other and equal in amplitude.

- **Simulation Results**

The proposed system model was simulated using MATLAB/Simulink software to assess the model's performance under ac fault condition. Ac faults that occur at the ac grid side can affect the system model correspondingly. For this purpose, a three-phase fault was initiated and simulated at the grid side of the proposed HVDC model. As in the dc fault, the fault timing was kept the same, as shown in Figure 4-14. The first ac fault was implemented in the ac grid side at time $t = 1.8\,s$ for $200\,ms$ when the VSCs were the only switching devices connected to the system, which is Connection 1 (Table 3-5). Connection 2 was implemented at $t = 2.5\,s$ after the connection of the diode rectifiers in the model; in this case, the fault was implemented at time $t = 3.8\,s$ and last for $200\,ms$. The graphs depicted in Figure 5-1 illustrate the performance of the system in the presence of an ac grid-side fault.

Both VSCs of the two windfarms were connected to the system at $t = 0.3\,s$, and the diode rectifiers were connected at $t = 2.5\,s$. Figure 5-1a illustrates a difference between the fault steady state in the two connections. Connection 2 presented a better model performance. After the fault clearance, Connection 2 also showed a better performance in terms of recovery time required for the system to return to its steady-state operating conditions.

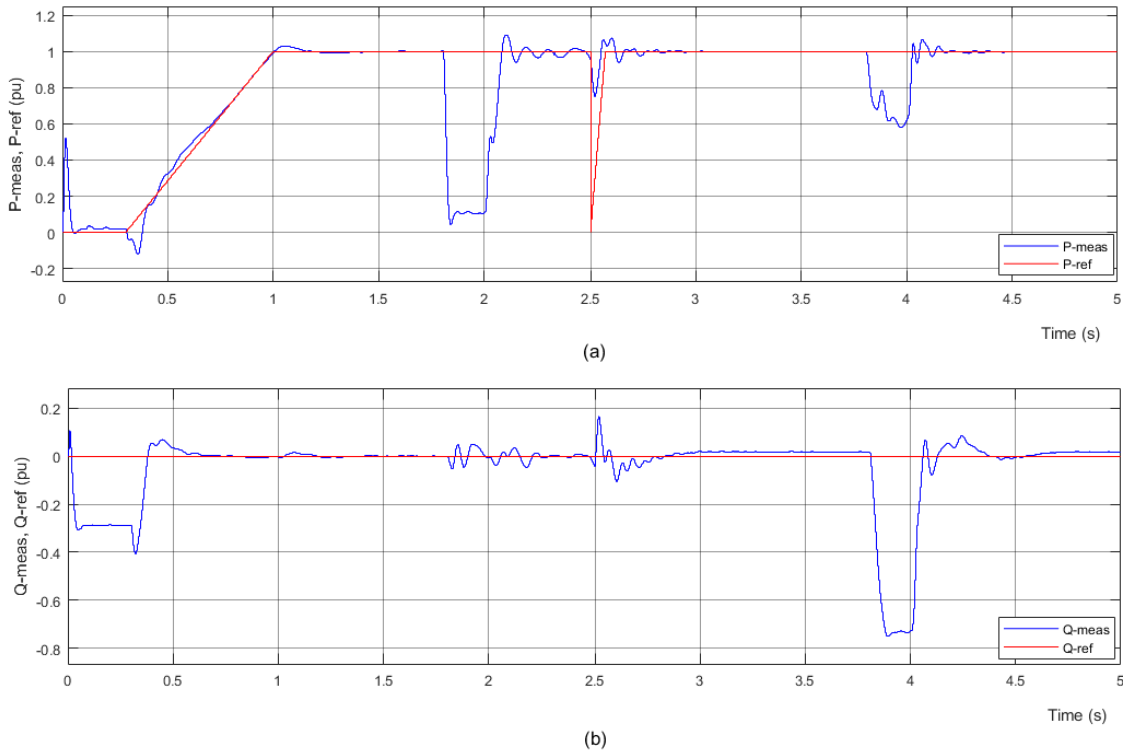


Figure 5-1 Measured (blue) and reference (red) of active and reactive power at PCC in pu: (a) active power and (b) reactive power

The same performance can be inferred from Figure 5-2, which shows the per-unit quantities of ac voltage and ac current at WFVSC1: both voltage and current presented a better waveform shape during Connection 2. The system performance was better in terms of the time required to return to its original state (steady-state operating conditions). Thus, based on the simulation results, an overall improvement in the system performance in Connection 2 (after the connection of passive elements) occurred.

Simulation results reveal that there is no difference for system response under the three-phase short circuit and for the three-phase to ground fault, and both connections yielded exactly the same response and results. This result, in fact, was expected because the short circuit between the lines is enough to cause severe conditions, and the connection to ground will not cause more damage to the system. Therefore, it sufficient to present the three-phase to ground fault.

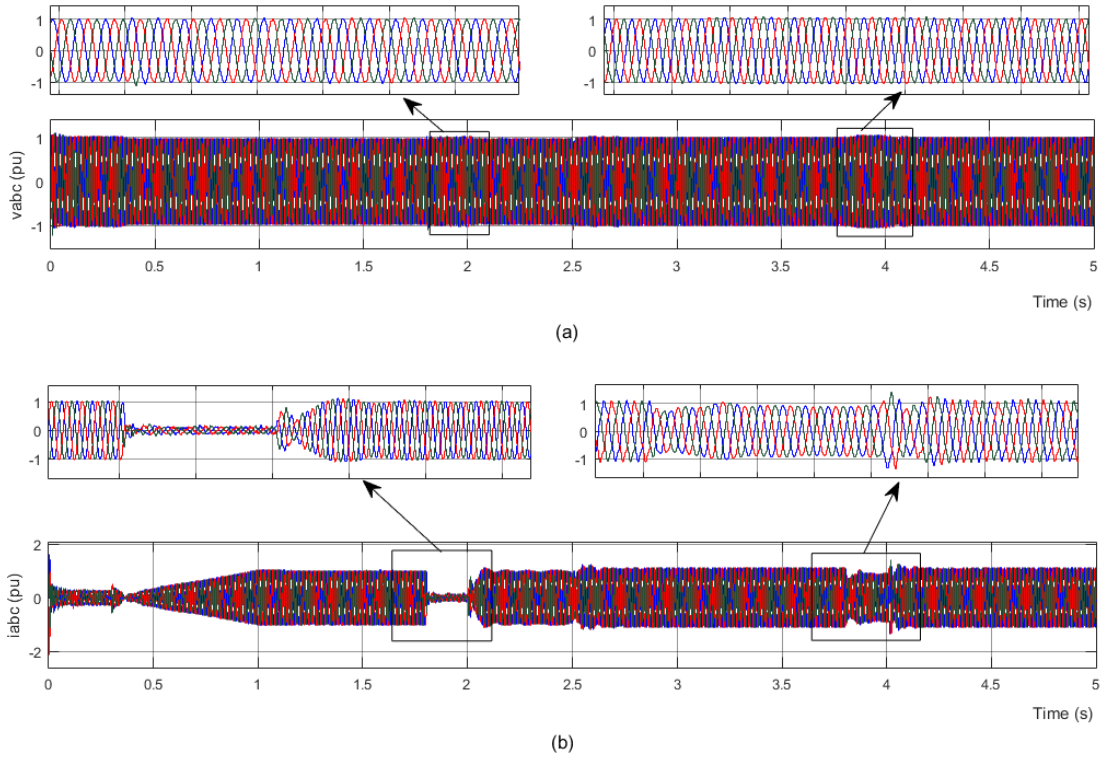


Figure 5-2 Three-phase ac voltage (a) and current (b)

The dc voltage response to the ac fault is shown in Figure 5-3, where the responses under the two connections show different patterns. For the first connection (Connection 1), the voltage increases gradually to approximately $1.2\,pu$ during the fault time ($200\,ms$). In the second case (Connection 2), the voltage had a much steeper increase to approximately $1.7\,pu$ within the first $50\,ms$ after the fault starting point, and then started to decay slightly.

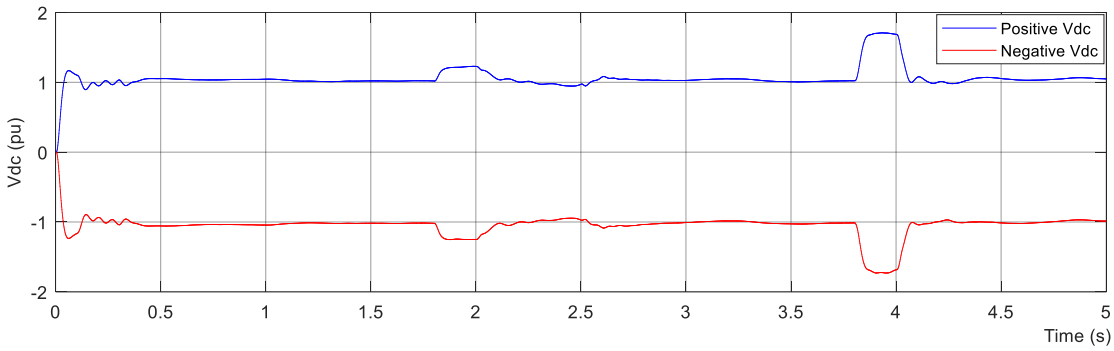


Figure 5-3 Positive and negative dc voltage measured at WF1 dc busbar

During the ac fault, the voltage on the ac side was reduced significantly, which leads to a reduction in converted active power at the GSVSC, and

consequently, the power on the two sides of the converter will be unbalanced. Therefore, the dc voltage will rise to a higher value [255, p.420]. The second connection shows higher peak dc voltage due to the connection of the diode rectifiers which changes the system dynamics.

Figure 5-4 shows the ac voltage and current measured at the grid side. The voltage during the fault presented a similar response in both cases. The voltage dropped to approximately zero in both connections. Furthermore, no noticeable difference was seen between the two cases after the fault clearance in terms of the peak value and the time required to return to the steady state. However, the second case showed a slightly shorter time to return to steady state.

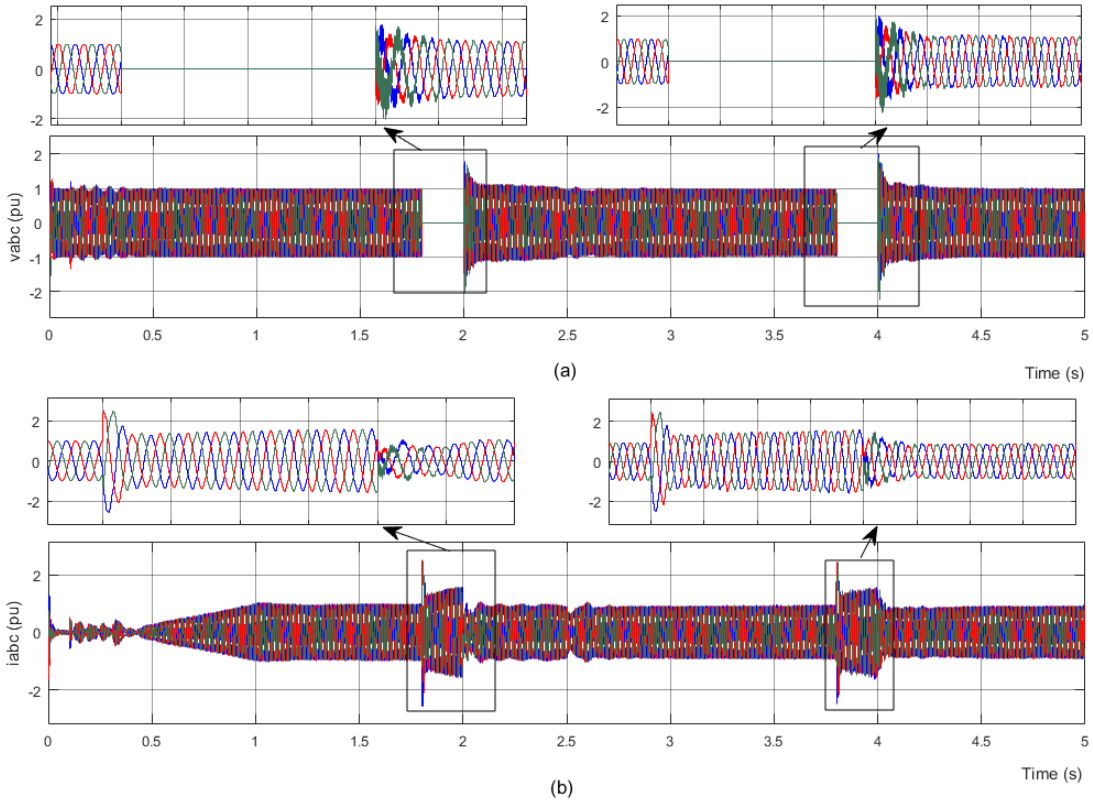


Figure 5-4 Three-phase ac grid-side voltage (a) and current (b)

The current waveform in Figure 5-4b also had the same shape during the fault for both connections. For the first $20\,ms$ (i.e. during one cycle), the current had an overshoot of approximately $2\,pu$, which differs between phases and depends on the phase angle and the instantaneous value of each phase; afterwards,

both have a similar waveform. Then, the fault cleared after $200\,ms$ for both cases and the responses were quite different. In the first case, the current dropped to about $0.6\,pu$ for $0.5\,s$. However, this drop of current was improved in the second case (Connection 2). Generally, the connection of the diode rectifiers to the system improves the overall system performance after the fault clearance.

5.4 Unsymmetrical Faults

Most network faults cause, in general, voltage dips and present symmetrical components in the system as negative-, positive-, and zero-sequence components. Therefore, it is reasonable to include these symmetrical components in the control system of voltage source converters which are connected to the system [197].

PWM control of voltage source converters can be modelled in the SRF (synchronous reference frame) as two separate linear systems. These two systems are the RL system with an outer part of the control loop to control the dc voltage and an inner part of the control loop to regulate the current [160]. The output of the converter has no ripple in the case of balanced and sinusoidal waveform of the input waveform, except for the harmonics that are caused by switching of the valves. However, if the voltage is unbalanced, then low-frequency harmonics exist in both input and output waveforms, which causes a distorted signal output and may affect some sensitive devices such as medical instruments [160].

A dual controller to regulate the current was proposed in 1999 by H. S. Song & K. Nam [94] to account for ripple components that appear in the voltage of the dc link in an unbalanced voltage source. In their system, a separate control of negative and positive sequence components was employed to manage unbalanced voltage.

The negative and positive sequence [198] can be separated using two main methodologies [199]. The first method is implemented by considering the fact that the negative sequence component of the current appears as a double

frequency wave (2ω) in the positive sequence synchronous reference frame, which should be controlled and eliminated by the controller. In other words, i_{dq}^{p} is dc while i_{dq}^{n} is ac with 2ω in the positive synchronous frame, while in the negative synchronous frame the situation is reversed (i.e. i_{dq}^{n} is dc and i_{dq}^{p} is ac with 2ω) [200]. Hence, the separation of positive dq can be performed using a notch filter [98]. The second method to separate the positive and the negative dq component is implemented using delayed signal cancellation (DSC) [201,202].

5.4.1 Positive and Negative dq Separation

5.4.1.1 Separation Using Filter

To implement the controller, each of i_{dq}^{n} and i_{dq}^{p} must be dealt with separately. However, as mentioned earlier, i_{dq}^{n} appears as dc and i_{dq}^{p} appears as ac in the positive synchronous frame. Using this fact, i_{dq}^{p} can be separated using a notch filter. The measured current can be represented by the following [200]:

$$\begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \end{bmatrix} = i_o^p \begin{bmatrix} \cos(\omega t) \\ \cos(wt - \frac{2\pi}{3}) \\ \cos(\omega t - \frac{4\pi}{3}) \end{bmatrix} + i_o^n \begin{bmatrix} \cos(\omega t) \\ \cos(wt - \frac{4\pi}{3}) \\ \cos(\omega t - \frac{2\pi}{3}) \end{bmatrix} \quad \textbf{(5-4)}$$

where i_o^n and i_o^p represent the magnitude of negative and positive sequences, respectively. Hence, a positive reference frame can be written as follows:

$$\frac{2}{3}\begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \end{bmatrix} = i_o^p \begin{bmatrix} 1 \\ 0 \end{bmatrix} + i_o^n \begin{bmatrix} \cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix} \quad \textbf{(5-5)}$$

and for the negative reference frame:

$$\frac{2}{3}\begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \end{bmatrix} = i_o^n \begin{bmatrix} 1 \\ 0 \end{bmatrix} + i_o^p \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} \quad \textbf{(5-6)}$$

Equations (5-5) show that in the positive reference frame, the positive sequence is a dc signal, while negative components appear as ac with frequency equal to 2ω. For the negative synchronous reference frame, the situation is reversed (5-6). Therefore, the ac components can be removed from the reference frame using a notch filter (NF) to separate the positive and negative. The block diagram for NF is shown in Figure 5-5a.

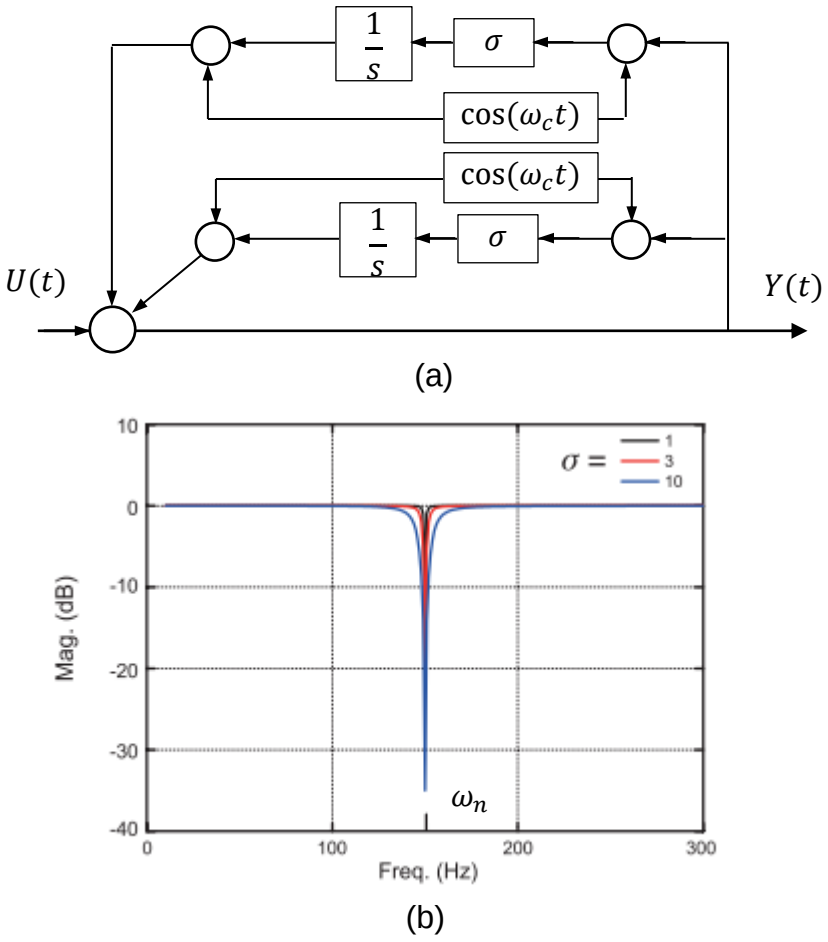


Figure 5-5 Notch filter (a) block diagram and (b) frequency response

The transfer function of this filter is defined as follows [256]:

$$[NF] \equiv \frac{Y(s)}{U(s)} = \frac{S^2 + \omega_n^2}{S^2 + \sigma s + \omega_n^2} \quad \textbf{(5-7)}$$

The sharpness of the notch filter is determined by σ, which is the inverse of the Q-factor, as illustrated in Figure 5-5b, and the centre frequency is determined by ω_n.

However, filters other than notch filter can be used, such as moving average filter (MAF) or low-pass filter. When using the MAF, the output signal is slightly smoother than for the LPF. As the name infers, the MAF works by averaging multiple points of the signal in the input to yield the output signal points. Mathematically, this is written:

$$y[i] = \frac{1}{M}\sum_{j=0}^{M-1} x[i+j] \tag{5-8}$$

The MATLAB/Simulink implementation of this filter is shown in Figure 5-6

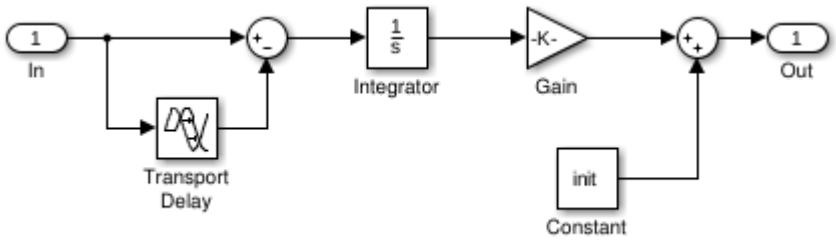


Figure 5-6 Implementation of moving average filter in Simulink

5.4.1.2 Delayed Signal Cancelation

This method can be utilised to obtain a separate positive and negative voltage (v_{dq}^{p}, v_{dq}^{n}) or current (i_{dq}^{p}, i_{dq}^{n}) in the SRF (synchronous reference frame). For purposes of the analysis, although the variables of the three-phase system are unbalanced, the system is assumed to be sinusoidal and equal to the orthogonal summation of the negative and positive sequences [98]:

$$x_a = x_a^p + x_a^n = x^p \cos\left(\omega t + \theta_x^p\right) + x^n \cos(\omega t + \theta_x^n)$$

$$x_b = x_b^p + x_b^n = x^p \cos\left(\omega t + \theta_x^p - \frac{2\pi}{3}\right) + x^n \cos\left(\omega t + \theta_x^n - \frac{4\pi}{3}\right) \tag{5-9}$$

$$x_c = x_c^p + x_c^n = x^p \cos\left(\omega t + \theta_x^p - \frac{4\pi}{3}\right) + x^n \cos\left(\omega t + \theta_x^n - \frac{2\pi}{3}\right)$$

where x represents the supply voltage, current, or input voltage of the converter; $x_a^n,\ x_b^n,\ x_c^n$ and $x_a^p, x_b^p,\ x_c^p$ are the three-phase negative and positive sequence components, respectively; $x_a, x_b,$ and x_c are three-phase system variables; x^p, x^n are the peak values of positive and negative sequence, respectively; ω represents the power supply angular rotation frequency; and θ_x^n and θ_x^p are phase angles. Generally, any balanced three-phase voltage can be transformed into a balanced, stationary two orthogonal voltage using the Clarke transformation, $\alpha\beta$. However, the unsymmetrical yet sinusoidal system (low harmonic distortion system) can be described as follows [202,257]:

$$e_{\alpha\beta}(t) = e_{\alpha\beta}^p(t) + e_{\alpha\beta}^n(t) = E^p e^{(j\omega t+\theta^p)} + E^n e^{-(j\omega t+\theta^n)} \quad \textbf{(5-10)}$$

where E^p, E^n are the peak values of the positive and negative sequence, respectively. Then, the DSC method to separate the negative and positive sequence components in the $\alpha\beta$ domain is

$$e_{\alpha\beta}^p(t) = \frac{1}{2}\left[e_{\alpha\beta}(t) + je_{\alpha\beta}\left(t - \frac{\tau}{4}\right)\right] \quad \textbf{(5-11)}$$

$$e_{\alpha\beta}^n(t) = \frac{1}{2}\left[e_{\alpha\beta}(t) - je_{\alpha\beta}\left(t - \frac{T\tau}{4}\right)\right] \quad \textbf{(5-12)}$$

where τ represents the grid voltage time period. These equations can be implemented as illustrated in Figure 5-7 [257]. Substitution of (5-10) into (5-11) and (5-12) yields

$$e_{\alpha\beta}^p(t) = E_p e^{j(\omega t+\theta_p)} \quad \textbf{(5-13)}$$

$$e_{\alpha\beta}^n(t) = E_p e^{-j(\omega t+\theta_n)} \quad \textbf{(5-14)}$$

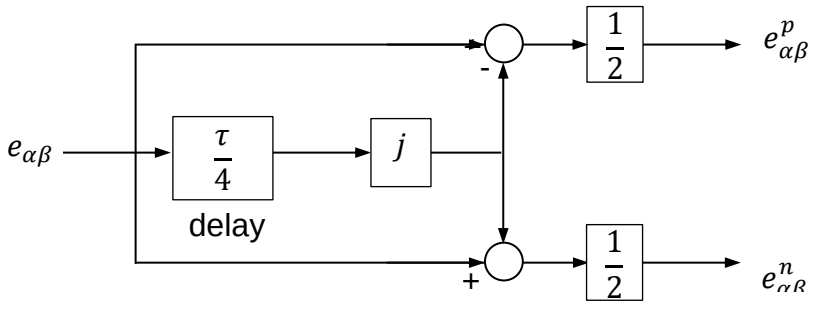


Figure 5-7 Implementation of DSC

The outputs of both positive dq and negative dq before and after applying the filter are shown in Figure 5-8. However, simulation results revealed that any low-pass filter could be used.

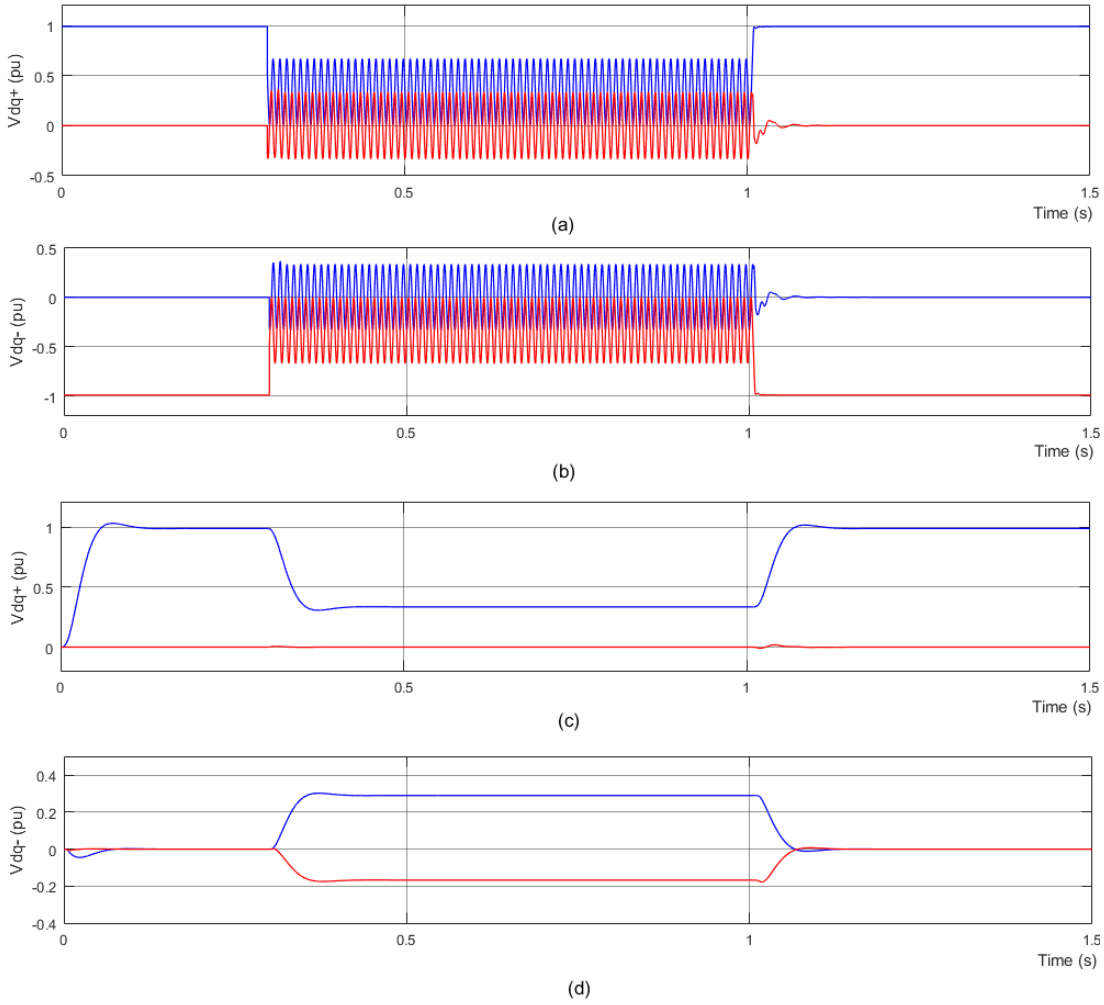


Figure 5-8 $Dq^{\pm}$ component of voltage (a, b) before applying filter and (c, d) after applying filter (blue for positive and red for negative components)

5.4.2 Unbalanced Source of Voltage

The converter ripples of active power correspond to the dc busbar voltage ripples. Then, the apparent power calculation shows this effect. The apparent power of the converter under an unbalanced source of voltage is expressed using positive- and negative-sequence components:

$$S = \frac{3}{2}\left(e^{j\omega t}e_{dq}^{p} + e^{-j\omega t}e_{dq}^{n}\right)\left(e^{j\omega t}i_{dq}^{p} + e^{-j\omega t}i_{dq}^{n}\right)^{*} \quad \textbf{(5-15)}$$

Where the superscript "$*$" refers to the complex conjugate; p, n denotes the positive- and negative-sequence, respectively; and S signifies the apparent power (VA). The active and reactive dc power components (P_o and Q_o) and double-frequency sine and cosine components can be used to find the instantaneous active and reactive power ($p(t)$, $q(t)$) using (5-15) as follows:

$$p(t) = P_o + P_{c2}\cos(2\omega t) + P_{s2}\sin(2\omega t) \quad \textbf{(5-16)}$$

$$q(t) = Q_o + Q_{c2}\,cos(2\omega t) + Q_{s2}\,sin(2\omega t) \quad \textbf{(5-17)}$$

In the above equation, the terms P_o, P_{c2}, P_{s2}, Q_o, Q_{c2}, and Q_{s2} are defined as follows:

$$P_o = \frac{3}{2}\left(e_d^p\, i_d^p + e_q^p\, i_q^p + e_d^n\, i_d^n + e_q^n\, i_q^n\right)$$

$$P_{c2} = \frac{3}{2}\left(e_d^p\, i_d^n + e_q^p\, i_q^n + e_d^n\, i_d^p + e_q^n\, i_q^p\right)$$

$$P_{s2} = \frac{3}{2}\left(e_d^p\, i_q^n - e_q^p\, i_d^n - e_d^n\, i_q^p + e_q^n\, i_d^p\right)$$

$$Q_o = \frac{3}{2}\left(-e_d^p\, i_q^p + e_q^p\, i_d^p - e_d^n\, i_q^n + e_q^n\, i_d^n\right)$$

$$Q_{c2} = \frac{3}{2}\left(-e_d^p\, i_q^n + e_q^p\, i_d^n - e_d^n\, i_q^p + e_q^n\, i_d^p\right)$$

$$Q_{s2} = \frac{3}{2}\left(e_d^p\, i_d^n + e_q^p\, i_q^n - e_d^n\, i_d^p - e_q^n\, i_q^p\right)$$

The active power controls the dc voltage. From (5-16), for unbalanced operational conditions, the voltage source produces double-frequency active power components which lead to the dc link voltage ripples. Therefore, both the cosine component P_{c2} and the sine component P_{s2} should be eliminated by controlling them to zero to remove the ripples of the dc link voltage.

Conversely, the unity power factor is produced by controlling Q_o. The double-frequency component (the cosine component Q_{c2} and the sine component Q_{s2}) have no effect on the power factor because their average values equal zero.

From (5-16) and (5-17), the reference current components (both positive- and negative-sequence) can be found as:

$$\begin{bmatrix} i_d^{p*} \\ i_q^{p*} \\ i_d^{n*} \\ i_q^{n*} \end{bmatrix} = \frac{2}{3D} V_{dc}^* I_{dc}^* \begin{bmatrix} e_d^p \\ e_q^p \\ -e_d^n \\ -e_q^n \end{bmatrix} \quad \textbf{(5-18)}$$

where $D = (e_d^p)^2 + (e_q^p)^2 - (e_d^n)^2 - (e_q^n)^2 \neq 0$

and V_{dc}^* represents the reference voltage of the dc link, and I_{dc}^* is the output of the dc link voltage controller. Equation (5-18) is the basis to control both positive and negative sequences separately, as shown in Figure 5-10 [160].

5.4.3 GSVSC Control Algorithm under Unsymmetrical Faults

This control pattern was designed with the idea of making the grid-side VSC (GSVSC) control the dc link voltage (V_{dc}), and the GSVSC keep the voltage at a predetermined fixed value in steady-state conditions. A cascaded control scheme, which is used to regulate the converter contains inner and outer control loops for current control and dc-link voltage control, respectively [160]. For instance, [103] used a dual control strategy to regulate the negative and positive dq currents in the SRF in the inner control loop and the outer control loop to regulate the dc voltage in [94]. However, there was no control on the reactive power. Therefore, in this thesis, a reactive power control was proposed alongside the dc voltage in the outer control. Thus, the outer controllers control both dc voltage and reactive power in the grid-side VSC. This control scheme may be considered as a generalised control scheme, which can be used for both balanced and unbalanced conditions.

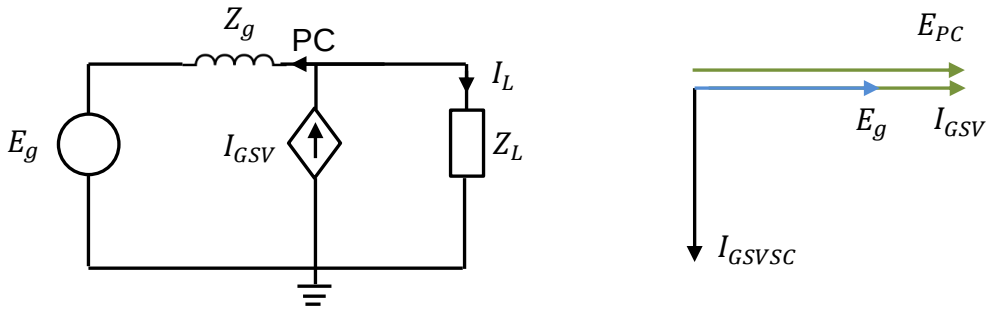
The GSVSC can be used to supply to the grid with the required reactive power during grid-side faults. In this case, the GSVSC is used as a static compensator (STATCOM) to comply with the grid code requirements. Thus, GSVSC is used as a controlled current source, or more specifically, voltage-controlled current source [258].

Figure 5-9a illustrates one phase of the GSVSC equivalent circuit, and Figure 5-9b illustrates the GSVSC vector diagram functioning as STATCOM. Grid

impedance Z_g is considered as a pure inductive load impedance Z_L to be infinity ($Z_L = \infty$). The relationship between E_g and PCC (point of common coupling) voltage and I_{GSVSC} is

$$V_{PCC} = E_g + Z_g . I_{GSVSC} \quad \textbf{(5-19)}$$

where I_{GSVSC} refers to the current of the GSVC, and the maximum allowable current is governed by the GSVSC capacity. In full-scale converters, the GSVSCs are able to supply reactive current equal to $1\,pu$ or less. By supplying the grid with a certain amount of the rated current, the grid behaviour is changed; for example, if the supplied current is limited to $0.5\,pu$, the system will behave exactly like one with no compensation [259]. However, suppling a current of $1\,pu$ allows the grid voltage to recover within $600\,ms$ after the clearance of a fault [259].



(a) (b)

Figure 5-9 GSVSC operation: (a) Equivalent circuit and (b) Vector diagram of GSVSC operation

If an unbalanced voltage dip occurs in the grid, both sequence components (the positive and negative) are used in the GSVSC. The block diagram of the GSVSC control system is illustrated in Figure 5-10. In steady-state conditions, the positive sequence reference current and the negative sequence reference current of the GSVSC controllers are determined by the output voltage of the dc link and the reactive power controllers. In the case of a grid fault, dc link voltage control of the GSVSC is not used in the control; hence, the GSVSCs supply reactive current. Therefore, the positive sequence component of the active current reference (I_q^{p*}) equals zero, or:

$$I_q^{p*} = 0 \tag{5-20}$$

The control scheme could follow any grid code to supply reactive current, which is required to stabilise the voltage. However, the control system in this work uses the E.ON grid code, as depicted in Figure 2-17 and Figure 2-18. In addition, the level of voltage drop determines the reference value of the reactive current as follows:

$$\begin{cases} I_d^{p*} = 0.9\,pu & \text{if } 0 \le E_q^p \le 0.5\,pu \\ I_d^{p*} = 2.186 - 2.57.E_q^p & \text{if } 0.5 < E_q^p \le 0.85\,pu \\ I_d^{p*} = 0 & \text{if } E_q^p > 0.5\,pu \end{cases} \tag{5-21}$$

where I_d^{p*} is the per-unit value of the direct axis ($d-axis$) reference current of the positive sequence component, and E_q^p is the per-unit value of the quadrature ($q-axis$) of the positive sequence component of the grid voltage.

Moreover, both the $d-axis$ and $q-axis$ of the negative sequence component reference currents equal zero. Hence, the unbalanced components of the current that is supplied to the grid can eliminate any unbalanced component of the current that passes to the network. Thus:

$$\begin{aligned} I_d^{n*} &= 0 \\ I_q^{n*} &= 0 \end{aligned} \tag{5-22}$$

Typically, a PI (proportional integral) controller was used to regulate the voltage of the dc link to eliminate the error signal (ΔV) between the reference voltage and the measured voltage of the dc link. The value for ΔV has to be considered for the transition to be fast after the clearance of fault and the voltage regulator of the dc link. Therefore, the initial error signal, ΔV_{dc_init}, will equal zero:

$$\Delta V_{dc\_init} = 0 \tag{5-23}$$

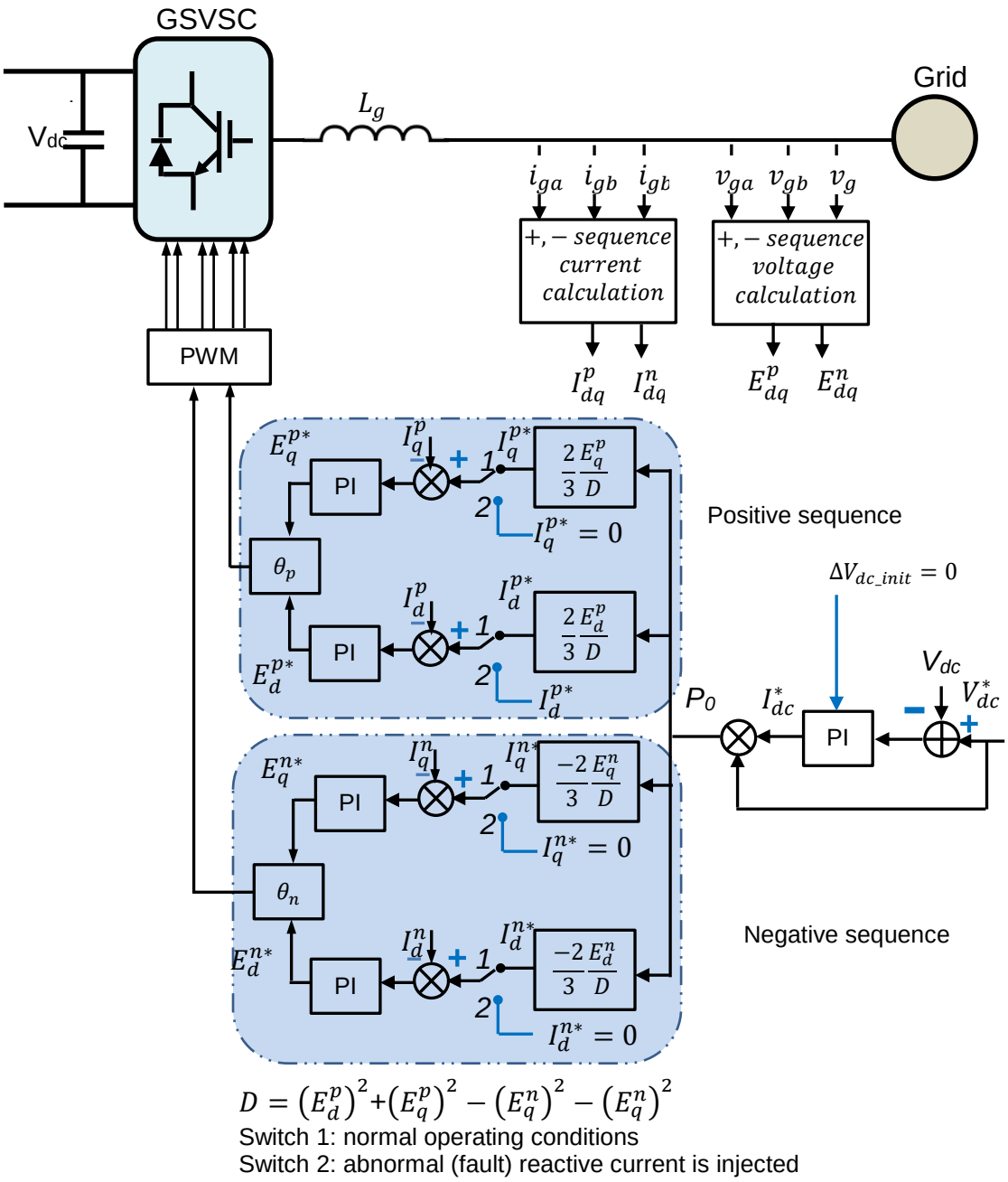


Figure 5-10 GSVSC control system diagram under unbalanced conditions

5.4.4 Generalised Control Scheme

The previous control strategy presented in Section 5.4.3 was proposed with idea that it control the dc voltage at the dc link. However, no reactive power control is found within the control scheme. This was achieved by using additional components such as adding energy storage, dc chopper, and improvement to the control strategy. However, this is valid for small power

systems such as single wind turbine, for a windfarm with several hundred megawatts, energy storage devices are not feasible.

Then in this thesis, a Generalised Control Scheme (GCS) was proposed to achieve the defects of previous control strategy. The GCS strategy may be considered as a generalised solution because it benefits from the sequence separation and adding a reactive power control to the outer loops as shown in Figure 5-11.

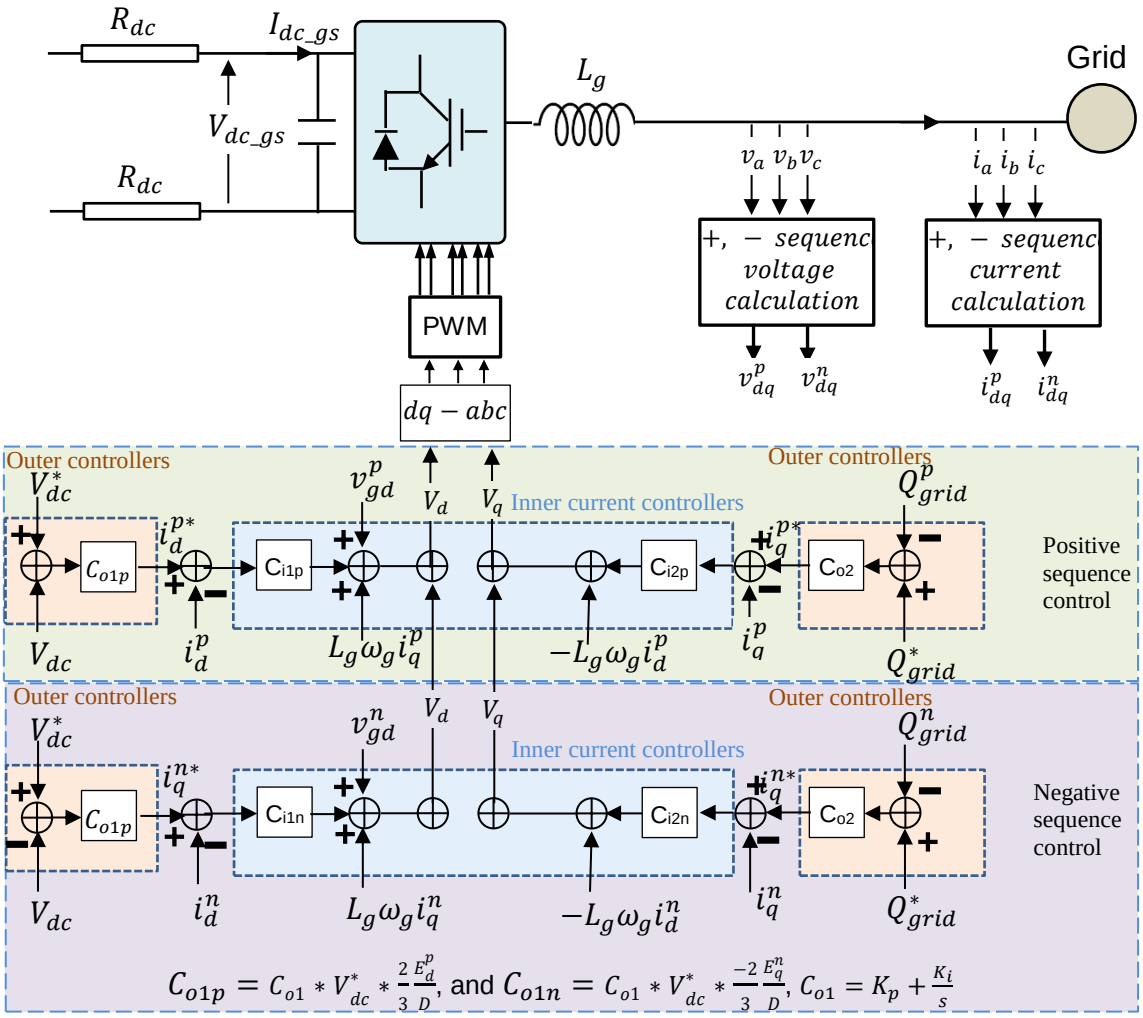


Figure 5-11 Generalised GSVSC control

The GCS system combines the control systems in Figure 5-11 and Figure 3-9. Hence, the analyses of section 3.4 and section 5.4.2 are still valid and can be applied to design the inner and outer current control loops.

The concept behind the GCS is that the reactive power is added to the outer loop, which is calculated by the instantaneous reactive power value. Then, from (5-17) the following formula is used to calculate the instantaneous reactive power:

$$q(t) = \frac{3}{2}\big[\big(-e_d^p\, i_q^p + e_q^p\, i_d^p - e_d^n\, i_q^n + e_q^n\, i_d^n\big) + \big(-e_d^p\, i_q^n + e_q^p\, i_d^n - e_d^n\, i_q^p + e_q^n\, i_d^p\big)\cos(2\omega t) + \big(e_d^p\, i_d^n + e_q^p\, i_q^n - e_d^n\, i_d^p - e_q^n\, i_q^p\big)\sin(2\omega t)\big] \quad \textbf{(5-24)}$$

Under an ideal grid condition (balanced steady-state condition), the negative sequence voltage and current are zero, as shown in Figure 5-8. Then, the terms $-e_d^n\, i_q^n + e_q^n\, i_d^n = 0$ and the second and the third terms in (5-24) equal zero. Thus, equation (5-24) is reduced to equation (3-34) on page 87:

$$Q = \frac{3}{2}\big(e_q i_d - e_d i_q\big) \quad \textbf{(5-25)}$$

Therefore, the control system in Figure 5-11 will work exactly as the one presented for the balanced conditions in Figure 3-9 in section 3.3.6.

5.4.5 Simulation Results

The proposed model was validated using the control model in Figure 5-11 under a single line-to-ground fault at the grid side. Figure 5-12 illustrates both the active power (P) and reactive power (Q) in the case when a single line-to-ground fault occurs at the grid-side converter. The blue lines represent the measured values, and the red lines are the reference values. Two faults were introduced in two different operating modes. The first fault occurred at $1.8\,s$ (Connection 3; refer to Table 4-2 on page 142), and the second fault was at $3.8\,s$ (Connection 4). Both faults lasted for $200\,ms$. Note that the protection system was not included in the model during this simulation.

Figure 5-12a depicts the active power based on the GCS. The active power first decreased to approximately $0.03\,pu$. Then, it increased to $0.15\,pu$. The important note is that the active power did not fall to zero due to the fault. After

the fault clearance, the active power increased to $1.35\,pu$. Then it dropped to $0.2\,pu$ and returned to the steady-state value of $1\,pu$ within approximately $0.5\,s$.

During the second fault, the model's performance was slightly better than it was for the first fault. This means that the connection of diode rectifiers improves the model's performance. The active power decreased to $0.05\,pu$ instead of $0.03\,pu$. Then, it increased to approximately $0.85\,pu$ instead of $0.15\,pu$. After the fault clearance, the active power fluctuated between $0.95\,pu$ and $1.05\,pu$ for approximately $0.5\,s$, which is better than the performance of the first fault. The fault conditions in the second case (Connection 4) can be considered an improvement of the performance in terms of the overshoot for the active power after the fault clearance.

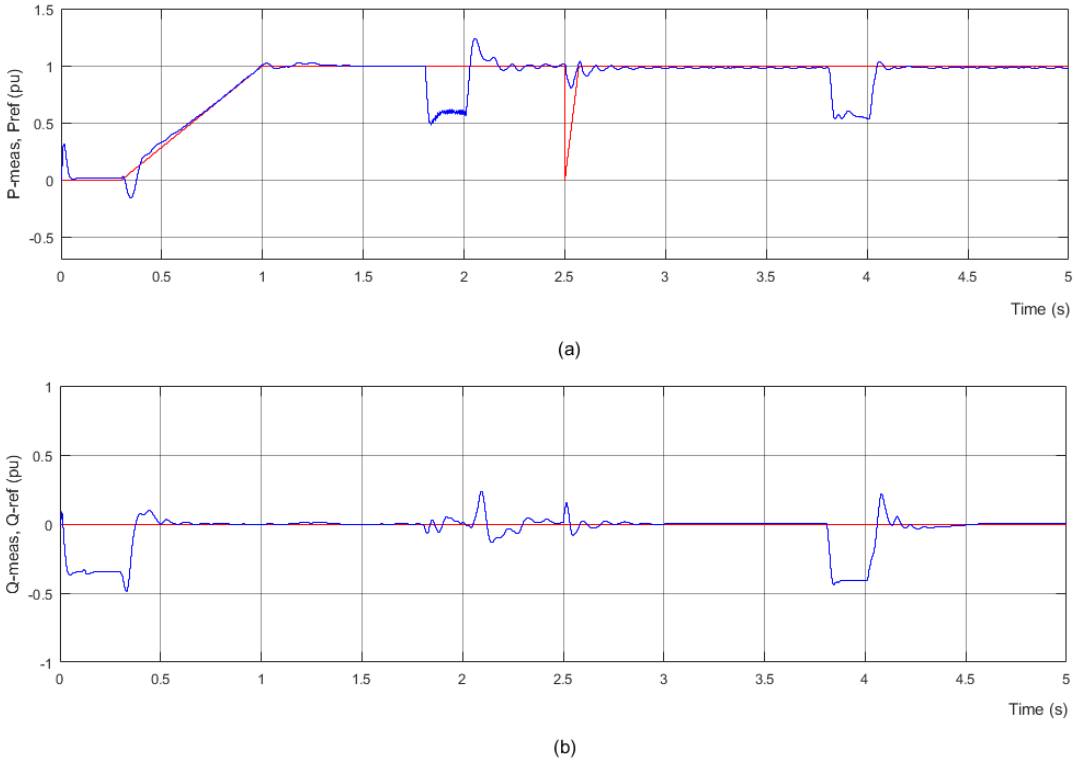


Figure 5-12 Active power (a) and reactive power (b) at PCC (unsymmetrical)

However, as shown in Figure 5-12b, the performance of the model for the reactive power was slightly different: the model's performance was better without the connection of the diode rectifiers. The reactive power performance means that a phase shift occurred between the ac voltage and current. The

phase shift angle came from the fact that the passive rectifier does not control the active power.

For the picture to be complete, the three-phase voltage and current need to be illustrated: they are presented in Figure 5-13. The ac voltage had unnoticeable fluctuation of about 10% due to the first fault, and fluctuations were less in the second fault.

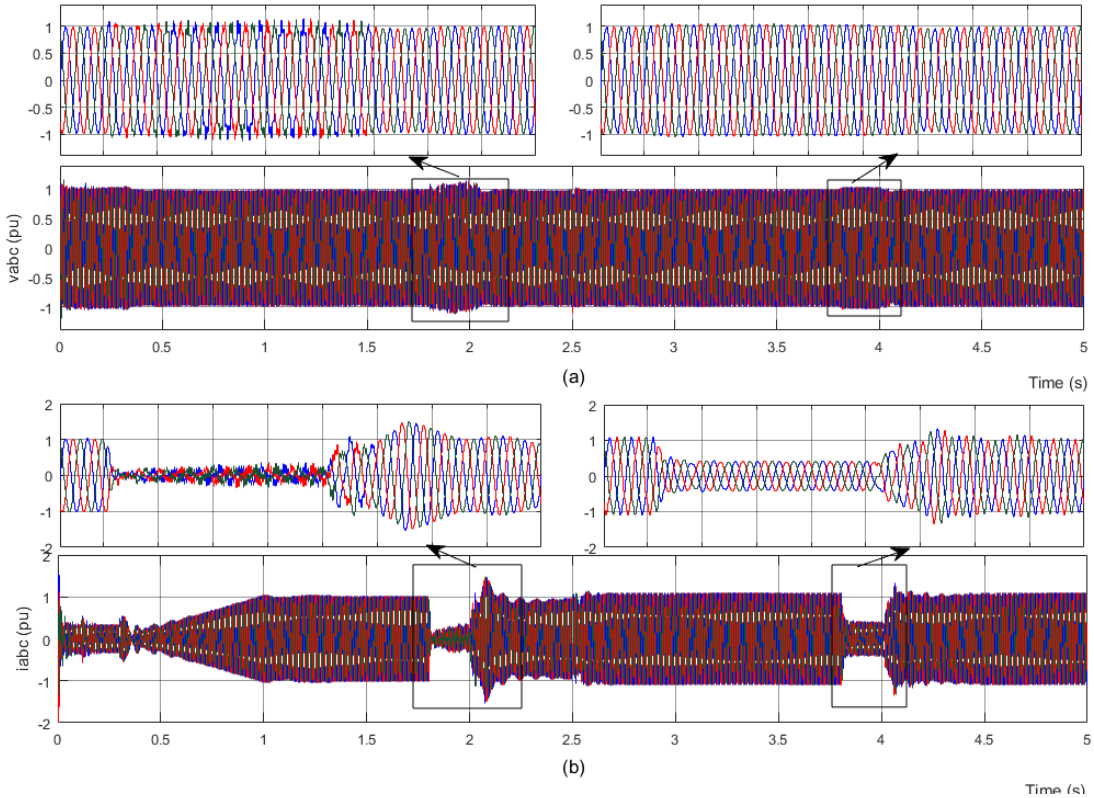


Figure 5-13 Three-phase ac voltage (a) and current (b) at PCC (unbalanced)

The current waveform, shown Figure 5-13b, fluctuated in an analogous way for active power. The distortion in this case was higher than that for the ac voltage during the fault and after the fault clearance. However, no overcurrent occurred during the fault or after fault, as in the case of a dc fault.

The grid-side active and reactive power at the grid-side converter during the unbalanced fault are shown in Figure 5-14. The active power began at time $t = 0\,s$, with zero. Note that the grid-side converter controls the dc voltage and the reactive power. Therefore, there is no reference power in Figure 5-14a. The

active power was at zero value until $t = 0.1\ s$, which was the time when GSVSC connected to the model. However, both WFVSC1 and WFVSC2 were connected at $t = 0.3\ s$. Therefore, some fluctuations can be seen until the connection of WFVSC1 and WFVSC2 before the power started to ramp.

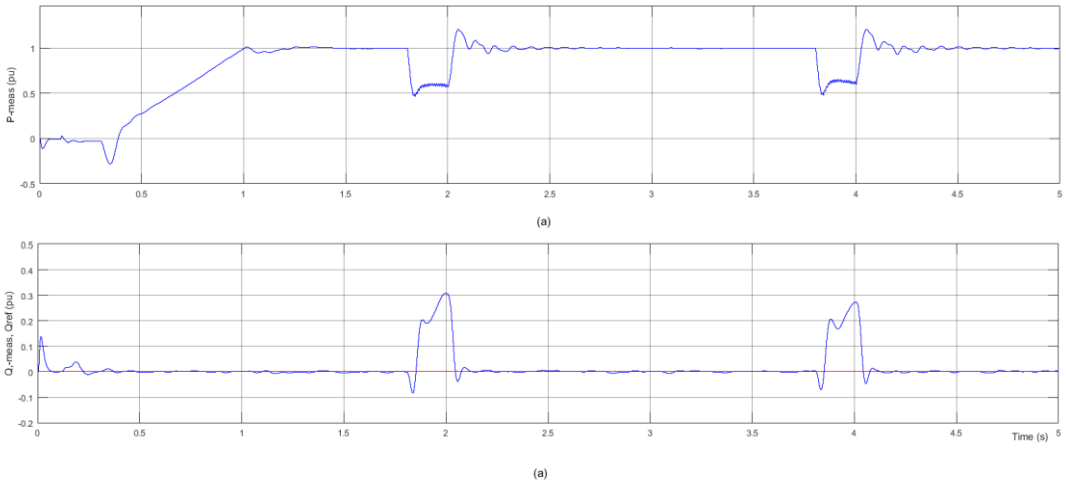


Figure 5-14 Active (a) and reactive (b) power at grid-side converter (unsymmetrical)

The first fault started at $t = 1.8\ s$; the active power dropped to $0.1\ pu$ and the reactive power increased to $0.45\ pu$ within approximately $40\ ms$. Then it increased slightly to $0.6\ pu$ with some ripples. The increase and the decrease were approximately linear with time. After the fault clearance, the active power started to increase to approximately $1.3\ pu$ before it finally settled down at its rated value. The second fault was started at $t = 3.8\ s$; this caused the active power to decrease to $0.48\ pu$ within $30\ ms$. Then the active power gradually increased to $1\ pu$ within approximately $100\ ms$. After the fault, the power increased by about $1.2\ pu$ and experienced fluctuations before settling down at $1\ pu$. Thus, the proposed model improved the performance of the system slightly in terms of fluctuation and the time required to stabilise.

However, from the reactive power point of view, the VSC model with the diode rectifiers performed slightly better than the conventional model. The reactive power was increased to $0.32\ pu$ in the first fault and to about $0.27\ pu$ during the second fault, as shown in Figure 5-14b.

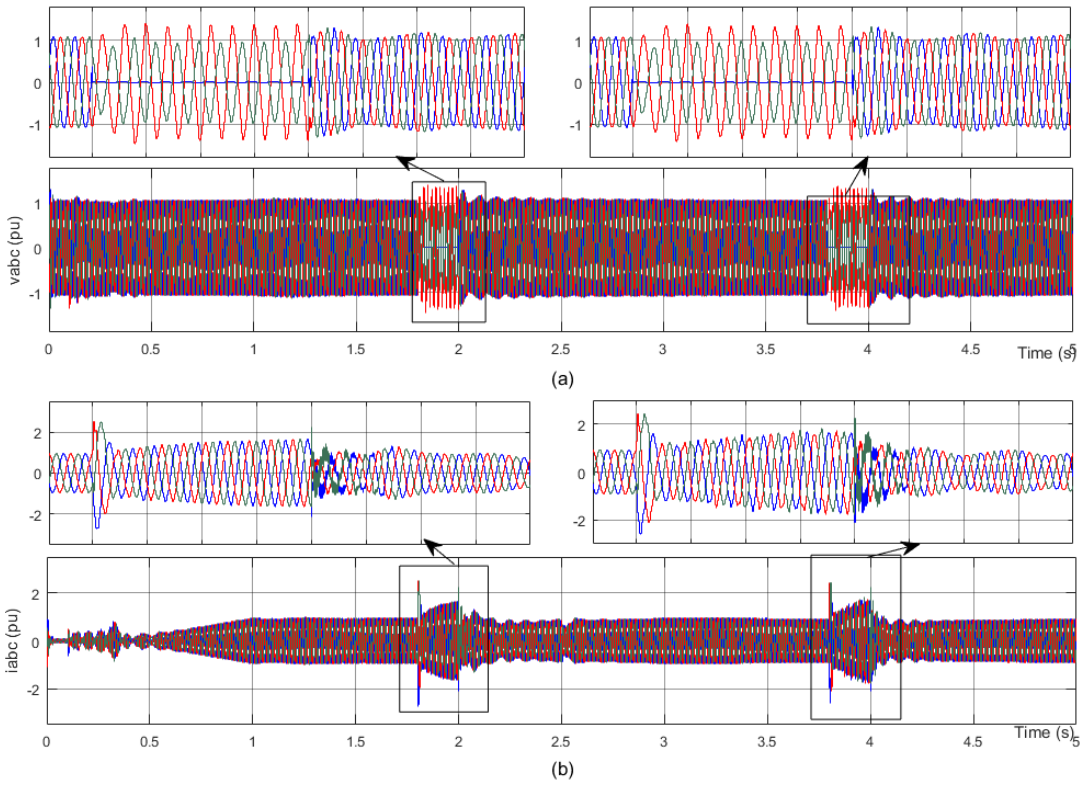


Figure 5-15 Three-phase ac voltage (a) and current (b) at grid side (unsymmetrical)

The ac grid voltage and current are shown in Figure 5-15. Although the grid voltage showed some disturbance before $0.3\ s$ due to the charging currents of reactive elements, after the connection of the VSC converters it reached its rated value of $1\ pu$. During the first fault, the faulty phase voltage became $0\ pu$, while for the other two phases it increased to about $1.5\ pu$ on average between the start and the end of the fault. It returned to the rated value after the fault. The same performance was repeated during the second fault.

Conversely, the ac grid current (Figure 5-15b) showed a different pattern. During the fault, the faulty phase current increased to a substantially high value of about $2.5\ pu$ and $2.45\ pu$ during the first and second faults, respectively. This high current is dangerous to nearby equipment. The fault current is generally characterised by several factors, including the fault resistance, cable impedance, and short-circuit ratio capacity (SCR). In the test, the fault location was chosen to be close to the busbar where the measurement was taken.

Figure 5-16 shows the dc voltage under the unbalanced ac grid fault. The figure shows that the performance of the model without the connection of the diode rectifiers was slightly better than the case after the connection of the diode rectifiers. Generally, the overall performance is required $20\ ms$ to reach the max overvoltage ($1.15\ pu$) in the first case, while required about $60\ ms$ to reach the max voltage at about $1.33\ pu$. The overvoltage in first case did not exceed the grid code, but the second case, it exceeded the grid code limits although it did not require fast protection algorithm.

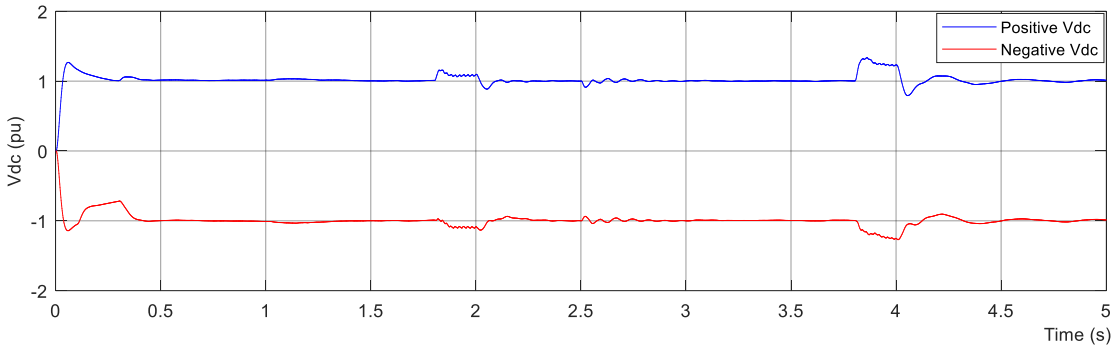


Figure 5-16 Positive and negative dc voltage (unbalanced)

5.5 Summary

This chapter introduced the ac fault in the ac side of the proposed model and its impact on the converter and dc side. The balanced ac fault can be dealt with in a similar way as the conventional method for the steady state. because such a fault still has balanced three-phase voltage and current. However, single line to ground and double line to ground leads to unbalanced between the three phases. Therefore, negative sequence component will be present and affect the dc-link voltage, which should be considered in the control system. Thus, the separation of symmetrical components into positive dq and negative dq using DSC was presented and used in the control system. the dual current control strategy was suggested. Due to the lack of reactive power control GCS was proposed and simulated to account for the presence of negative sequence component and add the reactive power control in the outer loop.

6 FAULT DETECTION AND PROTECTION

6.1 Introduction

In an MTDC system, two types of faults can occur: ac faults and dc faults. Each type has its own characteristics. In any case, the protection against each type of fault should be sensitive, selective, fast, reliable, robust, and seamless, which means the system should be able to isolate the faulty part and run the healthy parts in a secure state. VSC-based HVDCs are vulnerable to dc faults due to large discharge currents from the dc capacitor.

Therefore, it is important to interrupt the fault current before exceeding the limit values of connected equipment. This action requires a fast fault detection algorithm and fast circuit breakers, which can detect and interrupt the current before it exceeds the set value. Typically, fault detection algorithms depend on a communication network that should provide information about the system status from different parts to determine the fault occurrence in a certain part. The fault-detection algorithm should be fast, and the usual time is about $1\,ms$ [90, p.234]. After the fault detection, a trip signal should be sent to the involved circuit breakers. The circuit breakers should respond to the signal within a short time to interrupt the current. However, the circuit breakers of today's technology can trip and isolate the fault within approximately $0.2\,ms$. Table 6-1 summarises the interruption times for different circuit breaker types [260].

In fault analysis studies, the time to the peak current of the fault is important to be identified because this time determines the CB interruption speed. For example, in [260], three categories of faults were identified in the system based on the rise time of fault current and the peak fault current, as shown in Table 6-2.

However, the fault current value and the time to peak depends on several factors including the system capacity, type and location of fault, system topology, and fault impedance. The fault current rise time in dc systems is much higher than in ac systems because the reactance of the line limits the rate of the current rise. Therefore, the protection of HVDC systems against dc faults is

more challenging than against ac faults. Therefore, in dc fault, it is important to interrupt the fault current before it exceeds the current carrying capacity of the breaker and other equipment. Table 6-1 shows maximum interrupting current capacity.

Table 6-1 Interruption times of circuit breakers

Circuit breaker type	Switch time	Max breaking current
Super MRTB[7]	$27-41\ ms$ ($19\ ms$ contact separation and $8-22\ ms$ arching time)	$\approx 4\ kA$
Hybrid CB	$27\ ms$ ($19\ ms$ contact separation and $8\ ms$ arching time)	$\approx 5\ kA$
Hybrid fast switch	$\approx 2\ ms$	$\approx 6\ kA$ [8]
Solid state CB without auxiliary circuit	$\approx 0.2\ ms$	$\approx 6\ kA$

Detecting the fault and determining its location are further challenges because this process should be fast and should ensure the aforementioned requirements, such as sensitivity and selectivity, quickly. Due to the low resistance and negligible reactance, the traditional distance protection which depends on an impedance relay is not effective. Thus, in dc systems, this may depend on signal processing techniques such as wavelets for dc fault detection and location [90].

[7] Metallic return transfer breaker; used for the current commutation from the ground to a metal path when there is a restriction on the allowable dc current time through the ground.
[8] Higher current carrying and current interruption capacities can be achieved that can be found in the literature. For example [111] stated that 16 kA can be achieved.

Table 6-2 Time to peak fault current and peak current

Category	Fault current (amplitude)	Time to peak after fault
Cat I	5 kA	$15\ ms$
Cat II	50 kA	$10\ ms$
Cat III	65 kA	$2\ ms$

In alternative current, the current passes through zero periodically, which is the major difference between ac and dc current. Therefore, dc breakers need to adopt active or passive oscillating structures to produce a current zero-crossing point [204]. The dc breaker interrupts the fault current soon after the zero-point current detection.

A comparison between dc CBs from a cost viewpoint for different voltage levels is presented in [261]. For low and medium voltage grids, the solid-state circuit breakers offer the lowest cost. However, additional on-state losses, which lead to an increase of life-cycle cost, should be considered. Therefore, mechanical CBs with a snubber circuit are the attractive solution. For high voltage, solid-state dc CBs are a more attractive solution [261]. The next section addresses ac fault protection, although the focus of the chapter is on dc analysis.

6.2 AC Side Protection

The protection in an ac system is well developed. Therefore, the main focus of this chapter is the challenging topic of dc faults. However, dc fault protection may be achieved using ac circuit breakers. When a fault occur, all of the ac CBs associated with the MTDC system will trip. Then, each VSC must determine which dc CB to open. The determination process can be accomplished by measuring and comparing the current magnitude and the direction through each breaker. The switch with the largest positive fault current is selected [93].

The ac power is provided to the converter transformer by a short- or medium-length transmission line in offshore windfarm applications. Nonetheless, such transmission lines require a protection scheme. The protection should be high-

speed and protect against ground and phase faults. The protection, in this case, can be some form of a pilot relay [195, pp.936, 937].

The protection zone of the ac bus is between the HV winding of the converter transformer and the current transformer of the breaker source side, which includes the reactive power compensation and the harmonic filters. This zone may be protected by using the current transformer neutral end of the shunt connection. This protection generally uses bus differential relays [195, p.937].

Placing ac CBs on the VSC's ac side to protect the HVDC system is economical. However, ac CBs need a longer time to interrupt the fault current, which is usually two cycles ($40\ ms$ in $50\ Hz$ systems) [93].

6.3 DC Fault Characteristics in VSC-Based HVDC Systems

To design a protection system for a certain MTDC, the fault characteristics should be known as a basic requirement. When a dc short circuit occurs, the fault current is characterised by three stages. The first stage is the dc capacitor stage. The dc capacitor at both ends of the dc cable starts to discharge to the fault soon after the fault occurrence. The second stage is the freewheeling diode stage. This stage starts after the dc capacitor voltage drops to zero. The IGBTs are blocked, leaving the freewheeling diodes to conduct the full current. In this stage, the current decays exponentially from its initial value of I_o. This decay is described by $i_{cable} = I_o e^{-Rt/L}$. The third stage is the grid-side feeding current, which starts after the cable current drops to zero. The equivalent circuits for these stages are presented in Figure 4-10.

6.4 DC Circuit Breakers

In ac transmission systems, circuit breakers have been used for years for applications involving interruption of load or fault current. High-voltage ac circuit breakers generally need about two cycles (i.e. $40\ ms$ at 50 Hz system). The ac CBs typically benefit from the natural zero-crossing point to minimise arcing. However, ac CBs cannot be used to interrupt dc current in HVDC systems because dc has no zero-crossing point. Consequently, this technology needs to

create an artificial zero-crossing point using a resonant circuit which is either a passive or active circuit. Moreover, the rate of fault current rise is high because of the lack of reactance. The high rate of increase requires a short interruption time in the range of $(1-2\,ms)$. Solid-state switches can avoid the need to create the zero-crossing point by quickly interrupting the fault current, but such switches have high on-state resistance, which increase the transmission losses [90]. Research studies on the subject of dc breakers may be categorised into three categories. These categories are traditional circuit breakers, solid-state circuit breakers, and hybrid circuit breakers [204].

6.4.1 Traditional DC Circuit Breakers

This type of circuit breaker, in general, consists of an oscillatory circuit, which is an LC circuit. The LC circuit is required when the dc fault current must be interrupted by generating oscillating current to create a zero-crossing current. The LC oscillating circuit could be an active or a passive circuit, and hence, the dc circuit breakers are classified accordingly, as shown in Figure 6-1. Both types of traditional dc circuit breakers are suitable for low- and medium-range voltage and power applications. However, the tripping speed is much slower than the capacitor discharging speed [204].

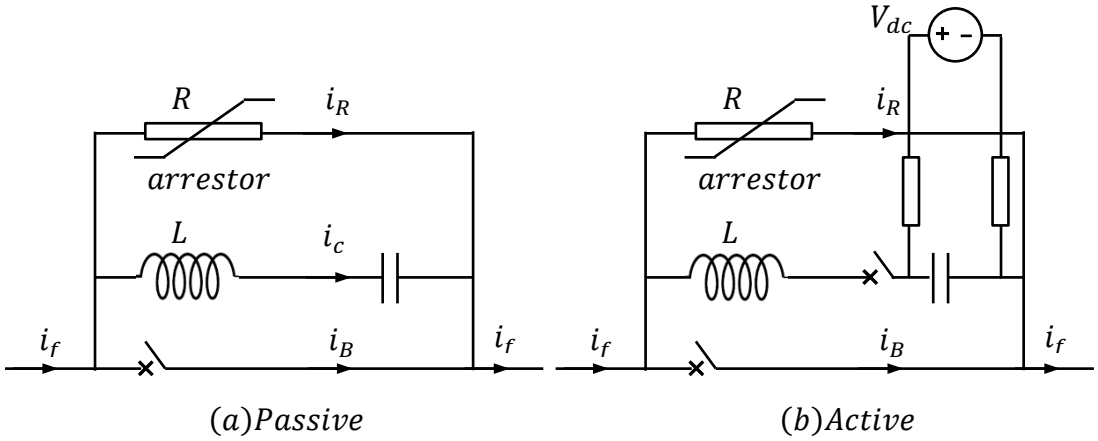


Figure 6-1 Traditional circuit breaker structure (recreated from [204]**)**

6.4.2 Solid-State DC Breakers

To improve the interruption speed of fault current, solid-state dc breakers (SSB) were suggested, which use semiconductor switches such as IGBT or GCT in

the main path of the current flow. These semiconductor switches are used as antiparallel pairs to enable the bidirectional flow of current interruption capability. The switches are also connected in parallel with a surge arrester (or MOV[9], metal oxide varistor), as illustrated in Figure 6-2.

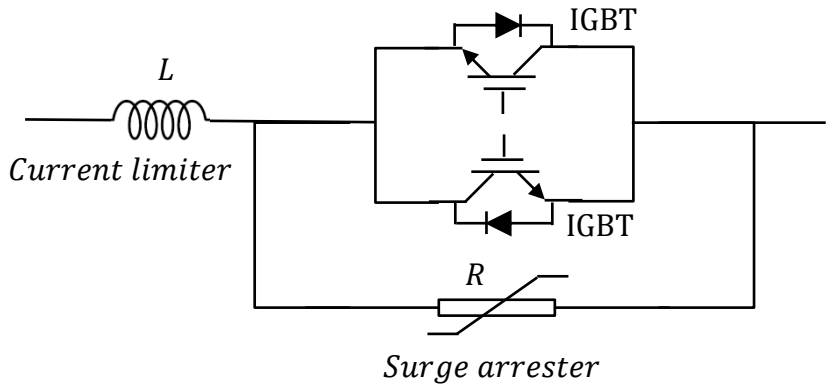


Figure 6-2 Solid-state circuit breaker structure

In such types of dc CBs, the current passes through the semiconductor switches. Therefore, it has high on-state resistance, which leads to high power losses. The high on-state losses under normal operating conditions are the major disadvantage of solid-state breakers which are higher than the other dc breakers significantly. The semiconductor switches are turned off as soon as the trip signal is received after the fault current detection. Switching off the semiconductor switches results in rapid increase of voltage. Consequently, the surge arrester, which is designed to block the voltages that exceed the rated voltage of the dc bus, starts conduction; hence, the line reactance is demagnetised [261].

Solid-state circuit breakers offer the best performance because there are no mechanical parts in them. This leads to an excellent ability for current flow and a significant reduction in turn-off speed [261].

[9] MOV is a resistor with nonlinear characteristics, which consists of ZnO (Zinc Oxide) elements, and is typically used in low- and high-voltage power protection applications.

6.4.3 Hybrid DC Circuit Breaker

The construction of hybrid dc breakers (HCB) combines a mechanical switch breaker (disconnector) and a solid-state breaker. Therefore, in theory, it achieves the advantages and overcomes the disadvantages of both types. Thus, the hybrid dc CB offers reduced on-state power losses of the mechanical switch CB, and the fast interruption speed of the solid-state CB [205]. Few hybrid dc breaker prototypes are available [262]. A design by ABB is illustrated in Figure 6-3 [263].

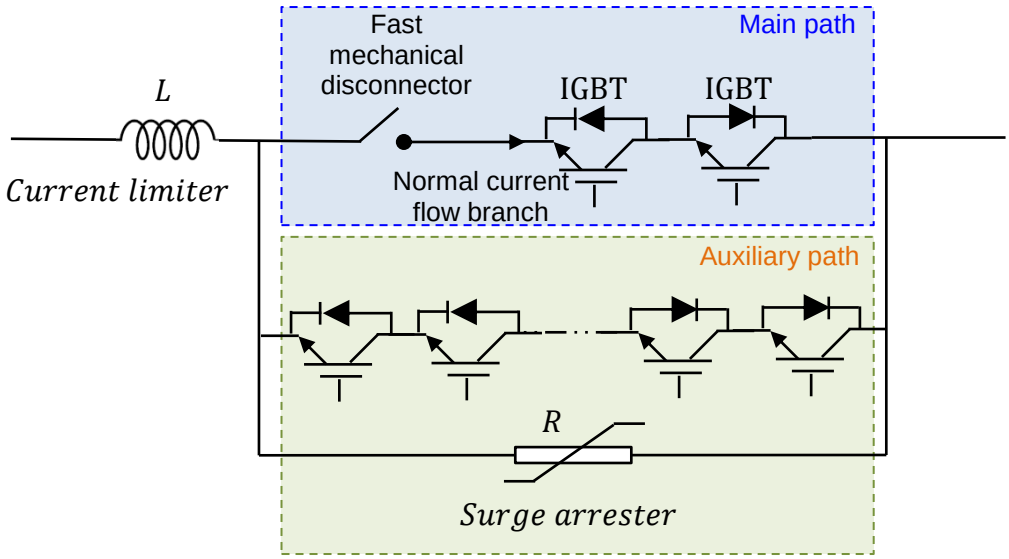


Figure 6-3 Hybrid direct current circuit breakers

During typical operating conditions, the current passes through a fast-mechanical switch (disconnector) and solid-state switches. No current passes through other branches during normal state operation. The number of semiconductor switches in the main path is less than the number required for solid-state dc CBs. Therefore, the on-state resistance of HCB is less than the resistance of SSB, accordingly [111]. Once an overcurrent is detected, the current is commutated immediately from the main to the auxiliary path, which operates as a solid-state dc breaker. The semiconductor switches in the main path are used to commutate and bypass the current to the auxiliary path. Then, the mechanical switch disconnects the main path without arcing. Next, the semiconductor switches in the auxiliary path are switched off.

Thus, the HCB could be used as a current-limiting device by controlling the current in the auxiliary path. This operational mode gives the protection strategy more time before permanently tripping or reclosing the breaker. The recloser process can be accomplished via commutating the current back to the main path by closing the disconnector and switching on the solid-state switches in the main path. Otherwise, the solid-state switches in the auxiliary path are switched off, which results in rapid voltage increase. The increase of voltage leads to bypassing it to the surge arrester, which is typically designed to conduct when the voltage exceeds the design limit of $1.5\,pu$ [205]. The surge arrester carries the current of the fault after switching off the semiconductor switches in the auxiliary path to provide the necessary reverse emf to force the fault current to $0\,pu$ and absorbs the stored energy of the inductive elements [205].

The operating speed of the hybrid dc breakers critically depends on the speed of the mechanical switch. The operating time of the circuit breaker is defined as the time from receiving the open command to the time when full voltage is withstood. The longer time requires higher breaking current capability. This time is typically less $2\,ms$ [205,264]. The dc fault characteristics in the proposed model in the previous chapters did not exceed this time. Hence, this type of breaker has sufficient speed and can be used to protect the proposed model.

6.5 Fault Detection and Protection Method

The critical requirement to design an MTDC system is a reliable protection strategy that can detect faults rapidly and select and isolate the faulty part while leaving the healthy parts in normal operation. Thus, this minimises the impact on the MTDC. The hybrid HVDC breaker characteristics become feasible, which interrupts up to $16\,kA$ current within $2\,ms$ [265]. These characteristics are sufficient for the proposed system.

In power systems, the change of frequency, dc under voltage, and overcurrent are detected by measuring devices. In practice, the detection could take several sampling times to finish [104]. Fault detection in an HVDC system is categorised by direct measurement methods and signal processing methods.

Measurement-based methods include derivative protection, overcurrent protection, differential current, and distance protection methods [266]. Currently, the traveling wave theory is the basis of most techniques employed for fault detection and fault location [267]. The handshaking method [268] and wavelet analysis [269] are techniques that can be used for this purpose.

A simple schematic diagram of derivative protection is shown in Figure 6-4. This protection scheme includes the measurements of both voltage and current. Then, the derivatives are obtained. To determine the fault occurrence, the derivative weighted sum must be compared with a predetermined threshold. This can be described mathematically as follows:

$$\varepsilon = K_1 \frac{dI}{dt} + K_2 \frac{dV}{dt} \quad \textbf{(6-1)}$$

where the $\frac{dI}{dt}$ sign, which is the current derivative, gives the fault direction. However, the main disadvantages of the derivative protection scheme are determination of the weighted derivatives (K_1 and K_2) and the threshold, which requires extensive studies [270, p.44]. Moreover, this scheme is suitable for point-to-point topology due to these disadvantages.

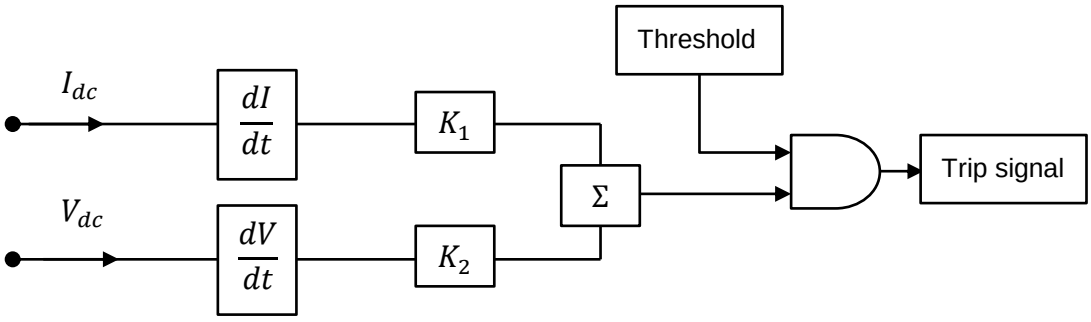


Figure 6-4 Derivative protection configuration

Figure 6-5 shows the proposed model and the points at which possible faults may occur. The impact of each fault location gives a different system response, as shown in Table 6-3. The current directions indicated in this table are given in Figure 6-5 by the blue arrows. The fault response differences are the key to determine the faulty part and isolating the fault using appropriate breakers.

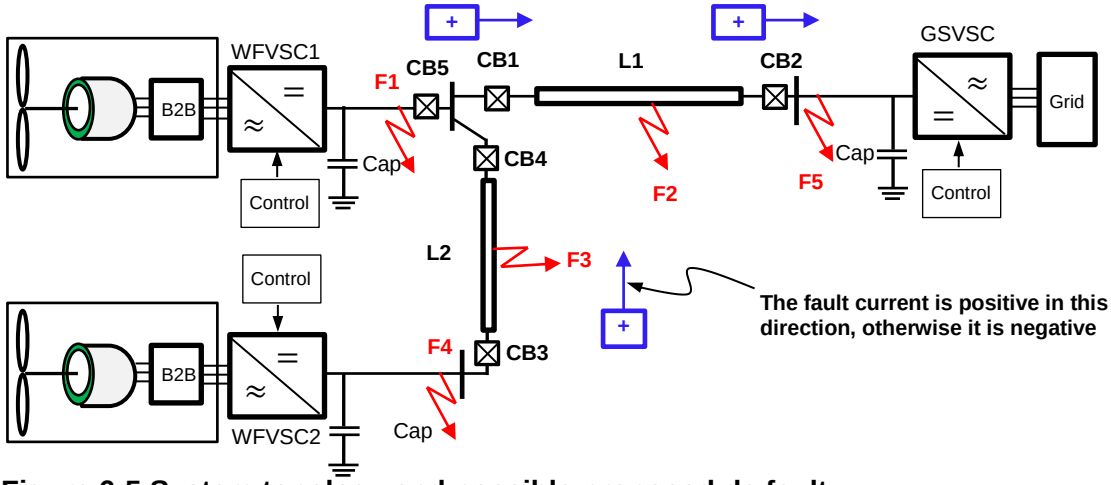


Figure 6-5 System topology and possible proposed dc fault

Table 6-3 Circuit breaker current directions during faults

Fault	Dc current direction				
	CB1	CB2	CB3	CB4	CB5
F1	-	-	+	+	-
F2	+	-	+	+	+
F3	-	-	+	-	+
F4	-	-	-	-	+
F5	+	+	+	+	+

A suggested fault detection and tripping algorithm based on Table 6-3 was proposed and implemented in this thesis. This algorithm can determine the faulty line and trip the corresponding breakers when the fault exceeds the predetermined highest permissible dc current. According to the algorithm, each fault (F1, F2…. or F5) causes tripping of the associated breakers as follows:

- Fault F1 trip CB5
- Fault F2 trip CB1 and CB2
- Fault F3 trip CB3 and CB4
- Fault F4 trip CB3 and CB4
- Fault F5 trip CB1 and CB2

The following figure presents a flow chart of the suggested algorithm:

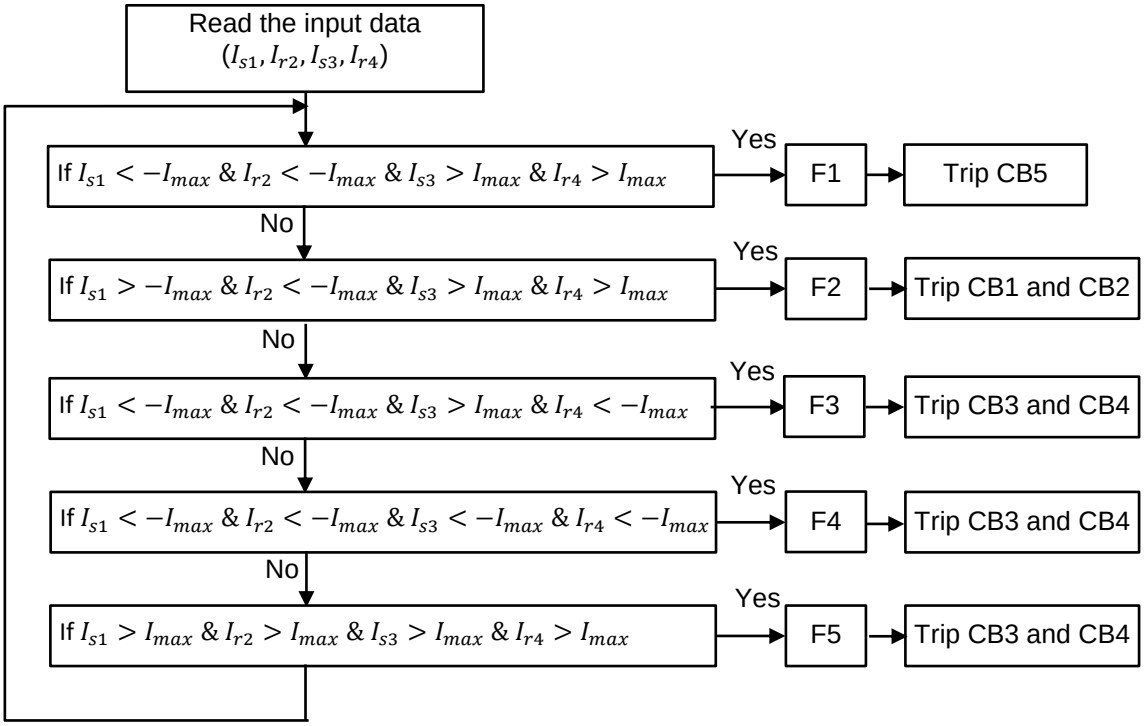


Figure 6-6 Flow chart for fault detection algorithm

In the above algorithm, the subscript s and r refer to the sending and receiving ends, respectively. It is not necessary to measure the current at the breaker CB5 due to the sufficient amount of information that is provided from the other four measurements. This algorithm requires communication between the cable ends to determine the fault location and isolate the faulty part.

6.6 Simulation Results

A Simulink model was designed, implemented, and operated to test a protection system (see Figure 6-7). The algorithm shown in Figure 6-6 was implemented using a MATLAB function which has four inputs. These inputs were taken from a signal builder to represent the current at the sending and receiving ends of each cable. The MATLAB function has five outputs; each represents a certain fault F1-F5 (Figure 6-5) depending on the signs of currents, as illustrated in Table 6-3.

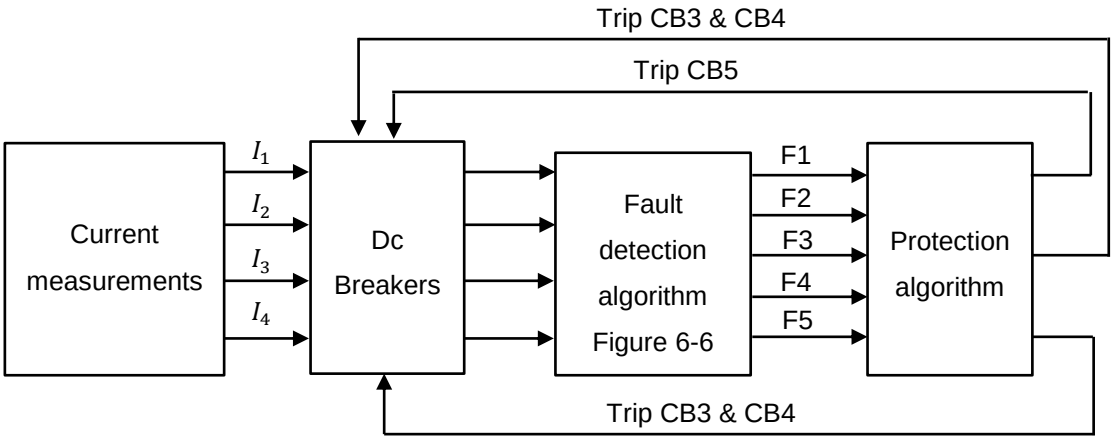


Figure 6-7 Protection algorithm implementation

The detection/location algorithm was designed based on the proposed model topology. In this algorithm, it is required to measure the currents at four CBs only; CB5 can be excluded because the four CBs provide the necessary information. These four measurements are the ends of the two dc cables shown in Figure 6-5. Therefore, it not necessary to go through into the detailed model and a simplified model can be used to assume these current magnitude and directions.

The detection algorithm involves a delay before sending a trip signal to the associated breaker—this delay can be specified separately. In this project, $10\,ms$ was chosen and can be varied from zero to any delay time as required. The algorithm also applies reclosing of a breaker to prompt if the system has restored its normal operation after the reclosing. The reclosing process also involves a delay.

Figure 6-8 depicts the normal output of the detection algorithm, where a fault F1 was initiated from $t = 1\,s$ to $t = 1.5\,s$ and again $5\,ms$ after the fault was interrupted. This time involves the delay for protection and recloser timing. The output is either 1 or 0, which is required for the breaker to be closed or opened, respectively.

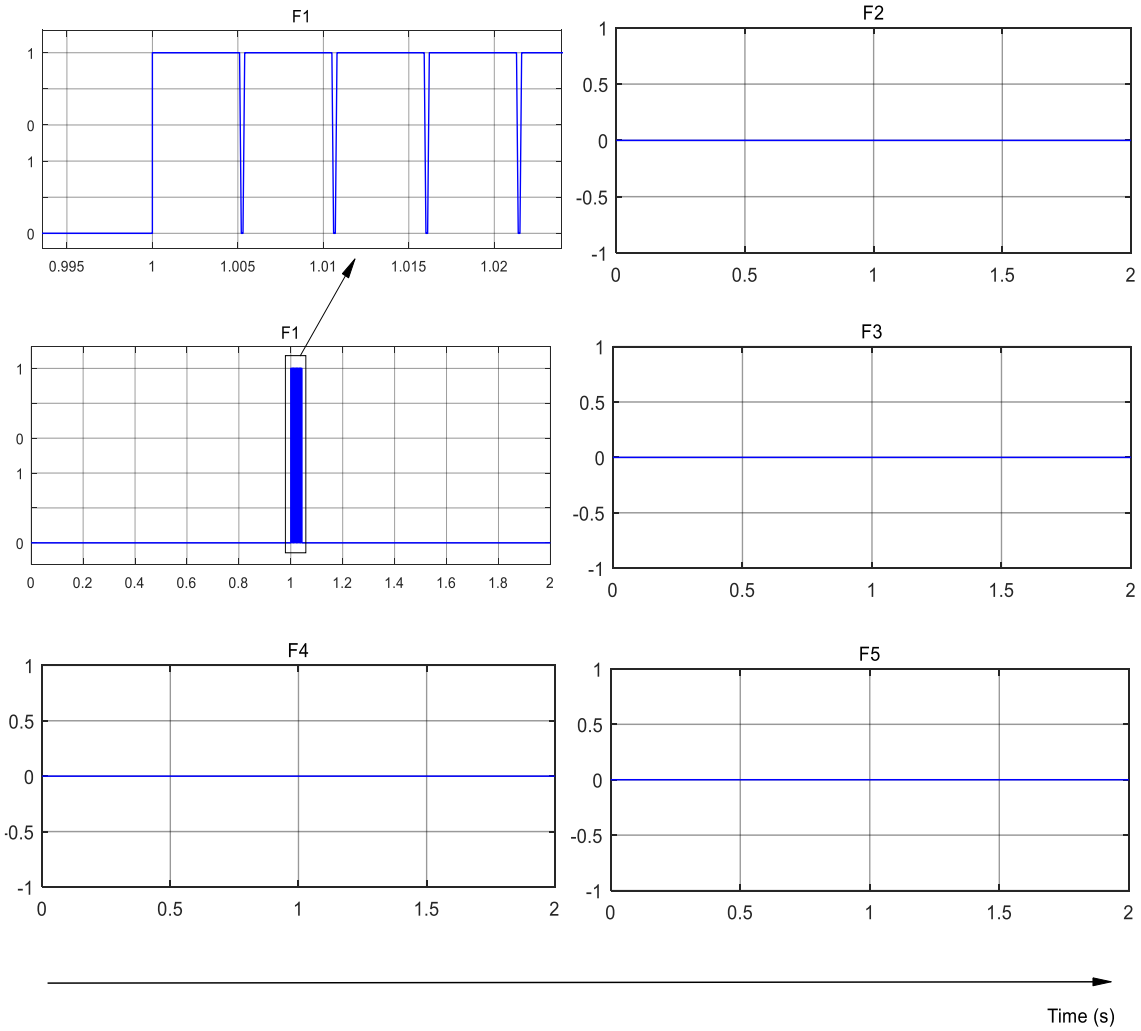


Figure 6-8 The output of the detection algorithm (1 is fault)

The tolerance current was set to $1.5\,pu$, as shown in Figure 6-9. The first trip signal was to the breaker at time $t = 1.005\,s$. The breaker was at open-state for $0.1\,ms$, which means that no current passes through it. A reclosing signal was sent to the breaker, and after the chosen delay-time ($5\,ms$), another trip signal was sent to the breaker since the current still exceeded the $1.5\,pu$ limit. These reclosing attempts were repeated for eight times, as shown in the figure below. After the eight reclosing attempts, which can be reduced or increased, the breaker stayed at its block-state, which means that the fault is permanent.

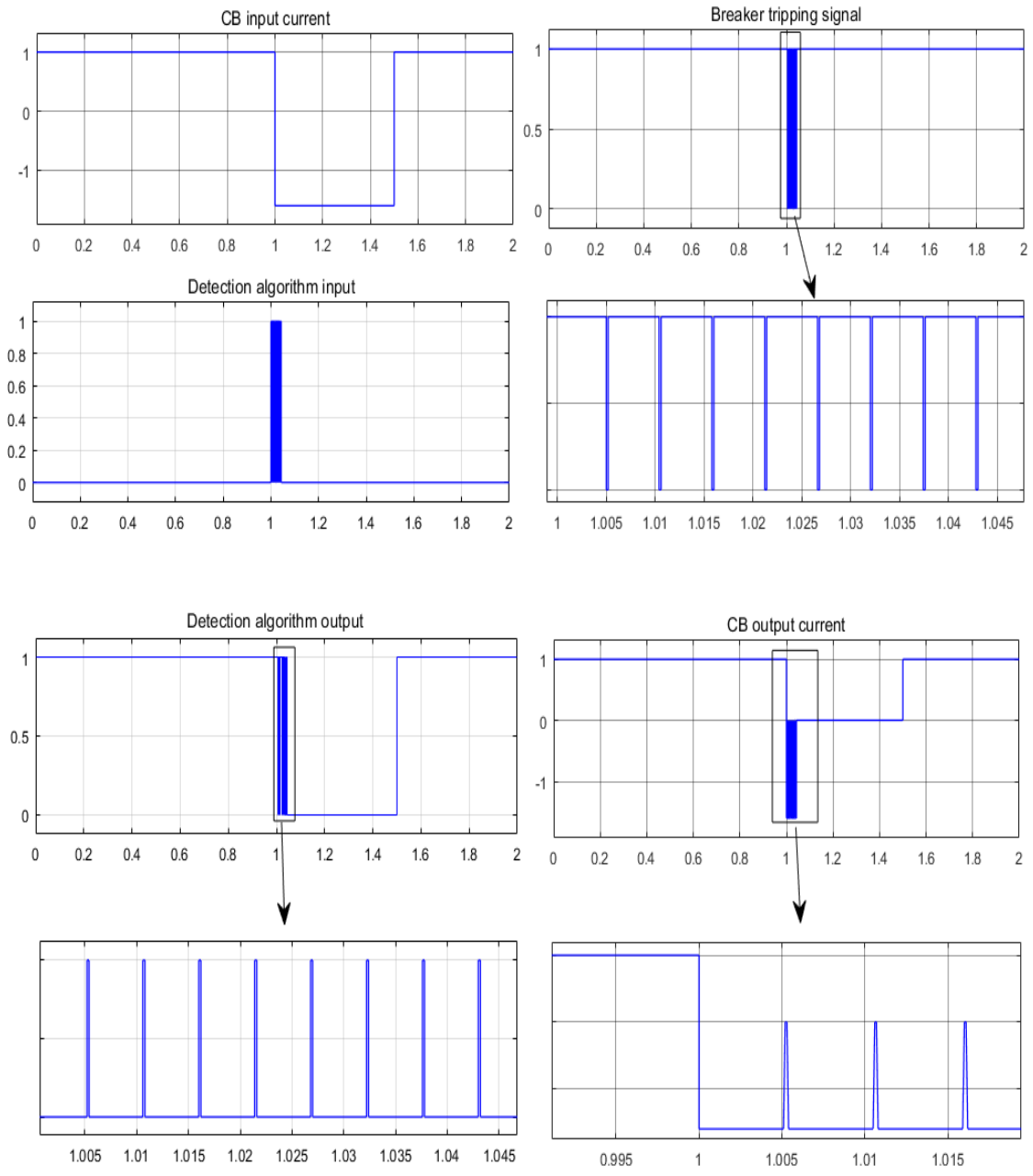


Figure 6-9 Breaker currents and trip signal

After the fault clearance, output of the model returned to normal, the model resumed normal operation, and the breakers returned to their closed state, with current passing through it normally. The reclosing attempts were done automatically, similar to the breaker in practice. The model decided that the fault was permanent after the eighth reclosing attempt; hence, no further reclosing attempts were made, and the breaker was blocked. Although in this system the

reclosing after the fault clearance occurred automatically, in real systems this can be accomplished manually.

6.7 Summary

This chapter tries to complete the proposed model by designing, implementing, and simulating an algorithm that can detect, locate, and isolate the faulty part by tripping the necessary dc circuit breakers (DCCB) to protect the model against the dc fault. For this purpose, a fast acting DCCB was utilised because the dc fault current increases substantially to high value with short time. The algorithm was designed specifically for the proposed system and implemented using MATLAB/Simulink model.

The detection/location algorithm was designed based on the proposed model topology. In this algorithm, the currents of CB5 was excluded because the current measurement at the other four CBs, which are the two ends of the two dc cables, provide the necessary information. Therefore, it not necessary to go through into the detailed model and a simplified model can be used to assume these current magnitude and directions.

The current due to the dc fault increases to high values within short time which requires correspondingly fast algorithm that can detect/locate the fault current before it exceeds the limit value. However, this algorithm requires a communication to provide the information about the current status at the two dc cable ends. The communication reduces the reliability and increases the detection time.

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7 CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER WORKS

7.1 Conclusions

Semiconductor technologies have witnessed significant development because of advancements that allow power transmittal by HVDC less expensively and more conveniently than by HVAC. A VSC technology based on IGBT appears promising due to the advantages of controllability and flexibility over the LCC technology. VSC can overcome the difficulties offered by LCC due to the ability of IGBT valves to switch on or off as required. The advantages of VSC such as power direction reversal, flexibility, and controllability simplify MTDC construction.

IGBTs are relatively more expensive, which is reflected on converter capital cost of the VSC. The proposed mixed topology that includes series connection of two diode rectifiers and VSC, was introduced and investigated in this thesis. This topology reduces the cost by a significant factor. Each component converts one-third of the total power. Rectifiers series connection helps to increase the output voltage at the dc busbar in a similar way to battery series connection. Nevertheless, this configuration is not suitable for applications that require bidirectional power flow, such as those that connect two power systems. This configuration is suitable for offshore windfarm applications. The bidirectionality can be achieved by changing the converter topology using switches. Inductor and capacitor filters are required to eliminate higher-order harmonics that produced by the valve switching from the output.

The converter topology was introduced in two configurations: one has the VSC connected at the bottom of the two diode rectifiers and the other has it between the diode rectifiers. The first connection enables the VSC to control the voltage based on its own voltage, while the other topology enables the VSC to control the total voltage measured at the positive and negative busbar voltage. Simulation results showed that there was no difference between the two arrangements during normal system operation. However, during a dc fault, the

first connection gave unbalanced peak values, which was not the case when connecting the VSC in the middle in the second case. The proposed model shows an improvement over the conventional topology in terms of the peak overcurrent and overvoltage elimination and the time required for model to return to its steady state operation after the fault clearance.

HVDC transmission topology, such as monopolar and bipolar dc transmission lines, can affect the dc fault characteristics. However, in bipolar dc transmission systems, for example, it is possible to isolate the negative pole while keeping the other pole in operation in case of a negative pole-to-ground fault. This operation mode requires installation of a dc breaker on each pole. Pole-to-pole faults are less common than pole-to-ground faults and affect the system severely.

Generally, VSCs are vulnerable to dc faults because these faults can cause destructive results to the overall system. Throughout the fault, the current increases substantially in a short period of time. Thus, a reliable protection system that can detect, locate, and isolate the faulty part rapidly is necessary.

The time development of dc faults in a system was shown to be substantial and superpose all capacitive resources in the system including the dc capacitor, dc cable, and ac grid. The total fault current is the sum of all these fault current contributors. Therefore, dc breakers should be fast enough to interrupt the current before it exceeds the highest permissible value. Several types of dc breakers can be used, including solid-state dc circuit breakers and hybrid dc circuit breakers. The first type is faster than the other types. However, its on-state resistance is much higher than that of the hybrid breakers due to the larger number of IGBTS in the series path of the former. The hybrid dc breakers have relatively lower on-state resistance but higher interruption time. Also, the circuit breaker cost plays a vital rule in HVDC protection. It was shown that solid-state circuit breakers become less expensive in high voltage applications compared to the other breakers technologies.

Alternatively, in the ac grid side unbalanced fault are more frequency. Moreover, it is difficult to obtain a balanced three-phase operating condition in

distribution system. Consequently, a negative sequence of voltage and current will be present at all times in most power systems. The knowledge of faults in ac power networks is well-developed. However, in MTDC networks connected to the ac system, both symmetrical and unsymmetrical faults of the ac grid affect the dc cable voltage and current and cause the dc voltage to rise. Hence, to receive the full benefits of VSC transmission, advances of technology are necessary to ensure the ability to function in severe grid fault conditions.

A dual current control strategy was suggested to control the dc voltage in the outer control loop and the current in the inner control loop during the unbalanced operational conditions. Negative and positive dq currents in the synchronous reference frame were controlled separately in this control scheme. Due to the lack of reactive power control, other components, such as a dc chopper and energy storage devices can be added to be used in wind turbine applications; however, this solution involves extra cost. Therefore, a reactive power control scheme was proposed alongside the dc voltage in this thesis in the outer control. Thus, the outer controllers regulate both dc voltage and reactive power in the grid-side VSC. This control strategy is known as the generalised control scheme, and it can be used for both balanced and unbalanced conditions.

To account for unbalanced ac faults, the control in this case should be modified by converting the dq in normal operation into positive and negative dq-axis, which means that four loops are needed. The separation of negative dq and positive dq is solved using many methodologies. However, delay signal cancellation (DSC) was chosen due to its the simplicity of implementation, accurate results, and relatively short simulation time required for the block to run to produce results.

In any case, however, the protection scheme of an MTDC system should be sensitive, selective, fast, and reliable. Specifically, it must be designed to isolate the fault reliably from the system in a short period of time after the occurrence of the fault, while maintaining the remainder of the system in a secure operational condition. This requires a fast detection algorithm to detect the fault quickly and

a fast-acting dc circuit breaker. Ac circuit breakers are insufficient for dc faults because ac breakers require two cycles or $40\,ms$ to isolate the fault and also require a zero-current crossing point for the operation. Consequently, dc circuit breakers should be developed for fast fault tripping and to avoid the need for a zero-current crossing point.

The protection system design and fault detection algorithm to detect and locate the faulty part needs information from both ends of all cables. This means that the communication between relays is needed. Moreover, detailed analysis about rated currents and voltages at each part should be conducted. Information about permissible values of the connected components, according to the grid code or the manufacturer datasheets, should be known. An automatic recloser after the fault detection can be used to determine whether the fault is permanent or not. After two reclosing attempts, if the current is not at the normal rated value, the detection algorithm determines that the fault is permanent and blocks the dc breakers. However, the number of reclosing attempts can be reset to any number.

7.2 Recommendations for Future Works

In this thesis, the major work was about the design, modelling, and operation of an MTDC model that includes a topology of a series connection of two diode rectifiers and a VSC. However, this research may continue in the following fields:

- To improve the reliability of the MTDC model, several topologies can be implemented, such ring topology or star with central ring topology. Moreover, the reliability of the current topology can be studied and assessed. Generally, the diode rectifiers are more reliable than the IGBT devices due to the existence of the gate. Regarding the dc transmission, the current topology has one line but the ring topology includes two lines, which improves the reliability and increases the cost.
- The thesis can be extended to include a windfarm model that contains several wind turbines; each wind turbine has a back-to-back converter

and its own control model. The arrangement of wind turbine within the windfarm can also be analysed regarding cost and performance.

- Modular multilevel converter (MMC) VSC can replace the three-level converter, which improves the model performance under abnormal operating conditions and affects the overall cost. In this case, the switching pattern from the SVPWM should be designed and the total cost should be analysed.
- Fault-tolerant control is a crucial feature that can be obtained through redundancy and can be studied for semiconductor devices.
- This thesis is based on the use of MATLAB/Simulink to validate the proposal. However, a practical implementation of the model is not an easy task due to the high power and voltage. A scaled-down model can be implemented to validate the proposal and provide practical results.
- Voltage measurements was carried out so that when connecting the VSC in the middle the voltage measurement was taken from the total pole to pole voltages and when connecting the VSC in the middle the voltage was measured at the VSC voltage. however, reversing the voltage measurements can be investigated.

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APPENDICES

Appendix A Transformation of Coordinates

The coordinates transformation from a three-phase reference frame coordinate system to a two-dimentional rotating coordinate system, or dq, is also called Park's transformation. This transformation can be accomplished via the following two steps:

1) Transform the three-phase system abc into a two-phase stationary axis system, αβ.

2) Transform the αβ stationary coordinate to a dq rotating coordinate system.

Figure A-7-1 illustrates the two steps. A vector representation in multidimensional space of n-dimensions is done by multiplying an n-dimensional vector transpose of coordinate units by the vector representation of a vector. Hence, in three-phase, which is three-dimensional space, this is

$$X_{abc} = [a_u \quad b_u \quad c_u] \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{A-1}$$

The transformation between two different axes is

$$X_{\alpha\beta} = T_{abc-\alpha\beta o} \cdot X_{abc} \tag{A-2}$$

Here the transformation matrix is

$$i_{\alpha\beta 0}(t) = T i_{abc}(t) = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \tag{A-3}$$

$$i_{abc(t)} = T^{-1} i_{\alpha\beta 0(t)} = \begin{bmatrix} 1 & 0 & 1 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} & 1 \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \\ i_0(t) \end{bmatrix} \tag{A-4}$$

Then, transformation to dq is accomplished using the following conversion matrix:

$$T_{\alpha\beta 0-dq0} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2}{3}\pi) & \cos(\omega t + \frac{2}{3}\pi) \\ -\sin(\omega t) & -\sin(\omega t - \frac{2}{3}\pi) & -\sin(\omega t + \frac{2}{3}\pi) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad \textbf{(A-5)}$$

and

$$T^{-1}{}_{dq0-\alpha\beta 0} = \begin{bmatrix} cos(\omega t) & -sin(\omega t) & 1 \\ cos(\omega t - \frac{2}{3}\pi) & -sin(\omega t - \frac{2}{3}\pi) & 1 \\ cos(\omega t + \frac{2}{3}\pi) & -sin(\omega t + \frac{2}{3}\pi) & 1 \end{bmatrix} \quad \textbf{(A-6)}$$

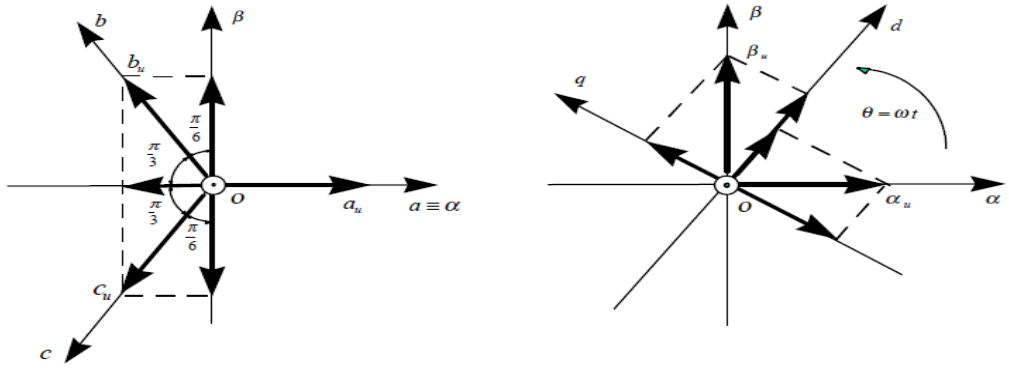

Figure A-7-1 Park's transformation vector diagram to convert three-phase coordinate system into two-dimensional coordinate system

Appendix B Per-Unit System

A comparison of different parts of a system with different ratings is simplified by using a per-unit (pu) system instead of the rating values. Moreover, with the pu system, the design and implementation of the controllers of HVDC VSC is easier.

The base power is equal to the equipment nominal power, while the base voltage is equal to the equipment nominal voltage. Generally, these values are taken from the name plate data.

$$Quantity\ in\ pu = \frac{SI\ Unit\ quantity}{Base\ value} \quad \textbf{(B-7)}$$

$$Power\ (S, P, or\ Q)\ pu = \frac{MVA_{actual}}{MVA_{base\_3\emptyset}} \quad \textbf{(B-8)}$$

$$Voltage\ pu = \frac{kv_{actual}}{kv_{LLbase}} \quad \textbf{(B-9)}$$

$$Current\ pu = I_{actual}(kA)\frac{\sqrt{3}kv_{LLbase}}{MVA_{base\_3\emptyset}} \quad \textbf{(B-10)}$$

$$Impedance\ pu\ (R, X, and\ Z) = Z_{actual}(\Omega)\frac{MVA_{base\_3\emptyset}}{kv^2_{LLbase}} \quad \textbf{(B-11)}$$

The base speed of rotating machines is equal to the synchronous speed. Regarding the torque, the base value equals the torque corresponding to the synchronous speed and base power:

$$Base\ torque = \frac{base\ 3-phase\ power\ watt}{Base\ (synch.)\ speed\ rad/sec} \quad \textbf{(B-12)}$$

The power factor will not change in pu.

- **Per unit across transformers**

For the case in which a transformer exists in a system, the voltage between its primary and secondary will differ from each other by a factor turn ratio, and the same change will exist in the voltage base, although the power rating is the same on both sides. For example, for an 11 kv/400 V transformer on the primary, 11 kv represents 1 pu, while on the secondary 400 V represents 1 pu. Therefore, the line-to-line voltage base is taken at a location and multiplied by the turn ratio on the other side of the transformer, if there is any. The current and impedance base will change accordingly, because the power remains unchanged. Unlike the voltage base, the current base, in this case, changes

inversely with the turn ratio. The base change for a transformer that has a turn ratio equal to N_p/N_s as summarised in Table B-1

Table B-1 Per-unit summary

Parameter	Primary side base	Secondary side base
Power base (P, Q, and S)	S_{base}	S_{base}
Voltage base (V)	V_{base}	$V_{base}.\frac{N_s}{N_p} = V_{2base}$
Current base (A)	$\frac{S_{base}}{\sqrt{3}V_{base}}$	$\frac{S_{base}}{\sqrt{3}V_{base}}.\frac{N_p}{N_s} = \frac{S_{base}}{\sqrt{3}V_{2base}}$
Impedance base (R, X, and Z)	$\frac{V_{base}^2}{S_{base}}$	$\frac{V_{base}^2}{S_{base}}.\left(\frac{N_s}{N_p}\right)^2 = \frac{V_{2base}^2}{S_{base}}$

The base in the dq reference frame also can be calculated:

$$V_{d\_base} = V_{q\_base} = \sqrt{\frac{2}{3}}\mathrm{V}_n \quad \textbf{(B-13)}$$

$$I_{d\_base} = I_{q\_base} = \sqrt{2}I_n \quad \textbf{(B-14)}$$

$$Z_{d\_base} = \frac{V_{d\_base}}{I_{d\_base}} = \frac{V_n}{\sqrt{3}I_n} = Z_n \quad \textbf{(B-15)}$$

$$S_{d\_base} = \frac{2}{3}S_n \quad \textbf{(B-16)}$$

Appendix C Symmetrical Components

Symmetrical components are a mathematical tool used to ease the study of unbalanced 3-phase faults in power systems. In contrast, symmetrical components can be used in both typical and fault conditions. The elementary idea is to convert an unbalanced system of N phases to N sets of symmetrical combinations of phasors with the aid of a linear transformation. Therefore, a 3-phase system, which is the most common system, results in three groups of "symmetrical" components.

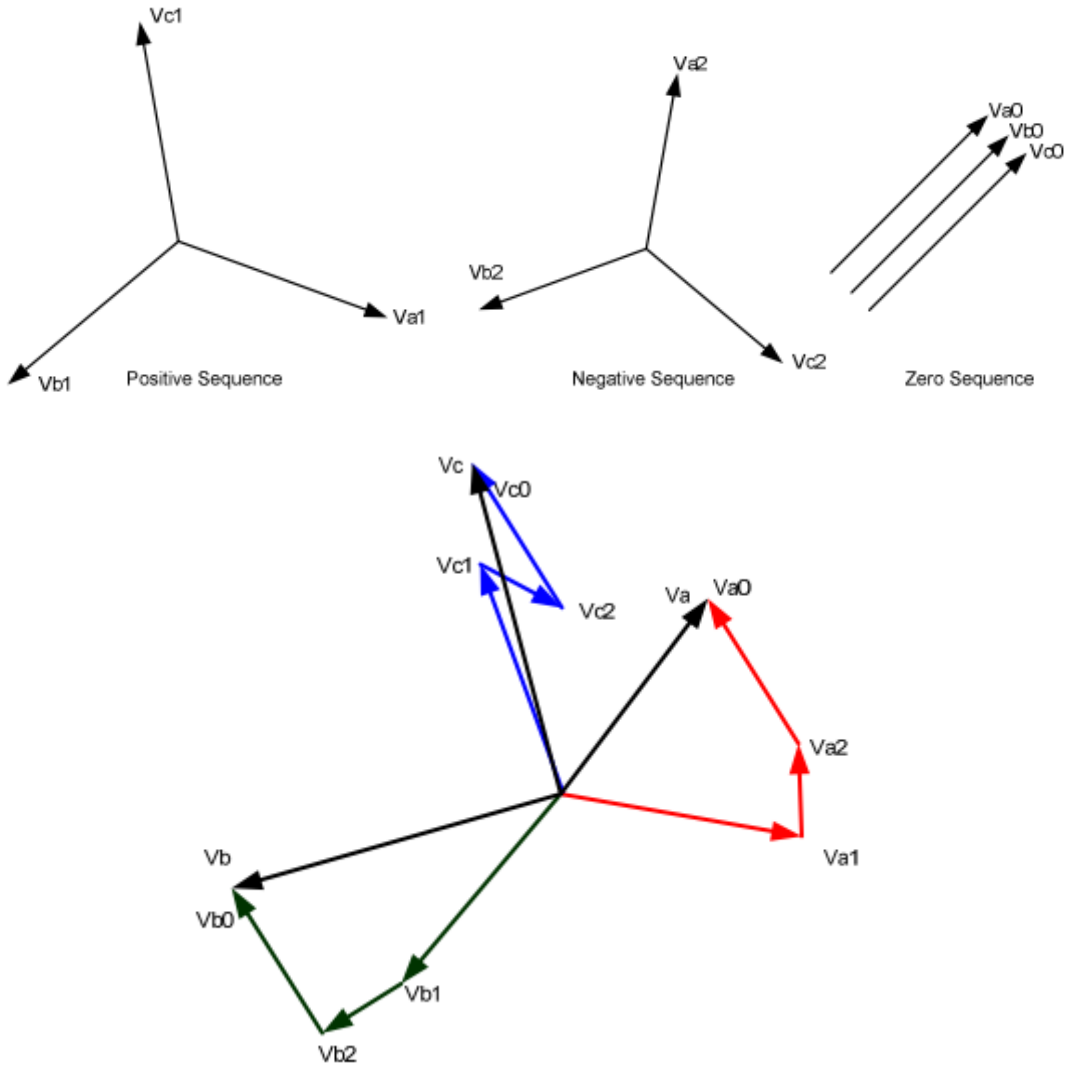

Figure C-7-2 Symmetrical Components

These components are often referred to as positive, negative, and zero sequence. The phase sequence of the positive is abc, while the negative has acb phase sequence, and the zero sequence phasors have no rotation, as shown in Figure C-7-2. Power system analysis using symmetrical components is much simpler, since the resultant equations are mutually linearly independent:

$$V_{abc} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} V_{a0} \\ V_{b0} \\ V_{c0} \end{bmatrix} + \begin{bmatrix} V_{a1} \\ V_{b1} \\ V_{c1} \end{bmatrix} + \begin{bmatrix} V_{a2} \\ V_{b2} \\ V_{c2} \end{bmatrix} \quad \textbf{(C-17)}$$

where the subscripts $0, 1,$ and 2 are the zero, positive, and negative sequence. They can be defined as

$$\begin{aligned} V_0 &= V_{a0} = V_{b0} = V_{c0} \\ V_1 &= V_{a0} = aV_{b1} = a^2V_{c2} \\ V_2 &= V_{a0} = a^2V_{b1} = aV_{c2} \end{aligned} \quad \textbf{(C-18)}$$

where $a = e^{j\frac{2\pi}{3}}$ or $1 < 120^{\circ}$ and V_0 are three equal vectors in the same direction, V_1 are three balanced vectors rotating in an anticlockwise direction, and V_2 are three rotating vectors rotating clockwise. Then, (C-17) can be written as

$$V_{abc} = \begin{bmatrix} V_0 \\ V_0 \\ V_0 \end{bmatrix} + \begin{bmatrix} V_1 \\ a^2V_1 \\ a\,V_1 \end{bmatrix} + \begin{bmatrix} V_2 \\ a\,V_2 \\ a^2\,V_2 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} \quad \textbf{(C-19)}$$

or

$$V_{abc} = AV_{012} \quad \textbf{(C-20)}$$

where $A = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix}$ and $V_{012} = \begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix}$

Also,

$$V_{012} = A^{-1}V_{abc} \quad \textbf{(C-21)}$$

where $A^{-1} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}$.