Fabrication, development and analysis of Film Bulk Acoustic Resonators on flexible polymer substrates

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PhD Thesis

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Abstract

It is the focus of this project to explore the possibility of achieving Radio Frequency (RF) micro-devices on flexible polymer substrates. To this end standard MEMS fabrication methods have been tailored to allow the integration of functional materials and device patterning for production of RF MEMS devices with flexible organic substrates. Material quality, device yield, performance and reliability are critical aspects of our study.
The project encompasses the use of a direct integration method for the creation of Film Bulk Acoustic Resonators (FBARs) on Liquid Crystal Polymer (LCP) substrates. An FBAR is a passive component used for resonance and filtering purposes. Its production on organic substrates would lead to a number of advantages including: overall cost savings, size reduction and ability of the device to be directly integrated on the printed circuit board (PCB) front-end with the other essential components (i.e. antenna) without the use of wiring and interconnections.
New fabrication process flows have been developed to allow the creation of FBAR microwave devices on LCP. First of all pre-processing of the polymer substrate is carried out to make it rigid and smooth. Substrate smoothness and stiffness are necessary in order to obtain functioning devices and for the substrate to comply to the standard fabrication methods. Rigidity is achieved through a backing method whereby silicon or glass are attached to LCP with an intermediate adhesive layer. The best way to achieve smoothness was found to be Chemical Mechanical Polishing (CMP). Standard fabrication techniques were then employed to deposit the metal and piezoelectric material and pattern them. Both bulk and surface micromachining were used and, in some cases, tailored to suit the new substrate's (LCP) tolerance limits (such as temperature and flexibility). Zinc Oxide (ZnO) piezoelectric is the preferred functional material and it is chosen due to its relatively low deposition temperature requirements (below 300°C) and its high frequency characteristics.
The creation of a front-to-back processed FBAR on LCP is successfully carried out at relatively low temperatures since the Zinc oxide (ZnO) functional material is proven to yield good crystallinity at a deposition temperature of 100°C and also because micromachining temperatures do not generally exceed 115°C. The final device is characterized through RF measurements, compared with simulations and standard FBARs and the polymer/ceramic integration reliability for device creation is briefly addressed.
In conclusion FBARs are successfully created on LCP with only minor complications related to LCP surface roughness and RIE etch of the polymer. The project lays promising prospects for RF MEMS devices on compliant organic substrates.

Acknowledgements

In memory of my beloved grandmother, Touran Moulavi, who passed away during the final stages of my PhD.

As with Heisenberg's uncertainty principle, whereby position and momentum cannot both have precise values at the same time, a PhD project is based on the same law: if the quality of the thesis is known with certainty then the hand-in time would not and, vice-versa, if the time of the hand in is known with certainty, the completeness of the work is not known. Since my deadline was known with precision, the latter case is true. Despite this I wish to have positively contributed to knowledge with this project and hope that the work will provide useful insights in the future for people working on polymer-based MEMS. It would be an honour to have an "on loan" stamp on the library copy of the thesis. This experience has been an intellectual one as well as one of personal growth.

I would like to thank first of all my parents for supporting me throughout my life and for trusting every decision I have made. Dr. Paul Kirby for giving me this opportunity and for teaching me the art of critical thinking through which I have gained the ability to re-evaluate my decisions each time with a new perspective. All of my colleagues, especially Rob Wright, who has been like a teacher throughout my journey, Carlos Fragkiadakis and Petros Gkotsis for spending their precious time and sharing their knowledge. Last, but not least, all staff members for providing the facilities and an excellent working environment.

Chapter 1

Thesis outline

1.1 Structure of Thesis

The structure of the thesis contains, first of all, aims and objectives which are targeted and clarified in this Chapter. The general objective is to create RF MEMS devices (FBAR) on microwave polymer foils (LCP) using standard MEMS techniques. This section is followed by an introductory one which includes a literature search in order to provide an appropriate background on the project's objectives and set the scene for the upcoming experiments. The literature search in Chapter 2 covers a background knowledge on RF MEMS and state of the art of MEMS on polymers. General material reliability is also explained, including thin film ceramics and thin film metals.

Prior to the presentation of the experiments, a list of apparatuses and the methods employed are explained in Chapter 3. Chapters 4 and 5 address processing topics relevant to the fabrication of the LCP FBAR, with the findings presented being obtained while developing a processing scheme for LCP FBAR. The experimental results include various sections based on specifically tailored FBAR on LCP fabrication process sequences which, first, face LCP substrate standardisation. This is done through pre-processing of the LCP with roughness reduction and rigidisation methods. It is only after substrate standardisation that the usual processing techniques such as metal deposition, ZnO thin film sputtering, layer patterning and removal and back RIE etching are explored on LCP. The importance of substrate rigidity and smoothness is proven throughout all of the standard fabrication steps. LCP and gold are, then, characterised in terms of their Young's modulus and yield strengths while ZnO, being a brittle material, is characterised in terms of its fracture strength.

Chapters 4 and 5 present the steps required to produce FBARs on LCP. The LCP-based devices are presented in chapter 6 where the RF performance is tested and compared to theoretical results (what is expected on LCP without back residues) and standard Si-based device. Chapter 7 discusses both multilayer and device reliability analyses. In this chapter optional device configurations are also explored that can be employed in the future to relieve excessive stress on the brittle ZnO. Finally Chapter 8 concludes the thesis with some final

observations, outlining the contribution of this project to the field and making suggestions for future work.

Concluding remarks in chapter 9 include: all of the observations made throughout the experiments, future work to be carried out and a list of the contribution to knowledge of this thesis. Finally the appendices contain any material properties, process details and Matlab codes that may further the reader's understanding of the work.

1.2 Scope, aims and objectives

Scope

The research area on flexible electronics and RF MEMS on polymer substrates has been underway in the past few decades. Substrate flexibility would allow increase in circuit density and the production of electronic circuits and devices on polymers would result in smaller, multifunctional, reliable devices with higher frequency abilities. Therefore the scope of this research is to investigate the knowledge of flexible electronics and high frequency MEMS on organic polymer substrates with the integration of an inorganic piezoelectric ceramic. To this end, the creation of LCP-based Film Bulk Acoustic Resonator (FBAR) devices, with the requirement of an inorganic ceramic deposition (ZnO), will be studied.

Aim

The research aims to further the field of flexible electronics by investigating the possibility of exploiting existing MEMS techniques and tailoring them appropriately for the creation of passive radio frequency (RF) components directly on polymers.

Literature has already presented some digital IC components (thin film transistors) and active MEMS devices (switches and tunable actuators) on polymers. This leaves us with the necessity of investigating the creation of low cost and high performance passive components on polymers for integration with the existing active ones. Passive components here refer to resonators and filters.

In this thesis the findings of a study to investigate the feasibility of producing high frequency MEMS devices on flexible substrates is described. Such a study fits within the field of microwave wireless communication systems which is constantly seeking new components and sub-systems with ever increasing functionality, improved performance, lower weight and cost.

Several MEMS-based devices fabricated on polymer substrates have been reported in the literature, including switches and pressure sensors. In this thesis MEMS fabrication techniques for incorporating a functional ceramic thin film on polymer will be employed. Thin Film Bulk Acoustic Resonator (FBAR) with Zinc oxide (ZnO) piezoelectric film will be used as a vehicle for developing MEMS processing on a flexible polymer substrate.

For the flexible substrate a novel polymeric material is used. This material is developed specifically for microwave applications and has already widely been used for Printed Circuit Board (PCB) development. Liquid Crystal Polymer (LCP) is the substrate of interest as, besides its desirable electronic characteristics such as low dielectric loss, it has thermal, mechanical and chemical advantages.

An investigation will be carried out on how to produce FBARs on flexible LCP substrates with the integration of a functional ceramic layer and the use of standard MEMS fabrication techniques, including front-to-back alignment. Standard MEMS fabrication processes have been chosen since methods used by the organic IC industry are basic and, if tailored to suit that of the more complicated MEMS structures, would see a slow transition. The most challenging steps in the fabrication are: substrate flatness for processing, substrate roughness reduction for proper ceramic material growth, multilayer reliability verification and

back-side processing.
The novelty of this research lies in the investigation of thin film functional ceramic integration on flexible polymers and, complex back processing of this combination. Furthermore RF performance of the devices must be assessed with a thorough assessment of possible factors affecting it. Device reliability is also critical as the ceramic/polymer integration gives novel devices.

The following studies will be included in the research:

1. Fabrication techniques used to carry out the task, including: substrate "standardisation" (flattening and smoothing), functional ceramic growth quality on LCP and its dependence on substrate smoothness and temperature and failure analysis of the multilayer. Hence an assessment of FBAR device processing will be carried out highlighting its challenges.

2. Device RF performance through transmission parameters followed by a general reliability assessment.

Part I

Introduction

Chapter 2

General background

The purpose of this chapter is to cover the development of technologies that have lead to the present project. The technology covering silicon devices is generally well established, although some fine-tuning is still carried out. Silicon-based components, however, have certain limitations in the applications domain due to the lack of flexibility and reconfigurability.

Polymer electronics have made an appearance in the past few decades in the integrated circuit (IC) field with digital electronic devices such as Light Emitting Diodes (LED) and organic transistors being sold commercially.

The gap now lies within the polymer Micro Electro Mechanical Systems (MEMS) industry and, especially, for radio frequency (RF) components aimed at wireless communications. While polymer-based MEMS sensors and actuators working within biomedical settings have already been proposed, devices that can be directly integrated with antennas and phase-shifters for RF communications have yet to be developed.

This is where the current work fits and, in order to fill in the existing knowledge gap, the fabrication of a Film Bulk Acoustic Resonator (FBAR) device is proposed. This resonator, adequate for signal filtering purposes, is usually implemented in the front end of communication systems alongside other components (antenna, phase shifter), in order for the assembly to then act as a duplexer. A polymer FBAR would allow ease of integration directly onto the other components without the need of extra interconnects which introduce parasitics and, therefore, signal degradation.

In this chapter an overview is presented of what has been done within the polymer microsystems area so far. An introduction to the principles of energy conversion within the MEMS domain (in particular piezolectric conversion) is given followed by a background of RF MEMS and a thorough section on FBARs. Surface topography will then be discussed as it is a major processing issue within our new flexible substrates. MEMS reliability will also be discussed in terms of thin film stresses, which is another factor affecting processing and eventual device yield.

2.1 Introduction

Micro-electro-mechanical systems (MEMS) are sensing and actuating devices with sizes in the micron domain. At the beginning of the 1990s, MEMS emerged with the aid of the development of integrated circuit (IC) fabrication processes [282]. MEMS have been applied in: microfluidics, aerospace, biomedicine, chemical analysis, wireless, communications, data storage, display and optics [72]. These devices make use of functional materials and their properties to convert mechanical displacements into electrical signals (sensors) and viceversa (actuators). The functional materials are mainly thin film ceramics which are implemented due to their electromechanical coupling capabilities. The sensing and actuating principles are based on various elementary physical principles, which can also be combined for more complex multifunctional devices.

According to Moore's law, circuit density on chips has roughly doubled every two year since the 1970s and, as mentioned by Kosko [126], to keep up with this pattern we have to move into the nano world. Another approach is to combine MEMS and integrated circuits (IC) in order to achieve device multifunctionality which automatically leads to overall performance improvement, size and cost reduction, high frequency achievement and energy savings.

A very important target, especially in the wireless communication industry, is the achievement of increased frequency application range with a high quality factor. Furthermore as stated by Fattinger et al. [65], 'the dominant trend in mobile communication is the reduction of cost and size of the components'. The use of organic polymeric substrates instead of the standard silicon ones, would help make both goals achievable.

FBARs offer the possibility of on-chip integration, which will result in substantial volume and cost reduction [136]. When considering size and cost reduction, the use of polymer substrates, more specifically Liquid Crystal Polymers (LCP), offers an advantage. Furthermore the use of LCP adds other characteristics such as versatility due to its flexible nature, low electrical losses, low moisture absorption and high resistance to chemicals.

In recent years polymer-based electronics has become of interest as it has proven to yield increased multifunctionality. This deformable organic electronics revolution started with solar cells and displays such as Organic Light Emitting Diodes (OLED) continuing onto paperlike displays, sensitive skins, and electronic textiles [303].

The use of polymers for the MEMS industry is at the forefront in terms of novelty, especially within the RF MEMS world. From an application point of view they provide advantages due to the following characteristics: bendability, thinness, lightweight, conformability and ease of packaging.

2.2 The importance of 'flexibility'

Flexible substrates are ever so imposing in the printed circuit board industry since, through their compliance, they allow increasing circuit density [76]. The integration of thin film functional materials with flexible substrates will introduce the prospects of low cost, high volume intelligent system manufacturing.

Substrate flexibility of devices has been an important step both in the microelectromechanical system (MEMS) and integrated circuit (IC) industries. The use of polymer substrate instead of silicon, glass or sapphire, would allow the use of the fabricated devices in many environments with a wide variety of high frequency wireless sensing applications including: environmental, bio-medical, industrial (i.e. aerospace and automotive), and consumer applications (i.e. consumer tags). In the microsystems world, there is great interest to achieve high frequencies in the GHz region for different applications and, as applications expand, so does the necessity to achieve robust microwave components.

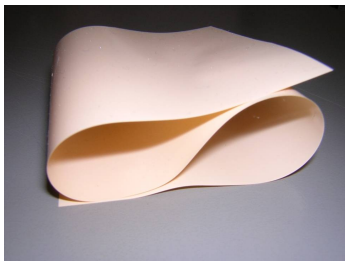


Figure 2.1: A folded Liquid Crystal Polymer substrate demonstrating its flexibility.

The turning point in this organic electronics trend was when in 1988 John Hopfield designed the first polymer memory chip. Today many researchers in the U.S. and Japan are designing nanoprocessors and transistors on polymers [126]. Hence, it can be said that, low-cost, ruggedness, light weight, versatility, unconventional form factors, high density, compactness, excellent dielectric properties and ease of manufacturability [76] of flexible internal circuitry (IC) have existed for a long time. The same is not true for the MEMS industry which is aiming to achieve similar goals.

Some examples of polymer-based IC devices are organic transistors, organic light emitting displays (OLED), sensors on foil and printed circuit boards (PCBs). Organic thin film transistors (TFT) for flexible displays and consumer tag applications using polymers including PET and polyimide were shown by Molesa et al. [194], Yuan et al. [312], Menard et al. [190], Hsu et al. [92], while a Schottky diode was produced by Liang et al. [160]. Liquid crystal displays are thin and flexible devices that use little electric power and can be used for microoptics. Molesa et al. [194] used inkjet printing for the production of an organic transistor. Lacour et al. [133] and Hsu et al. [92] created pn diodes and eye cameras on polymers showing the possibility of use of deformable substrates as

a promising approach to electronics on surfaces with arbitrary shapes. Kato et al. [112] demonstrated organic electronics for ultrasonic applications.

Since flexibility provides robustness and multifunctionality, research on polymer substrates for use in MEMS has recently started to gain attention. Substrate flexibility would allow the micro-devices to be folded and employed in many environments with a wide variety of applications including: high frequency wireless, environmental and bio-medical applications, industrial (i.e. aerospace and automotive) and consumer applications (i.e. consumer tags). Polymer-based devices will be more robust than silicon-based ones [292] since the technology enables production of light-weight, low-cost flexible electronics with high impact resistance [116]. Flexible printed circuits will allow flexible printed wiring (FPW) which has the advantages of low cost, ease of assembly, shock and vibration absorbance and 3D layout prospect [254].

The use of flexible circuitry as an assembly medium for easily providing embedded components and packages is well known [76]. The motivation to produce flexible MEMS will contribute to the direct integration of MEMS and microelectronic ICs with no use of interconnects which usually introduce unwanted parasitic effects. Embedded components have been shown to reduce parasitics [13]. Chip embedding in a multi-layer polymer packages was first accomplished in the early 90s by General Electric [282].

The direct integration of MEMS and ICs will yield what are called smart sensors, where more functions can be processed on one chip, simplifying the overall use and making the system more power efficient, reliable and accurate. In a smart sensor one can find the following components: MEMS device, microcontroller, digital signal processor, application-specific integrated circuit (ASIC), self-test, self-calibration and bus interface circuits [282].

Furthermore, the direct production of devices on polymers would facilitate the packaging process. Plastic packages offer the highest advantages, therefore having a polymer substrate as well as a polymer package would be beneficial as polymer to polymer adhesion can occur very easily at relatively low temperatures and without the need of adhesives which can lead to debonding [42] due to thermal coefficient of expansion (TCE) mismatch between layers. In fact TCE mismatch [238] can influence the adhesion between materials, hence, interfacial stresses. Using the same substrate and packaging materials would mean virtually no TCE mismatch, leading to less likelihood of interfacial stresses and delamination.

2.2.1 Polymer MEMS devices

As already discussed, the use of flexible organic substrates should drastically reduce costs [292], allow direct integration of MEMS with ICs and make packaging an easier task. MEMS devices are different from the IC ones in that the former are classified as mainly analogue, while the latter are digital components. MEMS make use of some physical principles to convert energy from one form (mechanical) to another (electrical) and vice-versa. The conversion principles

are many, the most common ones being piezoelectric, ferroelectric, piezoresistive and electrostatic.

As discussed at the beginning of Section 2.2, examples of polymer-based IC components are many. However, moving away from the digital IC industry, polymer use within the analogue MEMS domain is still in its infancy. Examples of polymer-based MEMS devices are cantilevers using SU8 polymer [106] and using PET [317] characterised by their bio-compatibility and high sensitivity. Tactile sensor arrays [62], electrostatic polymer microactuators [192] and a differential pressure sensors [131] have all been fabricated on polyimide.

Although not extensively, ceramics have also been integrated with polymers to create devices. PZT was attached to a polymer base using an adhesive to create ultrasonic transducers for sonodynamic therapy [309]. A micropump was created by attaching PZT to PMMA using epoxy resin [134].

Advantages of polymers over silicon are:

- Low cost given by the fact that silicon wafer fabrication is complex, while polymer is easily produced. Price estimations for 4 inch wafers: silicon price £20-40, Liquid Crystal Polymer from Rogers Corporation price £3.
- Flexibility for application in conformal circuits giving the possibility to reduce overall component size and weight and allowing system-on-a-package and 3D multi-layer integration [13].
- Low bonding temperature which allows ease of package through lamination. Packaging could be done by eventual lamination at glass transition temperature of the polymer (Tg), thus eliminating the vapour/water outgassing problem of the extra adhesive layer normally used in traditional packages. This way reliability of the overall MEMS can increase.

Disadvantages of polymers over silicon are mainly caused by low rigidity (Young's modulus) causing fabrication complications. Flexible devices experience variable stresses during the manufacturing process that may lead to substantial change in curvature. This leads to a change in the size of the work piece and ultimately to misalignment between different layers of the device [78]. Low rigidity also causes film strain development in the structure by built-in stresses in the deposited layers upon heating and cooling down [78].

2.2.2 Polymer MEMS fabrication methods

Due to the different characteristics of polymers as compared to silicon (i.e. chemical composition, temperature properties, mechanical and wetting assets), silicon-based surface micromachining techniques are not directly applicable to polymer processing [52], although some traditional MEMS methods can still be employed. Handling of flexible organic substrates requires the development of novel processes or suitably modified MEMS production processes that keep in consideration the low temperature tolerances and low rigidity of the polymer.

The new fabrication methods can combine processes used by MEMS and IC industries.

Manufacturing of devices on polymer typically involves roll-to-roll processing, inkjet printing and electrohydrodynamic printing [218] for printed electrodes, and screen printing , photoimaging and stamped circuitry [76] for patterning along with milling and laser machining for material removal.

Polymer electronics can be used with high density technologies, which lead to lightness and cost-effectiveness, such as Surface Mount Technology (SMT) [76]. SMT is a method for producing electronic circuits where, unlike through-hole technology, the components are mounted directly onto the surface of printed circuit boards (PCBs). Known SMTs are: Surface Mount Assembly (SMA) and Tape Automated Bonding, Gilleo [76]. The former is a package technology, while the latter allows direct connection of ICs and MEMS to circuits through what is called Tape Automated Bonding (TAB). Here chip bonding sites (i.e. gold solder bumps) can be bonded directly to the patterned conductors eliminating the use of wires [76].

Special UV-curable backbone-type polymers have been used to create 3D microactuators in polymer structures [96], [285], [284], [270]. The first group used a technique named IH Process (integrated hardened polymer stereolithography), while the other three groups used micromachined silicon moulds to obtain photoforming (or hybrid processing). Varadan et al. [283] used two types of polymers namely structural and sacrificial for micromachining of polymeric MEMS devices where the sacrificial polymer was an acrylic resin dissolvable in caustic soda.

Standard MEMS fabrication techniques for device creation on polymer substrates was carried out by Engel et al. [62] who created a tactile sensor array on polyimide, Liao et al. [161] who integrated functional materials directly onto PCBs for compact portable microelectronics and embedded systems, Kuoni et al. [131] who used standard RF sputtering of ZnO on polyimide for pressure sensor fabrication and Chen et al. [38] who created a shunt switch. The groups mentioned above all used standard micromachining techniques such as metal sputtering, photolithography and RIE etching to create their devices.

When employing standard MEMS fabrication techniques, though, the main challenges imposed by device production on organic polymer substrates are material handling and dimensional stability [76]. The many advantages that their low rigidity gives can, in fact, cause manufacturing challenges. The handling issue can be solved by "rigidising" it either through carrier frame mounting or rigid surface adhesion [76]. Polymers can be easily etched through CF_4/O_2 plasma in RIE as Chinoy [40] have also shown for benzocyclobutene (BCB) polymer removal.

2.2.3 The choice of polymers

The main interest within flexible substrates for IC and MEMS applications has been within the polymer domain and, more specifically, in thermoplastic polymers. Thermoplastics are those plastics that melt if they reach a specific melting temperature when heated. So far polyethylene terephthalate (PET), Kapton® polyimide (PAI), polytetrafluoroethylene (PTFE), polyetheretherketone (PEEK), polymethyl methacrylate (PMMA) and polystyrene (PS) have been the most widely employed thermoplastics.

However, in recent years, the development of Liquid Crystal Polymers (LCPs) among the thermoplastic family has gained considerable attention and become of great interest in the microelectronics industry mainly due to their excellent electrical characteristics. Low dielectric constant and dielectric loss make LCP a desirable candidate for high frequency substrate applications. Table 2.1 shows some thermoplastic polymers and their properties.

Table 2.1: Comparison of the properties of some typically used polymers

Polymer	**LCP**	**Polyimide**	**PET**
Melting point(°C)	315	-	260
Tensile strength (MPa)	200	231	320
Poisson's ratio	0.45	0.34	0.37-0.44
Modulus of elasticity (GPa)	2.255	2.5	2-4
Coefficient of thermal expansion (ppm/°C)	17 (tailorable)	20	20-80
Other characteristics	low moisture absorption (hermetic)	high moisture absorption (non-hermetic)	-

Liquid Crystal Polymer (LCP)

LCP is a white, opaque thermoplastic polymer containing densely-packed self-reinforced fibrous polymer chains called copolymer molecules (chemical organic structure shown in figure 2.2 a)). It is a class of partially crystalline aromatic polyester polymers based on p-hydroxybenzoic acid and was first produced in the 1970s [201] (material crystallinity shown in figure 2.2 b)).

The material has outstanding mechanical properties at high temperatures, tailorable coefficient of thermal expansion, excellent chemical resistance, inherent flame retardancy, low dielectric loss and good weather ability [95]. Its high hermetic properties make it adequate for incorporation in chemically harsh and wet environments [290]. LCP has excellent chemical resistance and is dissolved only in bis-trifluoromethyl phenol (i.e. Bayer 99%) [269], and potassium hydroxide (KOH) [177]. Due to these outstanding mechanical, thermal and electrical assets it is the preferred polymeric material to be used as a substrate as long as

the MEMS do not involve optical requirements.

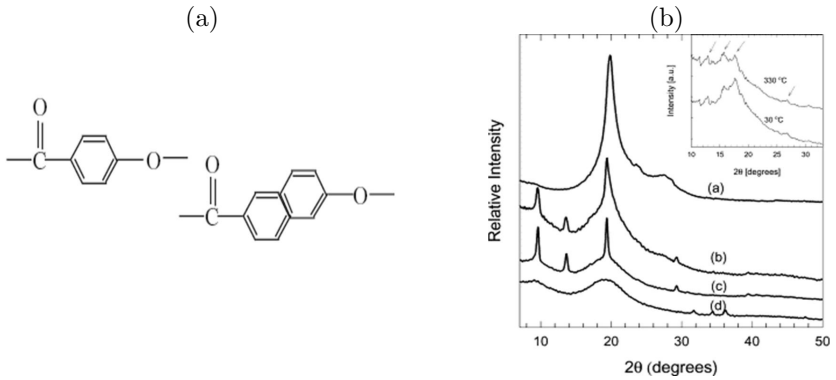


Figure 2.2: a)LCP chemical structure taken from Narushima et al. [201], b) XRD spectrum of LCP showing cristallinity peak at 20° taken from Lee et al. [145].

The creation of devices directly on LCP would erase, among others, the future problem of packaging interfacial delamination caused by the presence of dissimilar material systems since the package can also be made of LCP. Different thermal expansion coefficients in packages can compromise the adhesive integrity of the interfaces [265], therefore an all-LCP device and package would be desirable because LCP can be bonded to LCP through a simple lamination process with no need for adhesives. Other reasons for the attraction of an all-LCP device and package are the LCP's low absorption, therefore its excellent hermetic sealing properties, and also the elimination of the thermal coefficient of expansion (TCE) mismatch problem.

The use of LCP as a substrate for MEMS device development provides many advantages and some disadvantages with respect to the use of any other polymer choice.

Advantages

- Low dielectric constant, minimal dispersion in permittivity and low dielectric loss factor over the functional frequency range of 1kHz-110GHz [46].
- Good hermetic properties and low water absorption (0.04%) [46].
- Low and tailorable thermal coefficient of expansion [13].
- High resistance to chemicals and biocompatibility within the human body [13].
- Superior cost to performance index (low cost) surpassing FR-4 and ceramics [13].
- Resilience (not brittle).

- Ease of processing for packaging elements.
- Multilayer 3D vertical integration capability and good mechanical properties [51][53].
- Compatibility with sequential build-up process in a PCB foundry [13].
- High crystallinity of LCP results in high creep resistance (low creep) compared to other polymers [181] and leads to low plastic deformation under load.

Disadvantages

- Although flexibility is one of the main reasons for using LCP or polymers in general, this variable can be a disadvantage when processing since the manufacturing equipment is tailored to comply with flat, rigid substrates.
- The initial roughness on most LCP substrates largely deviates from the ideal of standard Si substrates (∼0.0045nm). Roughness of LCP is an unwanted feature and has been previously noticed by Gould et al. [80] who reported that small amorphous particles in the form of granules with diameters in the 0.16 to 0.40nm range decorated the surface of Vectra-A, while on the Vectra-B surface short rods which increased the surface roughness to 9.6nm were noticed. Suga et al. [262] studied the Cu/LCP interface after bonding showing that the Cu/LCP lamination causes the interface roughness to increase to 970nm when heat laminated and to 64nm when surface activated bonding (SAB) process.

LCP-based MEMS

Miniaturization with increased functionality at reduced cost has historically been the key driver for the evolution of electronics products on polymers [13] and liquid crystal polymer (LCP) proves to be a promising material for low-temperature and low-cost-large-format processing on an organic platform, maintaining superior RF performance in the mm-wave range [13].

Since LCP has advantageous electrical, mechanical and chemical properties, it will be the preferred polymer in our experiments. Electric properties of LCP were found to be advantageous through characterization method, where coplanar waveguides were produced on LCP for RF applications [275]. The polymer has the unique ability to perform as a substrate, dielectric, and sealant for multilayer 3D construction, therefore, an all-LCP package can be easily realized [13]. Embedded devices in LCP have been realized by a lamination process with cut-out cavities, as well as by a liquid polymer molding process [13].

Some of the earliest devices created with LCPs were flexible liquid crystal display devices [237], which used very little electric power. Examples of more recent LCP devices are: resistive temperature devices and electrode-cell conductivity sensors [23], MEMS humidity sensors Dean et al. [51], capacitive pressure sensors Palasagaram and Ramadoss [213], DeJean et al. [53], antenna arrays for

remote sensing systems [53], cantilever and membrane structures with transferred PZT used for microvalves in microfluidics [67], environmental sensors using a maskless method [70], coplanar waveguides for RF applications [275], microfluidic channels along-side tactile, flow and resonator-like beam sensors [62], Engel [61]. Ramadoss et al. [226] produced an RF shunt switch employing printed circuit board methods (or PCB-MEMS) using Kapton as the bridge.

Standard fabrication techniques, including pre-processing step additions, have been employed and slightly modified to adapt to polymer-fabrication. Due to polymer substrate compliance, there can be processing complications which have been overcome by rigid backing methods. Wang et al. [292] suggested that before fabrication the LCP film should be attached to a solid surface (i.e. silicon) with a dissolvable adhesion layer (i.e. photoresist), in order to eliminate warpage of the flexible polymer during fabrication. Furthermore roughness of LCP must be minimized or eliminated, and literature has shown CMP to be a popular method.

Key technical challenges for LCP-based MEMS manufacturing have been patterning and metallizing the LCP film. For patterning several methods have been used such as mechanical drilling, punching, plasma etching and laser ablation, for via and other feature formation in LCP. However, these processes require expensive equipment set apart from the main production line and LCP circuits made using these methods can become very costly [308]. Roll-to-roll processing has also been carried out for device fabrication on LCP [125].

Standard processing methods such as metal sputtering and evaporation and photolithography (including lift-off) have already been applied. Ti(50nm) and Au(100nm) have, so far, been the preferred metals due to their biocompatible nature [52]. Lift-off has previously been carried out with the use of LOL2002 negative-tone and Shiplay 1813 positive-tone photoresists [37]. Hess et al. [88] tried lift-off with a AZnLOF2035 negative-tone photoresist bi-layer.

The properties of LCP and the effects of cold plasmas have been investigated concluding that argon (Ar) ion bombardment and oxygen exposure activate the polymer's surface by increasing its wettability. Oxygen plasma, with altered power, can etch the LCP surface and the etch rate greatly increases with addition of CF_4 fluorocarbon [52]. For LCP oxygen plasma etching (etch rate=0.22-0.27μm/min), aluminium (Al) has been successfully employed as a mask [292]. Wet etching of LCP has also been carried out with 46% KOH at 60°C for pattern creation [51].

For packaging purposes LCP lamination and intermetallic flip-chip bonding have been investigated by Dean et al. [51] who proposed RF MEMS switches packaged in chip-on-flex modules by using LCP lamination process and intermetallic flip-chip bonding. The lamination process avoids both extra bonding layer usage, which causes outgassing of the organic materials, and high temperature procedures [38]. Thanks to the ease of LCP/LCP adhesion achievement through this simple low temperature process, the material has already been used to create packaged devices.

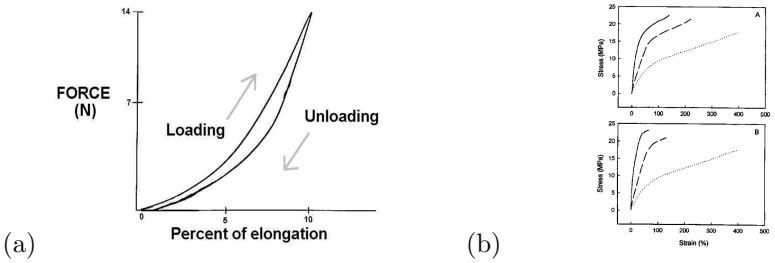
2.2.4 Polymer mechanical properties relevant to MEMS

Since polymers behave differently from rigid silicon substrates, the knowledge of their mechanical behaviour is of relevance if they are to be used as substrates in the MEMS and IC industries.

Polymers can be classified as viscoelastic materials according to their response to a loading condition. A viscoelastic material is one whose response continues to change over time even after the load is removed [19]. Viscoelastic behaviour under uniaxial tensile stress experiences the following phenomena: creep, recovery and relaxation. Creep and stress relaxation describe the non-linearity in polymers and viscoelastic materials in general.

A viscoelastic substance loses energy when a load is applied and removed, therefore it has a non-linear (or non-Hookean) behaviour. The loss of energy is represented by a hysteresis loop in the stress-strain graph (see figure 2.3 a)), where the area of the loop is equal to the energy lost during the loading cycle [191]. The lost energy causes plastic deformation. Hysteresis, however, is not an issue for the LCP-based FBAR devices we will develop since the viscoelastic polymer is not an active part of the device. When fabricating structures such as cantilevers and bridges, the above-described hysteretic behaviour would be of relevance.

Stress-strain behaviour of non-linear viscoelastic polymers shown in figure 2.3 b).



(a) (b)

Figure 2.3: Stress-strain graph of viscoelastic material a) when loading and unloading (from Meyers and Chawla [191]), b)without the unloading step (from Lee et al. [142]).

Creep, recovery and relaxation

A characteristic feature of polymers is the way in which their response to an applied stress or strain depends on the rate, temperature or time period of loading [206]. The behaviour of polymers under constant load (creep and recovery) is known and is represented by a strain-time graph (see figure 2.4).

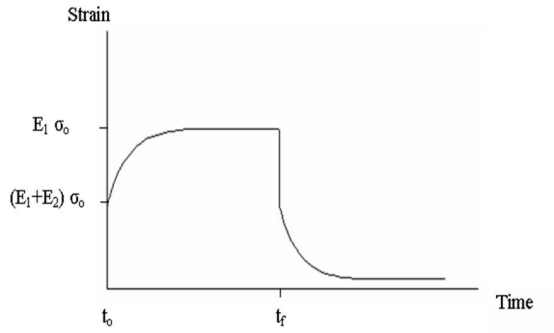


Figure 2.4: From Junisbekov et al. [109] Creep and recovery behaviour in viscoelastic materials represented in strain vs time graph.

Figure 2.4 shows constant stress σ_0 being applied from t_0 to time t_f between which creep behaviour is evident. For times greater than t_f the load is removed and we can see stress recovery. E_1 and E_2 refer to the spring constants of the elastic elements of the model.

Creep is a phenomenon which describes how polymers strain under constant stress and is plotted as strain VS time. Creep is the tendency of a solid material to slowly move or deform permanently under the influence of stresses as parts of the long polymer chain change position. It can be measured in various ways including continuous stiffness measurement based on nanoindentation system [158] or tensile testing method. The general creep equation is [191]:

$$\frac{d\epsilon}{dt} = \frac{C\sigma^m}{d^b} \cdot e^{\frac{-Q}{kT}} \tag{2.1}$$

where ϵ is the creep strain, C is a constant dependent on the material and the particular creep mechanism, m and b are exponents dependent on the creep mechanism, Q is the activation energy of the creep mechanism, σ is the applied stress, d is the grain size of the material, k is Boltzmann's constant, and T is the absolute temperature.

Recovery is the reduction of inelastic (plastic) strain with time after load has been removed [19].

Stress relaxation describes how viscoelastic materials, relieve stress under constant strain. In other words it is the reduction of stress with time while the total strain remains constant [19].Stress relaxation is described by equation 2.2 [109].

$$\sigma_{relaxation}(t) = \frac{\sigma_0}{1 - [1 - \frac{t}{t*}(1^{1-n})]} \tag{2.2}$$

σ_0 is the maximum stress at the time t* the loading is removed, and n is a material parameter.

Necking

Necking is a common polymer and, more generally, viscoelastic and ductile strain mode which leads to material failure. Here large amounts of strain localize in a small region of the material leading to a decrease in local cross-sectional area. During uniaxial tension tests, most engineering polymers deform (with necking) inhomogeneously at relatively small strains i.e. ~ 1.2 engineering strain Fang et al. [64].

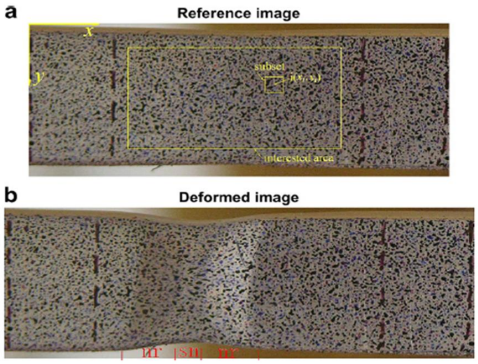


Figure 2.5: Necking of polycarbonate (PC) polymer [64]

Figure 2.5 shows how a polymer e delocalizes (moves) under constant stress before breaking. This means that rupture strain is high.

2.3 Electromechanical principles and Radio Frequency (RF) MEMS

Microsystem devices work on the basis of sensing and actuating through the employment of one or a combination of some basic physical principles. RF MEMS are combined with specific materials (functional materials) in order to exhibit electromechanical conversion and, therefore, to become capable of sensing or actuating mechanisms. Functional materials are usually ceramics although in recent years other smart materials have been investigated and exploited (even polymers).

RF MEMS, also called microwave MEMS, encompass devices operating in frequency regions 3MHz-300GHz while high frequency (HF) devices are a subgroup of RF ones ranging from 3MHz-30MHz [75]. As the requirement for wireless communications and protocols increases, microwave communication systems become important.

The high frequency technology revolution started with personal communication devices such as mobile phones, Global Positioning Systems (GPS), Wireless Local Area Network (WLAN) etc., but it is steadily expanding into other areas. Wireless technology, in fact, is not limited only to the consumer electronics sector, it is entering new areas such as: medical [119], environmental [311], power generation (energy harvesting) [104], automotive (with pressure sensors and accelerometers [5]), industrial (i.e. microrobots) [310], medical (i.e. imaging) [288] [224] and telemetric (i.e. RFID wireless systems for outside world communication) [107].

Miniaturization is what made the wireless phenomenon take flight. This is due to a simple rule of resonance frequency being inversely proportional to device size, which is also one of the reasons why in MEMS thin films are preferred over bulk materials. RF MEMS can be classified into active and passive components.

Active MEMS include microwave actuating switches [137], which is what started the RF MEMS technology development for microwave applications, and RF components encompassing: RF tunable capacitors [219], standard switches [205], comb-drive relay structures [247]. The advantages of these devices over their IC counterparts are many including high insertion loss elimination [219], improved isolation, broader range of operating frequencies and more linearity.

Passive devices include resonators, filters, transmission lines, phase shifters and antennas while active components encompass switches, amplifiers, mixers and varactors. Their role is essential in redirecting and/or filtering signals. Nowadays we are facing the challenge of developing low cost and low loss passive components for microwave and radio frequency applications. These low loss resonators and filters would improve the conception of active devices, and seek to reduce interconnection and packaging problems [186]. Passive elements are critical for wireless applications. High quality factor (Q), low loss, low cost and high performance RF passive components, such as resonators, filters and transmission lines are necessary as they need to be integrated with existing active components.

2.4 Film Bulk Acoustic Resonators (FBAR)

In the wireless telecommunication world, film bulk acoustic wave resonator (FBAR) bandpass filters for microwave frequency applications are very promising for use as RF MEMS filters since they can be combined to make up duplexers (transmitter/receiver modules). The FBAR will, therefore, be the chosen device in this study as an example of high frequency MEMS with thin film functional ceramic on polymer targeted for use in the ever growing wireless communica-

tions industry.

Before FBARs came into market some of the most common component architectures for bandpass signal filtering were: quartz crystal (low frequency ∼32kHz), Surface Acoustic Wave (SAW) and Bulk Acoustic Wave (BAW). Alongside Quartz Crystal Microbalance (QCM) and Surface Acoustic Wave (SAW), FBARs are a class of acoustic wave devices.

In recent years SAW and FBAR have been the most popularly used with the latter technology replacing also the former one thanks to its size reduction and higher frequency capability [63]. FBAR components offer small sizes, low cost, high quality factor, large power operation and compatibility with silicon low-cost process, enabling mass production and filter integration on above-IC processes [245]. All of these qualities make them good candidates for replacing more traditional filter technologies such as SAW and ceramic.

Electromechanical conversion in these devices is achieved through the piezoelectric phenomenon (explained in detail in section 2.4.2) whereby an applied voltage causes a physical stress and deformation of the material (direct effect) or, vice-versa, where a mechanical stress generates charge (converse effect). It is the electro-acoustic wave transduction principle that allows the use of such devices as filters, oscillators and transformers. Acoustic properties are determined by the intrinsic material parameters (i.e. density, elastic moduli) and geometric values (i.e. layer thickness)[174].

2.4.1 FBAR background and application

FBAR devices first appeared in the literature in the early to mid 1980's and, over the past years, they have gained mainstream interest and exploitations especially as RF filters for wireless networks within the following applications: cellular phone, satellite communication and wireless local area networks.

In 1989 by K.M. Lakin started the commercialization of the first FBARs with his TFR Technologies company, followed by Agilent in 1994 leading to an estimated number of fabricated FBARs per year of three billion in 2002 [136]. FBAR technology in the form of PCS duplexers first showed up in cell phones in 2001 [234], hence, the technological application is very new.

The functional part of an FBAR is made of a metal/piezoelectric/metal multilayer and its operation principle and preferred materials will be later described. The devices can be integrated with active devices without chip interconnects [233] which means better overall performance. The appeal of FBARs lies in their high frequency operation (1-16 GHz), very high quality factor (up to 1500), large signal handling capability up to several Watts (3W)[87] and compactness [195].

There are various types of FBARs, the most popular ones being:

- Membrane type FBAR with etched back and supported by the edge of the

structure (see figure 2.6 a).

- Air-gap type with a void gap under the resonator (see figure 2.6 b).
- Solidly mounted resonator (SMR) which has a Bragg reflector part generally made up of multiple alternating layers of both low and high acoustic impedance materials [127] (see figure 2.6 c).

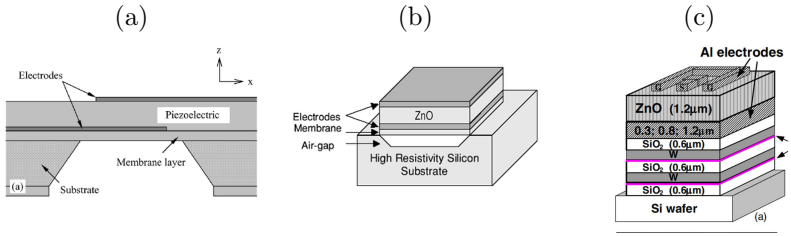


Figure 2.6: a)Free-standing FBAR from Southin and Whatmore [251], b) air-gap type FBAR resonator from Coventor [48], c)solidly mounted Bragg type FBAR from Pham et al. [221].

Throughout my project I will consider the membrane type FBAR (figure 2.6 a)) as it has low dielectric loss within the substrate, and low overall power loss.

The different FBARs all work on the same fundamental principle based on a traveling acoustic wave in a confined structure [173]. However the type of reflecting surfaces is different as in the membrane and air-gap type FBARs, it is air while in the SMR it is the Bragg reflector. The layer impedances, acoustic velocities, densities and thicknesses dictate the traveling wave's behaviour.

The effect of additional layers such as the metal electrodes causes medium nonlinearity [4] which leads to mechanical losses (acoustic attenuation), and spurious modes (2nd or higher order resonances also called harmonics). Hence, the non-piezoelectric layers are made extremely thin in order to reduce the acoustic attenuation and suppress the even harmonics caused by non-symmetric acoustic energy distribution along the thickness direction of the piezoelectric layer [215].

Impedance matching and apodization (changing geometry of device such that it does not have parallel side edges) also help in unwanted resonance elimination.

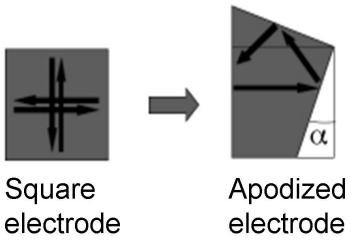


Figure 2.7: Square and apodized FBAR geometry from [77].

Since their introduction in the 1980s, FBAR applications have expanded. Some of the most common FBAR applications include.

- Low noise and balanced oscillators replacing electronic oscillators due to their better frequency stability which, in turn, is given by their higher Q (10 times higher) [3],[7].
- Voltage controlled oscillators (VCO) [214].
- Bio/gas sensors [73].
- Filters for mobile phones and GPS f$\geq$1GHz.
- Low-frequency RFID systems from 30-500kHz and high-frequency RFID tags in the following ranges: 13.56MHz, 850-950MHz and 2.4-2.5GHz. RFID are used for: logistics, asset tracking, equipment movement and traceability, item visibility and status, anti-theft evidence, authentication, manufacturing, calibration maintenance, healthcare, personnel identification, payment systems.

FBARs can act as coupled resonator filters when arranged in particular topologies to act as narrow bandwidth, high-Q two-port filters. One such topology is the ladder configuration (see figure 2.8 a)). They are very adequate for wireless components and remote sensing domains as they work in the gigahertz frequency ranges.

The ladder-arranged FBARs are being commercially used as duplexers (receivers and transmitters) applied for bandpass filtering at 1-2GHz, although higher frequencies can easily be achieved by varying various physical parameters such as, for example, the functional material's thickness [216].

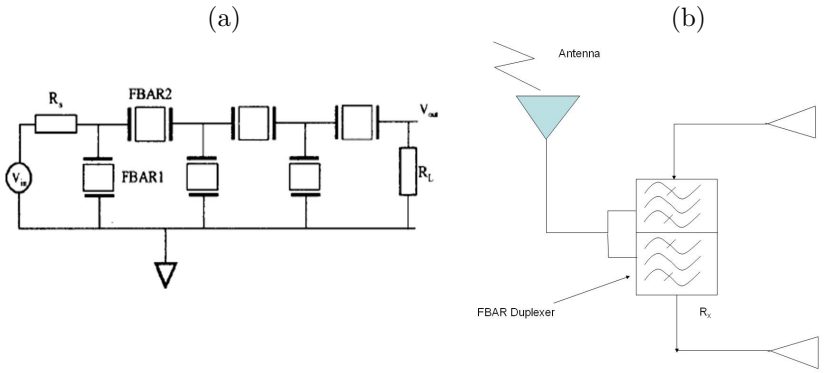


Figure 2.8: a)Ladder filter arrangement of FBARs from [259], b)FBAR implemented as a duplexer in an RF front-end device just after the antenna.

Standard fabrication of FBARs comprises metal deposition, piezoelectric material sputtering, patterning and bulk etching. The final FBAR device, therefore, consists of a free-standing piezoelectric layer sandwiched between top and bottom electrodes. The fabrication process flow is shown and described in Appendix A..3.

2.4.2 FBAR materials and principles

As we have already described, FBARs are made up of a piezoelectric layer sandwiched between two thin metal electrodes. The preferred metal electrode material is usually gold (Au). The favourite piezoelectric material candidates for standard FBAR production are Zinc Oxide (ZnO) and Aluminium Nitride (AlN) owing to their relatively low temperature growth (up to 250°C) and excellent electromechanical characteristics. However Lead Zirconium Titanate (PZT) has also been used in the past as the functional piezoelectric layer for FBARs [260], [122].

Piezoelectric thin films

Piezoelectric thin films are functional materials (usually ceramics) which allow electro-mechanical conversion. Piezoelectric materials have been used extensively in actuator and ultrasonic receiver applications [229] due to their high frequency characteristics. Piezoelectric MEMS applications vary from pressure transducers, force sensors, speedometers and accelerometers [18], hydrophones [207] and microphones [151]. [282]. Advantages of piezoelectric MEMS are that: it requires low power, has large output forces and has good signal to noise ratio [51].

Common piezoelectric ceramics are Aluminium Nitride (AlN), Zinc Oxide (ZnO) and Lead Zirconium Titanate (PZT). Among these we have chosen to use ZnO as a result of its high electrical resistivity [257], low dielectric constant and low loss. ZnO is an anisotropic crystalline piezoelectric semiconductor excellent for

resonator applications and has attracted great interests due to its ease of fabrication and low preparation temperature (up to 250°C) [97], [168], [294].

For a sputtered piezoelectric material such as AlN and ZnO, columnar direction/angle depends on incident angle between source and substrate and for high piezoelectric film coupling factor and piezoelectric constant it is important to have c-axis orientation perpendicular to substrate surface throughout the whole substrate. This is because the piezoelectric coupling constant is along this c-axis. Hence c-axis orientation and intensity dictate the piezoelectric coefficient quality (d_{33}) in the z direction. A 17° misalignment from normal, for instance, can reduce the coupling coefficient to half its potential value [89]. Figure 2.9 shows the c-axis orientation in the <002> plane.

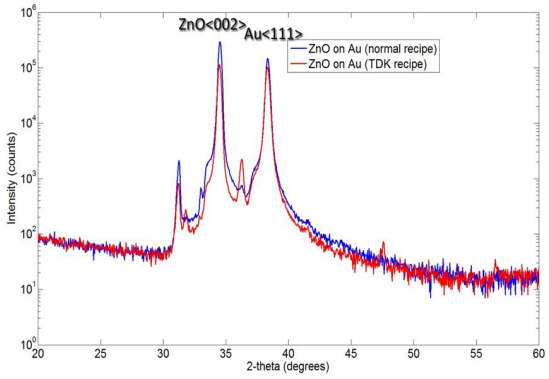


Figure 2.9: XRD plots of ZnO grown on 8nm Ti and 100nm Au deposited with normal and higher power recipe. Standard ZnO c-axis peak shows at ∼35° [Courtesy of Carlos Fragkiadakis].

The ≺002≻ oriented ZnO film provides a pure longitudinal mode. Hence the thin film is preferentially grown with excellent c-axis orientation in order to excite this pure thickness longitudinal mode. The unique physical properties of ZnO films that make it ideal for FBAR devices are its high frequency characteristics, large Q value as well as high piezoelectric constant [147]. Piezoelectric films of ZnO materials have stable dielectric constant (8.8), large Q value, high piezoelectric coupling coefficient (7.5%), high acoustic coupling (0.28), low insertion loss ∼0.4dB and suitable acoustic velocity (6330 m/s) [115]. Due to their large electromechanical coefficient, ZnO films are regarded as one of the most efficient ultrasonic transducers [97]. Table 2.2 shows some properties of the thickness extensional mode of ZnO ≺002≻ taken from [302].

Table 2.2: ZnO ≺002≻ properties from Wu et al. [302].

Acoustic velocity ($\mathbf{V}_a$) ($\mathbf{m/s^2}$)	**Coupling coeff.** ($\mathbf{k}_{eff}{}^2$) (%)	**Density** (ρ) ($\mathbf{kg/m^3}$)	**Dielectric constant** (ε)
6269	8.08	5720	8.6-10

Piezoelectric effect

This electromechanical phenomenon, first discovered in 1880 by Jaques and Pierre Curie, provides direct electro-mechanical coupling, has a wide range of application frequencies (mHz to 100GHz), requires low power, has large output forces and good signal to noise ratio [141]. Piezoelectric materials have strong coupling between mechanical displacements and electrical loads (and vice versa). A piezoelectric can use the direct or the converse effect depending on whether it is used as a transmitter (direct) or a receiver (converse). Figure 2.10 shows the direct and converse effects.

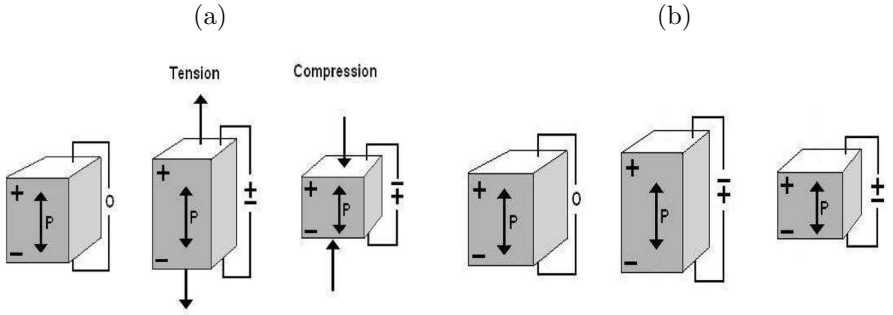


Figure 2.10: Piezoelectric effect: a)direct (transmitter) b)converse (receiver). Taken from Piezo-Optics [222].

Stress-strain relationship and electrical effects in a piezoelectric when the material is used as a receiver can be represented by equation 2.3 [229], while when used as transmitter it can be described by 2.4. Both of these equations are in the tensor format.

$$S = s^E T + dE \tag{2.3}$$

$$D = eS + \epsilon^S E \tag{2.4}$$

Where S is the strain, s^E is the compliance at constant electric field, T is stress, d is the piezoelectric coupling coefficient tensor which gives displacement when an electric field is applied, E is the electric field, D the electric displacement, e

is the piezoelectric constant, ϵ^S is the electric permittivity at constant strain.

We can expand the tensor format of equations 2.3 and 2.4 in matrix format where the vectorial components [229] take account of directional effects.

$$\begin{vmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ S_5 \\ S_6 \end{vmatrix} = \begin{vmatrix} s_{11} & s_{12} & s_{13} & & & \\ s_{12} & s_{11} & s_{13} & & 0 & \\ s_{13} & s_{13} & s_{33} & & & \\ & & & s_{44} & & \\ & 0 & & & s_{44} & \\ & & & & & 2(s_{11}-s_{12}) \end{vmatrix} \begin{vmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{vmatrix} + \begin{vmatrix} 0 & 0 & d_{13} \\ 0 & 0 & d_{13} \\ 0 & 0 & d_{33} \\ 0 & d_{15} & 0 \\ d_{15} & 0 & 0 \\ 0 & 0 & 0 \end{vmatrix} \begin{vmatrix} E_1 \\ E_2 \\ E_3 \end{vmatrix}$$

$$\begin{vmatrix} D_1 \\ D_2 \\ D_3 \end{vmatrix} = \begin{vmatrix} 0 & 0 & 0 & 0 & d_{15} & 0 \\ 0 & 0 & 0 & d_{24} & 0 & 0 \\ d_{31} & d_{32} & d_{33} & 0 & 0 & 0 \end{vmatrix} \begin{vmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{vmatrix} + \begin{vmatrix} \epsilon_{11} & 0 & 0 \\ 0 & \epsilon_{22} & 0 \\ 0 & 0 & \epsilon_{33} \end{vmatrix} \begin{vmatrix} E_1 \\ E_2 \\ E_3 \end{vmatrix}$$

The numbers represent the directions in the folllowing way:

$$\begin{array}{ccc} 1 & 6 & 5 \\ xx & xy & xz \\ & 2 & 4 \\ & yy & yz \\ & & 3 \\ & & zz \end{array}$$

Note that crystal symmetry determines whether a coefficient is nonzero, hence, the matrices are not fully populated. For ZnO, for example, the piezoelectric crystal is of 6mm symmetry Dua et al. [56] and since most FBAR applications require the piezoelectric layer to operate in the thickness extensional mode (d_{33}) the ceramic's preferred direction is along z-axis only, hence d_{33}, d_{13} and d_{15} are nonzero (also, again by symmetry,$d_{13} = d_{23}$ and $d_{15} = d_{25}$) [229].

The thickness extensional mode (d_{33}) of a piezoelectric material is the preferred one as it has the maximum electromechanical coupling coefficient (k_t^2) [108]. This parameter measures the efficiency of the piezoelectric material and is calculated at constant electric displacement (D) through equation 2.5.

$$k_t^2 = \frac{E_m}{E_e} = \frac{e^2}{c^D \epsilon^S} \tag{2.5}$$

Where E_m is the energy stored mechanically and E_e is the energy stored electrically, ϵ^S is the dielectric constant at constant strain, e is the piezoelectric stress constant and c^D is the stiffness coefficient at constant electric displacement.

2.4.3 FBAR operation and performance

FBARs operate through what are called the direct and the converse effects whereby the piezoelectric is excited through mechanical stress which then converts into an electrical response (direct piezoelectric effect) or viceversa (converse piezoelectric effect). In order for this conversion to take place, though, there must be signal transmission. This happens through metal paths (transmission lines) specifically tailored for the purpose.

Once the FBAR device is operating, its performance is dictated by many parameters such as: resonant frequency (f), quality factor(Q), coupling coefficient (k^2_{eff}), insertion loss and Figure of Merit (FoM). These FBAR variables are highly related to the quality of both the piezoelectric and electrode materials [24].

Signal transmission

Most RF MEMS make use of metal conductive paths to transmit and receive signals. These are called transmission lines and they are essential in communications technology as they provide electrical signals that are then used for electromechanical conversion by any RF component. Coplanar waveguides (CPWs) are a particular type of transmission line used for FBAR technology as they enable high frequency communication due to their Ground-Signal-Ground (GSG) configuration. The grounding is needed in order to keep signal integrity as it rejects common-mode noise signals (electrical interference with reference to the common or ground wire).

Coplanar waveguides are ideal for contact with RF devices because they avoid the introduction of stray inductances, which are usually caused by wire bonds. Furthermore CPWs facilitate high frequency transmission measurements, which are carried out with GSG probes, through S-parameter performance measurement. There are two fundamental modes in CPWs, namely even mode and odd mode.

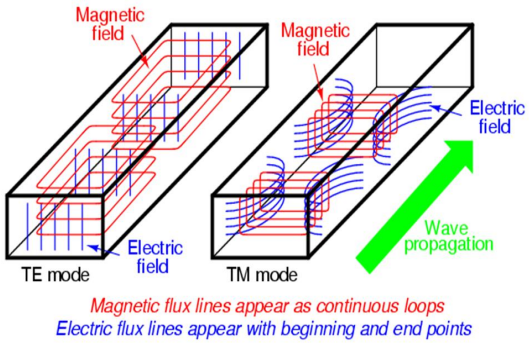


Figure 2.11: CPW de-coupled electromagnetic field representation from [258]. Electric field is transverse while magnetic field has a longitudinal component.

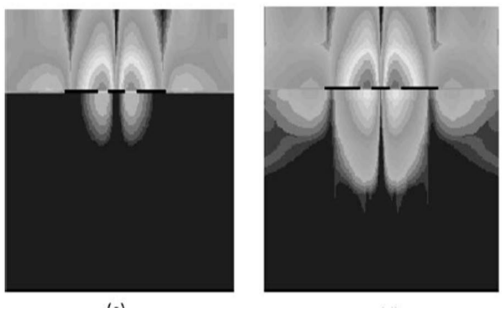


Figure 2.12: Substrate electric field penetrations in CPW structures [140].

Acoustic wave propagation

Because we are talking of acoustic devices, wave propagation parameters are essential. Given specific boundary conditions, there are various ways to solve for wave propagation within a medium depending on how many dimensions are considered. For the 1 dimensional case a simple lumped element analysis with Mason model is enough, while for the 3 dimensional case the Christoffel equation is employed. The latter will not be discussed as, for FBAR analysis purposes, we are only interested in one dimension, namely the thickness longitudinal mode.

The wave propagation parameters are of interest for the development of a one-dimensional model description of electrical characteristics for an acoustic structure. Consider a finite slab with plane boundaries z=z1 and z=z2 as shown in figure 2.13.

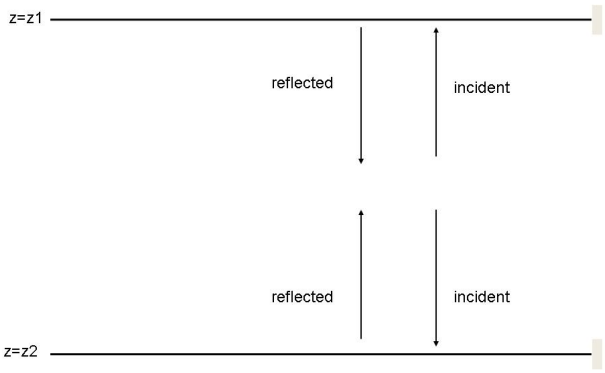


Figure 2.13: Finite thickness acoustic medium with right and left propagating plane waves and plane boundaries z1 and z2.

At each boundary of the slab there are incident and reflected waves. The interaction of these waves causes the resonance conditions that alter the electrical characteristics of the acoustic devices [230]. Particle displacement is given by u in equation 2.6 [230].

$$u = ae^{-jkz} + be^{jkz} \tag{2.6}$$

Where the a and b wave coefficients depend on the acoustic impedance mismatch at the boundaries. The particle velocities at the upper and lower boundaries are respectively represented by equations 2.7 and 2.8 [230].

$$v_1 = j\omega(ae^{-jkz_1} + be^{jkz_1}) \tag{2.7}$$

$$v_2 = j\omega(ae^{-jkz_2} + be^{jkz_2}) \tag{2.8}$$

Solving for coefficients a and b in terms of particle velocities v_1 and v_2 gives equations 2.9 and 2.10 [230].

$$j\omega a = \frac{v_1 e^{jkz_2} - v_2 e^{jkz_1}}{2jsin(kd)} \tag{2.9}$$

$$j\omega b = \frac{v_2 e^{jkz_1} - v_1 e^{jkz_2}}{2jsin(kd)} \tag{2.10}$$

Force at the boundaries is represented by equation 2.11, while the characteristic layer impedance is given by equation 2.12.

$$F = Acv \tag{2.11}$$

$$Z = \frac{ckA}{\omega} \tag{2.12}$$

Where A is the area c is the relevant stiffness of the propagating mode (in our case longitudinal) v is the layer's acoustic wave phase velocity and k the wavenumber (k=$\frac{\omega}{v}$). Substituting 2.7 and 2.11 into 2.12 we get equation 2.13.

$$F = Z(j\omega a e^{-jkz} - j\omega b e^{jkz}) \tag{2.13}$$

Hence substituting jωa and jωb from equations 2.9 and 2.10 we get equations 2.14 and 2.15 respectively.

$$F_1 = Z(\frac{v_1}{jtan(kd)} - \frac{v_2}{jsin(kd)}) \tag{2.14}$$

$$F_2 = Z(\frac{v_1}{jsin(kd)} - \frac{v_2}{jtan(kd)}) \tag{2.15}$$

Since trigonometric identity imposes that:

$$\frac{1}{tan(kd)} = \frac{1}{sin(kd)} + tan(\frac{kd}{2}) \tag{2.16}$$

F_1 and F_2 become:

$$F_1 = \frac{Z}{jsin(kd)}(v_1 - v_2) + jZtan(\frac{kd}{2})v_1 \tag{2.17}$$

$$F_2 = \frac{Z}{jsin(kd)}(v_1 - v_2) + jZtan(\frac{kd}{2})v_2 \tag{2.18}$$

Equations 2.17 and 2.18 lead to the lumped element representation of an acoustic transmission (or delay) line for a non-piezoelectric medium to be as represented in figure 2.14.

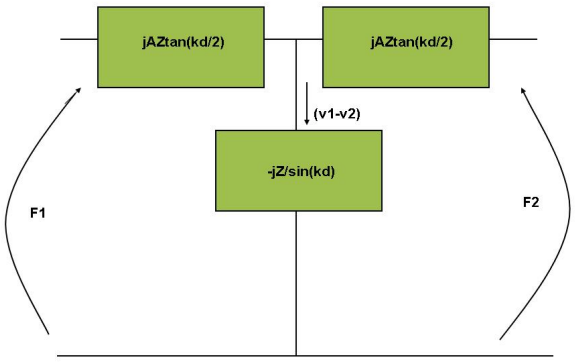


Figure 2.14: Lumped element representation of an acoustic transmission line of acoustic length kd for a non-piezoelectric medium.

However, when dealing with piezoelectric layers, there is one extra term relating the coupling between the electrical and the acoustic domains. Equations 2.17

and 2.18 will be represented as 2.19 and 2.20 [230].

$$F_1 = \frac{Z}{jsin(kd)}(v_1 - v_2) + jZtan(\frac{kd}{2})v_1 + \frac{h}{j\omega}I \tag{2.19}$$

$$F_2 = \frac{Z}{jsin(kd)}(v_1 - v_2) + jZtan(\frac{kd}{2})v_2 + \frac{h}{j\omega}I \tag{2.20}$$

Where $\frac{h}{j\omega}I$ is the electrical term with h being the piezoelectric slab thickness and and I the current through it. The lumped element representation of a piezoelectric acoustic transmission line is shown in figure 2.15.

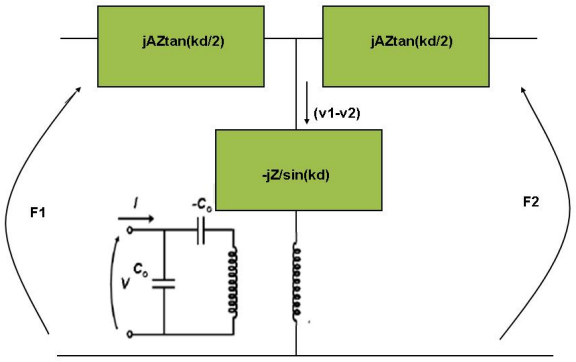


Figure 2.15: Lumped element representation of an acoustic transmission line of acoustic length kd for a piezoelectric medium.

The Mason lumped element representation of a composite three-layered resonating structure (see figure 2.16) is represented by figure 2.17, where we can see two mechanical ports and one electrical port of the piezoelectric layer. Each layer is treated as an acoustic transmission line and impedance mismatch, and the model represents the mass loading effect.

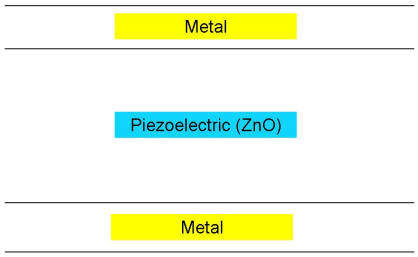


Figure 2.16: Composite structure made of multiple layers. The Mason model is based on the 1D analysis and boundary conditions of such an acoustic structure.

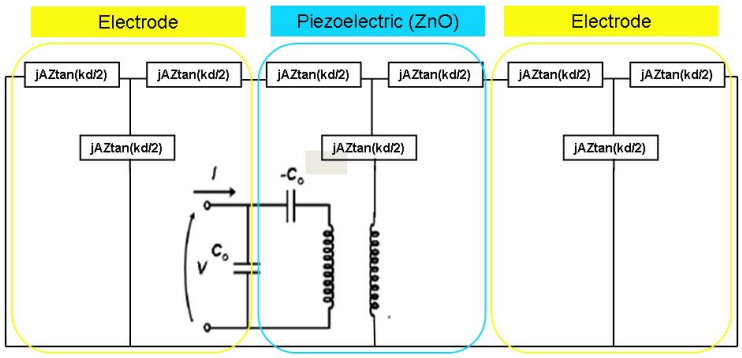


Figure 2.17: Mason model representing coupled resonator FBAR filter.

The 1D Mason model is used to derive the total acoustic impedance of the resonating multilayer.

FBAR impedance derivation

The electro-acoustic performance of an FBAR resonator is characterized by its impedance [202]. From the 1D Mason acoustic wave propagation model (explained above) and the characteristic layer impedance value, it is possible to derive the overall acoustic impedance of the FBAR.

CHARACTERISTIC IMPEDANCE

Characteristic impedance depends on the material properties of each layer. It is different from acoustic impedance as it does not account for reflected waves and does not have a positional dependence [176]. The characteristic impedance for non piezoelectric materials is given by equation 2.21, while for piezoelectric materials it becomes 2.22 [176].

$$Z_c = \sqrt{\rho c_{33}} = \rho \cdot v \tag{2.21}$$

$$Z_{c(piezo)} = \sqrt{\rho(c_{33} + \frac{e_{33}^2}{\epsilon_{33}^S})} \tag{2.22}$$

With ρ being the material density and c_{33} the material stiffness coefficient in the thickness direction and v the acoustic velocity; the other variables have been explained in section 2.4.2. Characteristic impedance is essential as it is used to derive the composite structure's acoustic impedance.

ACOUSTIC IMPEDANCE

The acoustic longitudinal mode (d_{33}) impedance, is derived from the 1D Mason model. For a single piezoelectric layer this is given by equation 2.23 [176].

$$Z_{sys} = \frac{1}{j\omega C_0}(1 - k_t^2 \frac{tan(kd/2)}{kd/2}) \tag{2.23}$$

Where C_0 is the static or clamped capacitance of the piezoelectric plate. This constant strain electrical capacitance given by equation 2.24.

$$C_0 = \frac{A\epsilon_{33}^s}{d} \tag{2.24}$$

The other variables are: k acoustic wavenumber ($k = \omega \cdot \sqrt{\frac{\rho}{c_{33}}}$), d piezoelectric plate thickness, A plate area and k_t^2 piezoelectric electromechanical coupling coefficient. For a piezoelectric layer sandwiched between two thin metal films the acoustic impedance equation becomes [176]:

$$Z_{sys} = \frac{1}{j\omega C_0}(1 - k_t^2 \frac{tan(kd/2)}{kd/2} \cdot \frac{(Z_{top}^* - Z_{bot}^*)cos(kd)^2 + j \cdot sin(2kd)}{(Z_{top}^* - Z_{bot}^*)cos(2kd) + j \cdot sin(2kd)(1 - Z_{top}^* Z_{bot}^*)}) \tag{2.25}$$

Equation 2.25 will be used for the future FBAR device analysis.

Here $Z_{top}^* = \frac{Z_{top}}{Z_{c(piezo)}}$ and $Z_{bot}^* = \frac{Z_{bot}}{Z_{c(piezo)}}$, where Z_{top} and Z_{bot} represent the zero impedance surface terminations at the electrode/air interface.

FBAR electro-acoustic principles

FBARs are classified as passive devices as they can be modeled simply by capacitor, inductor and resistor elements arranged in series. This coupled electro-mechanical model of the FBAR is represented by an electrical equivalent circuit called the Butterworth Van Dyke (BVD) model (see figure 2.18), where C_0 is the clamped piezoeletric capacitance (causes distorted resonant frequency) and L_m, C_m, R_m represent the motional (or mechanical) inductance, capacitance and resistance respectively. The BVD allows circuit modeling of the FBAR, which is thus represented as a simple one-port resonator.

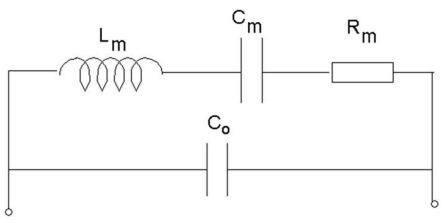


Figure 2.18: Coupled electro-mechanical Butterworth Van Dyke FBAR model.

In any piezoelectric element, a strong resonant response can be observed electrically only for those modes of vibration which have a high Q, and/or large electromechanical coupling [50]. Figure 2.19 shows the standard FBAR and its frequency response.

(a) (b)

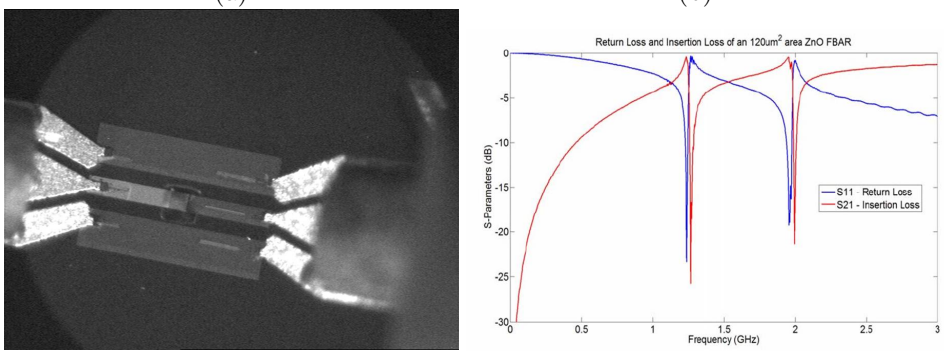


Figure 2.19: a)Standard 120x120μm^2 FBAR, b)frequency response for a 120x120μm^2 FBAR (courtesy of Carlos Fragkiadakis).

The FBAR resonator behaves as a static capacitor C_0 almost everywhere except in a very narrow range between series (f_s) and parallel (f_p) resonances in which it becomes inductive. FBAR becomes a pure resistor at series resonance (where L_m and C_m cancel each other out), which occurs when polarization is in phase with the applied electrical potential. Parallel resonance occurs when polarization is 180° out of phase with the applied electrical potential.

The two principal quantities characterising electromechanical resonators are the quality factor (Q) and the electromechanical coupling coefficient ($k_{eff}{}^2$). Q is defined as the ratio of stored energy to dissipated energy. Its value can be either measured from the s-parameter values (see equation 2.26) or calculated with equation 2.27.

$$Q_{measured} = (\frac{f}{\Delta f}) \tag{2.26}$$

$$Q_{calculated} = \frac{f}{2} \cdot \frac{\delta\phi}{\delta f}|_f \tag{2.27}$$

Where f is the frequency, Δf represents the bandwidth measured at 3 dB from the S_21 minimum, ϕ=$\frac{\Theta}{2}$, where Θ is the phase angle. Q is affected by air damping, clamping and surface losses.

Efficiency of the device is can be quantified through the effective electromechanical coupling coefficient (k^2_{eff}) parameter. This is slightly different from the electromechanical coupling coefficient (k_t^2) given by equation 2.5 as the former takes into account all parameters including electrodes. Hence k^2_{eff} can be either measured from s-parameter values (equation 2.28) or calculated through

equation 2.29 [34].

$$k^2_{eff_{measured}} = \frac{\pi^2}{4} \cdot \frac{f_p - f_s}{f_s} \tag{2.28}$$

$$k^2_{eff_{calculated}} = k_t^2 \cdot (1 + \frac{2\rho_{el} \cdot t_{el}}{\rho_{piez} \cdot t}) \tag{2.29}$$

Where f_p is the parallel resonance and f_s is the series resonance k_t^2 is the electromechanical coupling coefficient found in equation 2.5, ρ_{el} and ρ_{piez} are the densities of the electrodes and the piezoelectric material respectively, t_{el} is the electrode thickness and t is the piezoelectric thickness. For a ZnO FBAR, electromechanical coupling coefficient ($k_{eff}{}^2$) ranges from 7.5% to 8.5% [305]. Its value also depends on impedance mismatch between the piezoelectric material and the support layer, a large impedance mismatch causes more isolation (amount of the unwanted signal power reduced by the filter) and thus a large coupling coefficient.

The Figure Of Merit (FOM), is also important as it represents the overall resonator performance. It is is found through equation 2.30.

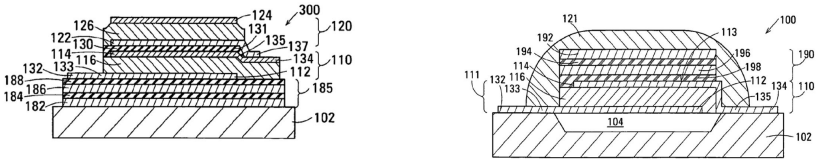
$$FOM = k_t^2 \cdot Q \tag{2.30}$$

2.4.4 FBARs and polymers

The advantage of LCP-based FBAR is to overcome some limitations and problems such as being able to carry Monolithic Microwave Circuit (MMC) integration of these with other components. An FBAR capable of being completely integrated with MMIC together with other active elements on existing semiconductor substrates (e.g., Si, GaAs), has already been proposed by Park et al. [217].

One way to ease the procedure of integrating FBARs with MMIC is to create them on polymers which allow both manufacturing and application advantages. State of the art of FBARs on polymer is extremely limited as so far only Bragg and air-gap type FBAR resonators have been proposed on organic substrates.

An acoustic Bragg reflector type FBAR has been proposed by Larson III John D. Ellis [138]. This comprises metal and plastic polyimide Bragg layers which acoustically isolate the FBAR from the substrate (see figure 2.20 a)). Larson III John D. Ellis [139] proposed the same resonator but with extra encapsulant covering the FBAR stack (see figure 2.20 b)).



(a) (b)

Figure 2.20: Bragg-type FBAR on polyimide and parylene a)from Larson III John D. Ellis [138], b) from Larson III John D. Ellis [139].

An air-gap type FBAR on LCP already was demonstrated by Park et al. [217], who stacked a liquid crystal polymer thin film on a silicon substrate having a cavity part. They used a 5μm dielectric LCP with the function of supporting the resonating part (metal/piezoelectric/metal) acting as an insulating layer.

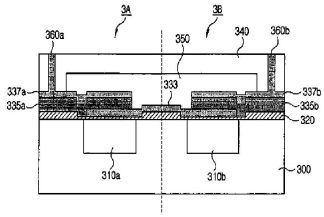


Figure 2.21: Air-gap type FBAR on LCP From Park et al. [217]

Furthermore, a packaged FBAR on PCB polymer was proposed by Lin et al. [162]. The RF device was assembled onto LCP PCBs by using a microcap method. This technique reduces interconnection and packaging problems.

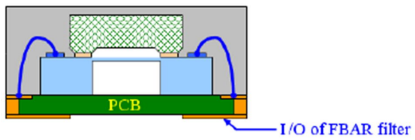


Figure 2.22: Packaged FBAR assembled onto LCP PCB from Lin et al. [162].

The use of LCP would allow direct integration of FBAR devices with other components such as microstrip-fabricated IC, antennae, phase shifters etc. It is thus easy to create duplexer receivers and transmitters (figure 2.23 b)) directly on the microstrip-produced components. This will eventually lead to cheaper and smaller integrated electronic gadgets such as mobile phones and GPS and

the ability of 3D MEMS production. The latter technology provides thick, robust sensor structures that are very sensitive to inertial forces and pressure but are insensitive to other environmental variables and causes of failure [128]. 3D integration of MEMS is expected to be an enabling technology of high-volume production for more than Moore applications (i.e. miniaturised wireless sensor nodes) [271].

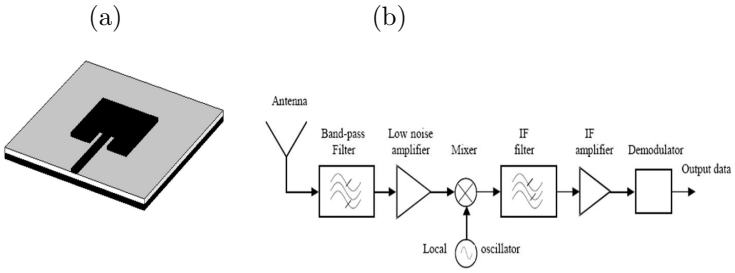


Figure 2.23: a)Patch antenna with microstrip feed , b)block diagram of basic radio receiver. Both figures taken from [225].

2.5 Surface topography: roughness, waviness and curvature

A key feature to consider when dealing with new substrates is surface topography and texture. This is because all substrates have different properties from each other in terms of rigidity, topography and texture. These parameters can all be considered and measured statistically and this approach for the analysis of surface nature is essential.

Surface texture is the repetitive or random deviation from the perfectly flat surface that forms its three dimensional topography [39]. It refers to the local deviations of a surface from its ideal flat shape. Accurate characterization of surface texture is critical for controlling the function and reliability of precision components and the processes used to manufacture them [39]. Texture is not a directly measurable quantity, but it can be measured through some intrinsic characteristics or parameters, namely: waviness, curvature, roughness, lay (direction of surface irregularities) and defects (pitting, scratching) [39]. In our studies we will concentrate on the first three.

2.5.1 A statistical approach

There is a very simple way to go about characterising surface topography, and this is through the use of statistical measures. The deviations from a standard (flat and smooth) substrate can be carried out through surface scanning measurement of peaks and troughs followed by adequate calculations. For roughness and waviness these calculations are the average or root mean square (also called quadratic mean) approaches. For average roughness we will use Ra, while for root mean square roughness Rq will be employed.

The definitions (average and root mean square) suggest what mathematical sampling method is considered for the varying quantities' statistical measure of magnitude. Average implies that, after scanning the surface, the asperity heights are summed and then divided by the number of asperities (see equation 2.31). For simplicity we will use roughness although the statistical methods shown below can also be used for waviness hence, instead of Ra one can use Wa (if referring to waviness instead of roughness).

Average values are easy to measure as they are good general guidelines of surface texture, they are well-established and understood, and there is a wide range of literature and standards available to explain them. Process engineers know that they can specify average roughness (Ra) and finish a surface within that specification [315].

$$Ra = \frac{1}{n}\sum_{i=1}^{n} x_i \tag{2.31}$$

Where $\sum$ is the summation of the values x and n is the number of values measured.

Root mean square is more complicated and can be described by equation 2.32. The difference between the average (Ra) and root mean square (Rq) roughness (or waviness) is an indication of the uniformity of the surface as the latter is more weighted by large values of peak height and valley depth. The Rq value is typically $10\% - 25\%$ larger than the mean value of roughness depending on the nature of the surface [170].

$$Rq = \sqrt{\frac{1}{n}\sum_{i=1}^{n} x_i^2} \tag{2.32}$$

To distinguish the roughness and waviness measurements from each other, cut-off filters are used after scanning. Here high pass and low pass filters are used to delineate roughness from waviness. High pass filters pass high frequency signals above the cutoff value allowing, therefore, roughness measurements, while low pass filters are used for low frequency waviness measurements. The user-selectable filters are in accordance with the ANSI B46.1 specifications [39]. The cutoff filters used are 20μm for short pass (high frequency) and 200μm for long pass (low frequency).

2.5.2 Roughness

Roughness is an essential parameter in the microsystems domain as it can affect the future material growth quality and adhesion. It can be defined as surface texture random irregularities and is usually caused by finishing and chemical processes. Roughness is the high frequency of waves between equidistant hollows [39] and can be measured in many ways among which surface profiling and atomic force microscopy.

Roughness reduction

Roughness is a MEMS reliability parameter as it can cause fabrication issues and affect the quality of the grown thin films. Wang et al. [292] found that LCP has a high surface roughness ($\sim$190nm) which tends to increase to 1.1μm through oxygen plasma exposure.

With the presence of asperities, misalignment of grown material grains occurs causing poor crystallization and bad quality of the thin films. This is because epitaxial grain growth of polycrystalline thin films is affected by strain energy which can be caused by a rough substrate. The dependence of AlN and ZnO piezoelectric quality and high c-axis orientation on substrate and bottom electrode smoothness is well known [99], [11], [110].

Chemical mechanical polishing (CMP) has become a a leading method for IC planarisation. CMP works on the principle of a rotating polishing pad that is covered with colloidal slurry which is a nontoxic alkali substance with good

removal selectivity and a good rate control [200]. A good slurry is one that reacts with polymer structural bonds, forming a weakened layer that is removed rapidly during CMP thanks to chemical and surfactant diffusion, surfactant adsorption, surface reactions [21]. The relative motion of the wafer and pad, combined with the applied down force and chemical activity of the slurry, erodes features on the wafer. Hence, surface topography is removed by a combination of mechanical and chemical effects Srinivasa-Murthya et al. [253].

CMP on polymeric substrates is a very new field. CMP of polymer requires the polymer material to be hard and strong, because if the polymer is too soft the abrasive might become embedded in the polymer [255]. As Borst et al. [21] noticed, the lower physical strength and higher chemical resistance of polymeric and porous low-κ substrates leads to challenges during CMP of polymers.

Borst et al. [21] polished benzo-cyclo-butene (BCB) and SILK^{TM} in both copper and HNO_3/surfactant slurries. They found that two different conditions developed when lap polishing polymers. The first polishing process condition consisted in surfactant adsorption on passivated polymer layer which yielded a low scratching and, because it does not break the structural bonds, it has low removal rate. In the second condition the slurry oxidised the polymer surface breaking structural polymer bonds and giving a low scratching, high removal rate outcome.

The most common type of polymer polishing pad is SUBA (800 and IV), while slurry types varied from Okamoto GRIND-Xe Simlox A1136 (specifically used for polymeric materials), ones used for copper removal to alumina and DI slurry [20]. Zhong et al. [319] employed a SUBA800 polishing pad mounted on an Okamoto SPP-600S CMP machine, slurry flow rate of 100ml/min, a chuck speed (in relation to sample) of 40rpm and three different types of slurry ILD1200 (fumed silica designed for oxide CMP), Mazin^{TM} SRS1 and SRS3, and Okamoto GRIND-X^{TM} (Simlox A1136) to remove of polymeric asperities. For LCP surface polish, silica microspheres have been used by Onodera et al. [211]. Wang et al. [290] employed a lap master polisher with 0.06μm slurry for 2 hours. Kingsley et al. [120] achieved 10-50nm Ra with alumina slurry.

2.5.3 Waviness

Waviness is is the low frequency (wide spacing) of waves between equidistant hollows [39]. It is a repetitive deviation caused by warping strains and heat treatments which can cause misalignment when producing device. In our case, as we will see, low rigidity is the primary culprit for LCP substrate waviness and the issue is solved through appropriate substrate backing methods.

Proper bonding with a rigid substrate can be a viable solution to waviness. A rigid substrate such as Si or glass is usually used and the backing can be carried out both with the use of an adhesive or epoxy layer or without it given that the substrate is taken close to its glass transition temperature (Tg) (a second order phase transition). In the literature we can find that wafer bonding with no adhesive layer has been carried out with the following conditions: T=300°C,

P=50-100bars, t=30-60min [131].

2.5.4 Curvature

Curvature is parameter which causes or is caused by stresses within a substrate or multilayer. It is, therefore, an indication of the presence of stress. Curvature comes into play when dealing with interfacial stresses and it can be measured in several ways including surface profiling methods.

In order to improve curvature and, therefore, reduce bowing it is essential to minimize stresses of a composite structure. In microelectronics stresses are usually caused by thin film deposition. Curvature measurement techniques and calculations will be introduced in later sections.

2.6 MEMS device yield and reliability

2.6.1 Device yield

Yield is the expected fraction (or percentage) of successful die from wafer [69]. It can also be defined as the percentage of devices that meet a certain performance specification. Yield is a parameter proportional to the inverse of chip size: as chip size increases, yield decreases [69].

To achieve high yield, manufacturing processes must be stable, repeatable and of high quality. To improve manufacturing process output, variability must be reduced through process control. Types of variability are: human error, equipment failure, material non-uniformity, substrate inhomogeneity and lithography spots.

For a given die size and defect density the larger the die size, the lower the yield. The basic model that we will use is represented by equation 2.33 [313].

$$Yield = \frac{n-d}{n}(\%) \tag{2.33}$$

Where n is the total number of devices of a wafer and d is the number devices not working per wafer.

There are other more sophisticated methods to calculate yield (also called sort) and this is through defect density. Probability that a die from a wafer is good after processing given defect density can be calculated in with a variety of equations including the the model represented by equation 2.34 which relates the yield to the number of masking steps.

$$Yield = \frac{1}{(1+AD)^m} \tag{2.34}$$

Where:
A= area of chip or die in cm^2

D= expected defect density per cm^2 per masking step. Usually ∼1 for silicon, more for other materials. Number of defects/number of samples
m= number of masking steps

2.6.2 MEMS reliability

When dealing with new material combinations or new device architectures, it is important to talk about reliability. Reliability is the ability of a device to perform a function for a period of time given some specified conditions [60] and its quantification is essential for the commercialization of products [197].

Reliability can be defined as the ability of a system to operate and perform its functions in both standard and unexpected circumstances. MEMS reliability assessment, in general, is more complex than integrated circuits as it must take into account several phenomena at once: electrical, thermal and mechanical phenomena. Because of this coupling within domains, not all MEMS failure mechanisms are well understood.

Failure mechanisms can be subdivided into: improper packaging techniques, mechanical (delamination), electro-mechanical, material deterioration, excessive instrinsic stresses and environmental effects [93]. Generally, packaging provides insulation of the device from outside environmental damage although some MEMS need to be exposed to the working environment. The process of packaging must be carried out in a secure way in order not to affect the devices. All of these create a reliability challenge.

There are various types of degradation mechanisms within the microsystems domain, which are generally similar for MEMS of all applications. Some failure mechanisms were mentioned by Spengen [252] and are listed below:

Table 2.3: MEMS degradation mechanisms

Degradation type	**Occurrence**
CREEP	metals
FATIGUE	metals given cyclic loading
STICTION	for low stifness materials or surface micromachined parts
STRESS CORROSION CRACKING	SiO_2
CHARGING	dielectric materials
LEAKAGE	dielectric materials
FRICTION and WEAR	silicon microstructures with sliding surfaces
PACKAGING and CONTAMINATION	environmental effects
DELAMINATION	TCE difference between materials
ELECTRICAL PERFORMANCE	power loss

Friction and wear are not a problem for devices with resonator applications,

but they come into play in devices with switching applications since there is physical contact between two or more surfaces.

Finding the right packaging given specific materials, configurations and environmental effects is also essential, and the package must be tailored to these parameters. A method for improving reliability of MEMS is to design with regard to the packaging of MEMS [223] since the packaging procedure can create various problems (i.e. outgassing of water/vapour from adhesive).

RF MEMS performance is determined in terms of electrical power management. Low loss (high power) transfer is a necessary feature for proper device functioning and reliability, hence, electrical performance should be well managed in MEMS devices since power loss of RF transmission in coplanar waveguides causes heat flow. This temperature rise in a device, if not accounted for, can be a major reliability challenge for the future application of the component.

2.6.3 Stress and reliability

Stress is one of the most important mechanical reliability parameters as it is a leading cause of device failure. Thin film stresses can cause mechanical and performance reliability issues.

Residual stresses

Thin film stresses can arise in many ways as stress originates from strained regions either within the thin films (grain boundaries, dislocations, voids, impurities) or at the film/substrate interface (lattice mismatch, different thermal expansion coefficient), due to dynamical (recrystallization, interdiffusion) or gas adsorption processes [124]. In order to prevent high stress before reaching the device stage, it is important to measure and assess this parameter during the fabrication process.

Stress analysis is one of the most essential features in this project as the use of new substrates means that old measurement approaches must be tailored to suit the compliant substrate. Residual wafer stresses can be measured with various techniques among which.

1. Curvature measurement technique.
2. Diffractional method.

For the curvature measurement technique film stress is determined after measuring the substrate radius of curvature with a surface profiler (i.e. Dektak), followed by implementation of the value retrieved in one of many equations. The equations and their principles are explained below.

- **Stoney method**: The most important equation from which to derive thin film stresses from substrate curvature measurements is called Stoney's

equation 2.35, which is an accurate way to quantify thermal and intrinsic thin film stresses on rigid substrates. The total residual stress on a thin film is σ_f.

$$\sigma_f = \frac{E_s}{1-\upsilon_s} \cdot \frac{1}{\kappa}\frac{1}{\kappa_0} \cdot \frac{t_s^2}{t_f} \tag{2.35}$$

Where subscripts s and f describe, respectively, the substrate and the thin film properties, E is the Young's Modulus, κ is the final radius of curvature, κ_0 is the initial radius of curvature and t is the thickness. Equation 2.35, however, is not suitable for flexible substrates. Stoney's formula is based on linear beam theory which assumes small bows neglecting rigidity of films. Linear beam theory is not valid for large deflections, as it neglects the square of the first derivative in the curvature formula and provides no correction for the shortening of the moment arm as the loaded end of the beam deflects [14]. Hence, using Stoney for thin films on polymers exhibits errors if the rigidity of films cannot be neglected [36]. For large loads it gives incorrect deflections which are larger than the length of the beam [14], this must mean that the stresses found given a large deflection are not true values.

- **K.S.Chen Method** [36]: In contrast to Stoney's equation, this considers the thin film Young's modulus effect. They consider complications arising when thin film rigidity is higher than substrate rigidity, which is the case for our samples as 1μm ZnO film has rigidity 1.9826e^{3}GPaKg/m^2 while 100μm LCP has rigidity 1.0165e^{3}GPaKg/m^2. They explain that the deformation undergone by the substrate is very large and, therefore, that geometrical non-linearity and mid-plane offset should be accounted for. Furthermore they account for TCE mismatch among layers (thermal considerations) but ignore intrinsic stresses.

  Curvature-stress relationship:

$$\sigma_f = Bow \cdot K_{st} \cdot (1 + 1.12(\frac{E_f}{E_s})^{1/5}(\frac{t_f}{t_s})^{1/3}(\frac{Bow}{t_s + t_f})^2) \tag{2.36}$$

  Where K_{st} is the conversion factor:

$$K_{st} = \frac{E_s t_s^3}{3(1-v_s)L^2 t_f^2 (1 + \frac{t_s}{t_s})} \tag{2.37}$$

  Where Bow is the bow also defined as the degree of bending of the wafer:

$$Bow = \frac{r^2}{2 \cdot \kappa} \tag{2.38}$$

  Where r is the wafer radius and κ is the radius of curvature.

- **Y.C.Tsui method** [280]: Consider both intrinsic and thermal stresses on the substrate σ_s. The intrinsic stress assumption introduces a variability issue which can be a drawback.

$$\sigma_s = \sum_{i=1}^{n}(\frac{E_s F_i}{b(t_s E_s + (i-1)wE_f)} + E_s(\kappa_i - \kappa_{i-1})\delta_1) - \frac{F_{CTE}}{bt_s} + E_s(\kappa_c - \kappa_n)\delta_n \tag{2.39}$$

where δ is the distance from neutral axis to the interface, w and b are the lateral dimensions, subscript n refers to the total number of layers and κ is the radius of curvature.

$$\delta_1 = \frac{w^2 E_f - t_s^2 E_s}{2(wE_f + t_s E_s)} \tag{2.40}$$

- **S.Wagner method** [235]: Considers biaxial modulus, intrinsic and thermal stresses for total residual film stress calculation σ_f. It also assumes moisture absorption mismatch for strain (ϵ) which we ignored.

$$\sigma_f = \frac{(\epsilon \cdot E_f)}{(1 + (E_f \cdot t_f)/(E_s \cdot t_s))} \tag{2.41}$$

- **J.I.Han method** [86]: It only considers geometrical effects for which neutral layer position is emphasized. Thermal effects are ignored.

$$\sigma_f = \frac{(E_s \cdot t_s^2)}{(6\kappa \cdot t_f(t_s + t_f))} \tag{2.42}$$

Each numerical model is based on specific principles. Note that in the equations the common parameters are: E_s (substrate Young's modulus), E_f (thin film Young's modulus), t_s (substrate thickness), t_f (thin film thickness), υ_s (substrate Poisson's ratio), κ (radius of curvature after deposition), κ_0 (radius of curvature before deposition for a 4inch rigid Si/SiO_2 wafer κ_0=1.84e8μm).

Thermal stresses

Stresses are a combination of thermal and intrinsic stresses. Thermal stress is caused by thermal mismatch between layers and is calculated theoretically through the following equation (2.43) [74].

$$\sigma_{th} = \frac{E_f}{1 - \upsilon_f} \int_{T_{anneal}}^{T_0} (\alpha_f - \alpha_s) \cdot dT \tag{2.43}$$

Where E_f is the film's Young's modulus, v_f is Poisson's ratio of the film, T_0 is the final temperature (room temperature in our case), T_{anneal} is annealing temperature and α is the thermal coefficient of expansion where the subscripts f and s indicate, respectively, thin film and substrate. It is important to be aware that the theoretical thermal stress value found by employing equation 2.43 is not fully accurate and will not match the experimental values found by equation 2.35. This is because of the omission of the intrinsic stress terms. Total thin film stresses are a combination of thermal and intrinsic stresses and, wile the contribution of thermal stress to the overall stress can be easily calculated, intrinsic stress prediction is not so straightforward.

To derive equation 2.43 consider the general rule for stress strain relationship in equation 2.44

$$\sigma = E \cdot \epsilon \tag{2.44}$$

Where σ is stress E is Young's Modulus and ϵ is strain. But we consider biaxial modulus (E*) as we are considering both x and y directions of substrate and film, this parameter is given by equation 2.45.

$$E^* = \frac{E}{1-v} \tag{2.45}$$

The stresses and strains are thermal and we know that thermal strain is found through equation 2.46.

$$\epsilon_{th} = (\alpha_f - \alpha_s) \cdot \Delta T \tag{2.46}$$

Therefore from equations 2.44 and 2.46 thermally-induced stress is:

$$\sigma_{th} = E \cdot \epsilon_{th} \tag{2.47}$$

And substituting equations 2.45 and 2.46 in equation 2.47 we get equation 2.48.

$$\sigma_{th} = \frac{E}{1-v} \cdot (\alpha_f - \alpha_s) \cdot \Delta T \tag{2.48}$$

As we can see equations 2.43 and 2.48 and are the same.

2.6.4 Physical reliability of thin films on polymer

Both metal and ceramic thin films on polymers have been deposited primarily for thin film transistor (TFT) applications within the IC industry. Novel material combinations such as that of flexible polymers with metals and brittle ceramics, always require a reliability assessment for the material multilayer and the eventual device. The composite is made of a thick compliant substrate, rigid metal and/or brittle ceramic.

The failure modes of polymer, metal and ceramic materials are very different from each other. Reliability studies should encompass both mechanical analyses and electrical performance variation of thin films on polymers. Mechanical investigation also includes adhesion quality between the thin films and the substrate as a poor adhesion undermines the future device mechanical reliability.

Metals on polymer

The interaction of thin metal films on polymers is of interest when talking about metal-polymer adhesion. Polymer surfaces are generally associated with low sticking coefficients and poor adhesion, which is disadvantageous regarding metallization of polymers [289]. Mackova et al. [179] studied silver (Ag) and gold (Au) atom diffusion in PET through Rutherford back-scattering, x-ray photoelectron spectroscopy and TEM, and determined the amount of metal and chemical structure in the surface layer confirming a creation of an intermixed metal-polymer interface.

While reactive metals always form relatively sharp interfaces with polymers, metals of lower reactivity diffuse into polymers at elevated temperatures and have a very strong tendency to agglomerate [66]. This interdiffusion enhances the interfacial adhesion by improving the adsorption of the polymeric material

[121]. It is chemisorption, a type of strong adsorption process, which provides the intrinsic adhesion forces between the polymer and the sputtered metal [121].

Failure strain of a metal film on a polymer substrate can be maximized by ensuring good adhesion between film and substrate [171]. This is why [249] tried to achieve a 10% improvement in polymer-metal (Au/polymer) interfacial adhesion. When the maximum strength and work-of-separation (cohesion) have been reached, delamination will take place and will propagate along the element boundaries [22] causing the metal to eventually crack. Figure 2.24 shows thin metal film crack mode when deposited on polymer.

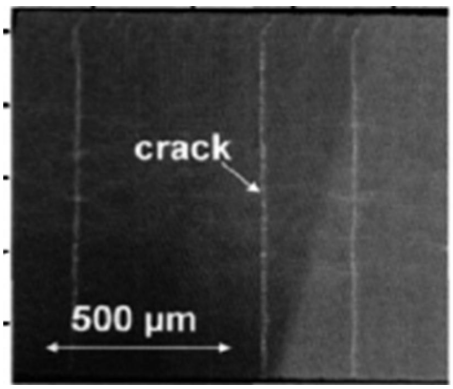


Figure 2.24: Gold stripe on silicone crack from [154].

When deposited on polymeric substrates, metal ductility has been shown to improve. This was established by many groups including Xiang et al. [303] through a 10% increase in metal strain, Li et al. [155] who noticed an increase of up to 20% and Lu et al. [172] with their Cu metal on Kapton stretched beyond 50%. The reason for this increase in strain sustenance of polymer-supported metal films is that, when the film is well bonded to a substrate, the local elongation in the film is suppressed by the substrate [303], therefore easing the strain localization which causes rupture of the metal film. Metal film to polymer substrate adhesion is important as when these are well-bonded, the local elongation in the film is suppressed by the substrate [157].

Metal thin films on polymer can also undergo strain localization (or necking) a form of plastic deformation when there is high resistance to sliding at the interface. The metal film can exhibit three types of tensile behavior: the film slides and ruptures at a small strain by forming a single neck, the film slides and deforms to a large strain by forming multiple necks, and the film deforms uniformly to a very large strain without sliding and necking [157].

Reliability of metals on polymer is not only limited to mechanical performance, but also electrical functioning. Ideally conductivity of the metal should not change with respect to strain on flexible substrate [243]. But, unfortunately, electrical performance of soft materials is poor [249]. As Someya and Sekitani

[249] already witnessed, mobility (which is directly proportional to conductivity) decreases for electrodes if bent in air for 100 days. Cairns [27] also noticed that for ITO on PET there is a change in electrode resistance as a function of strain and Cairns et al. [28] explained that the resistance of the ITO layer increases with strain. TFTs on polymers have proven to yield lower operation voltage [116] because the mechanical and electric properties of the metal-polymer interface are influenced by the degree of metal mobility in polymer [90].

One way to explain poor performance of metals on polymers is based on the resistivity principle (equation 2.49). By referring to figure 2.25 this principle is explained.

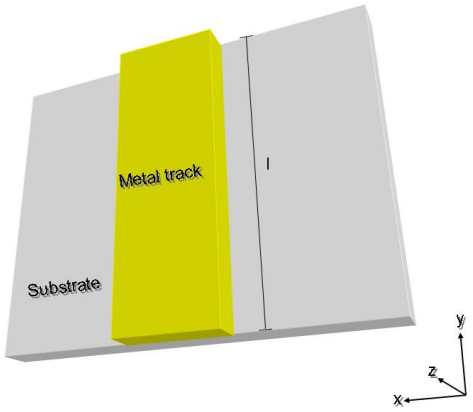


Figure 2.25: Metal track on a substrate with x, y and z coordinates.

$$\rho = \frac{Rl}{A} \tag{2.49}$$

Where ρ is the resistivity, R is the resistance, l is the length and A is the area of the track. When stretching the metal track in the y direction, the metal track length increases. An increase in l, according to equation 2.49 would lead to an increase in ρ and, therefore , a decrease in conductivity. In conclusion, conductivity depends on strain when this is applied in the current flowing direction.

In order to solve the metal on-polymer issue electrically conductive materials capable of bending and stretching should be considered. They have so far been developed for a wide range of applications such as smart clothing [312], flexible displays, stretchable circuits, strain gauges, high-deformation microelectromechanical systems (MEMS) Urdaneta et al. [281], medical and aerospace applications [304].

Ceramics on polymer

Ceramic on polymer is a recent research area. This combination is necessary if we are to achieve multifunctional devices on organic substrates and increase the application of polymer-based MEMS. However small, there already is literature of ceramic integration on polymers.

ZnO has been deposited on polymer substrates for thin film transistor applications [116], and RF sputtered on benzocyclobutene (BCB) and highly fluorinated polyether (HFP) for optical waveguides [35]. RF sputtering of ZnO was also carried out on polyimide substrates for optical applications [250] and for making differential pressure sensors [131]. Low temperature DC sputtering of ZnO was also done on polyethylene terephthalate (PET) [12]. Polyethylene napthalene (PEN) is another polymer onto which ZnO has been deposited by Chung et al. [44].

Residual stresses are ceramic a reliability issue, and refer to the combination of thermal (extrinsic) and internal stresses (intrinsic). Lee et al. [152] mentioned that intrinsic stress of ZnO is compressive, larger in magnitude than the thermal stress component, giving rise to an overall residual compressive stress in the ZnO film. Intrinsic stress in ZnO films is attributed to the accumulating effects of crystallographic flaws, especially originating from the impact of the energetic inlet gas atoms on interstitial or vacant sites in ZnO films during sputtering [166]. Intrinsic stresses are characterized by lattice strains and material crystal properties and are proportional to the roughness of the ceramic [166]. Thermal stress encompasses mainly thermal mismatch between the layers which then give rise to tensile or compressive thin film stresses. These are a consequence of high temperature substrate processing.

Moving away from ZnO, AlN has been RF sputtered at room temperature on polyimide [8], on PET (for physical sensor applications) [9] and on epoxy [94]. ITO DC sputtering on PET was reported by Cairns [27]. RF sputtered ITO was carried out for a wide range of polymers starting from as early as 1980: polyethylene teraphthalate (PET) [25], polytetrafluoroethylene (Teflon) [41], polycarbonate (PC) [130] and polymethyl methacrylate (PMMA) [184].

The most researched ceramic thin film on polymer has, so far, been ITO. Although a conductor, ITO is mechanically classified as a ceramic. Crawford [49] and S. Wagner [235] conducted stress, mechanical stability and reliability studies after depositing ITO on polymer. The former group found cracks on the ITO layers on polycarbonate. Cairns [27] and Han [86] also saw cracks with ITO-coated polymer substrates. The authors presented the ceramic failure modes and tehir results are shown in figure 2.26.

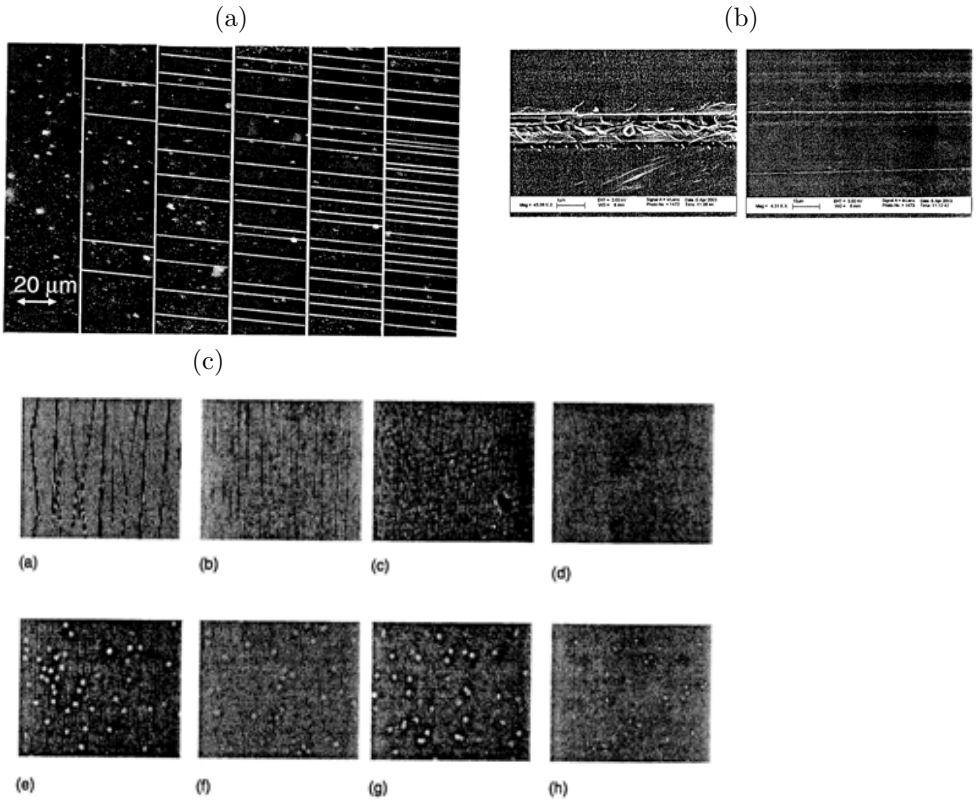


Figure 2.26: ITO ceramic crack modes: a) from Cairns [27] b) from Cairns [27] c) from Han [86].

Interfacial analysis can be used for mechanical characterisation and performance assessment of the ceramic-polymer multilayer. A laser spallation technique was used by Gupta et al. [85] to analyse the interface of various material combinations such as: polymer/ceramic metal/ceramic and ceramic/ceramic. The outcome of their studies was that the measured interface strength is related to the interfacial fracture energy. Although the literature on ceramic polymer interface studies is not abundant, Hoffman et al. [91] mentioned that a polymer/ceramic bimaterial interface has a fracture energy/area of 55J/m^2. This is quite good considering that for PZT ceramic on Pt/Si the energy release rate/unit area is 10.761-11.704 J/m^2 [318], and that epoxy on glass (soda-lime) has an interfacial fracture energy/area of 33 J/m^2 [231].

Ceramics on metal

Significant differences in the thermal and mechanical properties of ceramics and metals make it extremely difficult to obtain ceramic-to-metal joints with adequate mechanical integrity [204]. Segregation-induced embrittlement in metal-ceramic couples causes a slight reduction in the work of adhesion [165].

Further information about ceramic on metal behaviour is not necessary as the

metal thin films are very thin (100nm), one order of magnitude less than the ZnO ceramic we will use (1μm) and two to three orders of magnitude less than the LCP substrate (50-100μm).

2.7 Summary

This introduction chapter has reflected the main literature relevant to the upcoming experimental chapters. The chapter has described the work carried out worldwide on each of the topics of interest to the thesis.

Section 2.2 emphasizes the importance of organic-based devices giving examples of work carried out so far in terms of devices and fabrication methods employed. Here we see that polymer electronics has been of interest in the IC industry mainly, and is only just starting to be applied within the MEMS world. A comparison of various polymers explains why LCP is the favoured one, and polymer mechanics are briefly shown.

Section 2.3 presents an overview of electromechanical devices and their working principles, and introduces RF MEMS. Electromechanical conversion principles are listed and presented with some working examples. RF MEMS and their importance within the ever increasing wireless communications world is then described.

Since the device of main interest in this project is the FBAR, section 2.4 is dedicated to explaining about these devices. Literature of their background, application, fabrication methods, and operation principles, lay a strong starting point for our future device development purposes. Literature on FBARs on polymers is also shown, which is very small due to the novel nature of the topic.

Surface topography affects functional material growth and, device processing in general. This is why section 2.5 has been dedicated to introduce the main components of surface characterisation: roughness, waviness and curvature. Here, the importance of roughness and waviness reduction is explained giving examples.

In section 2.6 MEMS yield is briefly discussed showing that for high yield, process variables must be reduced. Device reliability is then discussed in terms of stresses. Although the causes of device failure can be many, we mainly concentrate on the thin film (metal and ceramic) stress-induced failure aspect giving examples of the integration of metals and ceramics on polymers carried out so far.

Chapter 3

Method and Apparatus

3.1 Introduction

This chapter is an overview of the methods and apparatuses employed throughout the project. The apparatuses employed for device fabrication (manufacturing equipment) and characterisation (imaging and analysis) are explained in this chapter. Furthermore, the softwares used for both data retrieval and simulation models are presented.

3.2 MEMS fabrication equipment

In order to create devices directly onto LCP, fabrication compatibilities must be taken into account. The production methods include: surface micromachining, bulk micromachining, bonding, material optical and electrical characterisation and device modelling.

Some of the equipment not listed below is: Logitech (lap polish), Electronic Micro System (EMS) spinner.

3.2.1 Sputtering

In a sputtering process energetic gas ions in a plasma are accelerated towards a solid target which provides the material to be deposited, the atoms are thus ejected from a this target due to the ion bombardment described, and deposited on a substrate. To enable the ignition of a plasma and the creation of energetic ions, usually argon is fed into the chamber [2] and the target undergoes RF or DC excitation. While in the dc-sputtering a negative potential of a few hundred Volts is applied to the target, in RF-sputtering an ac-voltage is applied.

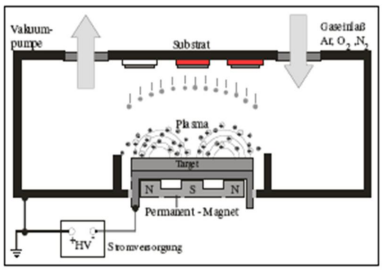


Figure 3.1: Sputtering equipment from [2].

In our experiments Nordiko sputtering system was used for sputtering metals such as chromium (Cr), platinum (Pt), titanium (Ti), gold (Au). While Cr, Ti, Au are RF sputtered, Pt is DC sputtered. Balzers was used for RF ZnO sputter.

3.2.2 Evaporation

We used an Edwards metal evaporator. In evaporation the substrate is placed inside a vacuum chamber (P<1.0E-3Pa), in which a block of the material to be deposited is also located. The source material is then heated to the point where it starts to boil and evaporate. The vacuum is required to allow the molecules to evaporate freely in the chamber, and they subsequently condense on the substrate surface [212].

3.2.3 Photolithography

Alignment is the adjustment of an object or feature position in relation with other ones. Alignment is more complex in 3D miniaturized devices than in IC manufacture as high aspect ratio 3D features can can cause problems for alignment systems with low DOF [180]. Bad alignment (misalignment) can be caused by many factors: mask error, optical distortion, wafer expansion, mask expansion.

Mask Aligners used were: Karl Süss MA56 for single sided alignment (front wafer features), and Karl Süss MJB21 for double sided alignment (front and back wafer features).

3.2.4 Dry etching

Reactive Ion Etching (RIE)

RIE is a technology which allows material etching through a chemically and physically reactive plasma, which is generated under vacuum by an electromagnetic field. High-energy ions from the plasma attack the wafer surface and react with it. The RIE system consists of parallel plates, where the wafer platter

situated on the bottom, enclosed in a chamber. As RF electromagnetic field at 13.56MHz applied to the wafer the platter ionizes the gas molecules through stripping of electrons initiating plasma.

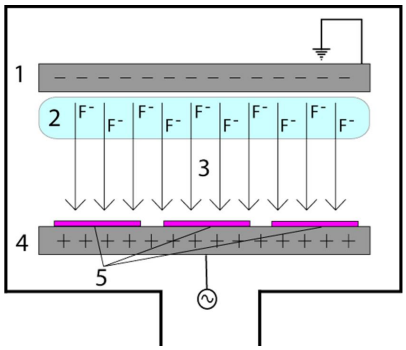


Figure 3.2: RIE etch system from [26].

The gases determine the chemical reaction involved in the process and, therefore, the type and composition vary depending upon the material to be etched. Gas pressure is maintained between 20-500mTorr by adjusting gas flow rates and/or the exhaust which directs the gas exits to a vacuum pump.

Deep Reactive Ion Etching (DRIE)

DRIE is a MEMS etching technique often preferred to RIE as it yields highly anisotropic deep trenches in silicon wafers with aspect rations up to 20:1. The Bosch process is exploited in our experiments using a Yamakawa machine. This technique can potentially create straight 90◦ walls, although practically the walls are always tapered by a couple of degrees.

The principle behind the ability of getting straight walls with the Bosch process is that the following modes are continuously alternated:

1. Plasma etch with ions (SF_6 for Silicon etch), which attack the wafer from a nearly vertical direction.

2. Passivation layer deposition (C_4F_8 gas) which condensates on the sidewalls, therefore protecting from lateral chemical attack and etching.

Barrel etching

This etch methd is used to gently etch fine traces of contamination, photoresist and moisture, and to oxidize carbon and organic deposits. To this end the following gas composition is employed at relatively low power: 10%oxygen, 90%argon.

3.3 Metrology of processed devices

3.3.1 Atomic Force Microscopy (AFM)

AFM is a 3D surface imaging technique consisting of the following parts: cantilever, tip, piezoelectric transducer, laser, detector and feedback electronics that control the cantilever. While the tip runs across a scanned surface, the operating principle involves the laser beam reflecting off the backside of the cantilever while the photodiode array monitors the height of the tip and the piezoelectric tube adjusts the height of the beam [59].

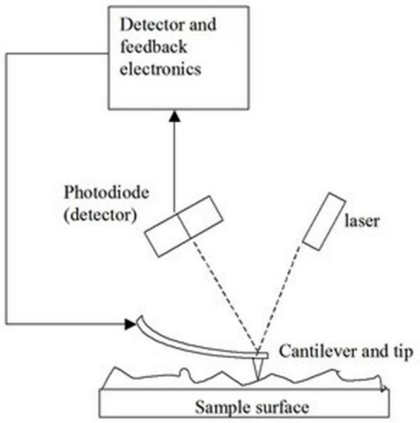


Figure 3.3: AFM setup from [59].

AFM is used in one of two modes, namely contact or tapping mode depending on the application. When used for surface topography measurement and imaging (i.e. roughness) the contact mode is preferred, while tapping mode is a method used to probe properties of materials through sample-tip interactions. The former involves continuous scanning of the tip on the surface the for latter the tip is oscillated at a high frequency and pushed into the sample-tip repulsive regime. For the tapping method, the slope of the force-distance curve, describing adhesion between tip and surface, is measured which is correlated to the sample's elasticity.

3.3.2 Scanning Electron Microscopy (SEM)

An electron gun containing a tungsten cathode filament emits an electron beam with energy 100eV-40keV. This electron beam deflects in the x and y axes when reaching the raster-scanned area. Energy is, thus, exchanged between the electron beam and the sample area resulting in: reflection of high-energy electrons (elastic scattering), emission of secondary electrons (inelastic scattering) and electromagnetic radiation. Detection for imaging in SEM occurs in two ways: secondary electron detection (from inelastic scattering) which is a low energy process, and backscattered electron detection (from elastic scattering)[240]. The secondary electron detection method has a better resolution and is, therefore,

used for imaging while the backscattered electron detection (which uses Rutheford backscattered spectrometry), with its higher energy, allows for sample composition analysis. Figure 3.4 illustrates what happens once the incident electron beam reaches the target.

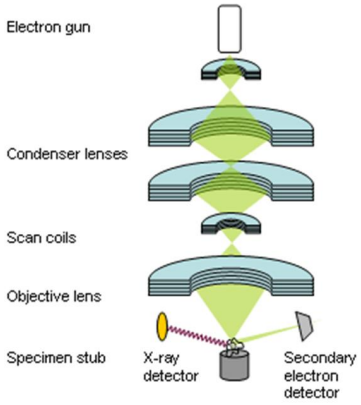


Figure 3.4: SEM from [256].

The only limitation for analysing a sample under SEM is that it must be conductive. Unconductive samples can either be coated with a nm layer of carbon or gold, or they can be analysed under an Environmental Scanning Electron Microscope (ESEM). The difference between a standard SEM and the ESEM is that the latter avoids the accumulation of electric charge on the sample through use of higher gas pressure in the chamber (up to 50Torr). The gas neutralizes negative charges on the sample through interaction with positively charged beam atoms.

3.3.3 Dektak

Dektak 3RD® is a surface profiler which determines surface topography of a sample such as curvature, waviness and roughness. It uses a stilus to scan linearly on a surface unlike AFM which scans the area of the surface. This linear scan allows for substrate curvature measurements which can be used to calculate stresses. Furthermore the advantage of Dektak over AFM comes into play when dealing with large height steps and roughnesses.

Dektak Veeco surface profilometer complies with ANSI B46.1 specifications for surface roughness and waviness. Using Dektak it was possible to measure both waviness and roughness with data points of 500, scan resolution 10μm/sec. The roughness and waviness were filtered out from the trace by high pass and low pass filtering respectively. The chosen cutoff frequency was 50μm/sec (cutoff frequency = $\frac{1}{100 \cdot (scanlength)}$) as suggested by Chi et al. [39].

Dektak was therefore used in our experiments to take simple roughness measurements, but also curvature and waviness for bonded substrates which help in the assessment of the quality of two bonded substrates.

3.3.4 XRD

X-ray diffraction is the result of the conversion of electron beam into x-ray photons. Its operating principle of crystal structure detection is based on Bragg's diffraction law (see equation 3.1) which is used to explain x-ray beam reflection at certain angles.

$$2dsin\theta = n\lambda \tag{3.1}$$

Where d is the interplanar spacing, n is an integer determined by the order given, θ is the angle between the incident ray and the scattering planes and λ is the wavelength of the x-rays. d spacings depend on the cell size, they determine the position of the peaks. Peak intensity is caused by crystallographic structure, atom position and thermal vibration of elementary cell. Figure 3.5 shows the principle of x-ray scattering based on Bragg's law.

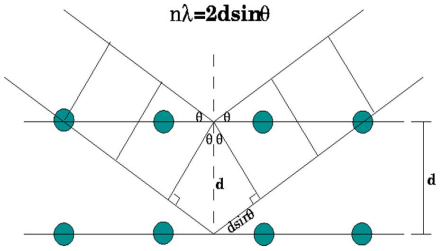


Figure 3.5: Principle of Bragg's law x-ray scattering from [314].

X-ray diffraction method can only be used for materials in which the arrangement of the atoms has a regular pattern. These encompass organic and inorganic crystalline materials which make up to 95% of solids.

A Siemens D5005 X-ray diffractometer with scan size 10x5mm was used in our experiments. This uses Bragg-Breantano geometry and a Cu $K_{\alpha l}$ X-ray diffractometer for the study of single crystal and thin film phase and crystal orientation characterization. The instrument is made of the following components and is shown in figure 3.6: goniometer (allows rotation of sample holder and detector), detector, monochromator (used as a filter to stop k_{beta} radiation and diffract only k_{alpha}) and stage.

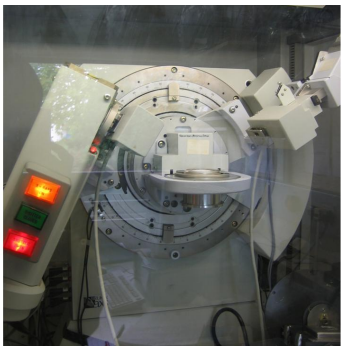


Figure 3.6: An x-ray diffractometer from [274].

X rays are produced in an x-ray tube. The tube consists of two metal electrodes enclosed in a vacuum chamber. Electrons are produced by heating a filament cathode (for the Siemens we use this is a copper filament) which is at high negative potential. The electrons, thus, accelerate towards the water-cooled, ground potential anode. X-rays are the manifestation of the loss of energy of this impact [267]. In order to collect the data, the sample and stage are rotated up to 180°, while an image sensor records the reflection intensities.

The continuous spectrum is caused by the constructive interference produced by x-ray/electron collision with the target atoms and loss of energy. Constructive interference means that the diffracted beam's scattered ray waves are in phase and, therefore, reinforce one another producing a diffracted beam [242].

Rocking curves

In order to analyse the intensity of the crystal at a specific 2θ angle rocking curves are ideal. This method involves the use of an x-ray diffractometer where the incident angle is fixed and the reflected angle is varied. The stage holding the sample will rock back and forward between two specific angle values between which we can find the desired crystal value and intensity.

3.3.5 Electrical and microwave testing

The dielectric constant, dielectric loss and resistance of materials are measured on a Wayne Kerr precision component analyser 6425 and two probes. The instrument allows for measurements to be taken between 30Hz and 300kHz frequency. The set frequency and impedance were calculated directly by the device.

For high frequency measurements in the 30kHz-3GHz range on transmission line structures (coplanar waveguides (CPW)) defined on the substrate, a Hewlett Packard Vector Network Analyzer (VNA) HP8753D was used. For this two-port network a swept (or continuous) RF source electrically excites the device to get piezoelectric resonance through transmitted and reflected power properties and the VNA records these electrical signal response characteristics.

3.4 Modeling and simulation

Two software packages have been used for simulation of fabrication effects and device functions: Matlab® and ANSYS Workbench®. Matlab® was also used to retrieve scattering parameter data from the VNA for post-processing.

Among fabrication parameters thermal effects on film stresses will be considered, while structural resonant frequency will be the main device function feature. The relevant material properties used in the simulation are shown in the Appendix.

The stresses and strains in the simulations are expressed in Von Mises which is the equivalent stress often used in design work as it allows the representation of an arbitrary 3D stress state to be done as a single positive stress value. Equivalent stress is related to the principal stresses by equation 3.2 [164].

$$\sigma_{VonMises} = \frac{1}{\sqrt{2}}\sqrt{(\sigma_x - \sigma_y)^2 + (\sigma_y - \sigma_z)^2 + (\sigma_z - \sigma_x)^2 + 6\tau_{yz}^2 + 6\tau_{zx}^2 + 6\tau_{xy}^2} \tag{3.2}$$

Equally, Von Mises strain and be defined as the equivalent strain taking into account the three dimensions. It is represented by the equation 3.3 [164].

$$d\epsilon = \frac{\sqrt{2}}{3}\sqrt{(d\epsilon_x - d\epsilon_y)^2 + (d\epsilon_y - d\epsilon_z)^2 + (d\epsilon_z - d\epsilon_x)^2 + 6d\gamma_{xy}^2 + 6d\gamma_{yz}^2 6d\gamma_{zx}^2} \tag{3.3}$$

3.5 Conclusions

This chapter has given us an insight to the upcoming methods used for device fabrication and analysis. MEMS fabrication equipments have been introduced and their basic principles explained. While sputtering and evaporation are deposition methods, photolithography is used for device patterning, and etching is employed when certain materials need to be removed.

AFM, SEM, FIB, Dektak and XRD are all surface metrology methods employed to analyse surface topography, material composition or quality. AFM, SEM, FIB and Dektak provide topographic information of a sample. SEM can also distinguish a material composition within a substrate. XRD gives information on both the materials present in a sample and their quality, based on the relevant material's peak intensity.

Part II

Results

Chapter 4

Preparation of Liquid Crystal Polymer foils for MEMS processing

4.1 Introduction

The aim of this project is to create front and back processed FBARs on LCP. As we can see from figure A.1, the standard method to produce these free-standing piezoelectrically actuated resonators is quite complex. The fabrication of FBARs on LCP can be even more intricate (see figures A.2 and A.3) because, as we will see in this chapter, it requires some extra steps for substrate "standardisation".

Successful fabrication of MEMS devices on wafers imposes some conditions on the properties of the substrate. The processing of MEMS devices requires that the substrate used for subsequent processing can be easily handled. Examples of particular relevance to this study are the flatness and smoothness of the substrate.

If the substrate flatness is poor there can be difficulties in the subsequent processing steps, particularly in photoresist spinning and in the use of an aligner for registering patterned layers to one another. Non-flat wafers can arise due to the intrinsic nature of the substrate or caused by the addition of layers which have significant stress causing the wafer to bow. If the wafer bow is too large, then the vacuum of the spinner and aligner chucks cannot overcome the bowing forces.

Another condition for substrate processing is for the sample to be smooth. Smoothness of a substrate is crucial for subsequent material deposition steps as deposited thin films conform to the substrate topography. For an appropriate piezoelectric material functioning, for example, the grains grown need to be perpendicular to the surface. A rough substrate would not allow successful perpendicular c-axis grain orientation.

In order to address the above issues of flatness and smoothness, pre-processing schemes are required for our new flexible and rough LCP samples. Some FBAR process flows are explained in Appendix A..3.

4.2 LCP ULTRALAM series

ULTRALAM RFlex3850 and 3800 LCP were obtained from Roger's Corporation and delivered in 457.2x304.8mm panels. The former is a double-side copper (Cu) clad LCP, while the latter is bare LCP. Cu clad LCP is widely used for patterning features such as transmission lines, antennas and phase shifters in Printed Circuit Boards (PCBs). The Cu can be etched in ferrochloric acid ($FeCl_3$) 38°Bé at room temperature through a two-step redox reaction [58]. Figure 4.1 shows cut LCP in its various formats, while figure 4.2 demonstrates the cross-section of the LCP types.

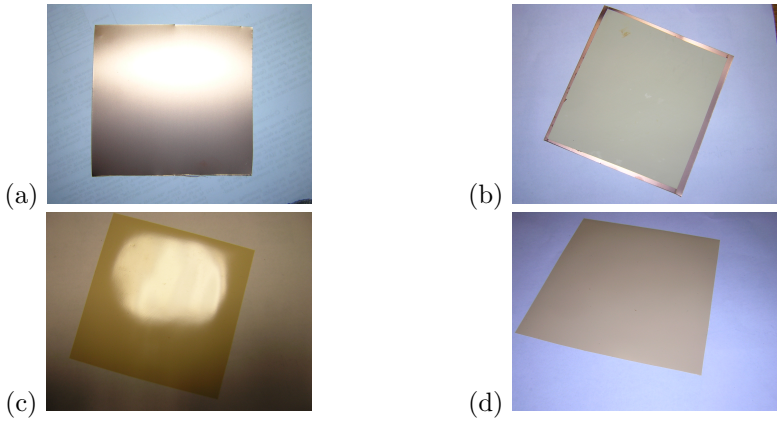


Figure 4.1: a)ULTRALAM3850 with Cu clad, b)ULTRALAM3850 with Cu clad removed from one side, c)front of ULTRALAM3800, d) back of ULTRALAM3800.

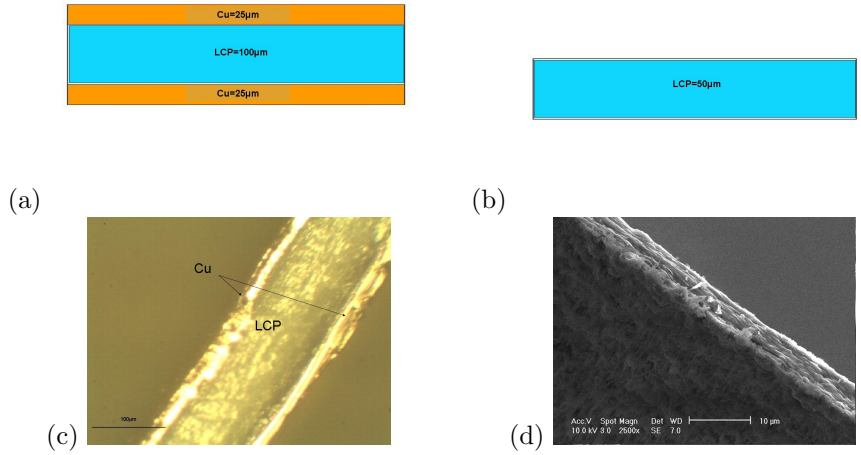


Figure 4.2: Cross sectional sketch of: a) ULTRALAM3850, b) ULTRALAM3800, cross sectional SEM view of: c)ULTRALAM3850, d)ULTRALAM3800.

4.3 Rigid backing for LCP flatness

It is essential to have a planar surface throughout processing as a non planar sample makes standard manufacturing steps such as spinning and alignment tasks impossible to achieve. Wang et al. [293] also observed difficulty in processing of a compliant LCP substrate. LCP is a flexible substrate and thus, by nature, unplanar as it is susceptible to bending when handled for processing. Process-induced LCP deformation is a common occurrence as handling, heat and coating-induced stresses all contribute to substrate deformation. As we will see, there are two parameters that make up flatness: waviness and curvature. The measurement and analysis of these two variables will be carried out due to its importance relating to the way they affect future processing steps.

S. Wagner [235] noticed the necessity of some sort of rigid backing as the processing steps cause the substrate to bend into a roll. To this end, we investigated a few ways to keep the LCP flat. These included: the use of the pre-existing Cu clad, the rigidity enhancement of the Cu with electrolated nickel (Ni) and rigid substrate backing through the attachment of glass or silicon. One possible planarisation method that was not tested due to process impracticality is tensioning the sample by mounting it on a carrier frame.

Both experimental and numerical quantification of waviness and curvature will be carried out for the rigid backing method (which proved to be the most successful approach). Quality assessment of bonding includes both LCP waviness and multilayer curvature measurements. Flatness, which encompasses low waviness and high curvature radius, is what we want to ultimately achieve.

4.3.1 Flexural rigidity

It is important to quantify the flatness parameter as it greatly affects device processing. Since, in our case, the flatness issue arises due to substrate flexibility. This means that under a given stress, the material deforms more than a stiff material. The parameter is quantified through rigidity calculation where, for a 4inch wafer, we consider the moment of inertia of a solid cylinder.

Rigidity of the multilayer is what needs to be achieved for the processing and measurement stages. Rigidity can be defined as the inflexibility (or resistance) to change. The parameters that affect rigidity are material density and Young's modulus. In order to find how much the rigidity affects the curvature we calculate rigidity (Rig) with equation 4.1.

$$Rig = E \cdot I \tag{4.1}$$

$$I = \int r^2 dm \tag{4.2}$$

Where I is the moment of inertia, E is Young's modulus, r is the radius of the wafer and m is the mass. Moment of inertia is the rotational analogue for linear mass and it describes the resistance of an object to changes in its rotation rate.

We assume our substrate to be a solid disc and the axis to be about its central diameter as shown in figure 4.3. Therefore moment of inertia equation becomes 4.3.

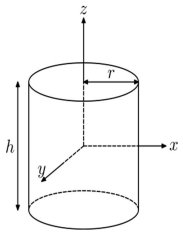


Figure 4.3: Solid cylinder with x,y,z coordinates.

$$I_x = I_y = \frac{1}{12} m(3r^2 + h^2) \tag{4.3}$$

From the above equations it is evident that with an increase of substrate thickness (h) rigidity (Rig) increases as well. Table 4.1 shows the rigidity calculation of each of the substrates involved in our samples. The parameter is affected by: Young's modulus, thickness and density of the layer.

Table 4.1: Rigidity of single material layers and combination of layers

Layer	**Young's modulus (GPa)**	**Thickness (m)**	**Radius (m)**	**Moment of inertia (Kg/m^2)**	**Rigidity (GPaKg/m^2)**
LCP	2.255	1x10^{-8}	0.045	4.5x10^{-7}	1x10^3
Cu	110-128	18x10^{-6}	0.045	5.2x10^{-7}	57x10^3
Ni	200	1x10^{-8}	0.045	2.9x10^{-6}	573x10^3
Si	150	4x10^{-8}	0.045	3x10^{-6}	450x10^3
Glass	69	5x10^{-8}	0.045	2.9x10^{-6}	183x10^3
LCP/Si	152.255	6x10^{-8}	0.045	4.8x10^{-6}	454x10^3
LCP/Cu/Si	262.255	6.25x10^{-8}	0.045	5.3x10^{-6}	511x10^3
LCP/Glass	66.255	6x10^{-8}	0.045	4.7x10^{-6}	187x10^3
LCP/Cu/Glass	176.255	6.25x10^{-8}	0.045	5.2x10^{-6}	245x10^3

4.3.2 Copper clad backing and nickel electroplating

For the Cu clad case the 25μm copper clad is kept on one side as a backing against process-induced LCP deformation. Cu clad backing could, later in the process, be used as an etch mask in RIE back etch for example. Using Cu as a mask for back-etching was also suggested by Hess et al. [88] as it allows saving processing time and ensures a better masking than photoresist.

In my experiments this method allowed the achievement of devices but did not always give enough support for the wafer to easily undergo some fabrication steps such as polyimide coating (see figure 4.4 a). This is why Cu clad thickening through Ni electroplating was investigated.

In order to thicken the substrate, nickel (Ni) can be electroplated on the (25μm) Cu clad. Here Cu is used as a seed layer for Ni electrodeposition. Electroplating consists in separating the elements of a compound by passing an electric current through a solution and it follows Faraday's law of electrolysis. The electroplating solution was made of nickel sulfamite (300g/L), boric acid (40 g/L), nickel chloride (10g/L) with 2L de-ionised water. Nickel can also be used as an RIE etch mask.

The rate of deposition, when electroplating, is controlled by the current. The higher the current, the higher the deposition rate. The equipment allowed up to 100mA of current to be generated and, with the employed electroplating settings (see table A.9 in Appendix A..1), a current of 38mA gave 1μm/hr Ni [private communication]. According to the calculations and table 4.1, 100μm of Ni should, in theory, provide more than enough rigidity hence, both 50μm and 100μm of Ni were deposited on the Cu.

Prior to electroplating, the front of the LCP/Cu samples is attached to a rigid Si substrate in order to avoid any stresses, arising from the Ni electroplating, to deform the substrate. According to Luo et al. [175] a current density of $\approx$1.4mA/cm^2 (which is what we have used) yields intrinsic compressive stress of around -100MPa. This would mean that, if stresses of similar magnitude are

experienced at the front of the wafer, a stress compensation and equilibrium would be reached. Figures in 4.4 show the same sample (sample 6) before and after Ni electroplating. The sample flattens as the extra Ni layer adds a certain degree of rigidity to the overall structure (see table 4.1).

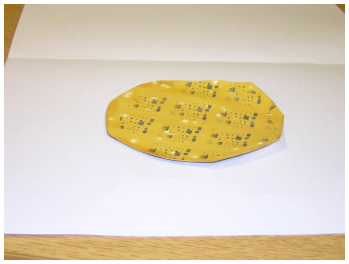
(a)  (b) 

Figure 4.4: Backing on semi-processed wafers: a) 25μm Cu clad without Ni backing, b)25μm Cu clad and 50μm electroplated Ni.

The electroplated Ni occasionally peels off the Cu and this delamination starts at the edges as shown in figure 4.5.

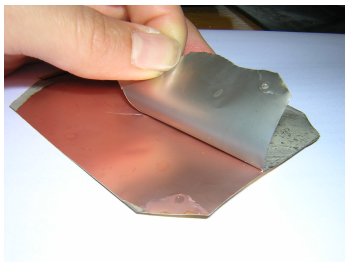


Figure 4.5: Delamination of nickel from Cu.

Pickling of Cu prior to Ni electroplating was tested as a method of adhesion enhancement between Cu and Ni whereby the sample was dipped in a pickling solution (presented in Appendix A..1) for 10s. The immersion of metals in an acid solution is known to remove surface fire scale and oxides. Pickling showed an improvement in adhesion quality as the Ni did not peel off anymore. Adhesion quality was also studied with a peel test at a 30° angle after removing the electroplated Ni and sputtering Ti-Au at its back. As we can see from figure 4.6, the untreated Cu causes oxides formation on its surface to affect the adhesive quality of Ni (verified by the Ti-Au peeling off), while, when the Cu is treated, the Ti-Au does not peel off.

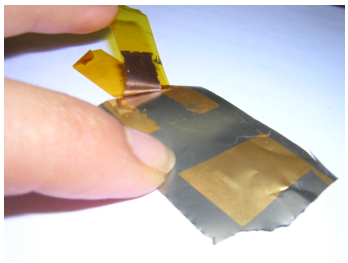
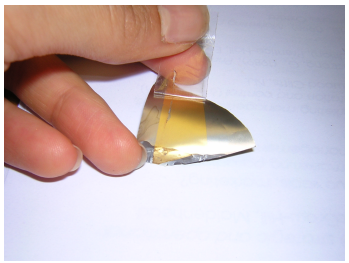
(a)  (b) 

Figure 4.6: Peel-off adhesion test for: a)untreated Cu, b)pickled Cu.

Neither Cu nor Cu-Ni backing of LCP showed to be reliable backing methods as the substrates still deform when subjected to high stresses induced by polyimide or photoresist deposition.

4.3.3 Rigid substrate backing

A viable backing method is essential in order to make the LCP easy to handle. LCP backing with silicon (or glass) through temporary attachment with photoresist and black wax was investigated. The method has already been adopted by Wang et al. [293], Hess et al. [88], Wang et al. [292], Zhang et al. [316], Wang et al. [292]. Bonding of the rigid substrate should be of enough high quality to withstand the following processes without detaching: bottom electrode deposition and patterning, ZnO deposition and patterning, top electrode deposition and patterning and backs-side pattern and etch.

Methods of substrate assembly

In our experiments various processes have been adopted to achieve maximum bond strength between LCP and Si (or glass).

First 2mL photoresist (or black wax) is applied to the wafer (glass or silicon) and the LCP spun at 3000rpm for 30s, cured at a temperature 90-120°C (preferably 115°C) for 30sec to drive off solvent and then the substate and LCP are attached and put on a hotplate at 100°C (minimum temperature required for wafer bonding). Both AZ4562 and S1818 photoresists were tested concluding that the former yielded better bonding as seen from the acetone test. Here the LCP/photoresist/substrate multilayer was placed in acetone and the time required for the photoresist to dissolve was observed. When the photoresist dissolves, it leaves the two substrates detached. It takes the more viscous AZ4562 8min to dissolve, whereas S1818 dissolves after only 1min. Black wax was also tested and showed that, when providing good wetting, it does not cause LCP/substrate debonding since it does not dissolve in acetone.

Some samples were assembled at atmospheric pressure, while other experiments were carried out with the bonding occurring in a vacuum chamber. The absence of atmospheric pressure has, in fact, previously proven to yield better bonding strength. This method might make it possible to allow the voids between LCP

and Si, which expand cause trapped air and contamination deLaat et al. [54] problems when bonding the flexible substrates on rigid ones. Methods of substrate assembly are discussed below.

- **Hotplate**. After photoresist deposition, attach two substrates together and put following on top: Si wafer (to keep planar and spread the weight evenly), cloth (as barrier for heat to dissipate in the metal weight), 20kg weight. Leave on hotplate at ∼100°C for 5-10min allowing the parts to attach. When sample weights are loaded onto hotplate, they act as a heat sink, causing heat dissipation through them. It is therefore important not to not start the 10 minute countdown until hotplate temperature has settled back to 100°C again. Bonding is carried out at atmospheric pressure (101,325 Pa). Figure 4.7 shows the setup.

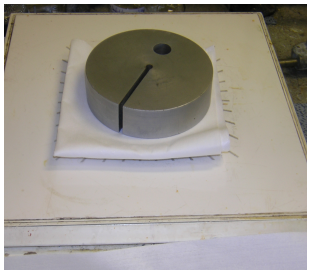


Figure 4.7: Hotplate bonding setup image.

- **GallenKamp Vacuum Oven**. The substrate is sandwiched between two glass masks and the assembly left in the chamber set at 100°C. The assembly is left to heat for 3hours after the chamber is pumped down to pressure 13.25mbar (2hrs) before the 20kg weight is put on. This is done because heat transfer occurs more slowly in vacuum environments and more time is needed to get the sample inside the oven up to temperature. The sample is left inside the vacuum oven for 5hrs. Figure 4.8 shows the setup inside the Gallen Kamp vacuum oven.

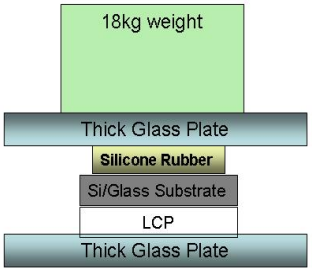


Figure 4.8: Assembly inside the vacuum oven.

- **Tailored vacuum bonding**. The difference with the GallenKamp vacuum oven method is that the substrate assembly is carried out within the vacuum environment, not manually. This is better because the bonding occurs inside the vacuum chamber, allowing, thus, for all the contaminants and voids to be pumped out before the bonding takes place. A 15 minute pumpdown of the jig at room temperature is required to reach a pressure of 1mbar, prior to high temperature treatment. The jig is then placed on the hotplate (T$\sim$100°C) while still connected to the vacuum line for a further 15 minutes. Figure 4.9 shows the home made vacuum jug setup.

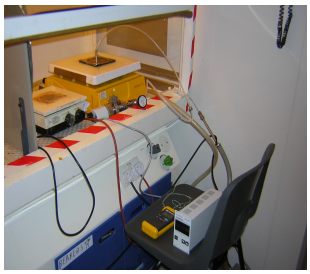


Figure 4.9: Home made vacuum bonding setup image.

Waviness measurement of substrate/adhesive/LCP multilayer

Waviness analysis is essential as it indicates the quality of the bonding between the layers, implicitly disclosing information about adhesive quality and bonding

method efficiency. A poorly bonded composite would show voids which would, later in the processing steps cause problems such as outgassing, de-bonding and misalignment. It is, therefore, important to keep these voids at a minimum.

We used glass substrates in order to visualise the voids causing waviness (average waviness Wa considered) and figure 4.10 gives us an idea of what these might look like. Figure 4.10 a) shows the back of the hotplate-bonded wafer, while b) shows the back of the vacuum-bonded wafer. We see less trapped voids in the latter, signifying a better bonding. Average waviness decreases by about 1μm (as given from Dektak scans in table 4.2).

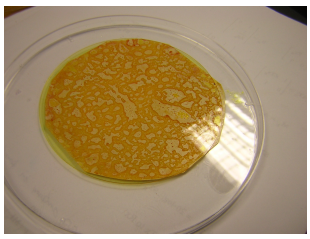
(a)  (b) 

Figure 4.10: Voids at back of a)hotplate bonded sample with average waviness Wa=2.63μm, b)vacuum oven bonded sample with Wa=1.50 μm.

Adhesion improvement was quantified through waviness measurement with surface profiling scans to quantify void formation. The available resource for waviness measurement in our case was a Dektak surface profiler, used at a a scan size 5mm (for waviness detection).

Table 4.2: Flatness measurement of uncladLCP/Si with Dektak scan size 5mm.

Bonding method	$\mathbf{W}_a(\mu\mathbf{m})$	$\mathbf{W}_q(\mu\mathbf{m})$	$\mathbf{W}_{maxdev}(\mu\mathbf{m})$
Hotplate bonding with photoresist	5.4	6.15	14
Hotplate bonding with black wax	3.37	3.98	9.72
GallenKamp bonding with photoresist	1.50	1.92	4.10
Tailored vacuum bonding with photoresist	0.80	1.12	1.7
Tailored vacuum bonding with 3μm black wax	0.32	0.41	1.4
Tailored vacuum bonding with 7μm black wax	2.63	3.24	9.50
WaferBond^{TM} HT adhesive	3.29	3.85	9.1
Tailored vacuum bonding with 1μm black wax, (ULTRALAM3850)	0.032	0.038	0.096
Tailored vacuum bonding with 1μm black wax, (ULTRALAM3800)	0.17	0.24	0.61

The hotplate bonding yielded the worst results because both the assembly and the bonding stages were carried out in atmospheric pressure environments. The GallenKamp oven results were slightly better since the bonding stage was carried out in vacuum at a pressure of 13.25mbar. The sample which showed the least amount of waviness was the Cu-clad ULTRALAM3850 vacuum-bonded to Si in the home-made jig with 1μm black wax. The waviness measurements, taken over a range of 5mm, show that the best method is tailored vacuum bonding with 1μm black wax in order to achieve as little waviness as possible (see table 4.2).

From the results in table 4.2 we can also derive a few other points. For example, using the same bonding method (tailored vacuum bonding) adhesive (1μm black wax) and substrate (Si), the Cu-clad LCP (ULTRALAM3850) yielded lower waviness Wa=0.032μm, than the unclad LCP (ULTRALAM3800) Wa=0.17μm. This can be explained by the fact that Cu-clad LCP is more rigid due to the extra Cu layer (see table 4.1) which helps holding the LCP more uniformly during its bonding with the substrate.

Furthermore we can say that bonding in vacuum improves the adhesion between the LCP and the rigid substrate, which is why others [277] also opted for this solution. Waviness quantification is a consequence of how many voids are trapped between the LCP and the glass or silicon. In conclusion we can say that the use of substrate, adhesive and LCP type are all important factors in order to gain low waviness and, therefore, good LCP/substrate adhesion.

Curvature measurement of substrate/adhesive/LCP multilayer

Besides waviness, curvature is another parameter that contributes to substrate flatness. A low radius of curvature (or high bow) can affect critical processing stages such as alignment and material grain growth. Curvature (a consequence of thin film and process-induced stresses) can, in fact, cause many problems such as: incompatibility with existing manufacturing equipment, device misaligment, failure of the piezoelectric ceramic such as cracking and piezoelectric material undesired prestressed state.

The bow can make wafer processing (i.e. spinning on chuck, alignment etc.) very difficult. High vacuum tailored bonding showed to yield a strong wafer bow in the structure. Although we cannot be sure about the cause for this, as it was not observed with other mounting techniques, the initial guess can include one or more of the following reasons: flexing of jig, lack of flatness of plates used to press wafer against and thermal expansion mismatch.

Curvature of the glass/black wax/Cu-LCP stack was measured with Dektak surface profiler. A Matlab code for equation 4.4 was written (as shown in Appendix A..8) based on the theoretical model presented by Townsend et al. [279] whose particular interest was the approximation for the case of thin films on a thick substrate. Their approach considers all effects including TCE (thermal consideration) on the curvature of a multilayer. They found the curvature value (κ) for a composite of thin films on a thicker substrate by highlighting the effect of each individual layer on the substrate described by equation 4.4 [279].

$$\kappa = \frac{\Delta T \sum_i E_i \gamma_i \frac{t}{2} [-\alpha_i + (\sum_j E_j t_j \alpha_j \div \sum_j E_j t_j)]}{\sum_i E_i t_i [(\frac{Nt}{2}) - (\frac{t^2}{3}) + (t - N)\frac{\gamma_i}{2} - \frac{1}{12}(3\gamma_i^2 + t_i^2 - t^2)]} \tag{4.4}$$

Where: α is the layer thermal expansion coefficient, E is the layer's Young's Modulus, ΔT is the annealing and ambient temperature difference, t is the total thickness of the composite, N is the neutral axis, z is coordinate distance normal to the linear dimension of the composite, γ is the total thickness subtracted by the coordinate distance normal to the linear dimension of the composite.

We applied the equation to predict the curvature for the different material stack combinations. Table 4.3 shows the validation of the experimental values (the measured curvature with Dektak) and the theoretical values (calculated for various multilayers with equation 4.4) for a tailored vacuum-bonded sample using 1μm black wax for high quality bonding at 100°C.

Table 4.3: Experimental and theoretical radius of curvature results for vacuum-bonded LCP to silicon with 1μm black wax (units=m).

Multilayer	**Measured (experimental)**	**Calculated (theoretical)**
LCP(100μm)-Cu(25μm) /blackwax/Si	-	35.0019m
LCP(100μm)/blackwax/Si	23.6m	26.1670m
LCP(50μm)/blackwax/Si	34m	52.7759m
LCP(100μm)-Cu(25μm) /blackwax/glass	3.12m	3.12m
LCP(100μm)/blackwax/Glass	-	11.5662m
LCP(50μm)/blackwax/Glass	-	23.0370m

From table 4.3 it is evident that the analytical values provide a good fit to the experimental results as they are in the same order of magnitude. The slight discrepancies can be due to either experimental factors (i.e. errors during measuring), or modeling inaccuracies. The model, in fact, does not account for the following:

- Lateral (x and y) dimensions as the model only accounts for thickness direction sizes.
- Non-linearities such as non-linear thermal factors and temperature distribution, which might play a role in the final bowing of the substrates.

However, the validation of the theoretical fit to the experimental results showed relatively good correlation between the two. This is why the model represented by equation 4.4 [279] was used to carry parametric studies for assessing the effect of different factors on the multilayer curvature. The parameters which determine the multilayer curvature are generally known to be:

- TCE mismatch among layers, which produces an inelastic thermal strain in the individual layers.
- Rigidity of composite which is determined by: E, thickness and density.

It is essential to determine the future device fabrication on the rigidly-backed LCP at this pre-processing stage and the study will help in having an initial idea of the future device yield in terms of alignment accuracy as the radius of curvature is proportional to alignment accuracy.

EFFECT OF MOUNTING SUBSTRATE ON CURVATURE: GLASS VS Si

Table 4.4 compares the difference of using glass or Si as a substrate. This study will be the basis for our future choice of rigid backing.

Table 4.4: Simulation of curvature when LCP bonded to glass or silicon as a rigid substrate.

Adhesive	**LCP type**	**Curvature on Si(m)**	**Curvature on glass(m)**
black wax 1μm thick	unclad 100μm LCP	26.1670	11.5662
black wax 1μm thick	25μm Cu cladded 100μm LCP	35.0019	3.4938
black wax 1μm thick	unclad 50μm LCP	52.7759	23.0370

Although the differences in curvature are not strikingly large, for all cases the radius of curvature of the composite on silicon is higher than that on glass, meaning that the composite bows less on silicon. This can be explained by the higher Si rigidity which, in turn, is given by its higher stiffness (Young's modulus). This suggests that it is the Young's modulus (stiffness) of the substrate that plays an important role especially as the TCE and the thickness of silicon (other determining parameters for curvature analysis) are very similar to that of glass. Si has almost double the Young's modulus value of glass.

Rigidity of the substrate is crucial, as we observe for the Cu-clad silicon substrate case. The extra 25μm Cu layer increases the overall thickness of the composite and adds rigidity, thereby increasing the radius of curvature for the silicon substrate case. With glass substrate, however, the curvature radius decreases with the addition of the Cu clad, suggesting that TCE mismatch among the layers has an overpowering effect upon the rigidity which is not resisted enough by supporting substrate stiffness. For these reasons the use of Si is preferred over glass. However for cases where features are meant to be seen, such as front to back alignment for back patterning of substrates, the use of glass will be unavoidable.

PARAMETRIC MODELING OF MULTI-LAYER CURVATURE

Parametric studies are carried out with the model suggested above in equation 4.4, in order to assess the parameters and the extent to which these affect the composite. This analysis will allow the assessment of the degree to which the encountered independent variables of the composite structure (adhesive thickness, LCP thickness, presence/absence of Cu, TCE of mounting substrate, E of mounting substrate), affect its curvature.

- **Effect of substrate TCE variation on overall composite curvature**
  For these simulations assume LCP thickness 100μm, black wax 1μm, pyrex glass thickness 500μm.

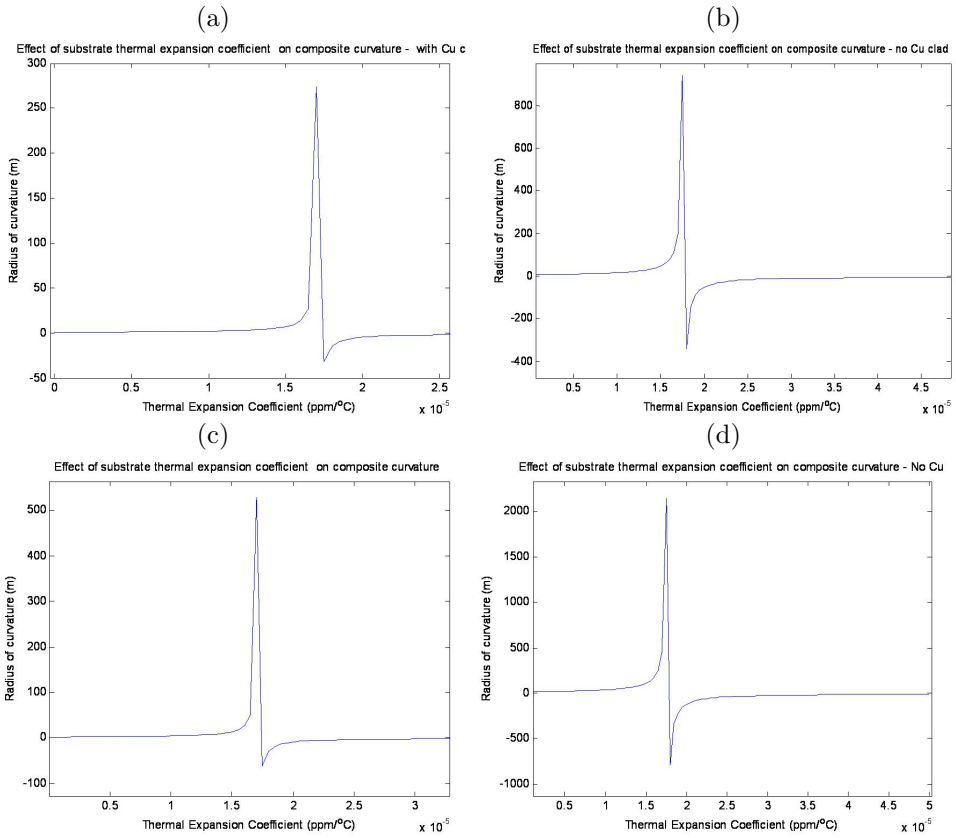


Figure 4.11: Composite curvature with respect to TCE variation of LCP: a) on glass (Cu clad LCP), b) on glass (unclad LCP), c) on silicon (Cu clad LCP), d) on silicon (unclad LCP).

For the glass substrate case (given E_{glass}=64GPa) from figure 4.11 a) we can see that with 25μm of Cu clad present, the optimum TCE would be 17ppm/°C reaching κ=274.4m, while from figure 4.11 b) for unclad LCP, the optimum substrate TCE would be 17.5ppm/°C reaching κ=939m. Past the TCE values mentioned the radius of curvature decreases. For the Si substrate case (given E_{Si}=150GPa) from figure 4.11 c) with 25μm of Cu clad of present, the optimum TCE would be 17ppm/°C reaching κ=529.5m, while from figure 4.11 d) for the unclad LCP, the optimum substrate TCE would be 17.5ppm/°C reaching κ=2147m. Past the TCE value mentioned the radius of curvature decreases.

The magnitude of the composite curvature is different when using silicon and glass, but the essential behaviour is the same. The silicon maximum radius of curvature (κ) is higher than that of glass for both cladded and unclad cases. This is due to the silicon's larger Young's modulus and, therefore, the composite's higher overall rigidity. We can conclude that as the TCE of the substrates increases to match that of either LCP or Cu, the radius of curvature increases to its maximum point which for the un-

clad case is (197.7m for glass and 2147m for silicon) while for the cladded case is 274.4m (529m for silicon).

For both glass and Si the radius of curvature is higher when cladded LCP is employed due to increase in composite structure's stiffness. After the peak curvature point, this drastically decreases into the negative curvature region, suggesting that if the substrate's TCE is larger than that of the LCP or Cu, the composite structure bows downwards. Negative curvature simply means that the vertex of the substrate lies to the right of the centre of curvature, where the radius of curvature is the distance between the centre of curvature and the vertex. Contribution of substrate TCE variation to overall composite radius of curvature is drastic and has a large effect on the bowing, which is why it is important to find a substrate which as similar TCE to that of the material it is being bonded to (i.e. LCP or Cu). The results also show the same cut-off substrate TCE for both Si and glass substrates (17 and 17.5 ppm/°C), but with different radius of curvature magnitudes. The radius of curvature is lower for the cladded case. This might be due to the low TCE of the material which does not counterbalance the high TCE of the substrate/adhesive matrix. Despite the magnitude of the composite's radius of curvature being different when using silicon or glass, since the behaviour of radius of curavture VS TCE is the same for both Si and glass, parametric studies from now on will consider only one of the substrates.

- **Effect of bonding layer thickness variation on composite curvature**
  In the experiments, the bonding layer (photoresist or black wax) thickness is varied from 1-3μm. The effect of the bonding layer thickness on the composite curvature is then assessed in order to understand the extent to which the curvature changes with given TCE and E. Assume LCP with thickness of 100μm and substrate thickness of 500μm.

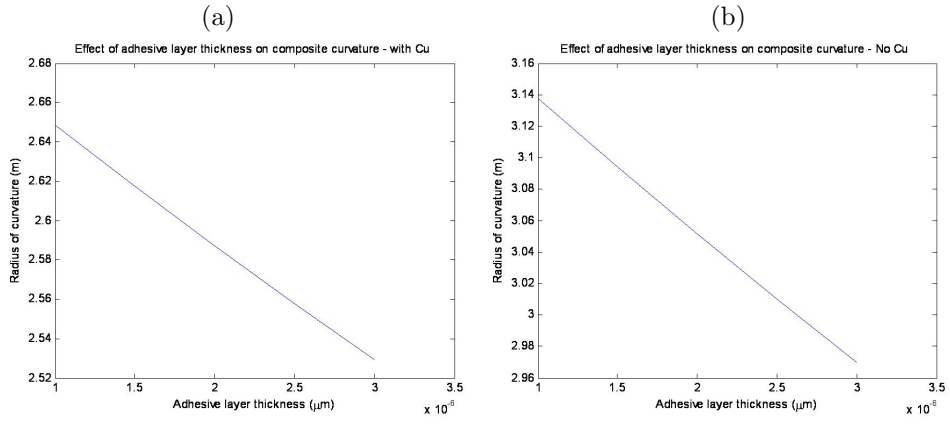


Figure 4.12: Bonding layer thickness effect on curvature a) with Cu b)without Cu.

Black wax thickness is inversely proportional to the multilayer radius of curvature for both unclad and Cu clad cases. This is because of its high TCE causing a thermal mismatch between layers. For Cu clad LCP, the radius of curvature is slightly lower (bowing larger) than for the unclad case.

- **Effect of LCP substrate thickness variation on overall composite curvature**
  For these simulations assume substrate thickness 500μm, black wax thickness 1μm while the thickness of the LCP is varied between 0 and 5mm.

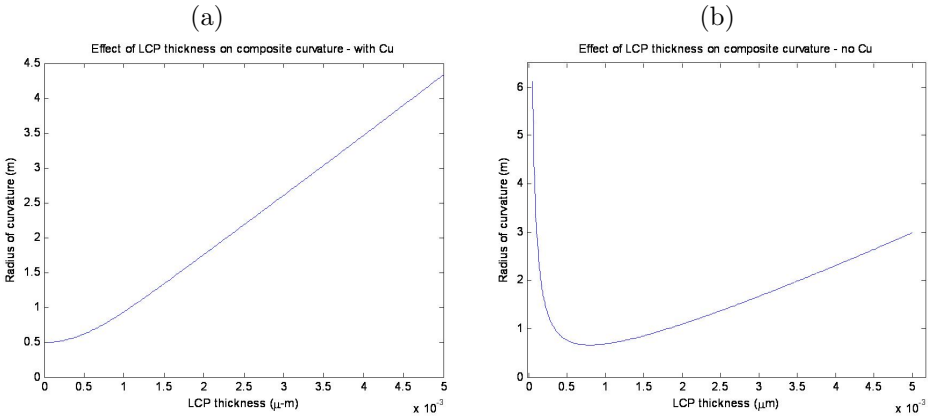


Figure 4.13: LCP thickness effect on curvature a) with Cu b)without Cu.

In general the variation in curvature with respect to LCP thickness is very small in both unclad and cladded cases because of LCP's low stiffness leading to its small contribution to overall rigidity. From figures 4.13 we can conclude that for cladded LCP, the bowing progressively decreases quasi-linearly with respect to LCP thickness which can be explained by the neutral axis shifting and, therefore, rigidity increase. For unclad LCP, however, the behaviour is different as, with increasing LCP thickness, the total composite curvature decreases down to a certain range, for then increasing again. For unclad LCP, a thickness of about 50μm (on glass) yields the lowest multilayer radius of curvature of 0.66m to then increase for LCP thickness of 780μm. This can be a consequence of the increase in position of the neutral axis plane (beneficial) dominating over the degrading TCE mismatch effect past the 500μm LCP thickness. For the unclad case, LCP thickness between 780μm and 5mm the radius of curvature increases as a consequence of an increase in neutral axis plane which is a sign of increase in multilayer thickness and, therefore, rigidity. The maximum radius of curvature of 6m was reached for the unclad case when the LCP is relatively thin. For both cladded and unclad cases, we can conclude that LCP thickness does not seem to play a major role on the effect it has on the radius of curvature.

- **Effect of substrate Young's Modulus variation on overall composite curvature**
  This study was carried out in order to analyse the effect of a potential substrate's E on the multilayer bowing. Assume substrate thickness 500μm, black wax thickness 1μm and LCP 500μm. As we will see the effects of Cu clad versus unclad LCP are well presented and a conclusion is derived on the effect of cladding on curvature.

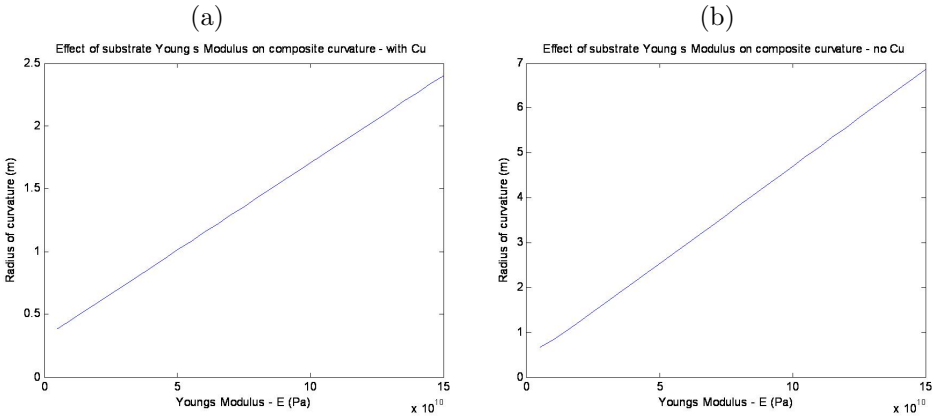


Figure 4.14: Substrate Young's Modulus effect on curvature a) with Cu b)without Cu.

From figure 4.14 we notice that the radius of curvature increases with increasing substrate stiffness. With the Cu-cladding the radius of curvature is lower than without the presence of the layer and the slope representing the increase in curvature w.r.t. Young's modulus is smaller indicating slower decrease in bowing. Intuitively, the extra Cu should make the multilayer more rigid due to an increase in overall thickness (higher neutral plane) and stiffness. This leaves us with only one other variable playing a part: TCE mismatch, which, has a negative influence on the composite curvature behaviour. The presence of the 25μm Cu should, in theory, increase rigidity but it has mostly a deteriorating effect on the multilayer due to its low TCE. This is the proposed theory as simulations show that by increasing the TCE of Cu (therefore assuming it is another material), the radius of curvature increases, signifying that a higher Cu TCE would counter-balance the high TCE effect from the substrate/adhesive matrix.

Observations on parameter effect on multilayer curvature

The importance of curvature analysis arises because of the later processing steps. In fact a low curvature (high bow) makes cleanroom processing a very hard task. Spinning and alignment steps are highly affected due to the vacuum not being able to keep the substrates in ideal contact with the chuck. Furthermore later alignment of devices is also affected.

Through curvature analysis, we found which parameters have positive and which ones have deteriorating effects on the multilayer bowing. By deteriorating we mean a decrease in radius of curvature. The results can affirm previous knowledge.

- High TCE mismatch between layers - deteriorating effect
- Increase in position of neutral plane by adding layers or increasing thicknesses - positive effect
- High thickness of each layer improves rigidity - positive effect
- High Young's modulus of each layer improves rigidity - positive effect

TCE of substrate has a great effect on curvature as also noticed by varying this value. The behavior showed highest curvature radius when the substrate TCE matched that of the LCP or the Cu. We also noticed how a high TCE caused by black wax during cool down, can counter-effect any positive effects of a composite's high rigidity. Bonding layer thickness had an inversely proportional relationship with curvature radius. LCP thickness did not have a dominant effect on multilayer radius of curvature due to its low stiffness which does not greatly contribute to overall rigidity. Substrate Young's modulus showed a major effect on curvature radius especially for the unclad LCP case. From the analytical curvature models, it is also evident that the radius of curvature for all cases was of a small order of magnitude, which should ideally be in the scale of x1000.

The ideal multilayer would be one which defeats the bowing effect, and should have the following characteristics:
Substrate: very high E, high density and TCE matching to that of LCP or copper. High thickness is also an option but it is not a preferred one due to incompatibility with microfabrication process equipment limitations.
Adhesive: low thickness and matching TCE with that of substrate and bonded layer (LCP o copper).

4.4 Observations rigid backing for LCP flatness

Despite table 4.1 showing that the presence of a 25μm Cu increases rigidity, the TCE mismatch between layers is so high when using Cu, that it nevertheless causes multilayer bowing. Simulations show that by increasing the TCE of Cu, the radius of curvature increases, meaning that the low curvature radius is a consequence of low TCE.

Cu cladding did not prove to be sufficient on its own for keeping the substrate flat at all times. Ni-electroplated Cu yielded better results in terms of low waviness. However, they are not fully acceptable for two reasons; first of all Ni adhesion to the Cu seed did not prove to be particularly good, second of all an eventual use of this metal as a mask for back etching contaminates the RIE chamber [private communication]. For these reasons, rigid (Si or glass) backing

will be considered for device production.

For the Cu-clad LCP case bonded to Si with black wax which, as we can recall, yielded the lowest (therefore best) waviness results, the high bow is due to a combination of the following factors: high bonding strength between the materials, high TCE difference between layers and low rigidity of the substrates.

Despite table 4.1 in section 4.3.1 showing an increase in rigidity with Cu presence, and from waviness measurement outcome being that a Cu-cladded LCP is best as it yields less waviness, in the parametric studies we noticed that the overall rigidity can be negatively counterbalanced by the presence of the Cu due to the high TCE mismatch between the layers. Therefore, from the curvature parametric models, we derive that an unclad LCP is best due to the higher radius of curvature. Thermal effects, which do not appear in the rigidity analysis or in the waviness measurements, must be accounted for during the bonding and fabrication stages.

We can conclude that the best bonding method is through the use of home made vacuum bonding at high temperature (100°C) with silicon using thin black wax layer. However, we must compromise waviness with curvature as the former is at its lowest when using Cu-clad LCP, while the latter parameter yields best results (high curvature radius) when using uncladded LCP.

4.5 LCP roughness reduction

After copper removal in $FeCl_3$, the LCP left on ULTRALAM Rflex 3850 series is very rough. Along with waviness and curvature, the problem of LCP roughness is also of essential importance and must be solved. Roughness can be defined as the measure of surface irregularities (asperities) and texture of a given sample, where the asperities are the vertical deviations of a surface from its ideal form.

Roughness of LCP substrate could cause fabrication issues such as poor quality thin film growth. AFM figures 4.15 show LCP measurements for both cladded (ULTRALAM3850) and uncladded (ULTRALAM3800) cases.

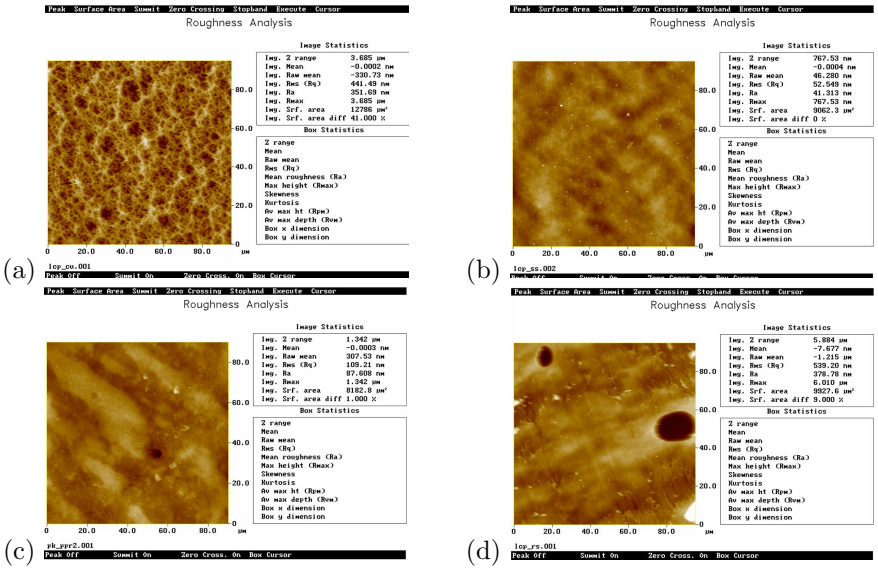


Figure 4.15: AFM measurements of a)ULTRALAM3850 (Ra=351nm), b)copper clad (Ra=41nm), c)front of ULTRALAM3800 (Ra=87nm), d)back of ULTRALAM3800 (Ra=378nm).

From figure 4.15 it is evident that, once the cladding is removed, UTRALAM3850 (a) is rougher than both the front (c) and back (d) of ULTRALAM3800. Figure 4.15 (b) is the AFM image of the Cu-Clad roughness. In general roughness may be the result of longitudinal and lateral forces generated during the material preparation [80]. Furthermore ULTRALAM3850 has a higher initial roughness than ULTRALAM3800 due to the method used for Cu-cladding. In order to clad LCP with Cu a surface adhesion improvement is needed which is often achieved by an O_2 plasma pretreatment of the LCP surface [316]. LCP roughness has previously been measured 190nm [292], 300nm [298].

The ideal roughness for radio frequency MEMS activation must be as close to 0 as possible. A roughness of 0.045-0.1nm is acceptable for FBAR applications [internal communication]. Smoothing is a process whereby the magnitude of surface irregularities is gradually reduced [261]. The surface roughness was minimised by Wang et al. [290] in two different ways: first with a covering method by using 3μm PI2610 polyimide spin, and second through a Chemical Mechanical Polishing (CMP) method using a lap polisher with 0.06μm slurry for 2hours. When speaking about roughness in our experiments it is important to keep in mind that short-range average roughness (Ra from nm to $\sim$100μm) is considered unless stated otherwise.

The importance of roughness tackling in MEMS fabrication arises due to the following reasons among many others:

1. Short range roughness scan size in nm leads to poor ZnO piezoelectric material grain growth (bad orientation) and, therefore, poor material quality and piezoelectric activity [11], [148]. Short range roughness, measured with AFM, occurs from the nm to 100μm range.

2. Long range roughness scan size μm leads to severe distortion of the metal-ZnO-metal structure on top of it, possibly giving rise to mis-alignment which can cause all sorts of problems (i.e shorted regions etc.). Long range roughness affects overall MEMS device production (photolithographic alignment) and performance. It does not have a major effect on grain growth. Long range roughness can be further described as the maximum surface peak height within the device area. Measurement of this parameter is up to 5mm and is carried out using Dektak stylus profiler.

The methods investigated to reduce the roughness of our LCP substrates were: polyimide coating, bis-trifluoromethyl phenol chemical polishing, hot pressing and lap polishing.

4.5.1 Polyimide coating

The method has previously been employed on LCP for the same purpose by Wang et al. [290] who started the process by prebaking their wafer at 90°C for 15s, spinning 3μm of PI2610 polyimide on LCP at a spin speed of 4000rpm (yielding film thickness of 1.3-4μm) and finally baking the wafer for 24hr at 90°C to ensure that solvents are driven out.

We followed the processes presented in Appendix A..1 where two different types of polyimide (with different viscosity values) were used. High spin speeds are needed to spread the viscous material evenly. The polyimide coating method proved to effectively reduce the roughness but it also causes high surface stresses as we will later see. Best process was Durimide deposited at 4000rpm for 45s and bake for 24hrs at 90°C. After polyimide deposition thickness was measured to be 11μm and Ra=5.6nm around the edges of the wafer, while at the centre the thickness was 15μm and Ra=0.02nm. Roughness at the center is less because when spinning, the thickness of the spun material is greater at the centre than at the edges [55]. A ramp time was needed since with a high viscosity substance better quality is given at lower acceleration and spinning time.

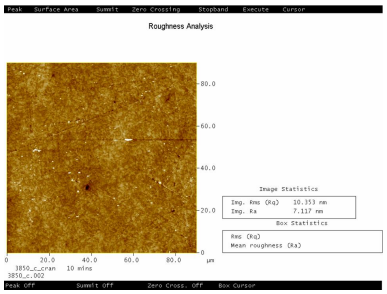
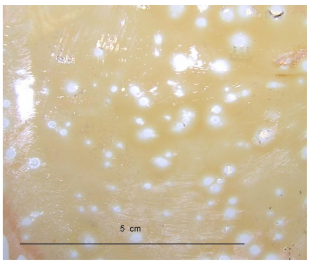


Figure 4.16: Roughness of Durimide-coated LCP at 2000rpm for 30sec. Surface average roughness (Ra) 7.12nm (at edge).

The deposition of polyimide is a very sensitive step as both the spinning and curing processes are susceptible to minimum variations and can condition the

final results. During the deposition process, in fact, bubbles might result in polyimide losing uniformity after spinning and curing (see figure 4.17).

(a) 

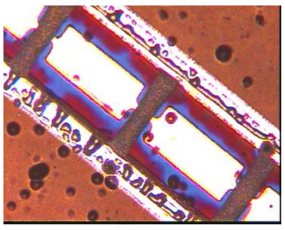
(b) 

Figure 4.17: Polyimide on LCP a)bubbles on polyimide as shown by experiments, b)bubbles observed by Guo et al. [83].

Furthermore curing time and temperature are crucial and sensitive as a slight change in either of those factors can cause the polyimide to not be cured enough, leading problems at the photolithographic stage, which will see the polyimide being affected by the photolithographic process. Figure 4.18 shows the polyimide affected by UV light due to its low curing time.

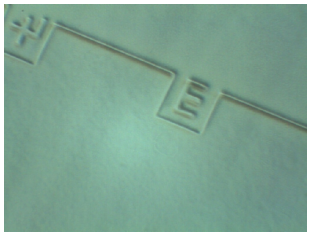


Figure 4.18: Polyimide affected by UV during standard photolithography.

This method, despite drastically decreasing LCP surface roughness is not the preferred one as the polyimide material introduces high surface stresses . Furthermore the polymer masks the good qualities for which LCP was chosen. LCP qualities are: electrical (low dielectric loss), mechanical (low TCE and low water absorption) and chemical (high resistance to chemicals).

4.5.2 Chemical polishing with bis(trifluoromethyl) phenol

The method has been shown by Tai-Shung [269], Ma and Chung [177] and consists in spin coating LCP with bis-trifluoromethyl phenol at 500rpm for 1 min and then placing the sample in vacuum at 70-150°C in order to remove solvent. The spin speed was chosen to be lower than conventional speed for wafer coating (3000-7000 rpm) in order to minimize centrifugal force and reduce radial orientation induced by spin coating. The sample should be placed under vacuum (reduced pressure) in order for the liquids to vaporize and boil off at a lower

temperature. Low concentrated solutions are preferred for smooth surfaces.

In our experiments 2mL of 3,5 Bis(trifluoromethyl)-phenol 95% from Sigma-Aldrich were spun onto a 4inch LCP substrate at 500rpm for 1min with acceleration and deceleration times of 5s each, the sample was then put on a hotplate at 150°C overnight to evaporate the solvents and then rinsed. This process was not effective as the roughness was not appropriately reduced. As seen in figure 4.19 the roughness was taken (from 411nm) to 377nm only. The two reasons for method failure are: lack of vacuum ambient that elevates to high temperatures, lower chemical concentration of 95% instead of 99%.

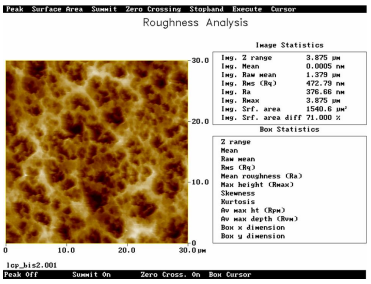


Figure 4.19: LCP roughness (Ra=376nm) after polish with 95% bis (trifluoromethyl) phenol.

This method will not be further taken in consideration as a possible way of roughness reduction.

4.5.3 Hot pressing

Hot pressing is based on the principle of pressing LCP while it reaches its glass transition temperature (Tg). This is the temperature at which the polymer flows. Above Tg organic polymers become soft and liquid and capable of plastic deformation without fracture. LCP has high glass transition temperature 230-260°C.

Initial trials

The first hot pressing trials were carried out with an ULTRALAM3850 LCP sample, with the Cu clad removed, sandwiched between two silicon wafers and put in vacuum oven. Dektak measurements of LCP surface before and after pressing were carried out. 5x5mm piece placed between 2 silicon wafers (2") on a hotplate at 240-250°C and pressed together for 10 minutes using an 8oz weight thermally isolated with several layers of clean room wipes. After cooling LCP prised off Si using scalpel. Figure 4.20 shows LCP surface Dektak after Cu removal, before hot pressing treatment. Figure 4.21 shows images (from Dektak screen) of LCP and Si after LCP and Si are detached.

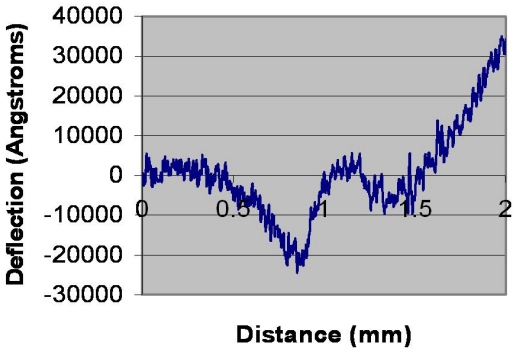


Figure 4.20: Dektak roughness scan before hot press trial (courtesy of Rob Wright).

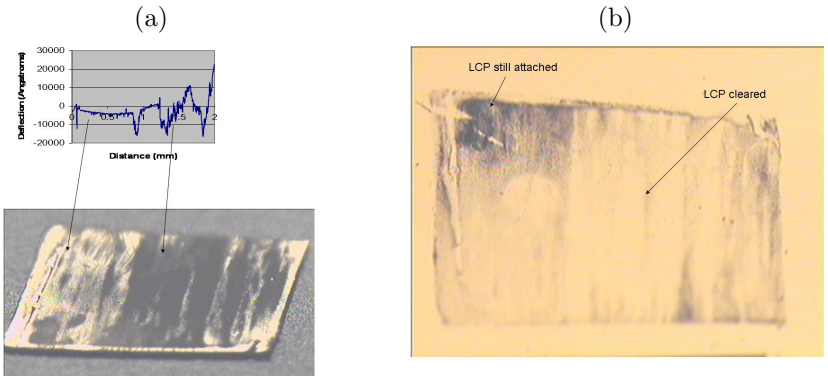


Figure 4.21: Initial hot press trial carried out in clean room. a) LCP surface after removal from Si, bright areas look shiny to the eye. b) Si surface after LCP prised off, dark areas are where LCP is still attached (courtesy of Rob Wright).

These trials proved to be successful although they were not homogeneous. In fact, the smoothing occured only in some areas, leaving other areas unaffected (as seen in figure 4.21) . This might be because the load was not distributed evenly on the LCP sample, causing only some areas to reach the glass transition temperature. Another reason might be the insufficiency of the load applied. This is why the Carver press method is considered.

Carver press method

The Carver press is a large scale hot pressing equipment. For the Carver press method, the LCP was sandwiched between two thin graphite sheets (melting temperature=3675°C) instead of silicon as the former is a flexible material, while the latter is brittle and could break under high pressures even with the

slightest surface unevenness. The initial graphite sheet texture was scanned with Dektak detecting an average roughness of Ra=1141nm (Rq=1746nm) for a scan range of 50μm. Table 4.5 shows the roughness results for the various trials of the Carver press method. Figures 4.22 show the state of the samples after hot pressing was carried out.

Table 4.5: Carver press method for roughness reduction scan size of 50μm.

Test	**Temperature (°C)**	**Pressure (tonnes)**	**time (min)**	**Roughness LCP(nm)**	**Roughness graphite(nm)**
Test 1	300	35	60	N.A. (sample disintegrates)	-
Test 2	250	25	30	N.A. (sample disintegrates)	-
Test 3	50	20	10	446 (Rq=543)	1090
Test 4	200	20	10	65 (Rq=80)	84 (Rq=100)
Test 5	250	20	10	41 (Rq=50)	85 (Rq=104)
Test 6	300	20	10	N.A. (sample melts)	-

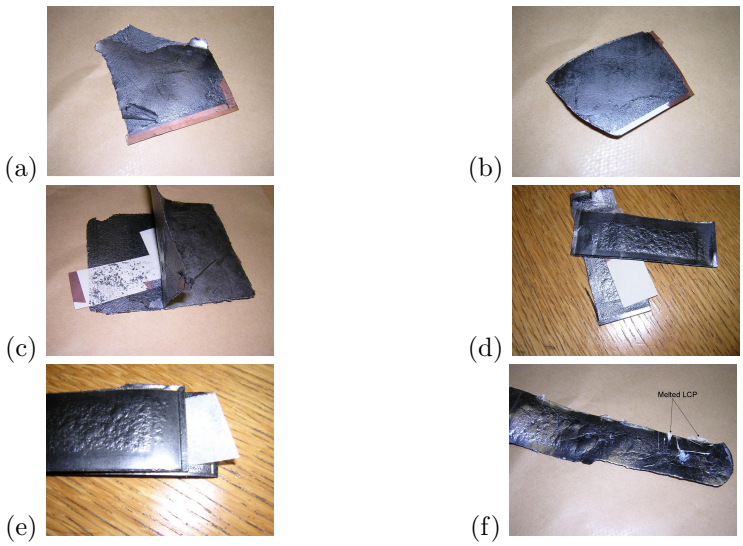


Figure 4.22: Figures showing samples after carver press method a) test 1, b) test 2, c) test 3, d) test 4, e) test 5, f) test 6.

Sample disintegrates with the following two conditions: temperature 300°C and any load, temperature 250°C and load larger that 20tonnes. When it disintegrates it melts and, in extreme cases, is absorbed by the graphite. The adopted Carver press is a large-scale oriented equipment, and possesses a high heat flux and relatively poor temperature control.

The effect of Carver press method was quantified in two different ways:

1. Dektak measurements on LCP and the graphite after pressing must match each other. If LCP is affected, then its surface is molded to the graphite's texture.

2. Final AFM measurements of LCP must deviate from their initial values.

When the temperature of the Carver press is set lower in order to avoid the high build-up temperatures, for test 3 the roughness measurements show that no change was made in the surface texture of LCP. The method proved that an acceptable smoothing of LCP can be achieved using conditions in Test 4. The LCP gained the surface texture of the graphite, meaning that at these conditions it is possible to achieve smooth LCP, given that the sandwiching material (graphite) does not possess a texture. The LCP sample replicated the graphite texture also for test 5, however LCP thinned out significantly. For an optimal planarization, a Carver press with accurate temperature control and flat sheet of graphite with no texture using test 4 settings are needed.

Observations on hot press method

The above tests have shown the possibility of using this smoothing method, the only drawbacks being equipment limitations. Due to the material sensibility to even the slightest temperature change, an accurate temperature control would be ideal in order to reach but not exceed the glass transition temperature (Tg) of 230-260°C. Hot pressing method also showed dimensional instability as it causes the thickness of LCP to decrease as a function of pressure, time and heat.

There are two ways to prove that the hot pressing method works. The first is that the roughness measurements on LCP and the graphite must match or at least be similar as the affected LCP will have a surface molded to the graphite's. If the LCP and graphite do not have similar surface texture by the end of the pressing, this means that glass transition temperature is not reached. The second is that the final LCP roughness should be lower than the initial roughness (in this case for LCP ULTRALAM3850 Ra$\sim$300nm).

Carver hot press method could well be applicable to planarising rough LCP using small-scale equipment as the hot press at Cranfield is not aimed for small-scale purposes. Among other things, a hot press with a more sensitive temperature feedback control is needed so that heat is not accumulated. In other terms, a well controlled process is needed if this method is to be further investigated.

If we were to pursue this route, then a material with smooth surface texture and high melting point (300°C) should be used instead of graphite.

4.5.4 Chemical-mechanical lap polishing (CMP)

So far the smoothing methods used have been either incomplete or unsuccessful. Hence we investigated the use of a more common smoothing technique for

polymeric substrates.

Chemical mechanical polishing (CMP) of polymers has previously been carried out on polycarbonate (PC) and poly-methyl-methacrylate (PMMA) [319], polished benzocyclobutene (BCB) [203], SiLK® [21], polyimide [20] and LCP [290].

Initial trials

In the initial trials, carried out at Cranfield University, a Logitech PM4 machine was employed for lap polishing. A silk cloth (DP-Dur®) surface was used with silica slurry (also used by Onodera et al. [211] for LCP polishing). Silica microsphere (diameter 0.06μm) slurry was chosen over alumina as the latter yields more defectivity (i.e. scratching, removal uniformity) on a rigid material such as silicon. It would, therefore, damage a soft organic material such as LCP.

LCP was polished with 0.04μm slurry for a total of 120min with 10kg weight and spin speed 35rpm. Surface roughness of LCP was measured intermittently between 10min and 120min with an atomic force microscope (AFM) (see figures and 4.23).

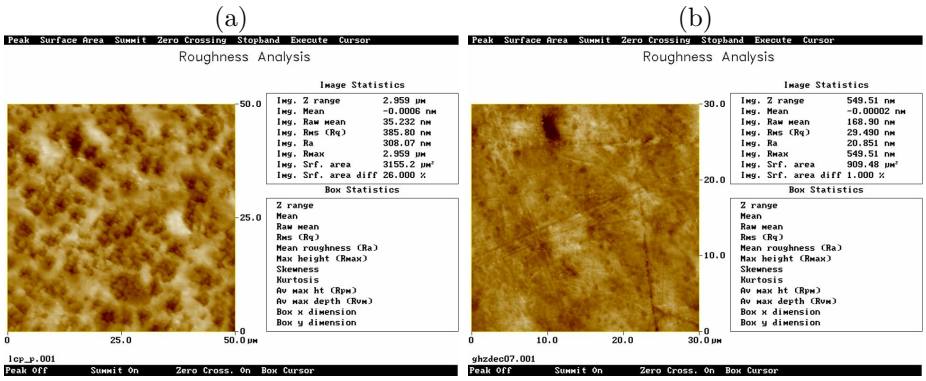


Figure 4.23: AFM images of surface LCP roughness after a)10 min lap polish (Ra=308nm), b)120min lap polish (Ra=21nm). Using: DP-Dur® 0.04μm silica slurry, 35rpm spin speed, 5kg weight.

The graph 4.24 gives average roughness (Ra) values, it is evident that roughness decreases relatively linearly with respect to time.

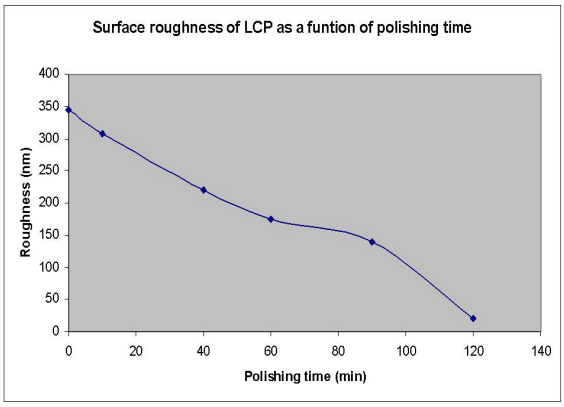


Figure 4.24: LCP substrate Ra values as a function of polishing time. Using: DP-Dur® 0.04μm silica slurry, 35rpm spin speed, 5kg weight.

The thickness of LCP after 120min polishing was measured through an RIE etch followed by a Dektak® surface measurement. As shown by the equation in figure 4.25 the slope is low (-0.02), meaning that the change in thickness through time is minimal.

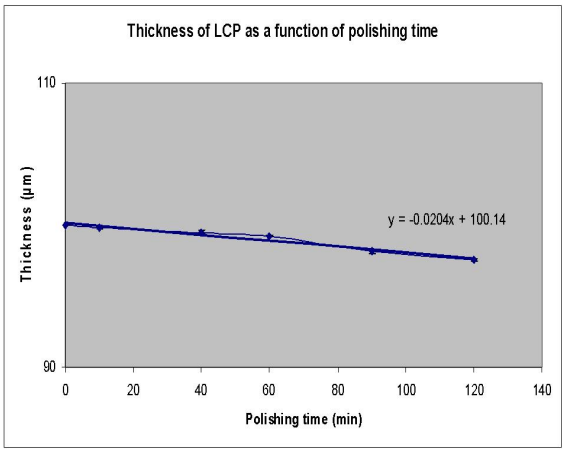


Figure 4.25: LCP thickness variation with respect to polishing time. Notice the small standard error.

LCP polishing is a very new field and was further investigated with tailored facilities at Tyndall National Institute (Cork, Ireland).

Tyndall trials

The LCP samples were attached to Si substrate with Brewer Scientific Wafer-BOND HT adhesive polymer (with process temperature capability up to 220°C)

ordered from [241] by spinning 2.5mL on Si at 3500rpm, baking at 220°C for 3min, putting LCP on it and roll the LCP/waferBOND/Si assembly. WaferBOND HT coating can be mechanically debonded by heating the wafer around 240-260°C for ≺5min, until the carrier can be slid from the wafer. WaferBond can be dissolved in acetone [241] when left for less than 15min. Because of this, the samples were detached and then reattached to silicon using the standard optimal vacuum bonding procedure and black wax (described in section 4.3.3).

The samples were polished with a Logitech CDP51 machine using FastPad PPG (IC-1000 analogue) and a colloidal alumina slurry (Eminess Ultra-sol A12) with 0.24μm size granules from 3M [1]. Downward pressures of either 2.07N/cm^2 or 3.45N/cm^2 were applied for times up to 20min. Table 4.6 shows the polishing conditions employed.

Table 4.6: Smoothing trials carried out at Tyndall National Institute (Cork, Ireland).

Sample name	**Reference substrate**	**Spin speed (rpm)**	**Spin time (min)**	**Downward pressure (N/cm^2)**	**Final Ra(nm)**
Sample 20	ULTRALAM 3800	1000	2	2.07	11
Sample 21	ULTRALAM 3850	1000	2	2.07	11
Sample 22	ULTRALAM 3800	1000	20	3.45	7
Sample 23	ULTRALAM 3850	1000	20	3.45	5

ULTRALAM 3850 (Ra∼350nm) and ULTRALAM 3800 (Ra∼50nm) both smoothed to average roughnesses of 10-20nm for samples 20 and 21 trials (see figures 4.26 a) and b)). In trials for samples 22 and 23 the roughness decreased to Ra∼5nm by increasing both polishing time and downward force (see figures 4.26 c) and d)).

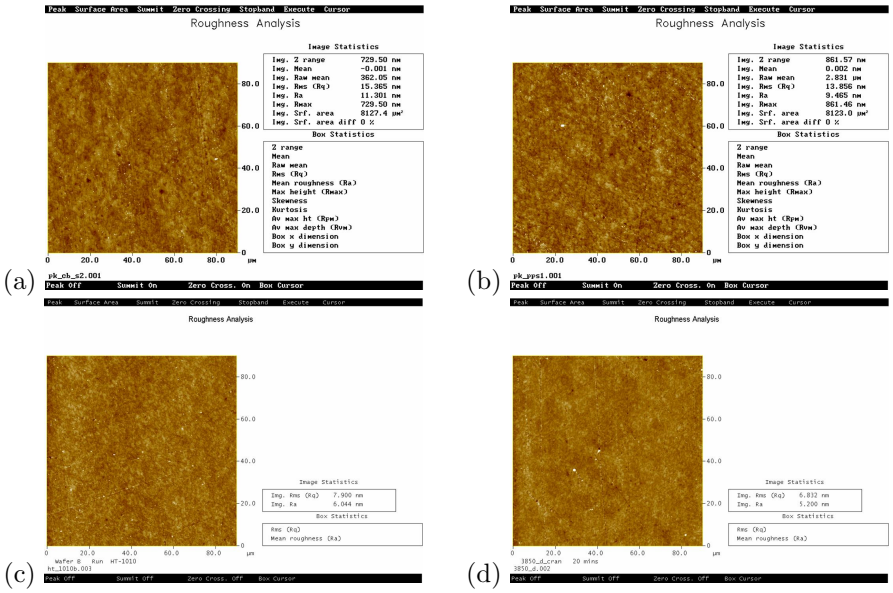


Figure 4.26: a)Sample 20(on cladded LCP ULTRALAM3850) (Ra∼11nm), b) Sample 21 (on unclad LCP ULTRALAM3800) (Ra∼8nm), c) Sample 22 (on unclad LCP ULTRALAM3800) (Ra∼6nm), d)Sample 23 (on cladded LCP ULTRALAM3850) (Ra∼5nm).

Compared to the lap polishing carried out at Cranfield, the ones at Tyndall yielded lower roughness but more scratches due to the alumina slurry harsh and aggressive nature. The lower roughness achieved can be because of the smaller size of the alumina slurry grains (0.24μm) compared to the silica ones (0.4μm). Because of the lower roughness achieved, the device yield on the Tyndall samples will be higher than any of the other lap polished ones done at Cranfield (see section 6.2).

Observation on CMP

The CMP method is a viable way to reduce roughness since it means that devices are created directly on the high-quality LCP substrate without the use of extra layers such as polyimide. The samples polished by Tyndall yielded very low roughness (∼5nm) results with the only disadvantage of surface defectivity. Ideally, in order to avoid surface scratches, the best way forward in the future would be to use the "slurry-free CMP pads" from 3M [1], with a microreplicated surface which is tailored for repeatability, fluid transport and long abrasive life [private communication from Alan Blake (Tyndall Institute)]. This method was not employed but is suggested as a future work.

4.6 Observation on LCP roughness reduction

Polyimide coating, chemical polishing and hot pressing methods used for LCP roughness reduction were all either incomplete or unsuccessful. Polyimide coating showed to introduce stresses and unwanted features for which LCP was initially chosen. Chemical polishing was altogether unsuccessful and hot pressing was incomplete due to lack of appropriate small-scale equipment.

Having carried out numerous trials on LCP in order to find the best solution for roughness reduction, we can conclude that CMP is the way forward. More specifically trials carried out by Tyndall, using tailored equipment for polymer treatment, have shown to considerably reduce the surface roughness of the LCP without compromising its integrity.

4.7 Electro-thermal stability of LCP

The electrical stability of a substrate with respect to processing temperature is important as this undergoes various heat treatments for MEMS production. For FBAR fabrication, for example, there are various stages including photolithography baking temperature (115°C) and ZnO sputter (up to 250°C). LCP electrical properties with respect to temperature were measured to understand thermal treatment effect on substrate stability.

After Cu etch and substrate polishing, the LCP was placed on a hotplate for 10min at a range of temperatures below and near its glass-transition temperature (<300°C). Au was then sputtered at both the front and the back of the substrate for then measuring the dielectric loss (tanδ) and dielectric constant (ϵ). Measurements were taken at 300kHz with 10mV (AC) applied, and the results shown in table 4.7.

Table 4.7: LCP dielectric properties before and after high temperature LCP treatment.

Temperature (°C)	**Dielectric loss (tanδ)**	**Dielectric constant (ϵ)**
No treatment	0.02	3.58
100	0.03	3.40
250	0.03	1.73

Dielectric loss of LCP is usually 0.02 while its dielectric constant is around 2.9 [276]. From the results it is obvious that the dielectric properties of LCP are not largely affected by temperature treatment. LCP dielectric properties do not change when subjected to glass transition temperature [276].

4.8 Observations on preparation of LCP foils for MEMS processing

It is possible to conclude that the best preparation parameters, in terms of LCP flatness enhancement and roughness reduction, consist in silicon backing with low thickness black wax ($\sim 1\mu$m) as adhesive layer and CMP polishing with high downward pressure, spin speed and appropriate polishing pad.

The substrate shows electrical stability after being smoothed and treated thermally. This means that even under relatively high processing temperatures, the substrate's electrical properties do not degrade, making it suitable for MEMS production.

Chapter 5

MEMS processing of LCP substrates for FBAR fabrication

5.1 Introduction

The previous chapter described pre-processing methods that condition the LCP for subsequent MEMS processing. A technique was described for attaching a silicon wafer to the LCP to create a rigid structure suitable for processing and the best method for flatness achievement was vacuum bonding of LCP on Si using 1μm black wax. Furthermore a CMP method was developed for smoothing the surface of an LCP making it suitable for metallisation and subsequent ZnO deposition. The smoothing method yielding the lowest roughness was that employed in sample 22 and sample 23 shown in table 4.6. MEMS processing techniques required to create devices on pre-processed LCP substrates are described in this chapter.

The use of MEMS processing techniques on polymer substrates is a relatively new field since organic electronics have only recently emerged in the IC industry. Because the design and production of alternative equipment can be an intricate and rather expensive task, standard microsystems fabrication techniques have been used in this project to assess the possibility of FBAR production directly onto LCP. By alternative equipment we refer, for example, to roll-to-roll processing (usually used for flexible electronics production) integrating not only metal deposition and patterning, but also ZnO deposition, patterning and back RIE etching of the material.

The standard MEMS processing procedure comprises the following steps: metal deposition, high quality piezoelectric material deposition, patterning, back to front processing for back feature generation and material removal. Some of the fabrication steps have been suitably tailored with respect to LCP's low rigidity in order to create devices. Prior to processing and film deposition, polymer surface treatment is carried out through surface clean with isopropyl alcohol.

The polymer substrate can also be treated under plasma gases to improve adhesion. The main device of interest is the Film Bulk Acoustic Resonator (FBAR) for which the various FBAR process flows are shown both in figure A.1 and in Appendix A..3.

The adaptation of MEMS processes to LCP can be a revolutionary step in the first few years that will see the transition of inorganic to organic materials for electronic device production.

5.2 Metal deposition on LCP

For LCP-based MEMS applications, electrodes must be flexible, water resistant, and mechanically robust [88]. Platinum (Pt) and gold (Au) are acceptable metals to be exploited as electrodes in MEMS as they are both flexible and robust. The reason why Au is generally preferred, though, is because of the added biocompatibility, low resistivity ($2.44e^{-8}$Ohm-m at 20°C), high acoustic impedance (63.8 MRayls) and its ability to offer a good base for ZnO crystallization. The last three characteristics make it ideal for FBAR device fabrication as we will later discuss.

5.2.1 Metal deposition and quality

Ti/Au, Cr/Au RF sputtering, Ti/Pt DC sputtering and Cr/Au evaporation were performed on polished LCP foils. The conditions for sputtered and evaporated metals are shown in table A.7 which comply to the standard parameters. The metal quality is analysed through imaging and X-ray diffraction (XRD). Figure 5.1 shows the different metals.

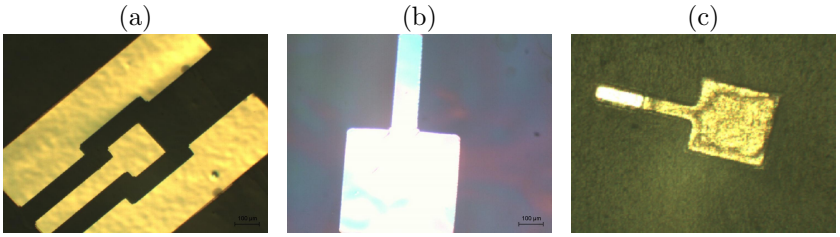


Figure 5.1: a)Au patterned and RF sputtered on LCP (Ra∼5nm), b)Pt patterned and DC sputtered on LCP (Ra∼5nm), c)Au evaporated on LCP.

All metals show relatively good quality when deposited on planarised LCP. The preferred metal deposition method is through sputtering both because of the metal quality but also because it does not cause high localised stresses thanks to the metal particles being smaller when they reach the substrate. It is well known that sputtered metals are better than evaporated ones when used as bottom electrodes. Furthermore the step coverage with evaporation is poor and so of limited use for devices with a lot of topography. For these reasons from

now on we will consider sputtered metals (more specifically Au) only, unless mentioned otherwise.

5.2.2 Metal roughness on LCP

XRD of Au reveals that the Au intensity and, therefore, quality depend on LCP surface roughness. LCP is with average roughnesses of 5nm, 20nm and 50nm is used to deposit Au. Bottom electrode roughness is known to affect functional ceramic (ZnO and AlN) growth as studied by Artieda et al. [11]. The higher the Au $\prec 111 \succ$ peak at 38°, the higher the future piezoelectric ceramic orientation will be. For ZnO d_{33} piezoelectric coefficient activity, is $\prec 002 \succ$.

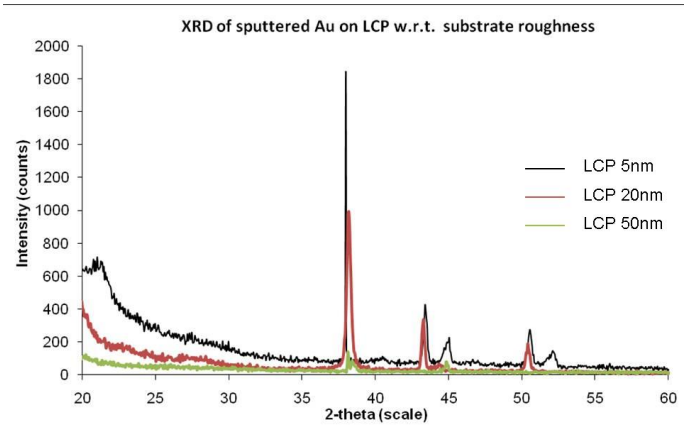


Figure 5.2: XRD of sputtered Au on LCP with different roughnesses. Au peak of interest is at ∼38°.

It is evident from figure 5.2 that, the smoother the LCP substrate, the higher and narrower the Au XRD peak in the $\prec 111 \succ$ direction. A high Au $\prec 111 \succ$ orientation will lead to better future ZnO $\prec 002 \succ$ c-axis growth.

Bottom electrode roughness is an important parameter for appropriate piezoelectric material (i.e. ZnO) $\prec 002 \succ$ c-axis orientation, which must be perpendicular to the substrate for proper piezoelectric functioning. The deposited metal usually replicates the roughness of the substrate it is deposited on. Figures 5.3 show this conformality for sputtered Au on LCP with various roughnesses.

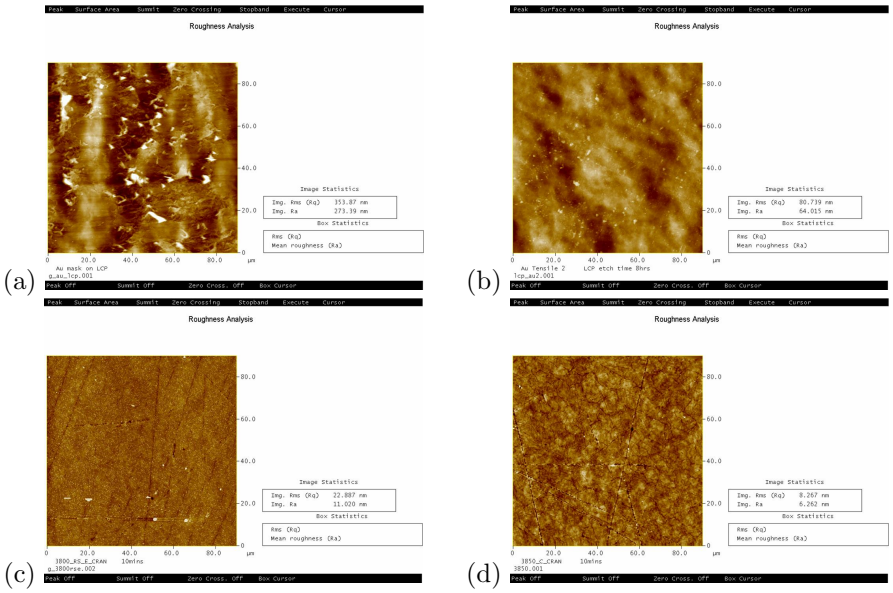


Figure 5.3: Au on LCP a)LCP Ra=220nm, Au Ra=273nm b)LCP Ra=50nm, Au Ra=64nm, c)LCP Ra=11nm, Au Ra=11nm, d)LCP Ra=5nm, Au Ra=6nm.

The metal roughness variation with respect to substrate roughness is shown in figure 5.4 where we can see a decrease. Here as LCP roughness increases the metal roughness also increases. This shows the degree of thin film topographic conformality with substrate roughness.

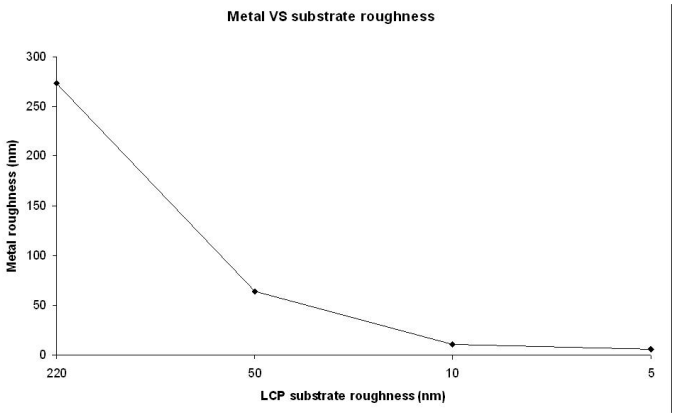


Figure 5.4: Decrease in sputtered Au metal roughness as a function of LCP substrate roughness.

5.2.3 Metal adhesion and strength on LCP

Metal adhesion

Adhesion between sputtered thin metal films and substrates is a very important parameter because it dictates the future metal strength. This depends on many surface factors, including cleanliness and roughness of the substrate onto which the metal is deposited. Cleanliness and roughness then determine the surface free energy density (or adhesion force) of the substrate which is the excess of surface energy density of a material compared to the bulk and is measured in N/m. The higher the surface free energy, the more adhesive strength potential there is on a material. It is important to assess the interfacial forces keeping the two together through adhesion studies.

Cleanliness is a top priority when processing wafers for MEMS fabrication as any contaminant can decrease the adhesion between deposited material and the substrate [193]. As we have seen, although roughness is unwanted since it can negatively affect metal and successive piezoelectric material growth quality, this heterogeneous nature of materials aids bonding strength. Rough texture, in fact, promotes wetting through: increasing surface area and providing mechanical anchoring sites [301].

We took AFM force-displacement measurements to calculate the adhesive force of a surface in contact mode. This method is carried out using a silicon tip with resistivity 0.01-0.02Ohm-cm, spring constant (k_{tip}) 0.14N/m, frequency 13kHz, tip length 448μm. The deflection d_{tip} was calculated in nm and represented by the vertical displacement in figures 5.5 a), b) and c). The surface adhesive force ($F_{adhesive}$) is then given by equation 5.1. Therefore, the higher the tip displacement (d_{tip}), the higher the surface adhesive force ($F_{adhesive}$) since the spring constant (k_{tip}) is an invariable parameter.

$$F_{adhesive} = k_{tip} \cdot d_{tip} \tag{5.1}$$

The tip deflection is represented by the vertical line in figures 5.5 from which we can derive surface adhesion force density values of rough LCP $F_{adhesive}$=8.28x10^{-4} N/cm and smooth LCP $F_{adhesive}$=2.94x10^{-5}N/cm. The results demonstrate that for the rougher LCP the surface energy is greater than for the smooth one by an order of magnitude, confirming what was declared by Wu [301] about roughness aiding to better adhesion. The silicon wa taken as a point of reference and its surface energy density was measured to be $F_{adhesive}$=5.48x10^{-4} N/cm, very close to $F_{adhesive}$=4-7x10^{-4}N/cm found by Wang et al. [291].

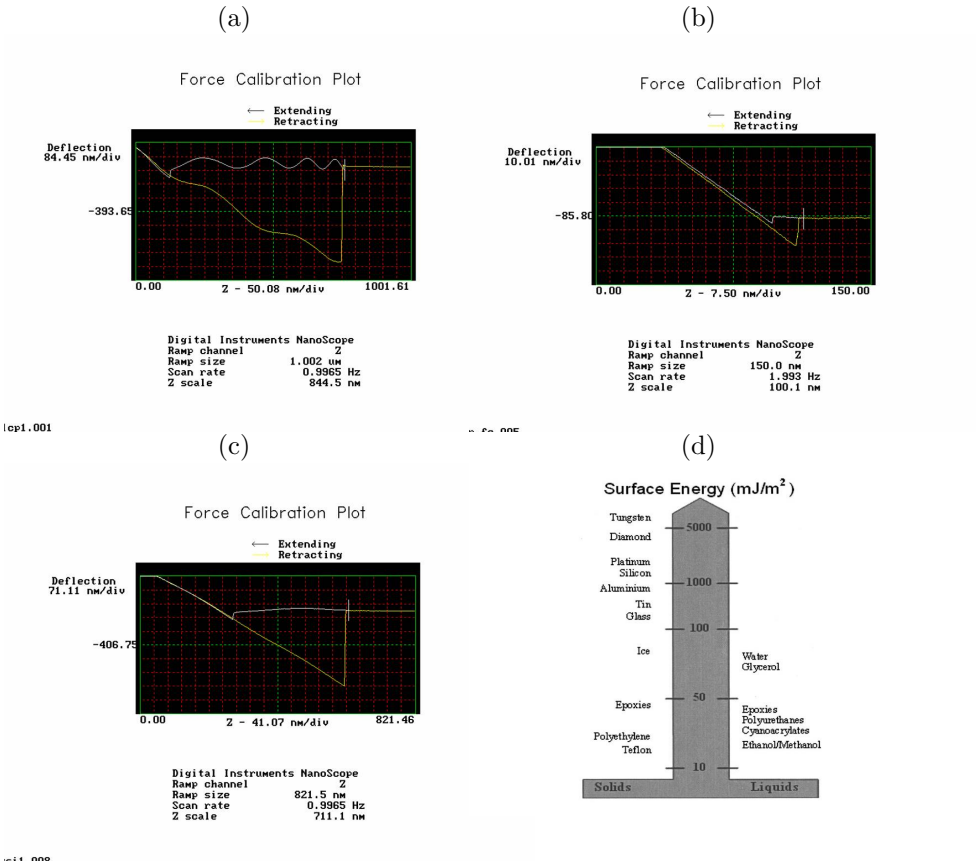


Figure 5.5: AFM force-displacement measurements for surface adhesive force calculations on: a)LCP Ra=220nm, b)LCP Ra=11nm, c)Si Ra=0.045nm. d)Adhesion energy of various materials (from Goss [79]), we see that polymers have low surface energy.

Yang [308] show that adhesion strengths of sputtered metal on LCP substrates are 7-9x10^{-7}N/cm, much less that what we found for both the smooth and rough LCP. Surface energy of Vectra A-950 (the LCP type employed in our experiments) was measured $\sim$4x10^{-7}N/cm by Ma et al. [178] and Kuixiang et al. [129]. Tai-Shung [269] found that surface energy of LCP in water is 2.55-7.28x10^{-7}N/cm. The surface adhesion force on our samples was three orders of magnitude higher than that found in the literature. Besides surface cleanliness, metal layer to LCP surface adhesion improvement is noticed when pretreating the LCP with argon plasma [289].

Metal strength

The adhesion quality between metal and the substrate is important because it dictates the future metal strength. Metal strength can be evaluated in terms of rupture strain which is the deformation it takes for the material to break or crack. For metals on polymers (i.e. polyimide substrate), large rupture strains

have so far been demonstrated [82], [156]. While a freestanding thin metal film usually breaks at a small strain, thin metal films on polymer substrates fail at larger strains (from one percent to a few tens percent). Local thinning causes low ductility of a freestanding metal film while, when on polymer, the compliant substrate delocalizes (moves) the strain field (dislocation) in the metal film, carrying it far beyond the rupture strain of a freestanding film [156].

In our experiments metal cracking occurred in the mode shown in figure 5.6 (Au crack mode), which is similar to what was found by [154] shown in figure 2.24. The metal crack is thought to be caused by organic residues on LCP prior to processing, and we can assume this as the sample (sample 8) did not undergo the standard isopropyl cleaning step, hence, showing some contaminant organic residues prior to top metal deposition.

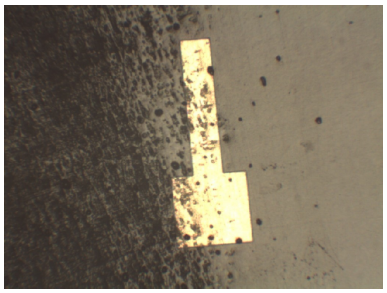
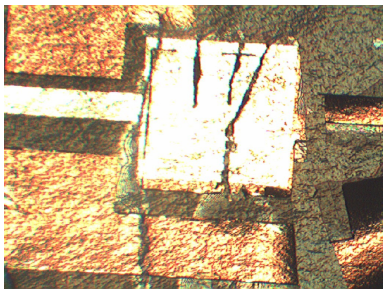
(a)  (b) 

Figure 5.6: Sample 8 a)Dirt on substrate surface prior to top electrode deposition causing bad adhesion, b) mode of top metal fracture on LCP/polyimide.

The Au metal yield strength on LCP will also be investigated through tensile testing in section 5.4.

5.2.4 Observation on metal deposition on LCP

The metal quality was acceptable on low roughness LCP. The peak of the $\prec 111 \succ$ Au direction was shown to increase as LCP surface roughness was reduced. The sputtered metal quality increased as LCP roughness decreased, its roughness was shown to be conformal to LCP roughness, and its adhesion strength was seen to decrease as the LCP roughness decreased. However the surface adhesion strength of LCP is still higher than that of standard Si substrate.

It can be concluded that smooth LCP is a viable substrate for high quality Au metal growth and high strength so long as the surface of the substrate is clean.

5.3 ZnO growth on LCP

ZnO is a particularly attractive piezoelectric material since good quality, high c-axis oriented polycrystalline films can be deposited at relatively low temperatures (up to 250°C). Low-temperature processing of functional materials is attractive for flexible electronics on temperature sensitive substrates. There is, therefore, good compatibility of ZnO with flexible plastic substrate materials. The study of RF sputtered ZnO quality on LCP is of interest as it installs the basis of successful growth of functional materials on non-standard substrates.

ZnO deposition on non-standard silicon substrates has previously been of interest. ZnO growth on glass [10], sapphire [264], temperature sensitive flexible substrate [30], plastic [29] and, more specifically, polyimide [131] have been carried out for a number of applications. These include mainly optical [264] and thin film transistor applications for active matrix display such as liquid crystal displays and organic light emitting diodes with low leakage current densities Carcia et al. [29].

ZnO quality is dictated by its low roughness and the degree of c-axis orientation. The preferential c-axis growth of deposited ZnO films depends on process conditions and the type of bottom electrode. As we have seen, the chosen metal for bottom electrode is Au since it enhances the growth of c-axis orientation in ZnO films [111]. Hence, prior to ZnO deposition, Ti(thickness$\sim$8nm)-Au(thickness$\sim$100nm) electrodes are deposited.

The 1μm ZnO is RF sputtered on the metal bottom electrode. Sputtering process conditions required for achieving 1μm ZnO are shown in table A.8 in Appendix A..1. Sputtering pressure used in our experiments was 25mTorr as has previously shown to give successful results [111]. This chamber pressure compromises well between a low cone, which yields small grains, and and increased one, which yields low intrinsic stresses [295]. Intrinsic stress is caused by imperfections which occur in the crystallites during film growth [45]. Imperfections are introduced by impurities, defects and lattice distortions in the crystal.

5.3.1 Conformality of surface texture

Since piezoelectric ceramic roughness is known to affect its electromechanical behaviour, we here study the relationship between initial substrate roughness and final ZnO sputtered roughness. Thin film deposition methods such as sputtering are generally known to yield uniform and conformal coatings. The main requirements for coating nano-featured materials are [246]:

1. Uniformity: good penetration into features.
2. Conformality: film texture matching surface texture.

Since sputtering systems yield films that are conformal to the surface they are being deposited on, it is necessary to start with very smooth substrates. To show this surface texture reproduction and quantify the conformality of our

ZnO-coated LCP, we demonstrate how various deposition stages of the processing affect the surface roughness of sample 20 and sample 22.

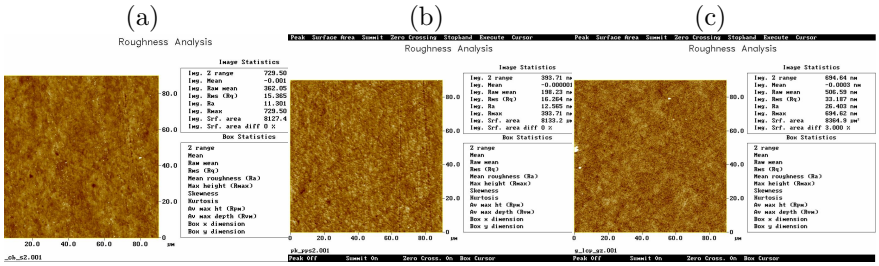


Figure 5.7: Conformality progression of sample 20: a) polished LCP (Ra=11nm) , b) LCP with Au (Ra=12.5nm), c) LCP-Au with ZnO (Ra=26.5nm).

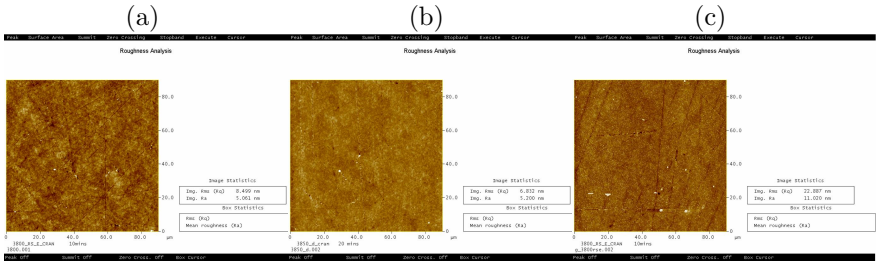


Figure 5.8: Conformality progression of sample 22: a) polished LCP (Ra=5nm) , b) LCP with Au (Ra=5.2nm), c) LCP-Au with ZnO (Ra=11nm).

Figures 5.7 and 5.8, show the progression of surface texture from bare LCP to Au-sputtered surface and, finally, ZnO-sputtered LCP-Au. It is possible to notice that the thin films reproduce the substrate topography, and that roughness increases as a function of the number of layers deposited.LCP roughness reduction for ZnO growth is important as it affects the ZnO roughness and grain growth quality. Furthermore, the ZnO quality and roughness are linked to deposition temperature. Therefore investigations on ZnO growth as a function of LCP roughness and sputtering temperature are carried out.

5.3.2 ZnO film quality as a function of LCP substrate roughness

Substrate roughness affects subsequent sputtered metal roughness which, in turn, affects the surface roughness of ZnO films, reducing the piezoelectric materials' quality factor (Q) and electromechanical coupling coefficient (k^2_{eff}). The dependence of piezoelectric roughness on bottom electrode roughness was also observed by Kang et al. [111] for ZnO, and Artieda et al. [11] for AlN.

In order to quantify the ceramic quality dependence as a function of roughness, LCP/Au samples with different surface roughnesses were used and ZnO grown

on them at room temperature (25°C). AFM, XRD, SEM and electrical properties were measured and compared to a standard sample.

First AFM measurements are taken to show the roughness of the LCP and of the deposited ZnO. From figure 5.9 we notice that the ZnO roughness decreases as LCP roughness lowers, in other words the ZnO roughness reproduction is proportional to that of the substrate roughness.

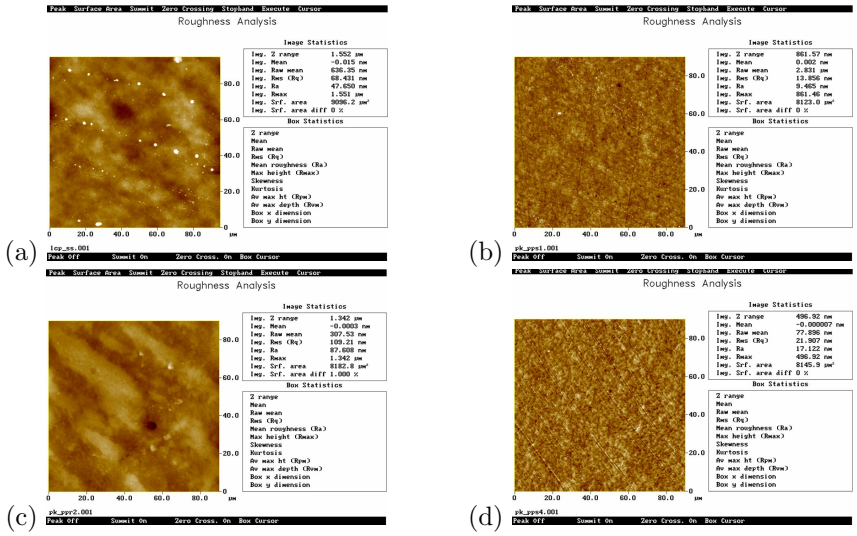


Figure 5.9: AFM images of surface ZnO roughness on a)LCP Ra=50nm, b)LCP Ra=10nm, c)ZnO on LCP(Ra=50nm) Ra=87, d)ZnO on LCP (Ra=10nm) Ra=17nm.

Figure 5.10 shows XRD and SEM scans determining ZnO growth quality on standard Si substrate, rough and smooth LCP.

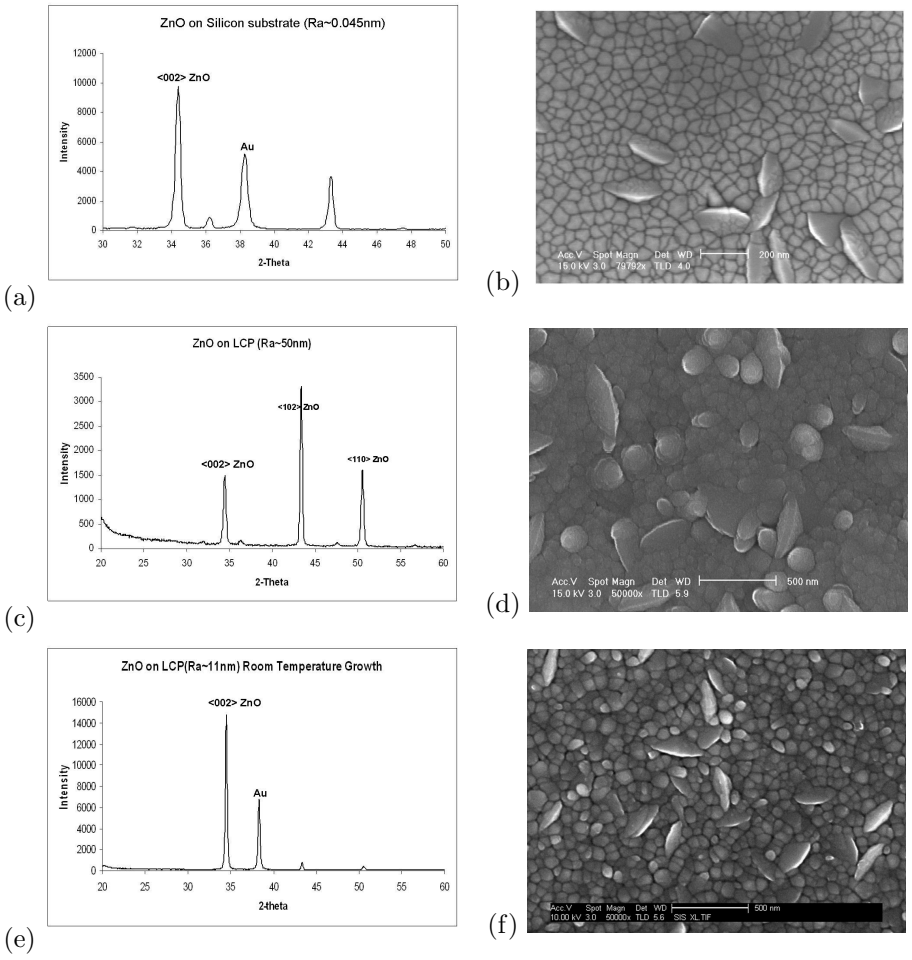


Figure 5.10: a)SEM of ZnO deposited on Si at 250°C, b)SEM of ZnO deposited on Si at 250°C, c)XRD ZnO deposited on LCP (Ra=50nm), d)SEM of ZnO deposited on LCP (Ra=50nm), e)XRD ZnO deposited on LCP (Ra=10nm), f)SEM of ZnO deposited on LCP (Ra=10nm).

By reducing average roughness of LCP from 50nm to 10nm, the ZnO sputtered average roughness value decreased from 87nm to 17nm (see figure 5.9). As a consequence, the ZnO shows an improved cristallization given by the higher XRD peak of the ZnO. We can see from figures 5.10 that the ZnO XRD peak at 2θ 34° has much higher intensity both for the standard silicon substrate (10000) and for ZnO deposited on LCP with smaller roughness (15000) compared to rougher LCP (1500). We can conclude that ZnO quality depends on LCP roughness reduction. Another way to further improve the ZnO quality, is by increasing the deposition temperature as we will discuss below.

5.3.3 ZnO on LCP as a function of deposition temperature

We have seen how the LCP substrate roughness affects the ZnO growth, now we are interested to know the effect of the deposition temperature on the ZnO quality when deposited on LCP. Low ZnO deposition temperatures produce rough surfaces with a randomly oriented structure, low density and high porosity ZnO films [296].

It is a known fact that ZnO quality is dependent on substrate sputtering temperature as findings within the department show that the ideal growth temperature of ZnO on a standard silicon substrate is 250°C. Ondo-Ndong et al. [209], Loa et al. [169] mentioned that the best crystallisation temperature for ZnO RF sputtering is 100°C which promotes high atom mobility and re-evaporation of the poorly combined structures [296]. However temperatures that are too high (∼600°C) have a degrading effect on the quality of the piezoelectric film [114].

In this section we investigate the effect of sputtering temperature on ZnO quality when deposited on smooth LCP (Ra=5nm). It is important to keep in mind that, when we talk about room temperature sputtering of ZnO, this is not entirely true as the Balzer's chamber heats up to around 80°C due to the plasma heating and the high power (250W).

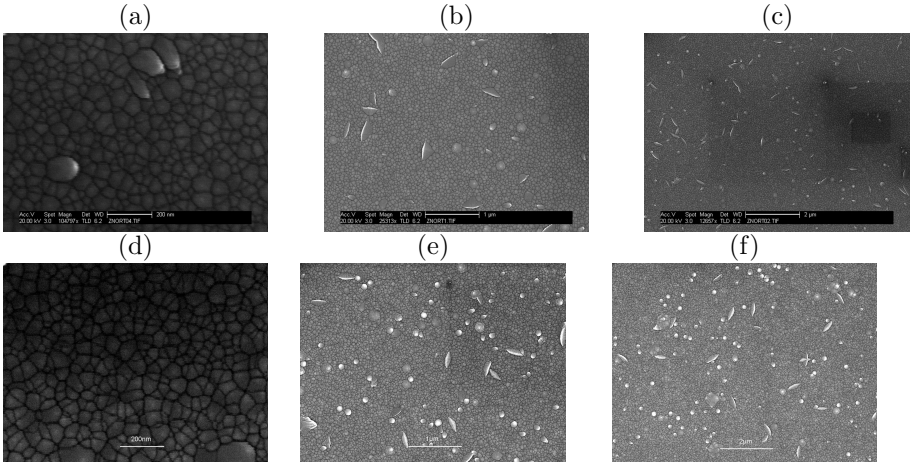


Figure 5.11: Room temperature ZnO sputtering at different magnifications: a)x100,000 b)x25,000 c)x15,000 d)x70,000 e)x35,000 f)x17,500.

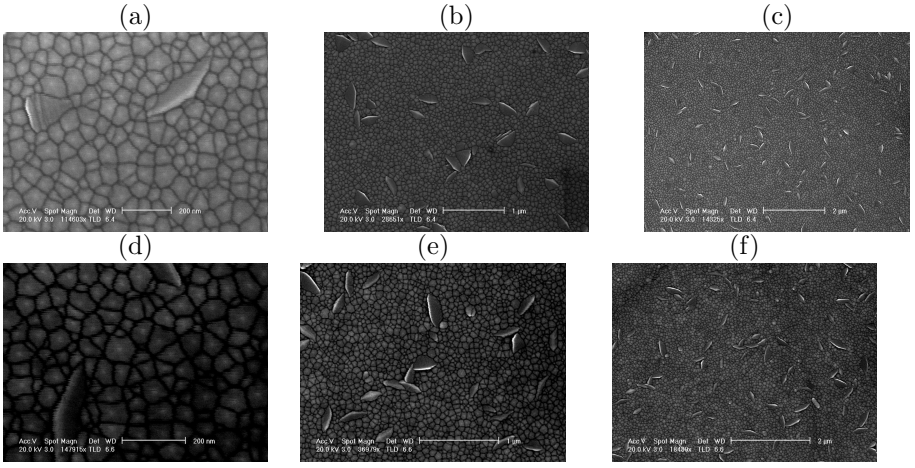


Figure 5.12: 100°C ZnO sputtering at different magnifications a)x100,000 b)x25,000 c)x15,000 d)x70,000 e)x35,000 f)x17,500.

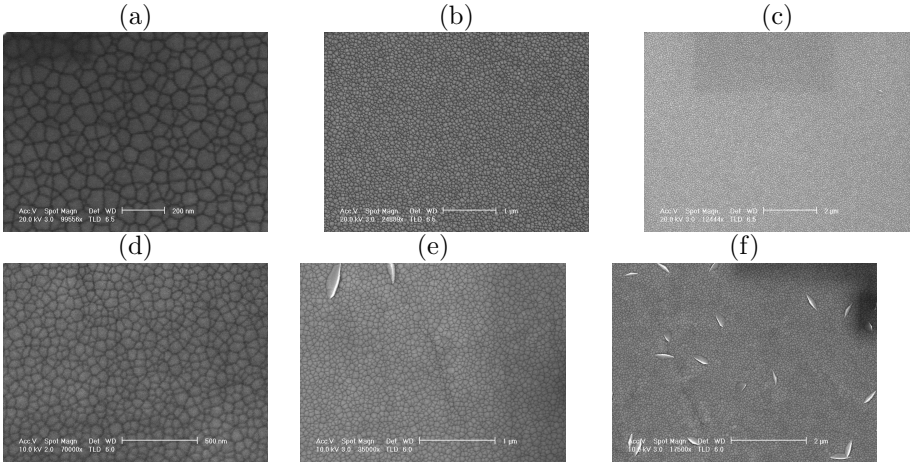


Figure 5.13: 200°C ZnO sputtering at different magnifications a)x100,000 b)x25,000 c)x15,000 d)x70,000 e)x35,000 f)x17,500.

From the SEM images we can tell that higher deposition temperatures yield much better crystal grains on LCP. However when depositing ZnO on LCP, it is safer to limit ourselves to temperatures below 200° due to LCP dimensional stability issues and thermal stresses. As we will later see, there is a tendency for the ZnO to crack at deposition temperatures >200°. Furthermore temperature-induced deformations (i.e. substrate waviness) affect the ZnO grain growth.

The degree of ZnO c-axis orientation can be quantified through XRD and full width half maximum (FWHM) sharpness measurements. For the latter, the sharper the peak the better the ZnO film quality. FHWM is calculated using rocking the curve method, where we are interested in the intensity of the rocking curve peak at about 2θ=34.5°.

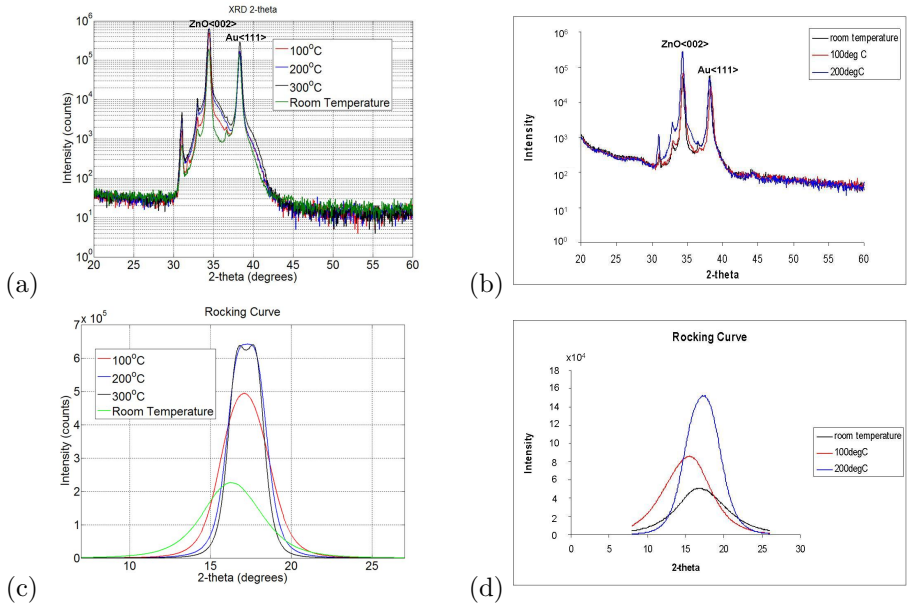


Figure 5.14: ZnO analysis: a)XRD on Si wafer (Courtesy of Carlos Fragkiadakis), b)XRD on LCP, c)FWHM on Si wafer (Courtesy of Carlos Fragkiadakis), d)FWHM on LCP.

Table 5.1: Sputtering temperature effect on ZnO quality.

Reference substrate	**ZnO deposition temperature(°C)**	**FWHM (°)**
LCP	23	4.7
LCP	100	3.2
LCP	200	3
Si	200	2.5

From figure 5.14 we can see that as the deposition temperature increases, so does the intensity of the ZnO XRD and the sharpness of ZnO FWHM curve. From table 5.1 it is evident that the FWHM values of ZnO on LCP are sharp and comparable to ZnO deposited on a standard substrate (for deposition temperature 200°C).

The best ZnO results are achieved when this is deposited on low roughness LCP (Ra=5nm) at a temperature of 200°C. However at this temperature we noticed some problems which involved the LCP debonding from the substrate due to adhesive failure. This could be caused by an increase in LCP waviness (debonding from the Si substrate) which leads to delamination and eventual cracking in some parts of the ZnO (see figure 5.15).

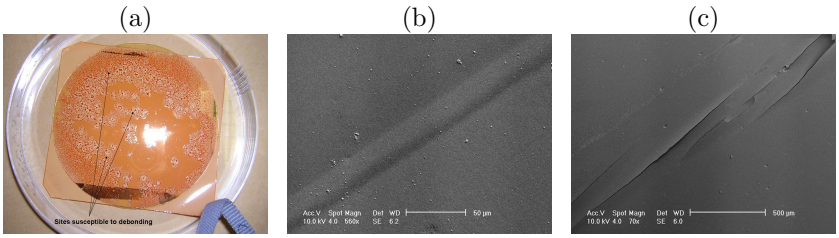


Figure 5.15: a)Back view of possible debonding sites. The debonding causes LCP waviness which leads to: b) ZnO/LCP waviness and c) ZnO/LCP delamination.

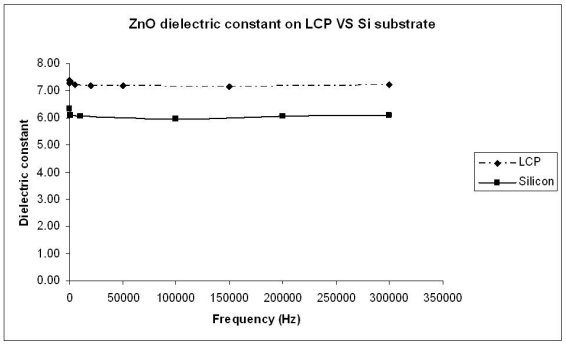
5.3.4 Electrical characteristics of ZnO on LCP

So far the material quality characteristics of the ZnO have been analysed from a materials perspective. Further analysis is required in order to assess the functional characteristics such as the electrical performance of the piezoelectric. To this end both low and high frequency measurement methods were employed to assess the dielectric properties of the material at a wide range of frequencies.

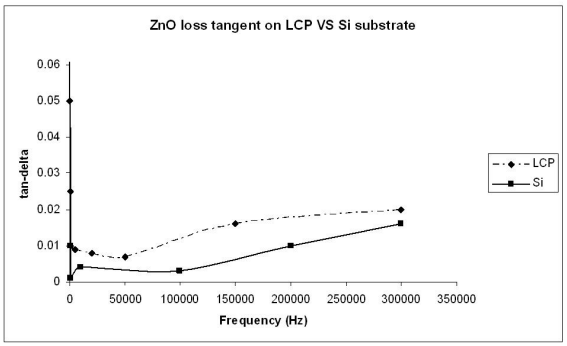
Electrical measurements for ZnO material characterisation involved capacitive dielectric measurements at relatively low frequencies (up to 300kHz) using Wayne Kerr Instrument analyser, and capacitance and dielectric value extraction at high frequencies (frequency range of 0-3GHz) from s-parameters using the VNA. Results were compared for ZnO on smooth LCP (Ra=5nm) and on Si/SiO_2 with a deposition temperatures of 100°C.

Low frequency ZnO electrical characteristics

The low frequency electrical characteristics (20Hz-300kHz) for ZnO on LCP are measured and compared with those of ZnO on Si as shown in figure 5.16.



(a)



(b)

Figure 5.16: Electrical measurements of ZnO on LCP and Si a)dielectric constant (ε), b) dielectric loss (tanδ).

As we can notice from 5.16, dielectric constant of ZnO on LCP is only slightly higher than that of ZnO on silicon. Nahm [199] explained that an increase of cooling rate increases the dielectric constant. In our case LCP-Cu on Si has a higher heat conduction than Si alone since thermal conductivity of LCP, in series with Cu and Si, allows faster heat dissipation and therefore higher cooling rate (see Appendix A..10). This means that once ZnO particles (hot from plasma) reach LCP they cool down more quickly. This theory can explain why the dielectric constant of ZnO on LCP/Cu/Si is higher. Dielectric loss is dependant on thin film roughness [102], which explains why the loss of ZnO on LCP Ra=5nm is slightly higher than that of LCP on Si Ra=0.045nm for the range of frequencies 20kHz-300kHz.

In the literature, ZnO with c-axis orientation has been found to have dielectric constant between 6-16 [105], [111] and loss tangent in the range of 0.02-0.05 [111]. Overall the results of ZnO on LCP were satisfyingly similar to those of ZnO on Si/SiO_2 and the ones found in the literature, leading to the conclusion that the use of an organic, non-flat substrate does not greatly affect ZnO growth quality if pre-treated appropriately through backing and roughness reduction.

High frequency ZnO electrical characteristics

Since FBARs and RF devices in general are actuated at frequencies higher than 1GHz, measurements up to 3GHz were taken with the Vector Network Analyser (VNA) in order to assess the high frequency characteristic functioning of the devices.

We need to investigate whether the ZnO in our LCP/Au/ZnO/Au multilayer functions properly as a capacitor when the back of the FBAR is not etched and, if so, whether it fits the capacitance curve. The transmission scattering (S_{21}) parameter curve form VNA measurements allows us to assess the capacitive nature and quality of the ZnO material. If the ZnO grows well, it should exhibit a capacitive behaviour (as shown in figure 5.17 a) and b)), where at low frequencies the impedance is high, but decreases as frequency increases. Transmission power (S_{21}) was measured for ZnO with 200x200μm^2 area and, from these measurements, capacitance and dielectric constant are extracted respectively with equations A.1 and A.6 in Appendix A..6 yielding the results in figure 5.17 c) and d).

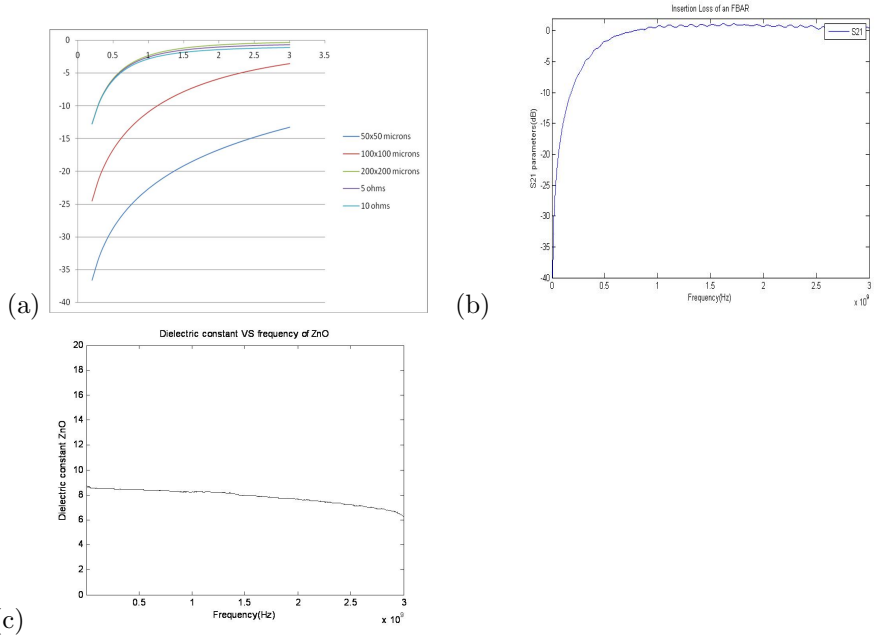


Figure 5.17: a)Simulated s-parameter capacitive behaviour for given device size [from Rob Wright], b)Measured s-parameter capacitive bahaviour (200x200μm device), c) Extracted dielectric constant (200x200μm device).

The capacitance fits with the expected value of C$\sim$4.4270pF [97] as I calculated it to be between 2.75-5pF (decreasing as a function of frequency). Since dielectric constant (ε) is proportional to capacitance, this value also decreases as a function of frequency from 8.4 to 6.2 (see figure 5.17 c)). The ZnO ε is close to the desired value 8-9 [208].

We can conclude that the ZnO on LCP (deposited at 100°C) shows the desired capacitance curve and that dielectric values derived from the s-parameters correspond to what is expected of ZnO for proper d_{33} piezoelectric functioning.

5.3.5 Observations on ZnO growth on LCP

In this section we have studied the ZnO growth quality on LCP as a function of two major parameters: surface roughness and deposition temperature.

Initial LCP substrate roughness was shown to have an influence on the subsequent ZnO roughness and grain growth quality, which then affects the piezoelectric performance of the device. Ideally ZnO should grown on low roughness LCP (in our lowest Ra∼5nm).

ZnO yielded the best crystallinity when deposited at 200°C. However it was noticed that with deposition temperatures greater than 100°C the bonding material between the LCP and the rigid substrate is affected as it reaches its glass transition temperature (Tg) leading to detachment of the LCP from the substrate. This is why for device production we used a maximum sputtering temperature of 100°C.

Furthermore, the electrical characteristics of ZnO on LCP (deposition temperature 100°C) compare well with the literature. Dielectric constant, dielectric loss and the capacitive curve with respect to frequency are very close to what is desired with slight discrepancies given by the LCP surface still not being fully smooth.

From the results given we can conclude that ZnO grown on LCP (Ra=5nm) at 100°C gives acceptable characteristics and can, therefore, be considered for future device creation.

5.4 LCP/Au/ZnO multilayer mechanical reliability analysis

When dealing with multilayers made up of different materials, the mechanical performance is of interest. It is essential to know that the combination of the layers is compatible and that it yields a reliable composite. In this particular project reliability implies that during application the LCP and Au metal do not cross their tensile strength limits and, more importantly, that the ceramic ZnO does not surpass its fracture strength limit. Fracture strength applies for ceramics and brittle materials only, and it is the local separation at the beginning of fracture given a normal stress.

A tensile test analysis allows finding the mechanical properties of each layer. Although the ZnO ceramic is our major reliability factor (due to its brittle na-

ture), the mechanical behaviors of LCP and Au are also of interest.

5.4.1 Equipment and procedure

Dogbone masks with length of 2mm,and width of 150μm were used (see figure 5.18). The dogbone samples were prepared first by attaching the LCP sample (Ra$\sim$11nm) to a silicon substrate followed by Au deposition, patterning and etch. The samples were then put through RIE until LCP was entirely etched through (roughly 7 hours for a 50μm thick LCP). At this point, the samples that were tested for Au behaviour were put in acetone to detach from silicon substrate, while the samples that had to be tested for ZnO behaviour were first sputtered with the ceramic and then detached from the substrate. Sample thickness varied depending on whether the Au (100nm) and ZnO (1μm) layers were added on the 50μm LCP.

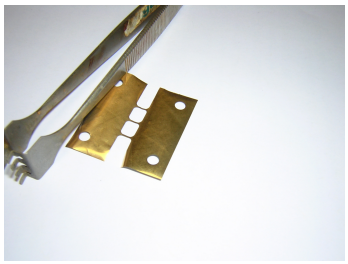
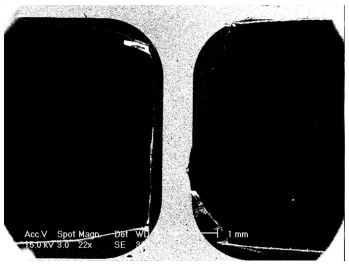
(a)  (b) 

Figure 5.18: Final dogbone sample shape used for tensile tests a)real-sized picture, b)under SEM.

For tensile testing a Deben microtest stage with maximum travel of 30μm and a maximum force capability of 20N was used. The equipment was controlled with a microcontroller through a Deben Microtest V.5.5.10 software, which also allowed result retrieval. The equipment was set-up under the SEM, therefore the tests were carried out at room temperature under vacuum. The SEM allowed images to be taken while the dogbone-shaped samples were put under tensile load. These images were then processed through a digital image correlation and tracking code developed at Johns Hopkins University by Christoph Eberl, Rob Thompson, Daniel Gianola. The code works on the principle of the sample strain measurement through pixel displacement tracking. The use of this code made it possible to collect the following parameters: Young's modulus (from stress VS strain graph), yield and fracture strength (from stress VS strain graph), creep and recovery (from strain VS time graph).

Since our metal and ceramic are deposited on a viscoelastic material, which is predicted to have dominant effect in the tensile measurements due to its larger thickness (50μm), it is important to understand the background of these non-linear materials under tensile test. The LCP will have a dominant effect in the multilayer structure because of its higher thickness. LCP (50μm thick) is 250 times thicker than the Au electrode and 50 times thicker than ZnO, hence it

plays a dominant role in the multilayer behaviour due to its thickness.

The viscoelastic properties of LCP are described in the introduction in section 2.2.4. Although not fully accurate, for ease of data handling it is assumed that ceramics and metals, because they are not viscoelastic, do not experience either creep or recovery.

5.4.2 LCP mechanical properties

The polymer substrate effect has a dominant effect in the multilayer composite structure due to its high thickness (50μm) compared to the other layers. Prior to breaking under tensile stress, necking was noticed. As we can see in figure 5.19 material thinning occurs in a specific area which we can distinguish due the shading.

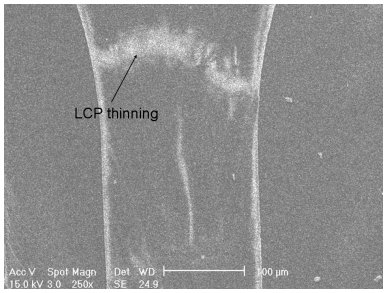


Figure 5.19: SEM picture of LCP under tensile stress. Necking is visible.

Creep and recovery

Creep and recovery were noticed in the polymer substrate, whereby past a strain of 0.135mm (once stress is removed) the polymer relieves stress under constant strain (see figure 5.20). Its behaviour resembles what was found in the literature with stress applied over an extended period (see figure 2.4 in section 2.2.4).

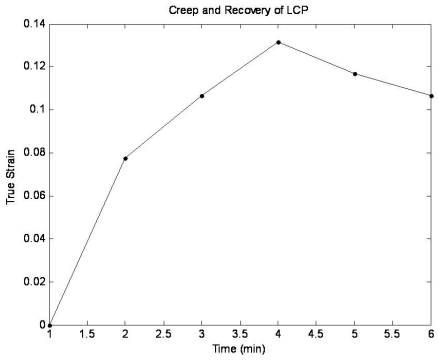


Figure 5.20: Strain VS time creep and recovery.

Low creep (high creep resistance) means that plastic deformation over long time is low given loads below the yield stress. Celanese [32] claim that their LCP (which is what we used from Rogers Corporation) has high creep resistance, hence good stiffness retention. High creep resistance is a desired characteristic for engineering plastics optimum performance, if these have to withstand long term loading.

Yield strength

LCP yield strength was derived to be ∼186.27MPa, which is very close to the LCP yield strength value of 200MPa suggested by Corporation [46]. Figure 5.21 b) shows the stress-strain relationship of LCP.

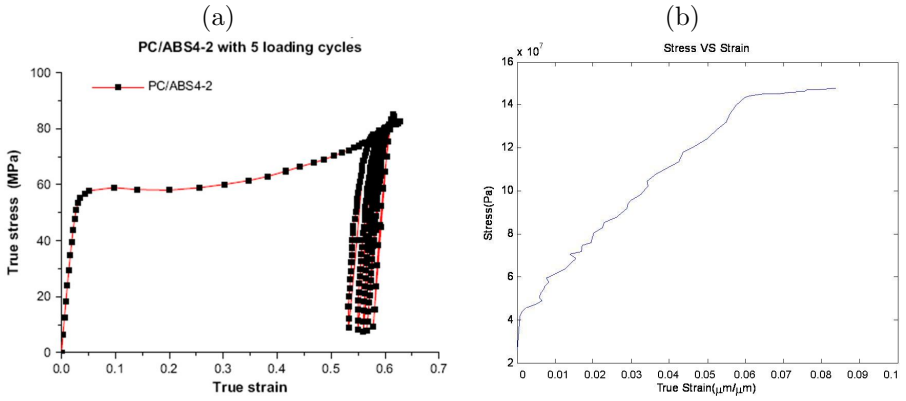


Figure 5.21: Stress-strain relationship of polymers: a)polyimide from Fang et al. [64], b)LCP experimental stress-strain.

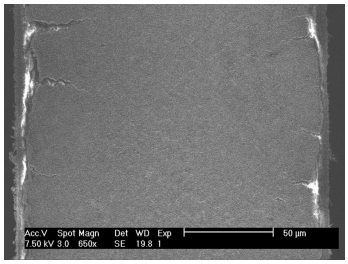
Young's modulus

From figure 5.21 b) we can also derive the Young's modulus (E). The E value was extracted through a linear curve fitting of the stress-strain graphs. From

figure 5.21 b) a value of E∼1.9GPa was derived. However, the results varied between 1.9-3GPa for various tests. The values were very close to the expected E=2.255GPa [46] for LCP.

5.4.3 Au mechanical properties

Figures 5.22 show the failure mode of Au during and after tensile testing. Fatigue of metals, and therefore cracking, is associated with the generation and motion of dislocations and accumulation of plastic deformation [159].

(a) 

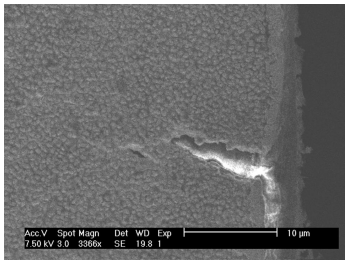
(b) 

Figure 5.22: Au failure modes after tensile testing: a) crack during tensile testing, b) crack during tensile testing (high magnification).

Yield strength

From figure 5.23 we can derive that Au yield strength is ∼36.3MPa at 6% strain which is close to what was estimated by Greer et al. [81] who measured a yield strength of 30MPa at 2% strain for Au.

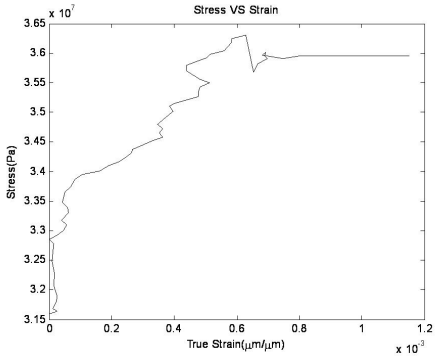


Figure 5.23: Au experimental stress VS strain.

Young's modulus

From the stress-strain relationship in figure 5.23 we can estimate Young's modulus of Au on LCP at 45.4GPa by fitting a linear curve. This is slightly less than what was found in the literature by Shi et al. [244] who calculated Au

thin film Young's modulus around 70GPa for thicknesses varying from 0.4 and 1.55μm. Our Au thin film was thinner (0.1μm), which might explain why the value we found is less than that of literature.

5.4.4 ZnO mechanical properties

ZnO ceramic inherent mechanical properties are of relevance for future device reliability. Hence its mechanical properties for the given conditions (relatively unplanar LCP substrate and ZnO sputtering settings) were assessed. One of the determining properties for future device reliability is ZnO fracture strength, which must be high. ZnO delamination mode is shown in figure 5.24.

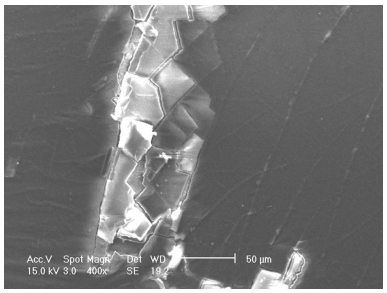


Figure 5.24: Cracking mode of ZnO after tensile testing.

Fracture strength

From the stress-strain graph 5.25 we can see a clear dip at 2.68GPa for a strain to failure of 0.00011μm, which is in a reasonable range as strain to failure for brittle ceramics is expected to be around 0.1 per 1000 [private communication from Petros Gkotsis]. The fracture strength of ZnO thin film found was, therefore, very similar to what was found in the literature where fracture strengths ranged from 3.33-9.53GPa [6].

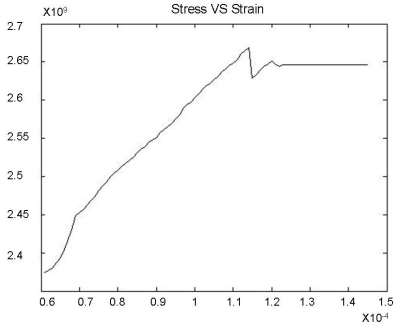


Figure 5.25: ZnO stress VS strain graph.

Young's modulus

From the stress-strain relationship in figure 5.25 ZnO Young's Modulus was calculated to be E∼54.5GPa.

5.4.5 Observations on multilayer mechanical analysis

The values found from the tensile studies for the mechanical performance of the materials confirmed what was suggested by the literature (where available). LCP properties confirmed what was found in the literature including its low Young's modulus. The material showed creep, recovery and necking behaviour prior to rupture. The material's high yield strength signifies that the transition between elastic and plastic deformation occurs at high strains. Au was also found to be subject to ductile fracture whereby, prior to failure, it undergoes yield stress. Its E was one order of magnitude higher than that of LCP. Given its brittle nature ZnO performed much more differently from both LCP and Au. No yield strength was observed in the ceramic, as the transition from elastic deformation to material failure was sharp. This behaviour underlines the brittle nature of ZnO, which is why we speak in terms of fracture strength instead of yield strength.

These results are important for the next sections as the future reliability analyses will require the measured stress values. ZnO fracture strength will be used as a comparison point for the future simulations whereby we will assess the extent to which various parameters (i.e. substrate deformation) affect the ZnO ceramic mechanical behaviour. Past the ZnO fracture strength the material would fail, leading to a damaged device.

5.5 Photolithography on LCP

Photolithography allows the patterning of the layers into desired features. In this project, photolithographic methods were employed and, in some cases, modified to suit the new substrate. Chen et al. [37] mentioned that lithography on LCP is more complex than on ordinary substrates due to LCP polymer having a vast quantity of pores.

Lee et al. [144] saw the improbability of conventional photolithography to fabricate patterns on flexible polymer substrate, due to the focusing and substrate handling issue associated with flexibility of polymer substrate. New maskless photolithography methods have therefore been investigated. These include: scanning electron-beam lithography (SEBL), focused ion-beam (FIB) lithography, multiaxis electron-beam lithography (MAEBL), interference lithography (IL), maskless optical-projection lithography (MOPL), zone-plate-array lithography (ZPAL), scanning-probe lithography (SPL), and dip-pen lithography (DPL).

Despite the availability of maskless photolithographic solutions for polymer substrates we employed classic photolithography methods for our LCP-based MEMS since it can yield high feature density on substrates. All the recipes and methods of these processes (bilayer, lift-off and reverse photolithography) are shown in the Appendix A..1. Proximity gap was increased from the usual 17.5μm up to 247.5μm in occasions in order to allow for the thicker multilayer and small substrate warpage (waviness) not to interfere and cause friction with the mask during alignment. Alignment accuracy was also discussed and quantified.

5.5.1 Bi-Layer and lift-off on LCP

Bi-layer is a method whereby a sacrificial photoresist layer is deposited and patterned. This is followed by metal deposition and subsequent lift-off of previously un-exposed parts of the wafer in acetone, leaving some patterned metal features. In our experiments bilayer and lift-off were carried out with both the standard and modified procedures shown in Appendix A..1.

Lift-off of metals on LCP has previously been carried out by Chen et al. [37] who used Cr-Au metal evaporation technique.Hess et al. [88] used negative-tone photoresist to obtain retrograde profile which greatly aided in metal lift-off on LCP.

Problems with bilayer and lift off were observed on our LCP substrates:

- Lift-off: impossibility to lift-off.
- Bi-layer and lift-off causing edge frills.
- Lift-off in acetone causing the the wafer backing to come off where used.

Impossibility to lift-off

On some of the samples the lift-off of sputtered metals did not occur even when left in acetone for 48hours. Figure 5.26 shows what happens when lift-off does not occur.

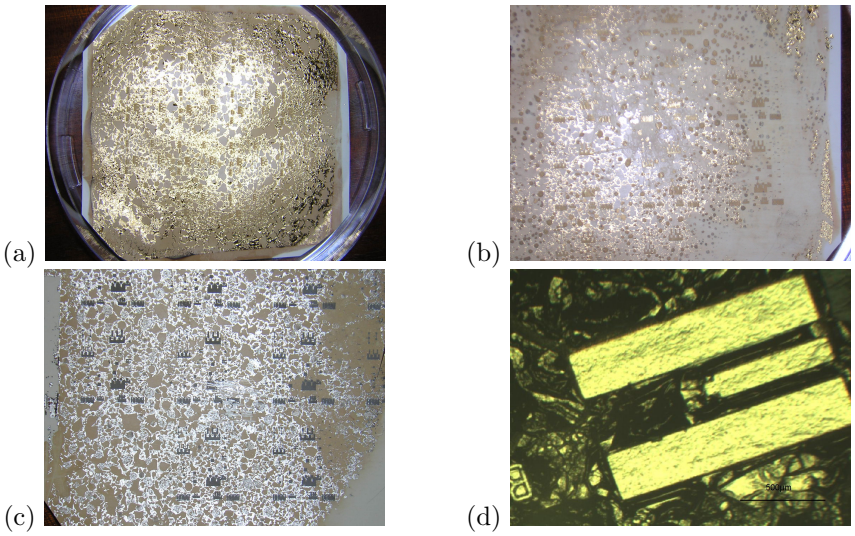


Figure 5.26: Impossibility to lift-off of : a)sputtered Au on LCP, b)sputtered Au on LCP (magnified), c)sputtered Pt on LCP, d)device view of c.

Causes for lift-off impossibility of sputtered electrodes:

- Interfacial polymerization through photoresist/polymer interaction. Polymerisation is described as the monomer-to-monomer bonding which leads to longer chain formation of polymers. Polymer-to-polymer adhesion with entanglement density in the interfacial region between polymer and developer [144] can happen due to plasma presence, overcuring or over-exposing the photoresist to ultra violet (UV) light.
- Low directionality of sputtering. Difficulty of lift-off when sputtering can arise because this deposition method does not provide the same directionality as evaporation does. Sputtering coats both the patterns and the developed sidewalls making it difficult for the acetone to infiltrate in the regions to be lifted off.

To address the metal lift-off impossibility a modified processes was adopted. To assess lift-off difficulty both modified bilayer and modified sputtering conditions (see Appendix A..1) were applied.

Through bilayer modification it is possible to assess whether it is the photoresist curing procedure that prevents the lift-off from happening. The bi-layer process modification did not solve the problem as difficulties in lift-off persisted and, in the small areas where lift-off did occur, pattern edges did not look well defined

(see figure 5.27). Modified bi-layer is not a viable solution.

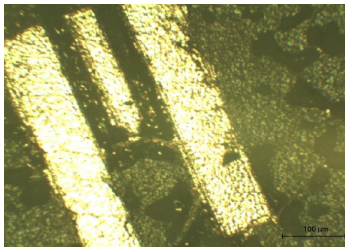


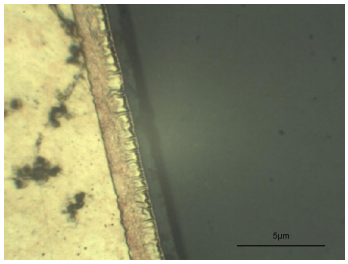
Figure 5.27: Modified bi-layer results undefined feature edges.

Through changing the sputtering parameters we were able to investigate on the photoresist/LCP polymerisation during sputtering. This did not seem to majorly affect the metal thickness which was measured to be close to the standard $\sim$ 125nm (close to 108nm). The Ar flow was decreased to 38sccm in order to ensure successful lift-off, therefore, eliminating any uncertain parameters. Failure to lift-off occurred even with lower sputtering power.

Edge frills

There is the usual problem of frills (or ragged edges) which, in our case, is caused by poor bilayer procedure. Ragged edges are a result of imperfect photoexposure during patterning [43]. They (shown in figure 5.28 a)) appear when there is no break in the metallization at the edges of features. Frills were only seen with sputtered metals and not for evaporated ones. Lift-off was originally only used with evaporated metals and evaporation is a directional deposition process which does not cause the risk of metal getting under the undercut.

One way to avoid getting edge frills on the devices is simply not to use bilayer and lift-off. To this end, an image reversal technique can be used that will allow the patterning of the devices after the metals have been deposited. This gives us well-defined features with clear, sharp edges as seen in picture 5.28 b).

(a) 

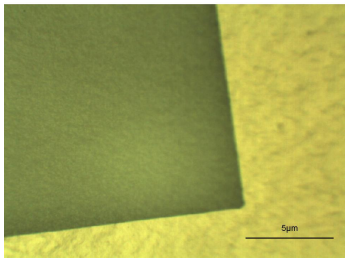
(b) 

Figure 5.28: a)Edge frill of sputtered bottom electrode metal caused by bilayer and lift-off process, b) No frill with feature etch after metal sputter deposition.

Detachment from backing wafer due to lift-off

Another issue caused by the bi-layer and lift-off process was the detachment of the LCP from the backing wafer during the lift-off step in acetone. The photoresist used to keep the silicon (or glass) substrate attached to the LCP eventually dissolved in acetone. Hence, two novel methods were suggested.

- Novel method for bi-layer which makes use of MF319 instead of actetone for lift-off of the bottom electrode. By avoiding the use of acetone, the LCP did not detach from its backing. The method is shown in table A.4 in the Appendix.
- Avoid bilayer and lift-off by using image reversal photolithography patterning (using positive photoresist) after blanket metal deposition. Process details are presented in table A.2 in the Appendix.

5.5.2 Alignment on LCP

The flexibility of LCP causes challenges in the alignment step. Common causes of misalignment can be: curvature, waviness, shrinkage and high TCE mismatch between layers. However, shrinkage of LCP is very small so it hardly created a problem. Residual stresses placed in the film during manufacture also cause dimensional instability.

Two of the best alignment accuracies (across wafers) were calculated on sample 13 between 10-20μm (see figure 5.29 a)) and on sample 21 between 5-10μm (see figure 5.29 b)).

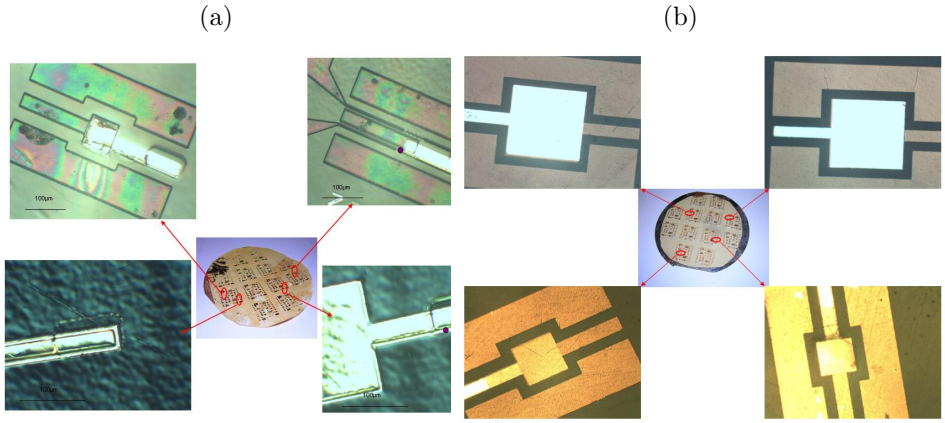


Figure 5.29: Alignment accuracy of devices across wafer: a) for Si-backed LCP hotplate bonding (sample 13), b) for Si-backed LCP vacuum bonding (sample 21).

Feature alignment accuracy was high considering that the mask aligners have a drift factor of ~5μm between alignment and exposure. The importance of decrease in substrate bowing and waviness through appropriate backing was demonstrated. Misalignment increase with decreasing radius of curvature was

also explicitly mentioned by Gleskova et al. [78]. In general, it can be concluded that the alignment accuracy of the devices on LCP is comparable to that of the devices on silicon.

5.5.3 Observations on photolithography on LCP

The use of bilayer and lift-off for bottom electrode creation should be avoided since it gives rise to various concerns including chances of having lift-off difficulties and 'frilly' edges. Blanket metal deposition followed by image-reversal photolithography and patterning should, instead, be carried out wherever possible. Avoiding bilayer on LCP and lift off eliminates lift-off problems, detachment of LCP from backing wafer and electrode frills.

By adopting blanket metal deposition and subsequent patterning method, the main consideration for a high alignment accuracy photolithographic process become substrate flatness, which encompasses waviness and curvature, and thermal expansion coefficient mismatch among layers. An acceptable alignment accuracy was achieved by using an appropriate backing method to keep the substrate flat.

5.6 LCP Reactive Ion Etching (RIE)

Etching polymers can be exceedingly challenging or exceedingly simple. The challenge springs from the fact that polymeric substances are widely varied in their make up [268]. Although LCP etch is possible in potassium hydroxide (KOH) solution, RIE was preferred due to its ability to provide many advantages including vertical walls and the avoidance of using a barrier layer (as we will see).

KOH is an isotropic etching method which leads to slanted walls. Chemical wet etching techniques are usually isotropic and yield sidewall angle taper of about a 45° Yang [308]. A tapered angle is undesired for our purposes as it adds to the overall device size. The method was not further pursued both due to both its isotropic nature and its fabrication process complexity (etch stop layer would be required in this case).

Another reason why RIE etching is preferred over wet etching is because it is a stress-free processing technique [68] well suited for the flexible substrate which, due to its high strain, deforms easily under stress. RIE etch also yields better uniformity (see picture 5.30).

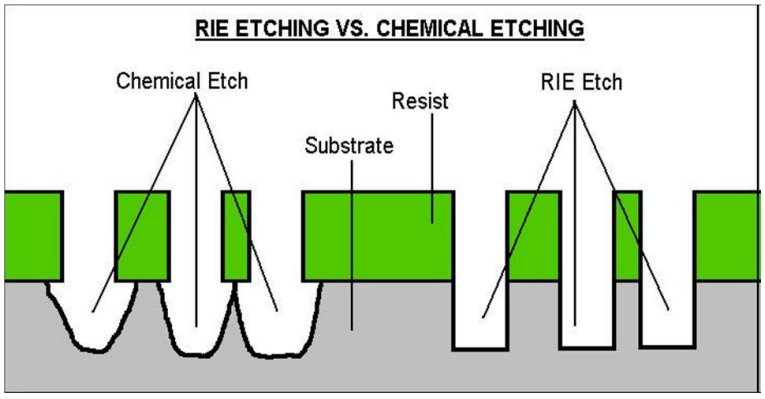


Figure 5.30: Wet and dry etching from [68].

Etching of LCP is an important bulk micromachining step for membrane-based devices and/or cantilever production. Membrane creation is the main focus of FBAR fabrication. Microfabricated membrane structures also serve other applications besides FBARs such as: pressure sensing, flow sensing, uncooled IR sensing and valves and pumps [183].

5.6.1 RIE etching conditions for LCP

LCP RIE was previously carried out by Wang et al. [292] who used oxygen plasma with a power of 350W, to achieve an etch rate ∼22-27μm/min. Gas composition, voltage and chamber pressure are the key parameters that affect LCP etch rate. This is why we carried out a study of parameter variation effect on LCP etch rate (table 5.2). It must be noted that the RIE chamber was prone to occasional contamination and that the results might have been affected by this.

Table 5.2: LCP RIE etching conditions (large etched surface areas).

Gases	**Flow (sccm)**	**Power (W)**	**Pressure (mtorr)**	**Time (min)**	**Etch rate (μm/min)**	**Surface roughness(μm)**
1. Oxygen (O_2)	60	120	70	20	0.1926	-
2. Oxygen (O_2)	60	150	70	20	0.2183	0.32(↑)
3. Oxygen (O_2)	60	150	100	20	0.53	1.5(↑)
4. CHF_3(15%)+(O_2)(85%)	3+17	300	70	20	0.65	1.98(↑)
5. O_2/Ar (85%)+CHF_3 (15%)	30+5	120	70	20	0.019	1.6(↑)
6. O_2/Ar (85%)+CHF_3 (15%)	30+5	120	100	20	0.42	1.2(↑)

From the results in table 5.2 we can derive that the main factors affecting the etch rate are the power (which is proportional to the voltage) and the pressure in the chamber. Increasing power increases etch rate while lower pressure decreases the number of free ions and, therefore, the etch rate. The combination of low pressure and high power yields good anisotropy and high etch rate. Unfortunately, due to equipment limitations, we were not able to carry etching at power ≻150W.

From table 5.2 we also observed that LCP roughness is proportional to chamber pressure, power and etch depth. Yang et al. [307] found that oxygen gas treatment of low-k SiLK ® polymer material increased the surface roughness from 1.08 ± 0.07 to 6 ± 1. Increase in surface roughness with chamber pressure was also noticed for Si substrates by Sugano and Tabata [263]. The roughness is attributed to surface reactivity (i.e. the reactant adsorption) and product desorption not being uniform on a microscopic level [135].

With all the processes it was noticed that LCP RIE etch yielded an anisotropic profile with vertical walls (no slope) as can be seen in figure 5.31.

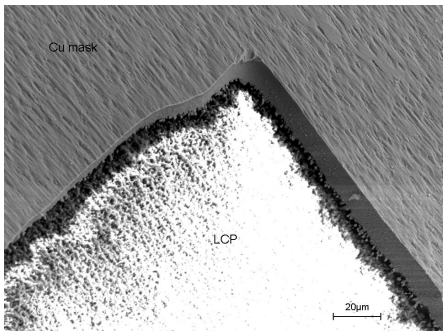
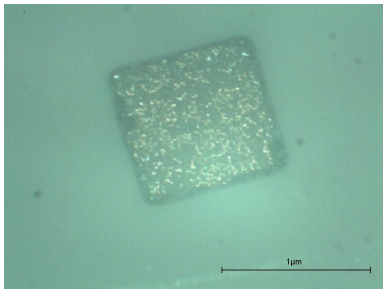


Figure 5.31: Anisotropic LCP profile with vertical walls (using process 3).

The devices around the outside of the wafer seemed to have a higher etch rate. The location-dependent nature of the etch rate led to over-etched and under-etched features as shown in figures 5.32. This could lead to low FBAR device yield for each wafer.

(a) 

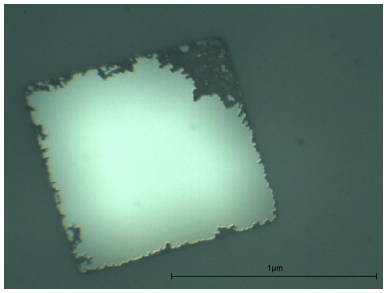
(b) 

Figure 5.32: Sample 18: a)etched 100x100μm^2 center feature, b)over-etched 100x100μm^2 LCP edge feature.

5.6.2 Material selectivity

In microsystems fabrication, when creating back-etched devices such as FBARs, piezoelectric and capacitive pressure sensors, and some types of cantilever, it is essential to know the material etch selectivity. Barrier layers are sometimes used to provide high selectivity and avoid over-etching of the back of the devices. For FBAR fabrication either silicon nitride (SiN_x) or silicon dioxide (SiO_2) layers are usually deposited on top of the silicon before any processing begins. These layers act as etch stop, providing high material selectivity.

In this project it was essential to assess the polymer (LCP) to metal (Au) and polymer (LCP) to ceramic (ZnO) selectivity. Process 3 and process 6 taken from table 5.2 were employed to quantify this parameter and RIE selectivity ratios are shown in table 5.3.

Table 5.3: Gas mixture effect on material selectivity using process 3 (Oxygen (O_2)) and process 6 (O_2/Ar(85%)/CHF_3) from table 5.2.

Process number	Materials	selectivity
3	LCP:Ti-Au	67:1
3	LCP:ZnO	44.5:1
6	LCP : Ti-Au	18.5:1
6	LCP : ZnO	2.5:1

Process 3 (O_2 only) was preferred over process 6 (CHF_3/O_2 mixture) since it showed higher selectivity of both LCP:Au and LCP:ZnO. The advantage of employing O_2 gas only, in terms of selectivity, was also observed by [268] who mentioned that the metal underneath should be unharmed by this etching gas composition. This is because oxygen does not produce volatile compounds on metals, so the etch rate for Au should be virtually zero.

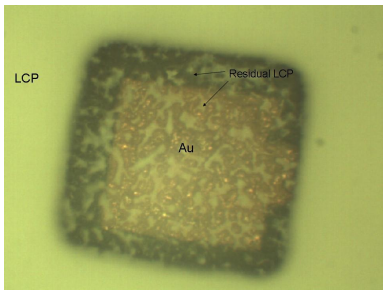
Despite metals being resistant to CHF_3, ZnO was affected by it. Although investigation of ZnO RIE etching is still in its infancy, it is known that this largely involves a process in which a volatile metalorganic zinc compound is formed. This volatile zinc compound was proven to be achieved through chlorine and hydrogen-related chemistry by Lee et al. [143], Guo et al. [84] and Schuler et al. [239] who used CH_4, H_2 and CHF_3-based plasmas to remove ZnO with an etch rate of around 5nm/min. O_2, however, does not seem to have any known effect on ZnO.

For the above-given reasons the preferred recipe was number 3. By using pure O_2 plasma gas the LCP:Au selectivity was high. Hence, a barrier layer was not necessary. One way to further increase LCP:Au selectivity is through increasing chamber pressure. This is because RIE is both a physical and chemical process, hence an increased pressure increases the etch rate in the chemically reactive materials (i.e.: LCP) but does not affect the chemically stable ones (i.e. metals). As chamber pressure increases, the mean free path of the ions decreases, decreasing the physical-caused etching and therefore making the chemical-related etching prominent in the system.

5.6.3 Backside processing and fabrication of free-standing membrane

For backside processing the general approach it to use a hard mask at the back of the substrate and carry front-to-back alignment with a double side mask aligner. The following were used as hard masks: photoresist, Cu, Ni, Au and Si. For all of these cases, except the Si case, the hard mask was patterned and then wet etched leaving the LCP exposed and ready for RIE. For the Si-backing case the procedure was slightly more complex. With this masking method the silicon is first masked either with photoresist or Al (see tables A.5 and A.6 in Appendix A..1) then etched through in DRIE leaving either LCP or LCP/Cu exposed.

Process 3 from table 5.2 (with O_2 gas) was chosen to successfully carry membrane etching and, hence, free-standing device structures. However, as we can see in figures 5.33, there were residues at the back of the free-standing membranes.

(a) 

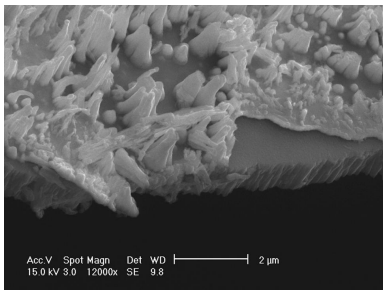
(b) 

Figure 5.33: Etch pressure 70mTorr (sample 16): a)free-standing device with LCP residues at back b) LCP residue close-up view.

LCP residues at the back of the device can be induced by the following reasons:

- The material's potential inhomogeneous nature. When etching an inherently inhomogeneous material, some parts etch faster than others, leaving polymeric residues in some areas at the back.
- The material's initial roughness. When etching a rough material the initial asperities are reproduced throughout the etch process. If this is the issue, it can be simply solved by reducing the LCP roughness on the back of the substrate (through CMP) prior to processing.
- The RIE etching process. One solution to get rid of the residues could be proceeding with high pressure etching in order. High pressures would allow better selectivity between LCP:Au and, therefore, virtually no risk to the Au being etched away.

By using process 3 but increasing the chamber pressure to 200mTorr, residues of LCP at the back of the free-standing device reduced (see figures 5.34).

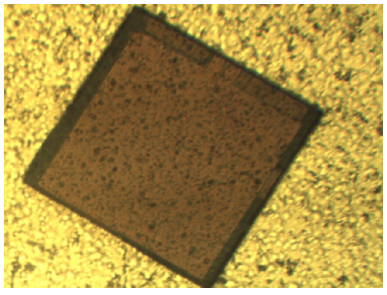
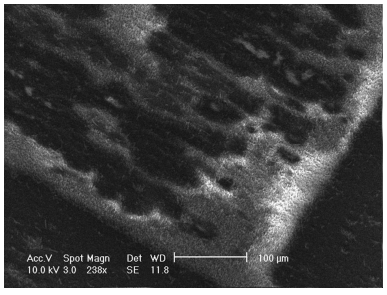
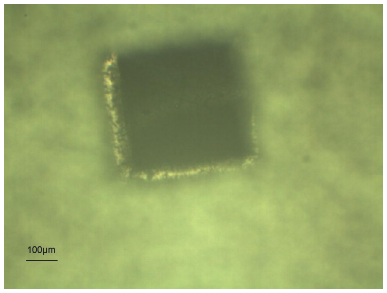
(a) 
(b) 

Figure 5.34: Etch pressure 100mTorr (sample 21): a)free standing device with LCP residues at back b) LCP residues (close-up view).

By using process 3 it was found that the etch rate of LCP for feature sizes larger or equal to 200x200μm^2 was $\sim$0.53μm/min, while for features between 50x50 and 200x200μm^2 the etch rate was $\sim$0.12μm/min. Hence, we can conclude that small features etch slower than large ones. This is because a larger feature has more area exposed for the supply of active species and the removal of etch products. In small features supply and removal of species are likely to be reduced as their transport to and from a smaller area is more difficult and, therefore, slows down the etch rate. Figure 5.35 shows the etch rate dependance on pattern size. Both devices are in the same area of the wafer (quadrant 3) sample 21 and etched for 7 hours.

(a) 

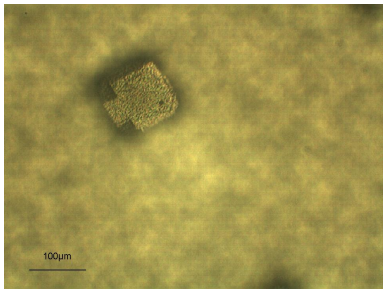
(b) 

Figure 5.35: Size effect on etch rate (sample 21) back view: a)overetched 500x500μm device, b)100x100μm device.

Furthermore, when dry etching, it is important to remember that the non-planar LCP surface and its propensity to attract contaminants to its surface, cause poor yield when etching very small features (smaller than 10μm) [52].

5.6.4 Observations on LCP etching

We have proven that the use of O_2 gas at high chamber pressure and high power yields high etch rate and very good anisotropic straight walls on the LCP.

The dependence of etch rate on device size and location inside the chamber was noticed. Eventual device yield issues can arise during membrane release involving over-etching of some devices (either large or at the edge of the wafer) and under-etching of others (either small or at the center of the wafer). Hence, etch rate instability can be caused by one or a combination of the following: feature size, feature location inside the chamber, and sample waviness which means that the sample is not fully flat in the chamber during etching.

LCP residues at the back of the free-standing device were also an issue. The residues were diminished RIE chamber pressure increase from 100mTorr to 200mTorr. Increasing the pressure allows a very selective removal among the materials due to a dominating chemical reaction (as opposed to physical removal). From sample 17 onwards the LCP residues at the back of the devices decreased.

5.7 Issues on MEMS processing of LCP substrates for FBAR fabrication

Manufacturing MEMS devices on polymers with standard microsystems fabrication techniques proved to be challenging. First of all substrate flexibility can be a source of many manufacturing problems. Furthermore the LCP's surface texture leads to some challenges. In this section we investigate the issues related to FBAR fabrication on LCP. Possible solutions are also suggested.

5.7.1 Roughness reduction issues

Topographic damage

Lap polishing, if not carried out with appropriate equipment aimed at microsystem processing (such as Okamoto corporation's semiconductor polisher and a relatively soft slurry), can cause visible surface striations which will later affect the metal deposition as shown in 5.36.

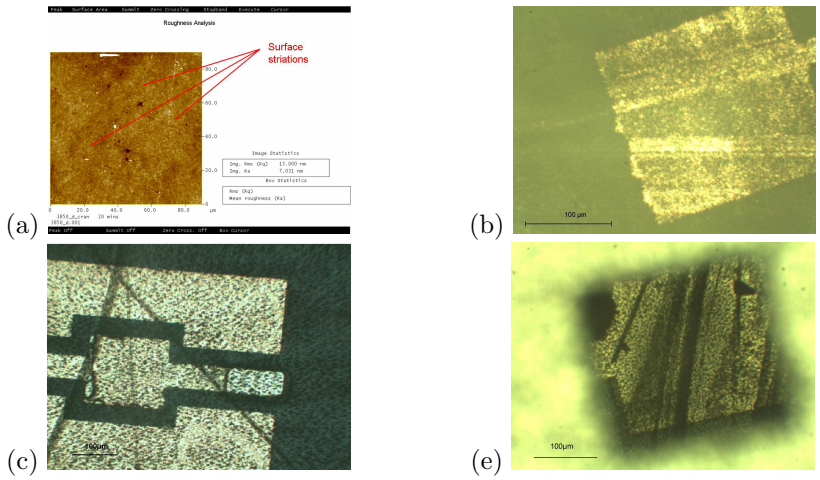


Figure 5.36: a)Striations on polished LCP , b) striations reproducing on bottom electrode Au(100nm), c) Au (200nm), e)striations after LCP etch (back view).

In figure 5.36 we can se that the substrate striation morphology is reproduced on the sputtered metals. CMP-induced striations are evident on LCP a), gold deposited on LCP b), ZnO deposited on LCP/Au c), and the back of the free-standing membrane.

Striations on LCP can be quantified by noticing an increase of roughness in the area which contains them. Figure 5.36 a) shows the AFM image of sample 21, which should have Ra∼5nm, however the striated areas lead to and increase of Ra∼7.1nm.

Surface stresses

Surface polishing introduces residual surface compressive stresses which make the flexible wafer curl. An measurement of surface stresses on LCP after polishing can be provided using the diffraction method or (sin square psi method) and represented in equation 5.2 [30].

$$\sigma = -\frac{E}{2v} \cdot \frac{\delta d}{d} \tag{5.2}$$

Where E is the Young's modulus, v is the Poisson's ratio, d is the position of the crystal peak before polishing and δd is the difference of the crystal position before and after polishing. Using the diffractional stress measurement technique, it was found that for a 120min lap polishing at 35rpm with silica slurry, a compressive surface stress with value 6.8MPa was induced. The stress induced by lap polishing is very small compared to, for example, polyimide coating, making it the preferred method.

5.7.2 Metal deposition issues

Sputtering on LCP has shown to create crater-like features on the substrate. This can be explained by the sputtering collision cascade phenomenon happening in the heat spike regime instead of the linear one. Heat spike happens when ions of the sputtered material are heavy and energetic (the material is dense) causing the collisions between them to occur near each other. Heat spikes near surfaces lead to crater formation [297], [103] characterized by an underdense region in the center of the cascade, and an overdense region around it. Since LCP is a soft material it is more susceptible to this mechanism than a hard material such as Si. Figure 5.37 showed burnt crater-like patterns on Au sputtered bottom electrode.

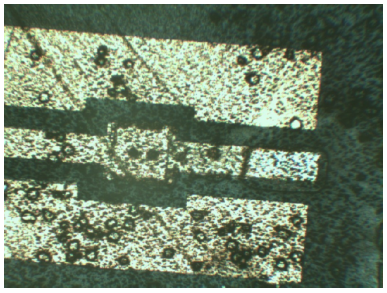


Figure 5.37: Crater formation during bottom electrode sputtering on (sample 9).

5.7.3 Photolithographic issues

The substrate low radius of curvature and high waviness can cause problems both in the alignment and in the feature development stages. Low radius of curvature can be an effect of the multilayer stress, while waviness is a result of

poor Si/LCP bonding.

Alignment damage

If the substrate is not fully flat, if it has a certain degree of waviness and/or bowing, the LCP rubs on the mask in the protruded areas, causing the features to be damaged. The features are affected and damaged by striation marks induced by the scrubbing action of the hard mask onto the softer LCP surface during alignment causing the photoresist to spread. This leads to the future device damage (see figure 5.38).

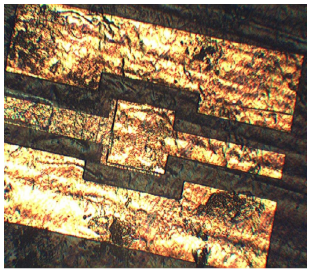


Figure 5.38: Ruined top electrode due to waviness and flexibility of substrate (sample 13).

Under and overdevelopment

The substrate's bowing and/or waviness, can lead to photolithographic under or overdevelopment of features and, therefore, inhomogeneous device production across the wafer. This implies that while some features are developed properly, others are either underdeveloped or overdeveloped during the UV curing stage. Underdevelopment causes impossibility of lift-off after metal deposition (figure 5.39 a)) while the overdevelopment leads to device full removal (figure 5.39 b)).

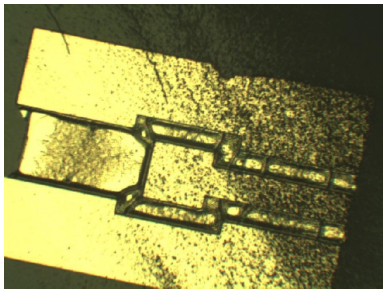
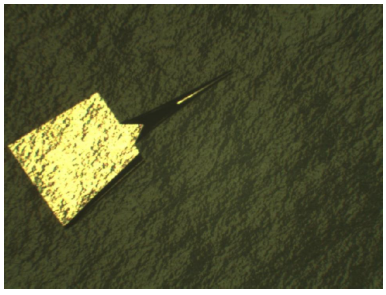
(a)  (b) 

Figure 5.39: Sample 13 a)underdevelopment of photoresist causing impossibility to lift-off metal, b)overdeveloped device.

5.7.4 Membrane etching issues

Membrane cracking

Membrane crack is believed to be caused by stress-induced deformation during fabrication. Residual membrane stresses are a consequence of the thin film's compressive stress. When the membrane is released through etching, the residual stresses can lead to buckling of this free-standing element. If these stresses exceed the yield or fracture strength of the materials, the membrane can fracture.

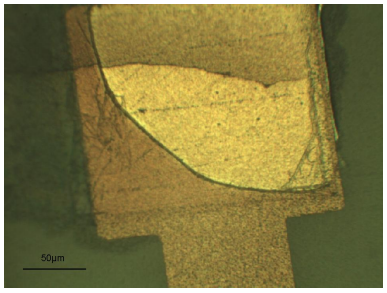


Figure 5.40: Free-standing FBAR membrane cracking due to residual stresses after RIE back etch.

Bottom electrode over-etching

Initial substrate roughness can cause many problems, as we have already mentioned. One further issue that this causes is the following. If the substrate is still rough before FBAR processing starts, when etching the membrane some of the bottom metal is also etched in the low-peak asperity regions of the substrate (see figure 5.41). This results in bottom electrode damage and leads to the eventual device behaving as an open when analysing it with VNA.

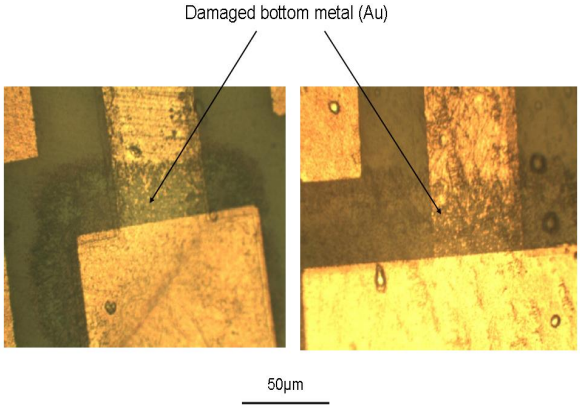


Figure 5.41: Damaged bottom electrodes caused by RIE etching the back of a rough LCP substrate (Ra∼50nm).

RIE substrate-to-metal etch selectivity becomes poor, the transmission line is damaged and this causes the device to act as a load instead of a resonator (see section 6.5.2).

5.7.5 Measurement issues

Analysis and measurement of new, non standard substrates is not always straightforward. Compliant and rough substrates cannot always rely on usual techniques and it is important to keep in mind that some measurement techniques carried out, such as XRD, curvature, optical and electrical measurements, can be affected by the roughness, waviness and low curvature of the LCP substrate. Therefore the methods have to be appropriately tailored to suit the specific cases

XRD and curvature measurement

Both XRD and curvature measurement methods require flat substrates. The angle of the incident x-ray scan can have major effects on the XRD results. Furthermore if the bowing largely deviates from the expected values, the profiler cannot detect the correct curvature value.

In some extreme cases of stress-induction the samples roll-up which does not agree with the requirement of specimen macroscopic isotropy [198] during x-ray and curvature measurement. Isotropy does not seem to be an inherent property of some of our samples (namely the polyimide-coated LCP) as curling shows the specimen's macroscopic anisotropic nature (y-axis larger than x-axis) as shown in figure 5.42.

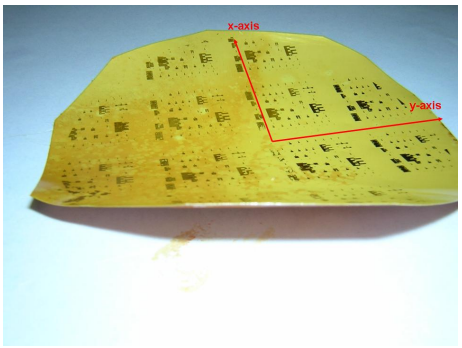


Figure 5.42: Figure showing anisotropic geometry of some samples when deforming.

Since polymer substrates are flexible and can undergo high deformation with thin film deposition, they must be attached to rigid backing at all times. This will also facilitate measurement taking.

Optical measurement

Roughness causes various kinds of disadvantages, including device-related drawbacks (low quality functional material growth). Roughness would make the use of optical metrology instrumentation impossible (i.e. Talysurf), which is why physical metrology techniques will be used instead wherever possible.

5.8 Processing story

This section ties up together all that has been carried out so far in terms of processing, putting into context the various fabrication steps. Table A.14 in section A..4 is a list of samples, which outlines the way they were processed. It is the scope of this section to explain the logic behind process development and modification from sample to sample.

5.8.1 Early samples

Samples 1-8 were early trials and were carried out on ULTRALAM 3850 Cu clad LCP as it was the first batch of the polymer available for use. These samples highlighted the need for flattening and reducing the roughness of the wafer.

Devices were not produced on them as they all failed at some stage. The most sensitive steps were: wafer backing, roughness reduction, bottom electrode deposition and general surface stresses induced by thin film deposition.

Due to the low stiffness of LCP, wafer backing was found to be a crucial part of device processing. Standard MEMS production techniques (i.e. use of vacuum chuck for holding the sample) did not apply when the substrate bowing was

large due to processing incompatibility. A low radius of curvature causes issues during material characterisation and measurement such as XRD analysis and surface profiling. Cu clad and electroplated Ni were used as backing materials but were not viable solutions.

A high surface roughness causes poor thin film growth (leading to non-functional devices) and impossibility of using standard MEMS optical metrology techniques. Roughness reduction introduces a variability parameter since the method by which this is reduced can affect metal deposition quality and substrate stresses. As shown in table A.14, for example, up to sample 8 the use of polyimide was popular, but this extra layer introduced unwanted stresses which is why after sample 8 CMP was preferred.

The ideal bottom electrode deposition method was also derived from these early trials. Bi-layer and lift-off did not suit the LCP substrate because of an interfacial polymerisation effect. Here, it was thought, the monomers of the LCP bonded with those of the photoresist during curing creating long polymer chain formation at the interface and, therefore, causing lift-off issues. Hence, blanket metal deposition with reverse photolithography and metal etching was the preferred solution.

Surface stresses on compliant substrates lead to wafer curling and feature misalignment during photolithography, which is why residual stress were examined. Residual stress studies are further addressed in chapter 7.

5.8.2 Later samples

Later samples included ones from 9 onwards and involved the use of both ULTRALAM 3850 and ULTRALAM 3800. These trials highlighted the importance of using a rigid backing such as silicon or glass with an intermediate adhesive layer (photoresist or black wax). Back-side processing method was investigated including the use of appropriate material as a mask for back feature etch.

Samples 10-13 made use of photoresist adhesive, however photoresist is susceptible to dissolve in acetone, which can cause the LCP to debond from the rigid substrate during the top electrode lift-off stage. Gold (Au) and photoresist were used as masks for the back-side etch of Si/LCP. Photoresist was shown to etch away easily during Si DRIE, while Au stayed intact. However Au is expensive.

Black wax was employed as the adhesive layer from samples 14-23 and was shown to be ideal as it was not affected by acetone. Aluminium (Al) was deposited at the back of most of these wafers to successfully act as the mask during DRIE and RIE etch. For cost reasons, Al was preferred to Au for use as masking layer.

Finally samples 20-23 proved the importance of an optimum CMP method for roughness reduction. Polymer-tailored lap polishing was carried out on these wafers showing a drastic decrease in roughness, a condition which is favourable for successful thin film deposition and proper device function.

5.8.3 Observations on processing story

As part of the MEMS processing requirements, the early samples showed the necessity of having flat and smooth substrates otherwise, leading to incompatibility of the samples with the standard fabrication processes.

Later samples showed the importance of rigid silicon backing of LCP as a viable rigidisation solution. The use of black wax as the adhesive layer was proven to be appropriate. Al was the preferred back-side mask and it was unaffected by DRIE and RIE etch processes. Furthermore, it was proven that an efficient CMP method can lead to drastic decrease in roughness.

In conclusion, the number of fabrication trials has helped us to develop the ideal FBAR processing conditions, which required both front and back development, using standard MEMS production techniques. The ideal FBAR-on-LCP fabrication parameters are: Si-backed LCP with black wax, lap polished LCP, bottom metal blanket deposition, appterning and etching, ZnO sputtering at 100°C and, finally, back masking with Al for DRIE etch of Si followed by high pressure (100-200mTorr) oxygen etch of LCP.

5.9 Observations on MEMS processing of LCP substrates for FBAR fabrication

In this chapter we investigated, among other things, metal deposition on LCP. First of all it must be noted that metals for bottom electrodes should always be sputtered and not evaporated. For sputtered Au, we concluded that metal quality depends on LCP roughness. Hence, good quality <111> oriented Au was achieved on low roughness LCP (Ra=5nm).

For ZnO deposition, we studied the dependence of the ceramic quality with respect to two parameters, namely LCP roughness and sputtering temperature. LCP roughness was seen to have a degrading effect on the ZnO <002> c-axis orientation. As the LCP, hence the Au, roughness decreased, the LCP quality improved. Surface analysis studies also revealed that, for LCP with Ra=5nm, the sputtering temperature which yielded the best ZnO crystal grains was 200°C. However, due to thermal-induced stresses causing ZnO failure in some parts of the wafer, a sputtering temperature of 100°C was considered to be more adequate. An electrical assessment of ZnO on LCP (Ra=5nm) at a sputtering temperature of 100°C revealed the results to be close to the desired values at both high and low frequencies. The ZnO exhibited the expected capacitive behaviour which showed transmission S_{21} decreasing with respect to frequency.

Multilayer mechanical analysis through tensile testing revealed the threshold values of our materials. LCP Young's modulus (E) was 1.9GPa with a yield strength (σ_y) of 186.27MPa, very close to the expected values. Thin film Au (100nm) had E$\sim$45.4GPa and $\sigma_y\sim$36.3MPa. Finally 1μm ZnO had E$\sim$54.5GPa and fracture strength 2.68GPa.

From the photolithography studies carried out we can conclude that bilayer and lift-off of bottom electrode metals should be avoided and replaced by blanket metal deposition followed by reverse photolithography. The use of bi-layer and lift-off on LCP presented many challenges including ones involving the inherent LCP properties (i.e. polymer-to-polymer interaction) and others that are common even in Si-based devices (i.e. edge frills). Alignment accuracy is another important photolithographic parameter. This was shown to improve when appropriate backing method was used, i.e. LCP/Si bonding in vacuum jig using thin layer of black wax.

RIE etch conditions were optimised in order to achieve both high etch rate and LCP:Au selectivity. It was also noticed that LCP etch rate depends on the feature size, as the size decreased so did the etch rate. LCP residues were still noticed at the back of the device. These diminished with an increase in etch pressure from 100mTorr to 200mTorr. Future investigation on complete LCP residue removal is still required.

Finally the processing story put into context the various fabrication steps leading to a fabrication improvement with the following conditions: LCP backed with Si and black wax, lap polished with appropriate tools, bottom metal blanket deposited and then patterned, ZnO sputtered at 100°C and, finally, the back masked with Al for DRIE etch of Si followed by high pressure (100-200mTorr) oxygen etch of LCP.

Chapter 6

LCP-based FBAR microwave performance

6.1 Introduction

FBARs were directly fabricated on polymer. The main fabrication process flows, which yielded the most succesful devices, are shown in figures A.2 and A.3. However there are more process flows in Appendix A..3. The reason for the large number of process flows indicates the number of trials for the FBAR processing on the LCP. This is because LCP does not have some of the requirements that standard substrates have for MEMS fabrication. First of all the LCP foil is not rigid and it, therefore, requires appropriate backing throughout device fabrication. Furthermore, as-received LCP is rough and must be polished prior to standard processing.

As we have already mentioned in the sections above, ICs are being produced on organic substrates as they offer lower cost and better performance than Si-based ones. Direct integration of RF MEMS devices on IC is desirable as it would reduce the total circuit area and eliminate the parasitics associated with the bond wires needed in off-chip components. An LCP-based FBAR could be easily bonded on organic PCB thanks to the high polymer-polymer interface quality achieved through a simple lamination process.

In this section we will first talk about FBAR yield on LCP in order to have a general idea on how the gradual processing tuning affects the final product which includes both fabrication and performance yield. FBAR performance will then be assessed through simulations and measurements of both LCP and Si based FBARs for comparison. Finally factors affecting LCP-based FBAR performance will be identified for future reference so that the processing can eventually be further optimised.

6.2 FBAR yield on LCP

In this project we have achieved an improvement in process control for FBAR production, which leads to higher device yield across a wafer with same dimensions containing the same number of devices. The FBAR mask used (see figure A.4 in Appendix A..5) is tailored for 4inch wafers and contains 12 squares with 47 devices each, for a total of 564 devices.

Yield was explained in detail in section 2.6.1 and can be subdivided into functional yield and parameteric yield. The former is characterized by defects (i.e. particles) causing shorting or open circuits, while the latter is the functional product that fails to meet the desired performance [189]. For our studies we will use the basic equation 2.33 in order to calculate the yield of each wafer. This is because we do not know the exact defect density of our samples (we need specific instruments) and equation 2.34 is too sophisticated for our purposes as we do not have the equipment to measure the defect density.

We should consider two types of yield. The first one is the fabrication yield, which refers to the percentage of devices that make it through the fabrication step and look like FBARs (qualitative approach). The second is the performance (or parametric) yield, which shows the percentage of devices that exhibit FBAR-like behaviour (quantitative approach), in other words, devices which exhibit resonant frequency and capacitive behaviour outside resonance such as that shown in figure 2.19 in section 2.4.

Although yield statistics are applied only once a standard process exists, its concept is essential in order to map the current processing potentials.

6.2.1 Fabrication yield

For the fabrication yield evaluation we considered the devices that made it through the front and back processing stages. Comparing sample 9 with sample 21 it is possible to see a yield improvement (see table 6.1). This is due to overall process optimization including appropriate LCP substrate rigidisation and roughness reduction. Process optimization refers to the reduction of parametric variations within the fabrication process. These variations can be: poor thin film growth, etching inaccuracies, mask misalignments, erroneous lithographic treatment, etc. [287]. Through roughness reduction and flatness enhancement of LCP we effectively contribute to eliminating some of the process variations.

Table 6.1: Fabrication yield using equation 2.33: devices that made it through the fabrication process (out of 564).

Wafer name	**Number of surviving fabricated devices**	**Yield (%)**
Sample 9	423	75
Sample 11	329	58
Sample 12	188	41.7
Sample 13	-	-
Sample 14	376	66.67
Sample 15	282	50
Sample 16	423	75
Sample 17	399	71
Sample 18	395	70
Sample 21	517	92

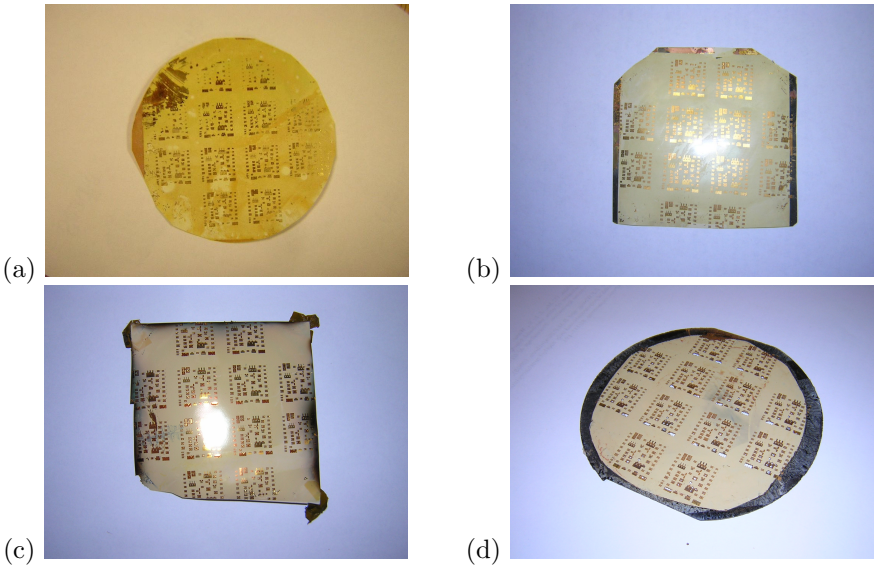


Figure 6.1: a)Sample 8 b)Sample 9 c)Sample 16 d)Sample 21.

From table 2.33 and figures 6.1 we can notice the progressive improvement of the samples (higher overall yield) due to process optimization. It is important to observe that these devices won't be considered for commercial use hence they were not included in the calculations. Misalignment can, in fact, cause sizing issues which are relevant when we consider that MEMS are getting smaller by the year and that one of the reasons for swapping inorganic Si with organic polymer substrates is to reduce the size. A drastic enough misalignment can cause clamping of the active device part and, as a consequence, mass-loading effect will arise conditioning its performance (see section 6.5).

6.2.2 RF performance yield

RF performance yield includes devices exhibiting an FBAR-like electro-acoustic response. It is important to mention that any traces with a resonance but without the expected 'capacitive' background as seen in figure 5.17 were ignored. This is because the capacitance is the basic behaviour of the ZnO for an FBAR.

Table 6.2: RF performance yield using equation 2.33: devices exhibiting FBAR-like response (out of 564).

Wafer name	**Number of working devices**	**Yield (%)**
Sample 9	3	0.53
Sample 11	2	0.35
Sample 12	3	0.53
Sample 13	-	-
Sample 14	8	1.42
Sample 15 (polyimide)	3	0.53
Sample 16	-	-
Sample 17	-	-
Sample 18	67	11.88
Sample 21	120	21.3

There is an evident device performance yield improvement from sample 9 to sample 21. While the earlier working samples (9-15) had low yield (0.3-1.42%) as we optimized the processing this figure improved to 21.3% (sample 21). Low yield of earlier devices can be explained by one essential process parameter, namely ZnO growth quality caused by LCP roughness. Some other causes of RF performance failure will be later discussed in section 6.5.

6.2.3 Observation on FBAR yield on LCP

Comparing table 6.1 with table 6.2, it is evident that performance yield is lower than fabrication yield. This is because the fabrication yield simply comprises the devices make it thorough the fabrication process and look like FBARs while performance yield implies FBAR-like electro-acoustic behaviour when the devices undergo electroacoustic measurements. The latter step can fail as the devices might not act like FBARs even if they look like them.

While fabrication yield did not improve greatly performance yield steadily increased. Comparing sample 21 with very first working samples (9-14), for example, we can see that the performance yield increases from 0.3-0.7% to 21.3% for sample 21 as the processing is optimized.

6.3 Simulated FBAR RF performance

There are various approaches to model FBARs including: Finite Element Modeling (FEM), mode-matching method, finite difference method [182] and acoustic boundary condition solution (or Mason model). Here simulations have been carried out in Matlab based on the Mason model's simple acoustic wave propagation principle. Acoustic modeling depends on mechanical factors of the various layers such as: physical properties (density, stiffness), geometry (thickness), electrical properties (substrate resistivity and ZnO capacitance) and acoustic properties (acoustic impedance and acoustic velocity).

Mason [188] proposed a fundamental model for linearised compressional waves to find transmission parameters using lumped component elements. Given the appropriate material layer parameters, the 1D Mason model is an analytical solution which helps in assessing the acoustic wave propagation effect in a multilayer, hence, determining the harmonics and the electro-acoustic behaviour of a coupled resonator filter.

Mason model accounts for mass-loading effects. Besides mass-loading, there are other factors that affect the acoustic behaviour of an LCP-based resonator: thickness, stiffness, density, acoustic loss of individual layers, surface roughness and visco-elastic modulus properties. Therefore the simple Mason model can be tailored to suit particular surface roughness and material visco-elasticity parameters through coupling of the effect of surface texture and substrate viscoelasticity. All models are presented in Appendix A..8 and will be explained accordingly.

6.3.1 Mason model FBAR simulation

The Mason model is a lumped element circuit representation of each layer that makes up a composite. It describes the electrical characteristics of an acoustic structure [230]. As we have mentioned above, the Mason model implicitly accounts for mass-loading effects on the acoustic response of the resonator. The mass loading model is solved through equation 6.1 [15].

$$Z_{mass} = R_{el} + (\frac{Z_{sys} \cdot R_{ZnO}}{Z_{sys} + R_{ZnO}}) \tag{6.1}$$

Where R_{el} is the electrode resistance and R_{ZnO} is the ZnO resistance (which depends on dielectric loss and capacitance) and Z_{sys} is the system impedance or motional branch of the resonator impedance with finite electrode thickness consideration given by equation 2.25 in section 2.4.3.

If we consider the simple 1D Mason model for a 200x200μm FBAR with ZnO thickness 1μm and etch stop layer (or buffer layer) thickness of 0.2μm (for the Si case only), we get the behaviour shown in figure 6.2 using equation 6.1 of the 1D Mason model.

The Si-based FBAR requires the buffer layer (also called etch stop layer) to protect the front features from the back substrate through-etch.

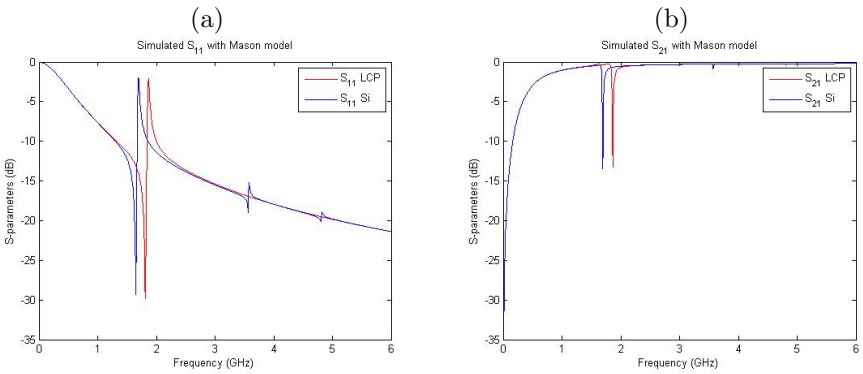


Figure 6.2: S-parameters of acoustic response for 200x200μm^2 FBAR a) Return loss (S_{11}), b) Transmission loss (S_{21}). Note that the LCP-based FBAR has no mass-loading effect due to buffer layer, while standard FBAR has a buffer layer of 0.2μm.

From figure 6.2 the main resonance frequency of an LCP-based FBAR is higher than the standard one due to etch stop layer elimination. Furthermore, without the presence of a buffer layer, there are no unwanted harmonics at 1.6GHz and 4.8GHz present within the designated frequency range.

6.3.2 Mason model coupled with viscoelasticity effect FBAR simulation

Theoretically a buffer layer for the LCP-based FBAR is not needed as we have already seen, however some polymeric residues at the back of the free-standing membrane were noticed (see section 5.6). While the simple mass-loading interpretation is sufficient for rigid layers of materials, this rigidity assumption is not valid for viscoelastic materials such as polymers [174].

In order to model the effect of extra LCP residues, a simple mass-loading effect is not enough as this only accounts for the real part of the modulus ignoring the attenuation caused by the the complex modulus of the material. Hence LCP viscoelasticity effect on the acoustic attenuation should be accounted for and modeled. This polymer/piezoelectric combination was previously modeled by [185].

Viscoelastic materials such as polymers have two modulus parameters: a real and an imaginary one. The real part determines the storage capacity while the imaginary modulus determines the energy loss. When added together, these two parameters yield the complex dynamic modulus (equation 6.2).

$$E = E' + iE'' \tag{6.2}$$

Where E' is the storage modulus (equation 6.3) and E" is the loss modulus (equation 6.4).

$$E' = \frac{\sigma_0}{\epsilon_0} cos\delta \tag{6.3}$$

$$E'' = \frac{\sigma_0}{\epsilon_0} sin\delta \tag{6.4}$$

If cyclic loading (such as a resonance frequency) is applied to viscoelastic materials, a phase lag (hysteresis) occurs, leading to the dissipation of mechanical energy and acoustic wave attenuation. The hysteresis represents strain lagging stress in a range between 0 and 90 degrees, where a 0° phase lag represents purely elastic materials while 90° phase lag shows a purely viscous material. A phase lag between 0 and 90 would represent a viscoelastic material.

Viscoelasticity has a great influence on the electro-acoustic response of acoustic wave resonators [174], which is why the necessity to couple the mass-loading effect with that of the viscoelastic one arises. If we add the viscoelastic impedance effect to the mass-loading one, we get an altogether different response for BAW resonator with thin LCP layer. The total impedance will be represented by equation 6.5 where the viscoelastic impedance is derived by equation 6.6 [174].

$$Z_{total} = Z_{mass} + Z_{visco-elastic} \tag{6.5}$$

$$Z_{visco-elastic} = jZ \cdot tan(\omega \sqrt{\frac{\rho}{E}} h) \tag{6.6}$$

Here Z is the acoustic impedance of the LCP and E is the complex viscoelastic quantity (or loss modulus) (E=3GPa [320]). Despite having assigned a set value for E in the simulations, it is important to know that it is directly proportional to frequency. The frequency dependence of E modulus was mentioned by Mason and Weitz [187].

Buffer layer thickness effect

A study of the effect of buffer layer thickness and back residue effect was carried out. This included simulations on LCP thickness effect on the FBAR resonance. We considered the viscoelastic-coupled mass-loading effect where, with increasing LCP buffer layer thickness, the viscoelastic properties gained influence on sensor response [174] characteristics such as frequency shift and loss/acoustic attenuation.

For ease of modeling the LCP residue effect in the calculations were considered to have a finite thickness corresponding to that of the buffer layer (SiN_x or SiO_2) thickness.

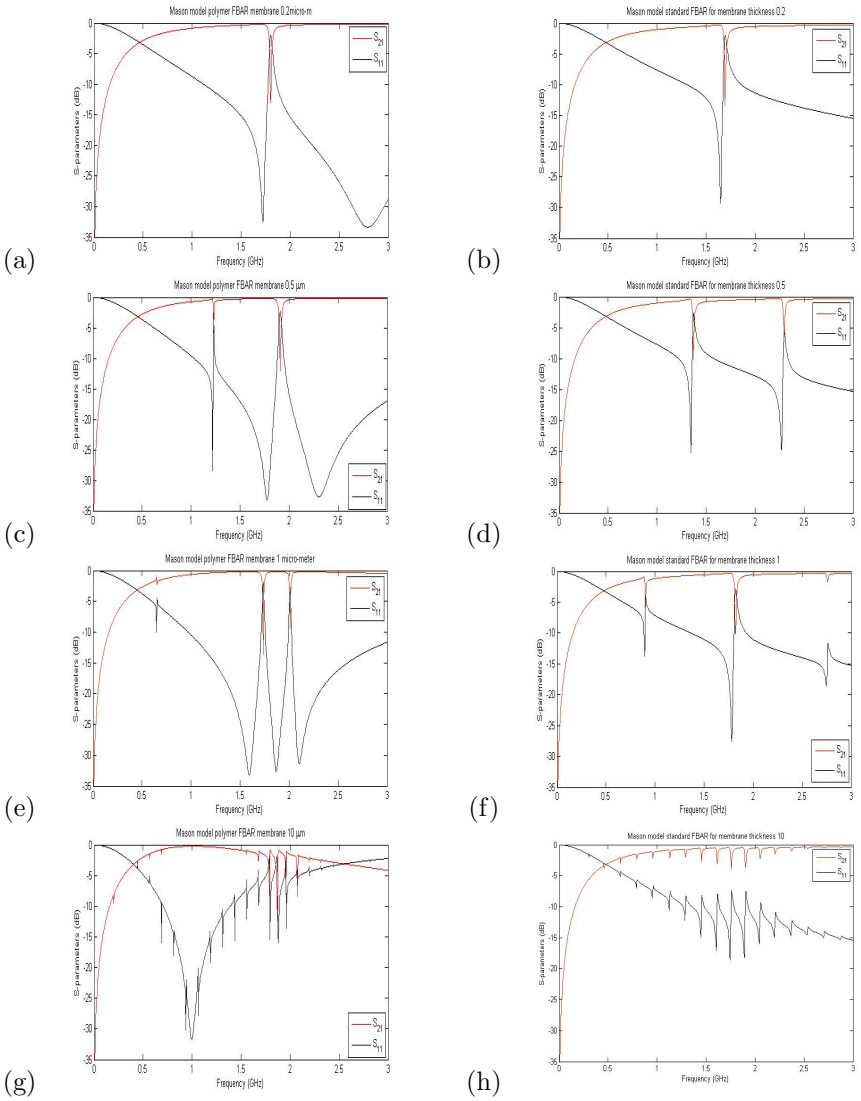


Figure 6.3: Effect of buffer layer with diferent thicknesses: a)0.2μm LCP, b)0.2μm Si, c)0.5μm LCP, d)0.5μm Si, e)1μm LCP, f)1μm Si, g)10μm LCP, h)10μm Si.

From figure 6.3 we see that, when residues of the polymer are left at the back of the device, LCP's visco-elastic nature causes the power and Q to dampen. This is because acoustic wave traveling in the piezoelectric thin film goes through the small LCP layer and, because of the presence of the loss modulus (dampening effect) in the LCP, a phase lag occurs leading to a dissipation of mechanical energy, acoustic wave damping (acoustic attenuation) and transmitted power magnitude decrease.

From the frequencies in figures 6.3 we can derive that SiO_2 (or SiN_x) buffer layer has larger mass-loading effect (higher density) than LCP (lower density),

therefore resonance frequency is lower. Acoustic impedance depends on the relation among layer thickness, wavenumber, frequency-dependent attenuation and material-dependent impedance. The second harmonic in the LCP-based FBAR seems to occur at a lower frequency and higher intensity than that of the standard FBAR. This spurious response is strongly dependent on the acoustic velocity ratios among the layers that form the FBAR [215] and, because of the presence of a loss modulus in the polymer, the acoustic energy distribution is less symmetric leading to even lower frequencies. This would, consequently, affect the frequency and intensity of the second harmonic resonant peak. LCP has lower acoustic velocity and density, which explains why its 2nd harmonic acoustic impedance is lower than that of the standard case.

6.3.3 Observation on simulated FBAR RF performance

When the thickness of the total acoustic layers increases by adding the acoustic loading layer, the frequency decreases [87]. By using LCP-based FBAR the extra buffer layer (SiN_x or SiO_2) is not required leading to theoretically higher frequencies than those of standard FBARs.

However, since we were unable to fully etch the LCP at the back of the FBAR, we considered the effect of LCP residues at the back of the composite resonator. Simulations including viscoelastic impedance effect on the structure, showed that (for thicknesses between 0.2-10μm) the low density of the LCP, caused the resonance frequency to be higher than that of a standard FBAR. Hence neither viscoelastic damping nor low LCP stiffness had relevant effects on the main FBAR resonance frequency.

6.4 Measured FBAR RF performance

Experimental microwave frequency measurements were taken with the Vector Network Analyser (VNA) which, before s-parameters measurement, is calibrated using SOLT (Short Open Load Through) method. The basis of proper FBAR electro-acoustic functioning is dominated by two variables: the capacitive nature of ZnO (related to the material growth quality and evaluated in previous sections) and electrode track resistance (which will be later measured).

For an FBAR without buffer layer the simulated scattering parameters (from Mason model) should be as shown in figures 6.4, which are used as a reference for the upcoming experimental results.

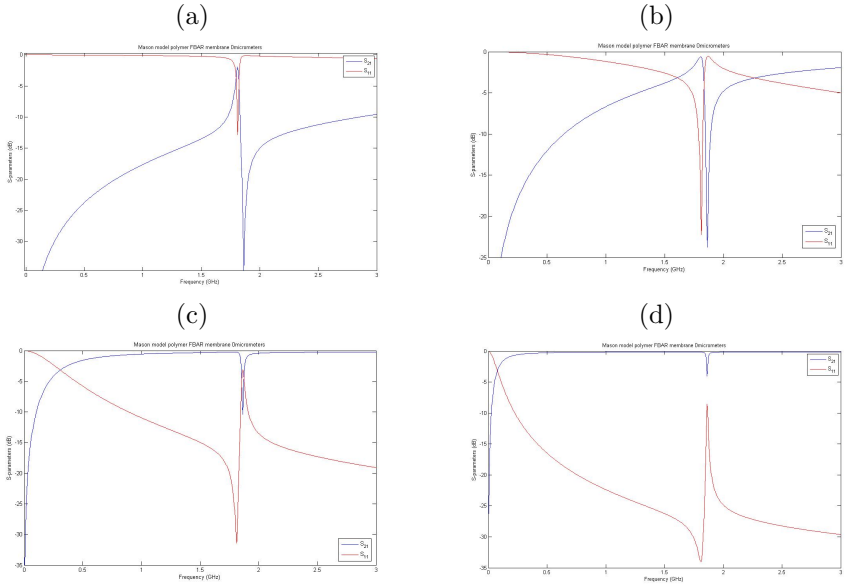


Figure 6.4: Simulated FBAR with no buffer layer. Lateral dimensions: a)50x50μm^2, b)100x100μm^2, c)250x250μm^2, d)500x500μm^2.

6.4.1 Final measured FBAR

The devices that made it through the first fabrication yield stage were analysed and validated with the simulations. Since device fabrication yield became relevant from sample 9 onwards, only these samples are considered for measurement and discussion. In the upcoming results only one device response is considered and discussed for each sample. S-parameters, representing the intensity of transmitted and reflected power in a device, are calculated. The responses are then de-embedded meaning that the effects of fixture and transmission line on the results are removed, hence representing the device data only.

Sample 9

Most devices on this sample shorted due to LCP substrate roughness and inappropriate subsequent ZnO growth. The best device yielding microwave response on sample 9 was a 50x50μm^2 FBAR. There were LCP residues left at the back with a thickness of $\sim$5μm. Figures 6.5 show the device.

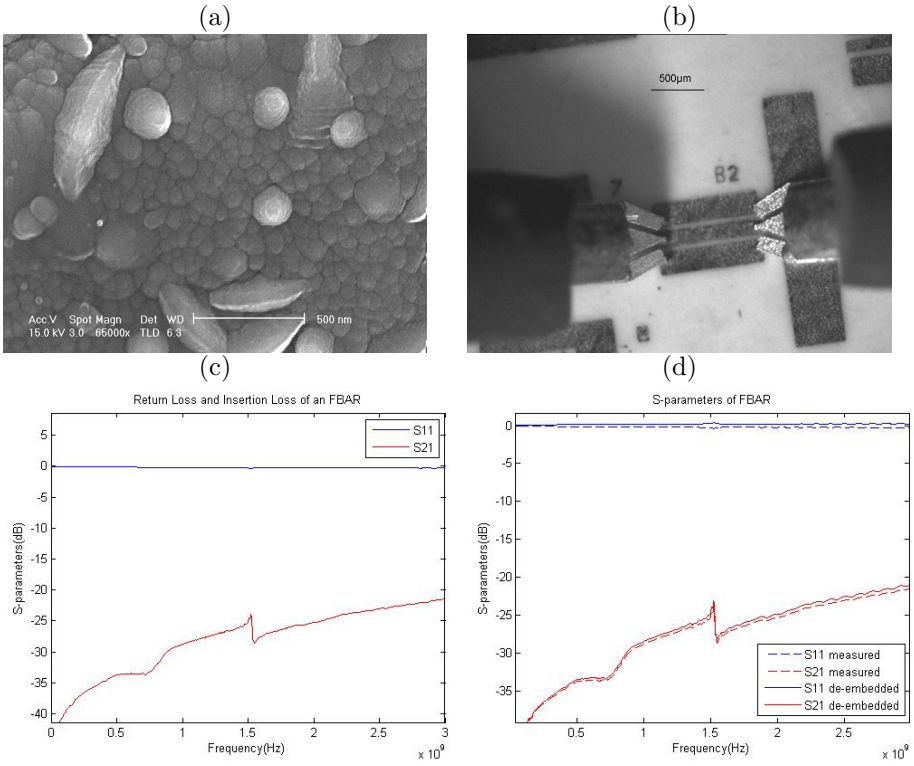


Figure 6.5: A 50x50μm^2 device with 5μm LCP residues at back: a)SEM image of ZnO, b)device measured under VNA, c)s-parameter measurement, d)comparison of measured and deembedded s-parameters.

Due to roughness, the transmitted power was not very strong. Furthermore, due to LCP residues at the back the Q dip around 0.7GHz was very low.

Sample 11

A 100x100μm^2 free-standing device showed the best FBAR-like properties.

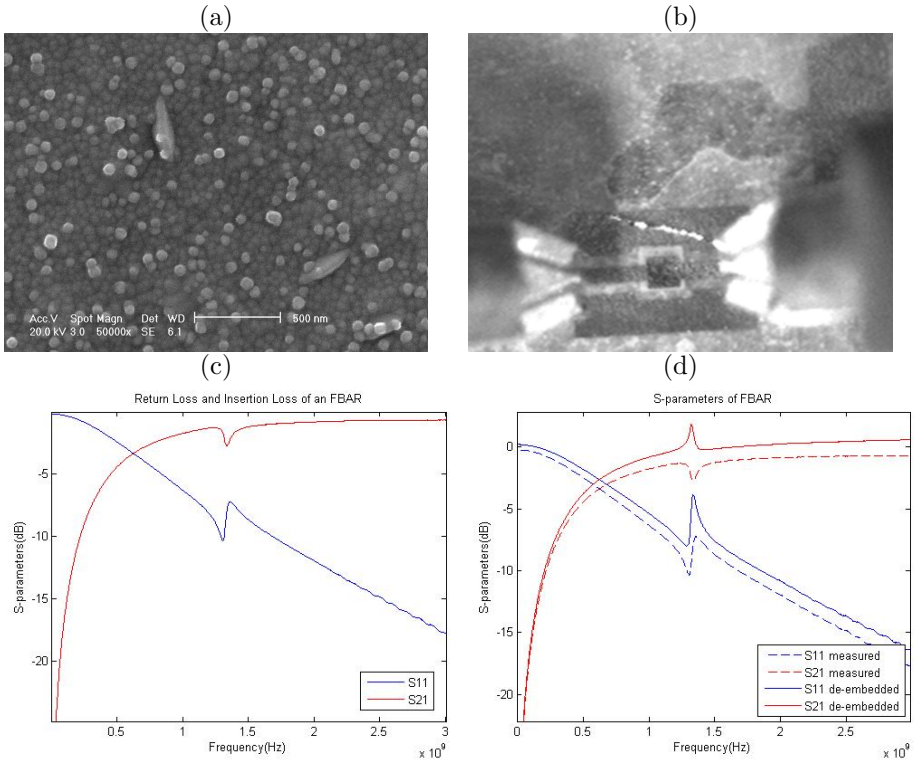


Figure 6.6: A 100x100μm^2 device: a)SEM image of ZnO, b)device measured under VNA, c)s-parameter measurement, d)comparison of measured and deembedded s-parameters.

Sample 12

The measured device was a 100x100μm^2 FBAR. Low Q is thought to be a consequence of substrate roughness resulting in poor ZnO material growth.

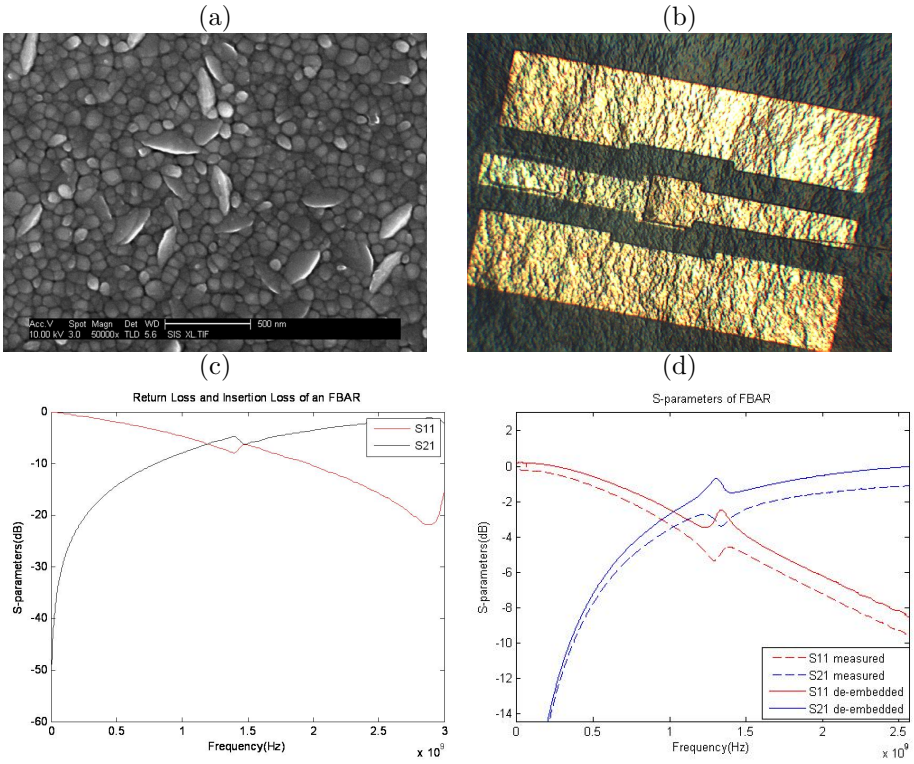


Figure 6.7: A 100x100μm^2 device: a)SEM image if ZnO, b) device image before LCP back etch and measuring, c)s-parameter measurement when released at the back, d)comparison of measured and deembedded s-parameters.

Sample 14

The measured device was a 250x250μm^2 FBAR.

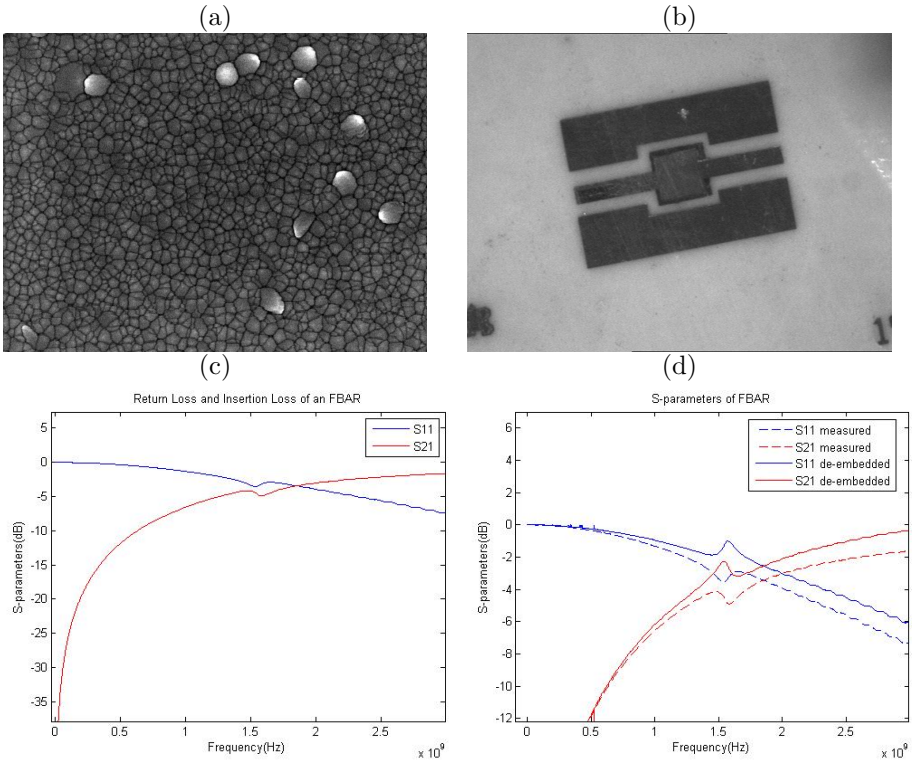


Figure 6.8: A 250x250μm^2 device: a)SEM image of ZnO, b)device measured under VNA, c)s-parameter measurement, d)comparison of measured and deembedded s-parameters.

Sample 15 (polyimide)

A 100x100μm^2 device was measured. Transmission power intensity was weak due to the CPW track resistance being high. Low intensity transmission power was caused by the suspended part of the transmission line being partially removed, causing an increase in track resistance (decrease in conductivity).

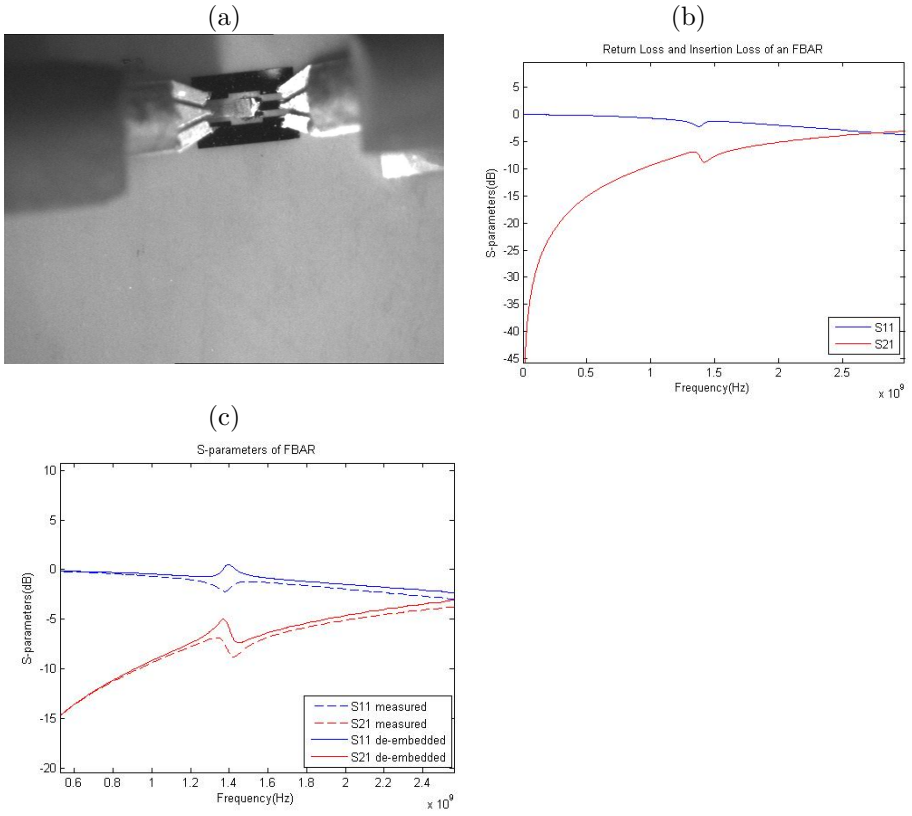


Figure 6.9: A 100x100μm^2 device a) while measured under VNA, b)s-parameter measurement, c)comparison of measured and deembedded s-parameters.

Sample 16

A 100x100μm^2 device was measured. The resonance frequency was high as the etched back had virtually no residues. However Q was still low due to surface roughness.

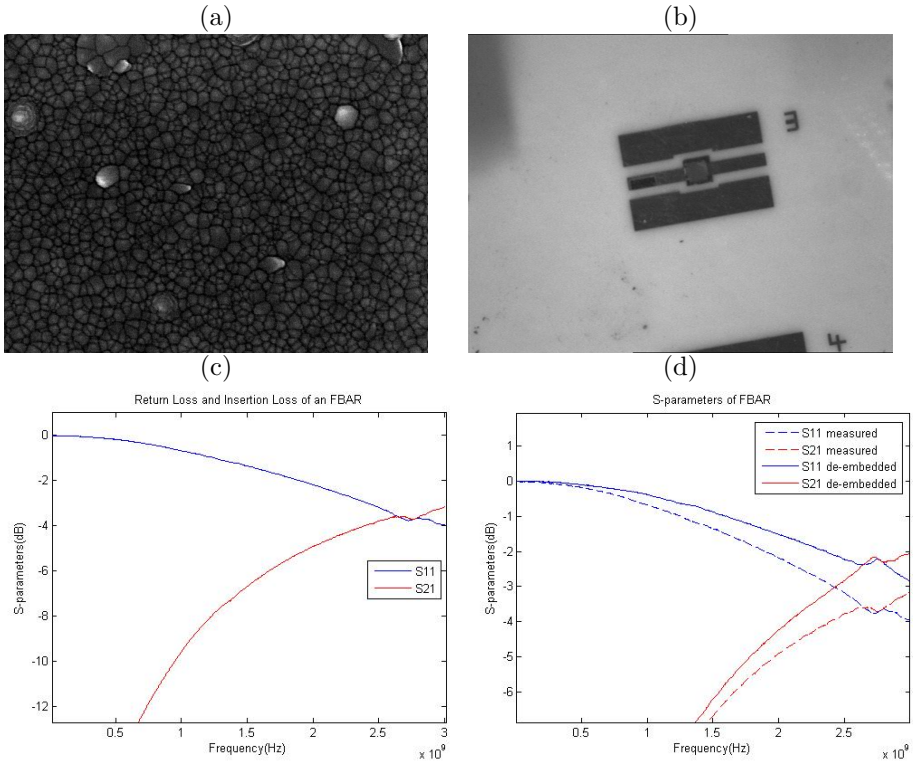


Figure 6.10: A 100x100μm^2 device: a)SEM image of ZnO, b)device measured under VNA, c)s-parameter measurement, d)comparison of measured and deembedded s-parameters.

Sample 17

A 500x500μm^2 device was measured. Due to the large size of the device, it was harder to get an even LCP etch at the back, so there were some residues left at the back causing a slight characteristic viscoelastic dip in transmitted power between 0.6-0.8GHz.

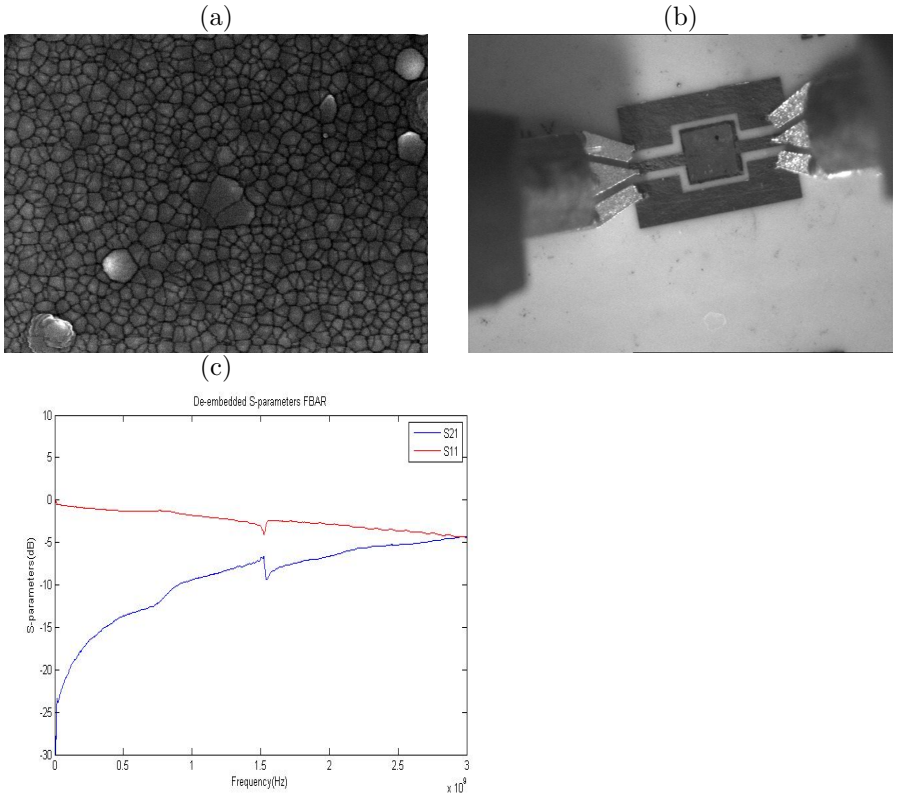


Figure 6.11: A 500x500μm^2 device: a)SEM image of ZnO, b)device measured under VNA, c)s-parameter measurement.

Sample 18

A 100x100μm^2 device was measured with better overall resonance characteristics, showing the effects of roughness reduction (Ra$\sim$17nm) and low back residues.

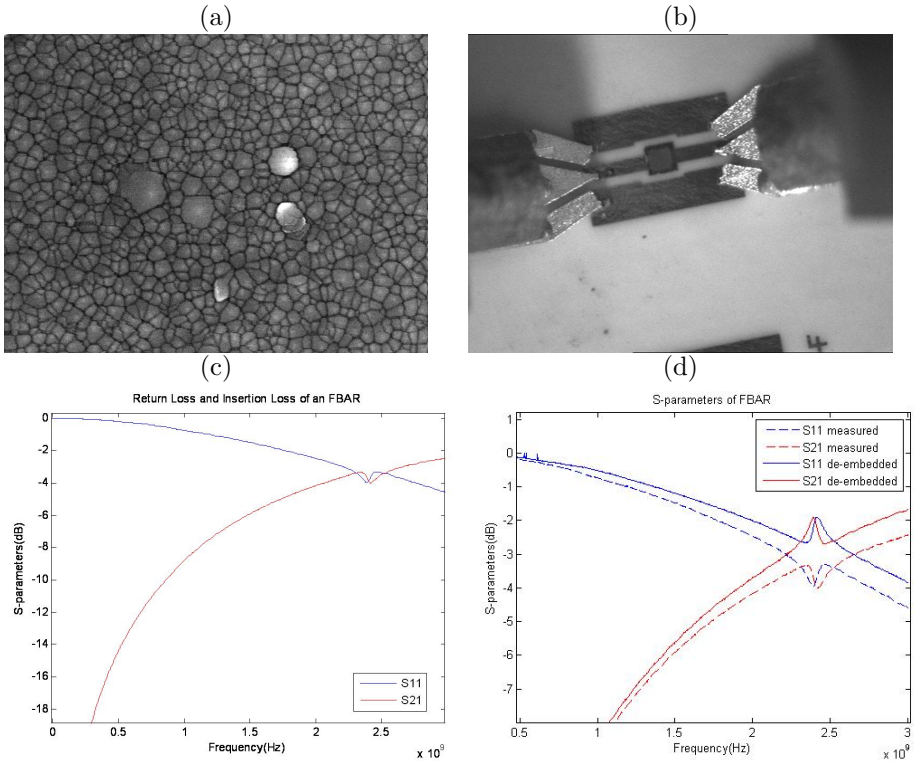


Figure 6.12: A 100x100μm^2 device: a)SEM image of ZnO, b)device measured under VNA, c)s-parameter measurement, d)comparison of measured and deembedded s-parameters.

Sample 21

By a further reduction of LCP to Ra∼11nm, we saw an improvement of the performance of a 100x100μm^2 FBAR.

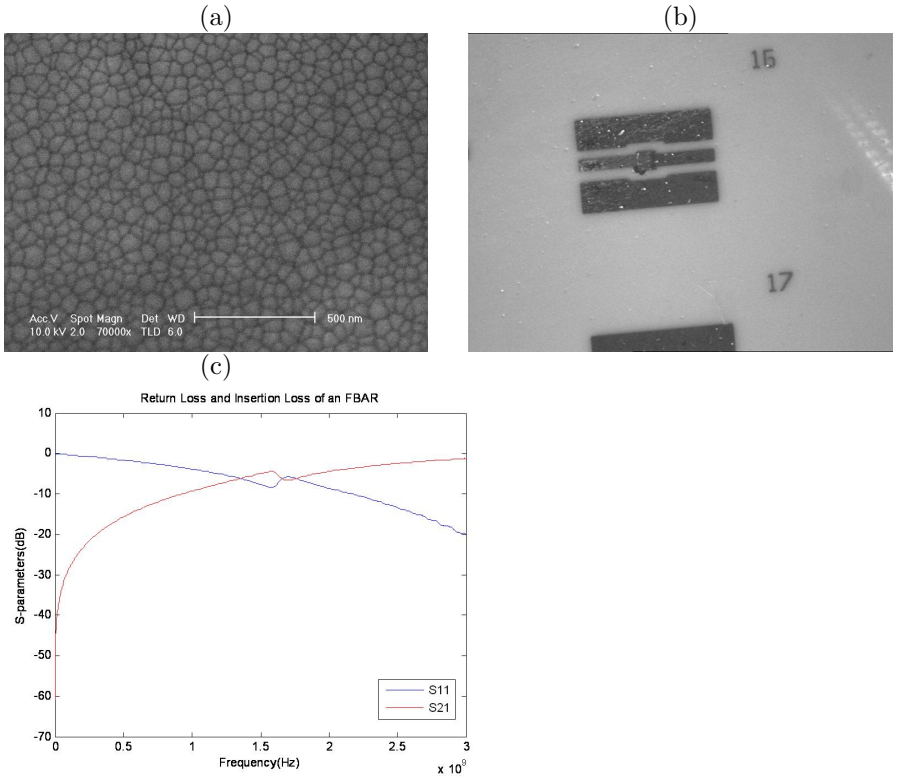


Figure 6.13: A 100x100μm^2 device: a)SEM image of ZnO, b)device measured under VNA, c)s-parameter measurement.

Q, k^2_{eff} of FBARs

The devices considered all had a background response (away from the resonance) like that of a capacitor. The resonance peak sharpness did not greatly improve even after de-embedding, meaning that the transmission line loss was not the main cause for low Q, but that the devices were lossy themselves. Frequency, Q and k^2_{eff} values were calculated after measuring the device's scattering parameters and de-embedding. S_{11} and S_{21} represent, respectively, the return and the transmission (or insertion) losses. The latter is a function of the transmission line characteristics and can include dielectric and conductor losses. Q can be calculated through equation 2.26 (section 2.4.3) and k^2_{eff} through equation 2.28 both presented in section 2.4. Q should ideally be around 1000 while k^2_{eff}, as stated in section 2.4.2, should be at least 7.5%.

Table 6.3: List of best FBAR responses for 1μm ZnO thickness.

Sample	**Device dimensions (μm^2)**	**f$_s$ (GPa)**	**f$_p$ (GPa)**	**k$^2_{eff}$**	**Q**
Sample9	100x100	1.55	1.5	0.0796	48.8
Sample11	100x100	1.67	1.54	0.1921	7.64
Sample12	100x100	1.52	1.49	0.0487	28.73
Sample14	250x250	1.6	1.55	0.0771	21.23
Sample15	100x100	1.5	1.42	0.1316	10.48
Sample16	100x100	2.8	2.67	0.1146	12.8
Sample17	500x500	1.52	1.51	0.0162	89.27
Sample18	100x100	2.48	2.34	0.1393	10.67
Sample 21	100x100	1.67	1.6	0.1034	13.3

Low Q factor was noticed and assumed to be caused either by LCP roughness (leading to acoustic attenuation) or by the presence of LCP residues at the back of the device. An acceptable surface roughness to be working towards for ZnO growth and FBAR production is 0.69nm [163] or, at most, 1.45nm [272]. Although Q was low, the devices showed potential FBAR-like characteristics. Both the capacitive nature of the ZnO piezoelectric and the large k$^2_{eff}$, important for proper FBAR functioning, were evident. With further roughness reduction and etch improvement, LCP-based FBARs could soon become a viable alternative to standard ones.

6.4.2 Observations on measured FBAR RF performance

For what concerns resonance frequency, the experiments validated the simulations as (given the same device dimensions) the frequency of FBAR on LCP was noticed to be higher than that of a silicon-based device. This is because of the lack of a buffer layer.

Even after de-embedding, the final LCP-based FBAR achieved had poor Q due to surface roughness still being relatively high. However a high k$^2_{eff}$ and a capacitive curve, signature of functional dielectric film, were noticed in all cases. The high k$^2_{eff}$ is indicated by the separation between the series and parallel resonances and is a sign of a good piezoelectric conversion performance.

The presence of LCP residues showed to influence the FBAR performance through overall acoustic attenuation and mass loading leading to slightly lower frequencies than expected and presence of spurious modes. The damped response is caused by the lossy LCP residues which, because of the lack of harmonics, were thought to be thin (see figures 5.33 and 5.34).

In general there is still room for improvement through LCP roughness reduction, which will lead to higher Q, and complete removal of LCP back residues, which will lead to higher frequencies and Q factor. The use of new materials such as molybdenum electrodes and AlN piezoelectric can also be considered.

Further troubleshooting for what might cause the poor FBAR performance is carried out in the next section.

6.5 Factors affecting FBAR device performance

Parameters that characterise good FBAR performance are: high frequency, low insertion loss, high quality factor and high coupling coefficient. We have seen that most of these are true for the LCP-based FBAR except for high Q. Rosenbaum [230] assigned poor Q to one or more of the following reasons: acoustic cavity attenuation, transducer attenuation, diffraction spreading in cavity, surface roughness, lack of cavity parallelization or attenuation in ground plane.

Since the low Q will not allow the devices to be taken to the production level, it is essential to fully understand the loss mechanisms of these LCP-based FBARs. In this section we analyse and understand the behaviour of our current devices in order to assess which variables mostly influence the retrieved measurements and, hence, how they can be improved. We will investigate on the factors affecting FBAR performance:

- Mass loading effect.
- Electrical contact problems: i.e. short or open circuits.
- Acoustic loss caused by ZnO surface roughness.
- Electrical loss and track resistance due to metal roughness.
- Measurement challenge on flexible substrate: contact pressure with probes.

Although there are many more, these are the ones that we managed to assess from the extracted and validated parameters, where the discrepancies of the measurements from the simulation were derived.

6.5.1 Mass-loading

Mass loading, which causes low frequency, low Q factor and high acoustic loss, can be a consequence of:

1. Presence of LCP viscoelastic material residue at the back of FBAR device.
2. Misalignment of the FBAR which causes one end of the device being clamped to the substrate.

The attachment of small mass can cause a large frequency shift [248] as can be calculated by equation 6.7.

$$\Delta f = \frac{2 \cdot \delta m f_0^2}{A\sqrt{\rho\mu}} \tag{6.7}$$

Mass-loading due to LCP residues

The effect of LCP residues at the back of the FBAR is assessed through both performance measurements and simulations.

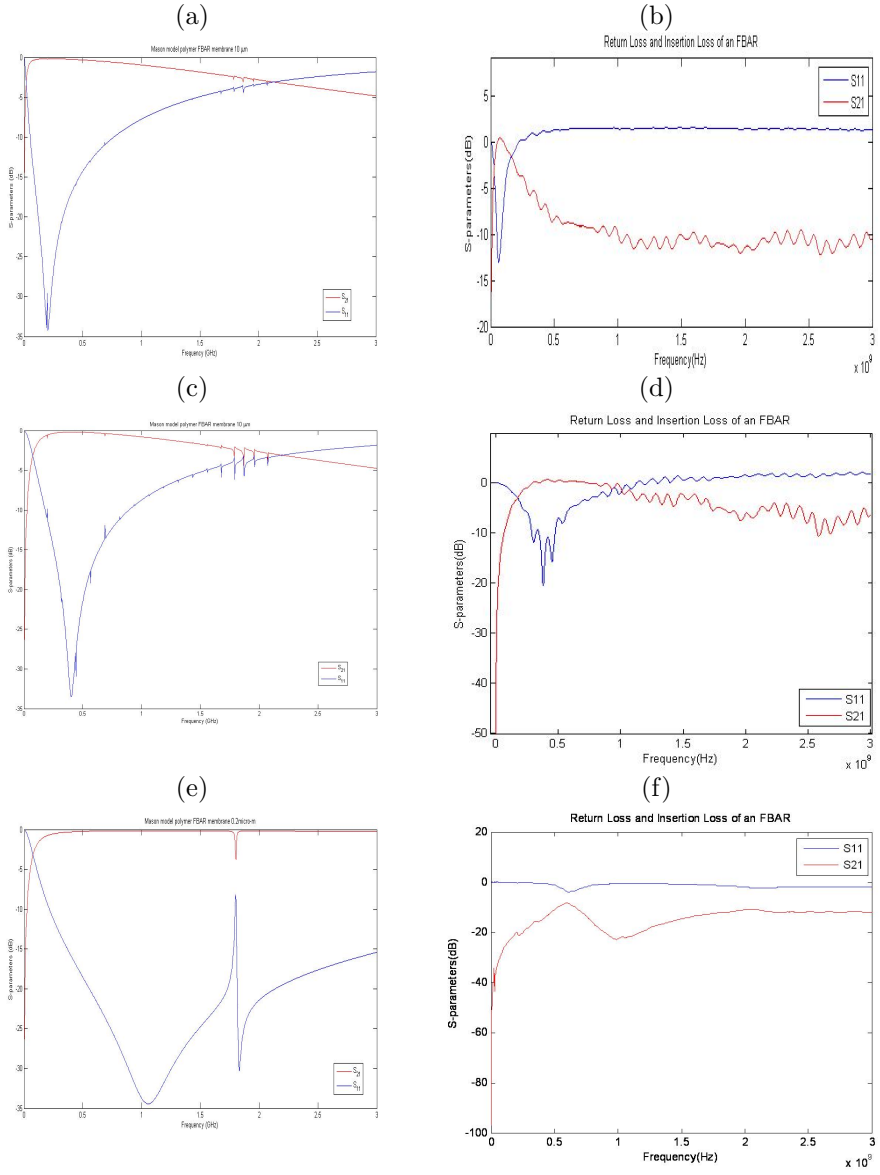


Figure 6.14: a)simulated 500x500μm^2 device with 10μm residue, b) experimental 500x500μm^2 device with 10μm residue , c)simulation for 500x500μm^2 device with 5μm residue, d)experimental 500x500μm^2 device with 5μm residue, e) simulation for 500x500μm^2 device with 1μm residue, f) simulation for 500x500μm^2 device with 1μm residue.

From figure 6.14 we can see that, given LCP of various thicknesses, the simula-

tions validate the extracted behaviour of a 500x500μm^2 FBAR. For the experimental results, the LCP thickness was reduced through etching.

Mass-loading due to misalignment

The dimensional stability of polymers is usually an issue and, despite LCP being known to have a relatively high dimensional stability, it is not ideal. Misalignment arises due to the relatively large TCE of the LCP (17ppm/°C). Misaligned devices experience clamping at the edges which leads to mass loading. Clamping effect on mass-loading was hard to simulate due to the 1D nature of the Mason model. Hence we quantified the effect of misalignment on frequency and Q experimentally. Figure 6.15 shows the final sample (sample 21) with slight misalignment (~5μm).

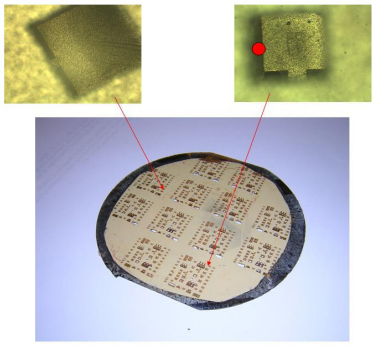


Figure 6.15: Sample 21 misalignment. The devices are shown from the back where a misalignment of 10μm is indicated by the red dot.

Taking two 200x200μm devices at either end of the wafer, we measured the s-parameters as shown in figure 6.16.

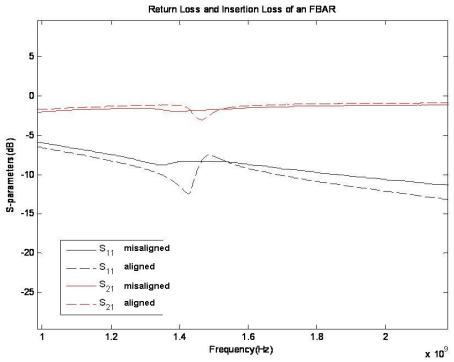


Figure 6.16: Misalignment causing resonance frequency shift and Q lowering in 200x200μm devices.

Figure 6.16 shows 200x200μm^2 misaligned devices, where the clamped edge evidently has a mass-loading effect as it reduces the frequency and Q. From figure 6.16 frequency of a free device is 1.43GHz, while that of the partially clamped device is 1.34GHz.

6.5.2 Shorts and open circuits

Fabrication stage problems can cause future electrical measurement misinterpretations. Fabrication issues are various: from bottom electrode frills and ZnO voids causing device shorts to metal transmission line damage leading to open circuit.

Shorts

When there are voids present in the ZnO, due to poor ZnO c-axis orientation, there is a possibility that the bottom electrode makes contact with the top electrode causing the device to short. Consequently the device does not act as a capacitor or resonator anymore, but as a coplanar waveguide (CPW).

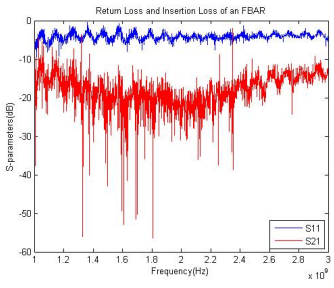


Figure 6.17: CPW-like response on FBAR due to short circuit between top and bottom electrodes caused by voids in ZnO.

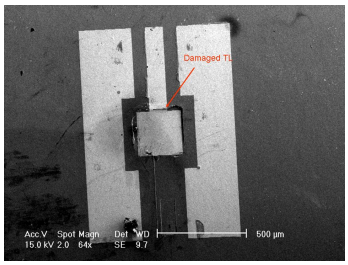
As seen by the S_{21} parameters in figure 6.17, the device acts as a CPW which suggests that there might be shorting occurring in the ZnO film. This shows the importance, among other things, of a smooth LCP substrate since it influences the ZnO growth directionality, hence, dictating the presence or absence of voids.

Open circuits

Open circuits can be a consequence of a damaged metal track. Metal tracks can be damaged during the RIE etch stage in two different ways.

The first mechanism is induced by waviness. A wavy surface causes parts of the substrate to be high and parts to be low making the higher parts more susceptible to high etch rates, hence, leading to a damaged and broken ground transmission line.

RIE-induced damage on Au transmission line can also be caused by rough LCP which leads to rough Au. This means that the high Au asperity zones are less resistant to RIE etch which will lead to damaged Au transmission line.

(a) 

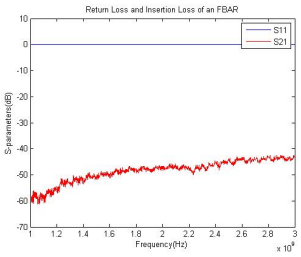
(b) 

Figure 6.18: 200x200μm^2 device on sample 21 (etched for 7hrs): a) damaged transmission line image, b) s-parameter response.

Figure 6.18 a) shows a damaged bottom TL. A destroyed transmission line acts as a capacitor and a capacitor with very small capacitance acts like an open circuit (see figure 6.18 b)).

6.5.3 Acoustic loss due to surface roughness

Acoustic wave loss in acoustic wave devices (i.e. FBARs) decreases the quality factor (Q). Surface roughness control is important to achieve as a rough surface can originate energy scattering loss [146] which then leads to acoustic attenuation [245]. The relationship between roughness (R_a) and acoustic attenuation (α_R) is given by equation 6.8 [245].

$$\alpha_R = c \cdot \frac{R_a^2 \cdot f^2}{\upsilon \cdot L} \tag{6.8}$$

Where c is a constant c=2.153, R_a is roughness of top electrode and has units in nm, f is the frequency and has units in GHz, υ is the acoustic velocity and has units in km/s, L is the distance between top and bottom electrodes and is measured in μm and α_R has units $dB/\mu s$.

The roughness of the ZnO grown on LCP of Ra∼50nm was measured to be about 200nm, whereas ZnO grown on Si of Ra∼0.045nm was around 8nm. The roughness-dependent acoustic attenuation derived is shown in figure 6.19 a).

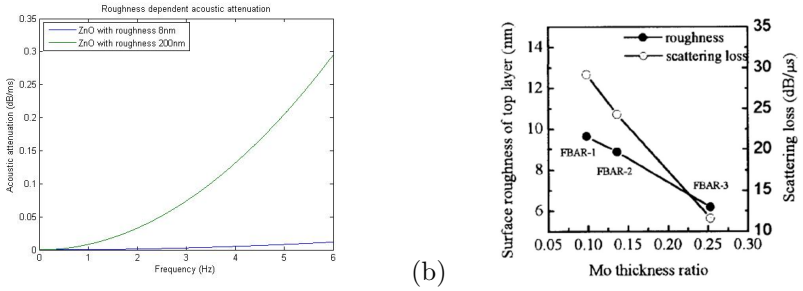


Figure 6.19: a)Simulation of roughness-induced acoustic loss of FBAR, b) s-parameter dependence on roughness from [146].

We calculated the acoustic attenuation term caused by the piezoelectric materials' surface roughness using equation 6.8. From figure 6.19 a) it is clear that acoustic attenuation is proportional to surface roughness. The acoustic attenuation α_R at resonance frequency of FBAR (∼3GHz) fabricated on Si in our simulations (2.9dB/μs) seems to be very close to that of the literature (10dB/μs) [146] (compare figures 6.19 a) and b)). Hence we can say that the attenuation results of the FBAR on LCP were correct leading, again, to the importance of LCP substrate smoothness.

6.5.4 Electrical losses due to roughness

Electrical losses in CPW can be divided in resistive and capacitive losses. Resistive electrical losses are caused by track resistance due to metal roughness. One approach to help us assess the effect of LCP surface roughness (hence Au roughness) on the electrical loss is to find track resistance.

Track resistance was calculated by using the method in Appendix A..7. First s-parameters were measured from thru line ABCD parameters, then the propagation constant (β, which is a secondary line constant) was calculated, and the values of the primary line constants derived. Primary line constants are: conductor resistance (R), inductance due to magnetic field (L), conductance (G) and capacitance between conductors (C).

Measurements were taken on a coplanar waveguide (CPW) which can be modeled as shown in figure 6.20.

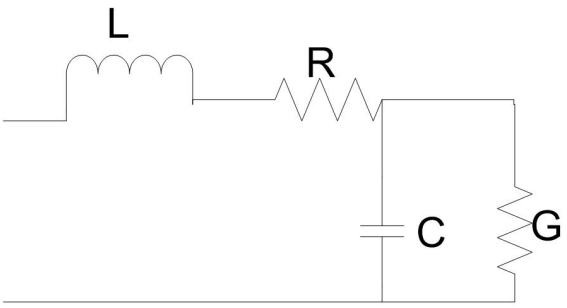


Figure 6.20: Model of a coplanar waveguide transmission line.

From this model we have two fundamental equations: the transmission line propagation constant (eq. 6.9) and the transmission line characteristic impedance (eq. 6.10).

$$\beta = \sqrt{(R + j\omega L) \cdot (G + j\omega C)} \tag{6.9}$$

$$Z0 = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}} \tag{6.10}$$

From Appendix A..7 we know how to calculate and predict both experimental and theoretical track resistances of Au metal track on LCP. After extraction of theoretical and experimental values, these were compared to one another. Table A.15 in Appendix A..7 shows the values used for the track resistance calculations on LCP.

Transmission loss was measured through VNA and then converted into track resistance with the technique shown in the Appendix A..7. Since transmission loss of Au CPW on LCP (Ra∼50nm) was higher than that of Au CPW on Si/SiO_2 (Ra∼0.045nm), track resistance on LCP was also higher than on Si due to LCP's higher roughness.

The theoretical resistance (R) of a gold slab with respect to frequency (f) is found through equation 6.11.

$$R = \frac{\rho \cdot l}{(2 \cdot \sqrt{\frac{2 \cdot \rho}{(2 \cdot \pi \cdot f \cdot 4 \cdot \pi \cdot 10^{-7})}} \cdot w)} \tag{6.11}$$

Where w is the width (20μm), l is the length (1mm), t is the thickness (100nm) and ρ is the material's resistivity.

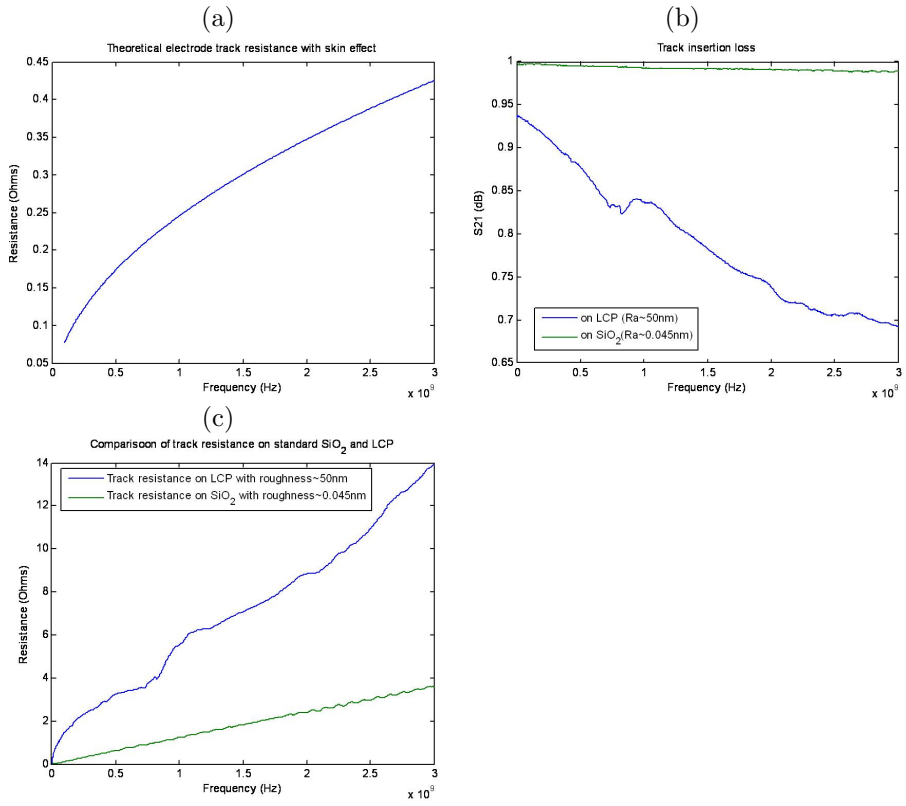


Figure 6.21: a)Theoretical track resistance, b)experimental transmission loss, c)experimental track resistance.

From figure 6.21 a) we can see that the track resistance should theoretically be ∼0.1-4 ohm for a frequency range of 0-3GHz. However this assumption does not take into account surface irregularities. Theoretical track resistance is much lower than experimental track resistance. Figure 6.21 shows b) the experimental S_{21} parameters (measured transmission loss) followed by c) the experimental track resistance extraction from transmission loss. From b) and c) we can see that both transmission loss and track resistance of Au on LCP are higher than on Si due to the LCP's higher roughness. The track resistance of metal on a rough substrate, in fact, is expected to be higher than on a smoother substrate, because the effective length on the track becomes larger while the cross sectional area and the resistivity of the material stay similar (see equation 2.49 from section 2.6.4).

We can conclude that surface roughness increases the metal track resistance values leading to less transmitted power (S_{21}). The slight discrepancy between experimental and theoretical values can be given by the fact that the dielectric loss mechanism was not considered in the model.

6.5.5 Measurement issues

As well as fabrication of FBARs on flexible substrates, electrical measurements on these compliant LCP surfaces can be a challenge. FBAR device measurement at microwave frequencies is carried out by making contact between probes and device metal tracks. Contact failure due to LCP flexibility and roughness, can be a liability as can lead to high resistances and cause measurement losses.

In this section we will analyse and discuss some of the reasons for high transmission loss in FBARs on LCP. The reasons are all somehow related to one or a combination of the following: substrate flexibility, substrate roughness and pressure-induced substrate strain.

Contact failure

Contact failure can be described in terms of the relationship of resistance to probe pressure applied on surface. Contact resistance between device and probe is a parasitic effect that can be minimized by applying higher contact force. The relationship between contact resistance and contact force (or pressure) is shown in figure 6.22. Contact force is usually in the nN-mN region.

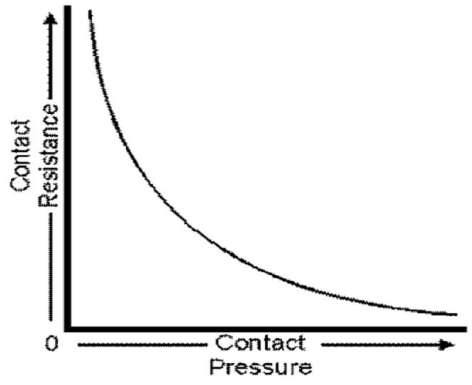


Figure 6.22: Contact resistance and contact pressure relationship between probe and substrate.

Electrical measurements with standard probes and equipment proved to be challenging as LCP flexibility made it difficult for the probes to make contact on the surface. The pressure provided by one probe on one side of the CPW would induce the lifting of the probe at the other CPW end. The solution was to keep the substrate flat and rigid at all times up to the electrical measurement stage. A flat, rigid substrate at the back of the LCP allows even contact between the probes and the device waveguides thus, diminishing the contact pressure problem. Even if the backing comes off during processing, the LCP wafer should always be mounted on a rigid substrate such as silicon or glass.

LCP surface roughness also causes losses related to contact resistance. Surface roughness and asperity behavior are critical factors that affect contact behavior at scales ranging from the nano to the micro in MEMS devices since asperity prevents the unlimited increase of the number of the micro-contacts [228]. On rough substrates less contact is made between the probe tip and the surface (less surface touches the probe) which leads to an intuitive conclusion, from equation 2.49 (section 2.6.4), that R is large. In other words, the contact area on a rough substrate is much smaller than on a smooth substrate (see figure 6.23), leading to higher contact resistance.

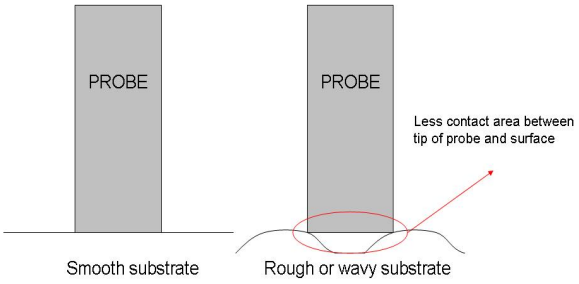


Figure 6.23: Contact area between probe and substrate. On a smooth substrate there is more contact area.

We have explained how the substrate's waviness and roughness contribute to increase contact resistance during measurement. This is because of the inverse proportionality between contact area and contact resistance. Solutions in order to minimize the contact resistance are: to have a rigid backing for the LCP, increase probe pressure onto the LCP and have a very smooth substrate.

Strain-induced track resistance

Metal tracks can experience strain when in contact with the probe even when mounted on a rigid substrate. This is due to the low Young's modulus of the LCP. During measurement when the probes are down on the substrate, this bends, stretches and deforms locally. The deformation is proportional to the contact pressure of the probes on the substrate. The more the probes exhibit pressure on the substrate, the more the substrate deforms, the track length increases, thus, causing strain and increase in track resistance [27].

When dealing with flexible electronics, substrate deformation and track resistance are proportional to the probe contact pressure. This causes concerns

about the validity of our electrical measurements. This strain-induced resistance relation has been shown mathematically with equation 6.12 [27].

$$R = R_0 \frac{1+\epsilon}{(1-v_s)(1-v_f)} \tag{6.12}$$

Where R_0 is the initial (strain-independent) track resistance, ϵ is the strain experienced, v_s is the substrate's Poisson ratio while v_f is the thin metal film Poisson ratio. Implementing equation 6.12 in Matlab (see Appendix A..8), the actual (strain-dependent) track resistance values were simulated, assuming: 1mm long Au CPW track, local strain of ∼0.2% (induced by contact pressure of the probes) and initial track resistance of R_0=50Ohm.

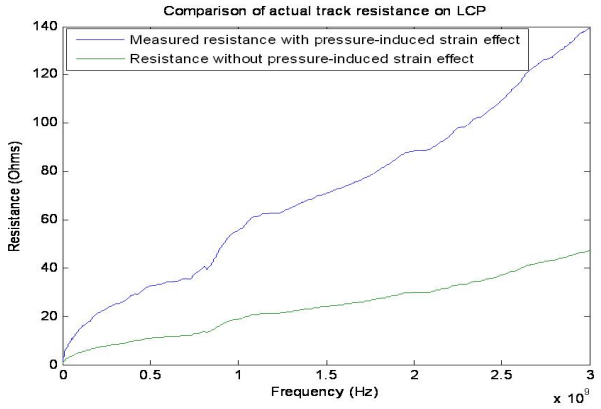


Figure 6.24: Removing the strain-induced resistance. Comparison of as-measured device and strain de-embedding of same device.

The retrieved transmission loss results were de-embedded with strain-induced track resistance values, in order to get the actual S_{21} loss which was lower than the as-measured one. Figure 6.24 shows that for an unstrained substrate and electrode, the track resistance is much lower.

6.6 Observations on LCP-based FBAR microwave performance

FBAR on LCP could be a breakthrough, not only because it would make use of a microwave substrate which is compliant and allows small and cheap future generation device production, but also because it can potentially eliminate the use of a buffer layer such as SiN_x or SiO_2. The elimination of a buffer layer would mean higher frequency range achievement and, potentially, higher Q.

In all of our devices low power transmission and Q were observed. Mass loading effects due to either LCP residues at back or device misalignment were seen

to have slight effects in the power spectrum, Q and resonance frequency of the device. The mass loading provided by a viscous material was very characteristic. Initial substrate roughness caused rough ZnO growth and poor piezoelectric performance (low Q), but it also lead to roughness-induced acoustic attenuation losses, calculated to be higher for ZnO Ra$\sim$200nm than ZnO$\sim$8nm.

Surface roughness of LCP, metal and ZnO had degrading effects on the overall device performance, such as decrease in frequency, Q and transmitted power S_{21} (due to rise in track resistance). Track resistance increase was caused by: substrate warpage, substrate roughness and low substrate Young's modulus leading to pressure-induced local strain.

Electrical property measurements should be taken by keeping the rigid backing behind the wafer as this allows even contact between the probes and the device waveguides, and eliminates the contact pressure problem. However measurement-induced S_{21} loss can arise due to substrate compliance through the act of exerting a force during probe-to-substrate contact whereby the metal track and substrate locally strain leading to track resistance increase. In conclusion, for low track resistance, a good balance between high probe-to-substrate contact area and low probe-induced strain is needed.

Chapter 7

Reliability of LCP-based FBAR

7.1 Introduction

Substrate flexibility has been seen as a characteristic advantage of our LCP-based RF devices. It could, however, also lead to disadvantages in the application front-end. This is because, for a given amount of stress, the low Young's modulus of the substrate causes greater deformation on an LCP substrate than a standard Si one. This larger deformation is what causes problems for our device reliability. As the substrate deforms, so does the functional thin film and, because this is a ceramic it is brittle, which means that it has little tendency to strain when subjected to stress, and fractures easily.

Because ceramic combination with polymers is a novel area, the reliability of this multilayer needs to be investigated. Ceramics are brittle, have poor toughness (fracture before plastic deformation takes place) and poor tensile strength ($\sim$250MPa)(because pores act as stress concentrators). Polymers are ductile viscoelastic materials, show creep behaviour and poor tensile strength (LCP$\sim$216Mpa). Consequences of thin film stress (metal and ceramic) on polymer are explained.

In the reliability study we are interested, first, in analysing the fabrication reliability. In other words what stresses are produced straight after ZnO deposition, which is the process step requiring the highest temperature. Fabrication reliability is followed by mechanical reliability whereby static and cyclic loading are applied in order to see whether the stresses reached are below the critical value of ZnO tensile fracture strength. Device configurations are also studied in order to relief the effect of unwanted stresses from the ZnO. Since the main goal is to avoid reaching the fracture strength of ZnO, the results are compared to this value. Some LCP/LCP packaging issues are tackled followed by the electro-thermal performance of the LCP as a substrate by simulating CPW track signal thermal response.

Preliminary reliability studies for polymer-based devices are carried out in order

to assess the following:

1. Fabrication reliability.
2. Multilayer mechanical reliability.
3. Device reliability: effect of flexible polymer substrate on brittle ceramic stress and novel device design that absorbs stress from the ceramic.
4. Packaging interfacial reliability: thermal stress induced by lamination process at interface and interfacial stress due to mechanical load.
5. Thermo-electric reliability: thermal effect on power loss when applying voltage to CPW track.

It is important to mention that, while the fabrication-induced reliability provides an absolute reliability analysis for the as-deposited ZnO, the other studies are only comparative and used to assess the degree to which different parameters affect the reliability.

7.2 Consequence of thin film stresses: crack and delamination

Thin film stresses can cause material failure such as cracks and delamination at the film/substrate interface. A study of stresses is therefore essential in order to understand and, if possible, prevent cracks in the ceramic films. Thin films made of different materials fail in different ways, such as cracking and delamination. Cracking and delamination are simply way by which materials release the energy caused by strain. In our experiments we deal with both Au metal and ZnO ceramic thin films.

7.2.1 Bottom electrode metal stresses on LCP

Compared to bulk metals, freestanding thin metal films usually have high strengths, but small rupture strains [155]. When the maximum strength and work-of-separation (cohesion) have been reached, delamination take place and will propagate along the metal/polymer boundaries [22] causing the metal to eventually crack.
In our experiments we noticed cracks on the bottom Au electrode of the devices (see figure 7.1) similar to those found by Cairns [27] and Crawford [49], who deposited ITO layers on PET (see figure 2.25 in section 2.6.4). In our Au thin metal films on LCP we noticed Au cracks at relatively high deformation strains, $\sim$6% strain although this figure can be improved to 20% [155] for really thin metals ($\sim$100nm).

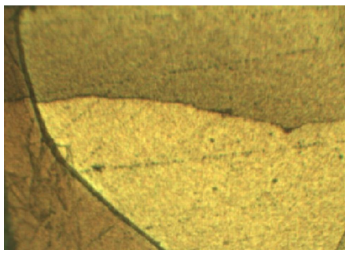


Figure 7.1: Au crack mode for 100nm Au.

7.2.2 ZnO thin film stresses on LCP

The possibility of ZnO cracking can occur at any stage, whether during processing when debonding the front of the wafer from the rigid substrate, or during measurement when trying to flatten the wafer out. ZnO cracking was also observed by many others including Kuoni et al. [131] who deposited ZnO on polyimide, and Chen et al. [35] who deposited ZnO on highly fluorinated polyether (HFP) substrates through RF magnetron sputtering. They all provided images showing the tendency of ZnO to crack when deposited on flexible substrates. This failure was believed to be stress-induced due to the crystalline nature of the film. High stress-induced cracks were also noticed for AlN on epoxy by [94].

ZnO failure is believed to be a result of either mechanically-induced manhandling or by sputter-induced thermal stresses in the film. The latter would be caused by a combination of the soft texture and the large CTE of the polymer substrate. If these residual stresses are compressive, as will be proven in section 7.3.1, they can lead to a delamination forming a web of blisters of very different morphologies [123], [47]. Delamination of ZnO caused by thermally-induced stress is shown in figure 7.2, while figure 7.3 represents cracking caused by mechanically-induced factors such as re-attaching the LCP to a rigid substrate.

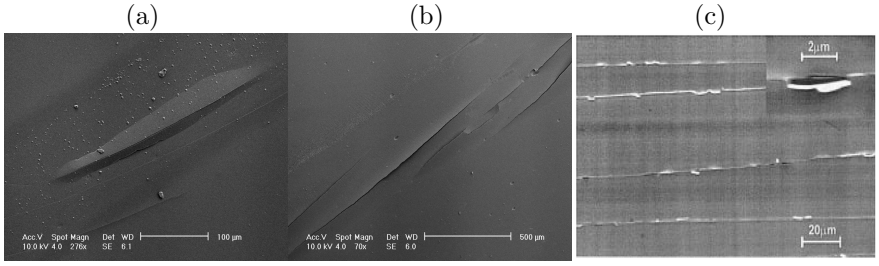


Figure 7.2: a) and b) show thermal-induced compressive stress (ZnO deposited at 200°C on LCP (sample 22) causing delamination of ZnO. d)Taken from [47].

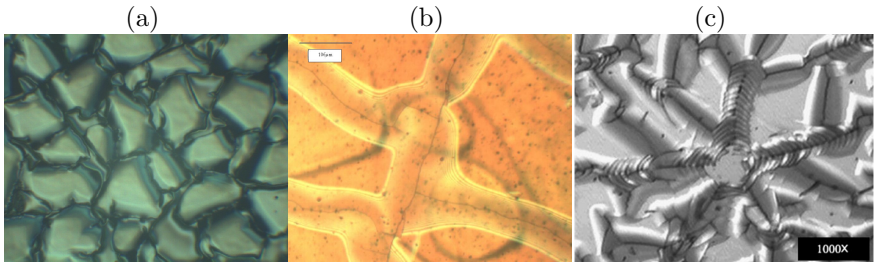


Figure 7.3: a), b) Man-handling mechanically-induced ZnO cracks on polyimide (experiments); c) ZnO crack on polyimide from from [35].

Thus delamination and cracking of ceramic under tension or compression (whether mechanically or thermally-induced) limit the use of our organic-based substrate's flexibility.

7.3 Fabrication and multilayer mechanical reliability

Integrating brittle thin films, such as ceramics, with non-rigid substrates is a challenge. The mechanical and thermal factors during fabrication induce stresses on the samples in different ways. Residual stress is a problem in most MEMS as can have deleterious effects in thin-film processing and in the eventual device response, especially when dealing with piezoelectric materials, which are based on the interaction of stress and voltage. Stresses can cause substrate curvature and in-plane distortions leading to alignment errors in integrated circuit processing and, as seen in section 7.2.2, can also lead to film buckling and delamination [31]. Stresses may lead to premature failure such as ceramic cracking (in the polyimide samples).

The high tensile stresses in the polyimide samples caused some of the fabricated devices to fail after RIE back etch by Au/ZnO curling upwards due to tensile stresses residing in the film (see figure 7.4 a)). The reason why the stress increased to the point of breaking the thin film away at the edges is because, as explained by Kawski and Flood [113], stress is proportional to bow which is inversely proportional to thickness. This means that as the wafer is thinned (in our case through RIE), the bow increases, breaking the device. This effect does not happen for LCP-based FBARs as the stresses are compressive (see fig. 7.4 b)).

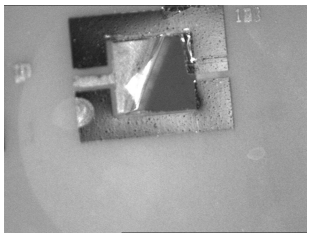
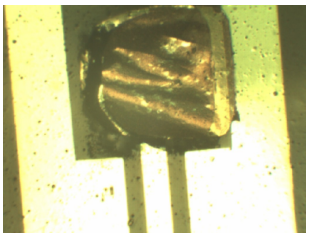
(a)  (b) 

Figure 7.4: a)Microscope image (50x) showing Au/ZnO/Au membrane curling up as a result of tensile stress, b)Au top as a result of stresses caused by front and back processing.

Due to the above reasons, it is important to calculate the thin film stresses as soon as they are deposited to make up a multilayer. A multi-layer refers to a composite layer combination which, in our studies, is made up of polymer/thin metal film/thin ceramic film. Because ZnO is the most brittle material and, therefore most susceptible to cracking, the following multilayer stress studies are those of the ZnO interface with the bottom electrode. ZnO is a ceramic and, therefore, has very little tendency to strain and deform before fracture often breaking in tension.

ZnO typically fails in one of two ways, either as a result of thermo-mechanically induced cracks or as a result of nonuniform temperature within the material [17]. The interaction of thin film with its substrate, is determined by thermal and intrinsic stresses which then cause tension or compression and, thus, substrate curvature. The problem of stress and deformation arises with flexible substrates because their low stiffness causes them to deform more physically, leading to potential thin film cracking.

When dealing with the integration of thin films (metals and ceramics) on polymers, it is important to consider whether these can survive large strains without rupture [266]. Induced stresses should not be higher than threshold values such as yield strength of metal and fracture strength of ZnO (F_s∼2.68GPa, 3.33-9.53GPa Agrawal et al. [6], 0.412GPa [210]) otherwise thin film failure can occur. The reason why we talk about fracture strength for ZnO is because the yield strength of ceramics is low as they undergo brittle fracture.

Thin film stresses are made up of fabrication-induced thermal stresses and intrinsic stresses within the film. In the next sections we simulate the thermally induced stresses and calculate the total stresses of the ZnO on the multilayer and compare the results. This comprehensive stress analysis allows us to understand the mechanical behaviour of the multilayer and gives us an insight into the pre-stressed physical conditions of our future devices.

7.3.1 As-deposited ZnO thermal-induced stresses: simulations

Standard microfabrication steps require temperatures at least up to 100°C. Piezoelectric ceramics undergo some kind of thermal treatment during their growth. Since intrinsic (or quenching) stress in ceramics is usually very small (less than 50 MPa) [132], we concentrated on analysing the stresses caused by fabrication-induced thermal treatments.

Sputtering systems (i.e. for ZnO growth), see a temperature increase. Even when the material sputtering was carried out at room temperature, the chamber temperature was recorded to be ∼80°C. This temperature was reached due the plasma (ionized/charged gas) inside the chamber. Since our goal was to focus on fabrication processes, it was necessary to analyse the extrinsic stresses, more specifically those caused by thermal mismatch. A thermal-induced stress analysis was essential in order to avoid film failure following deposition.

Thermally-induced stress studies were carried out with Matlab® with particular interest in a stress regime which accounted for fabrication temperatures up to 120°C for photolithography and up to 250°C for ZnO deposition. At these initial (or deposition) temperatures T_0, it was assumed that the layers were stress-free. Upon cooling, however, the large TCE of the LCP caused swelling and deformation of the compliant substrate which, in turn, translated into high stresses at the ZnO/substrate interface. As we have previously seen if interfacial stress exceeds the ZnO fracture strength, it can can lead to ZnO cracking. TCE values are found in table A.11 in Appendix A..2).

Through the assessment of thermal-induced strain, the stresses on the ZnO when the samples reached room temperature were calculated. To calculate thermal stresses equation 2.43 was implemented (see Appendix A..8).

Table 7.1: Thermal stresses on ZnO upon cooling after high deposition temperature.

Multilayer	**Stress (MPa) on ZnO for T_0=250°C**	**Stress (MPa) on ZnO for T_0=100°C**	**Stress (MPa) on ZnO for T_0=80°C**
Si/ZnO	-976	-339.5	-254.6
LCP/ZnO	-431.2	-150	-112.5
LCP/polyimide/ZnO	794.2	264.7	207.2
Si/Au/ZnO	-961.4	-334.4	-250.8
LCP/Au/ZnO	-434.4	-151.1	-113.3
LCP/polyimide/Au/ZnO	840	292.2	219.1

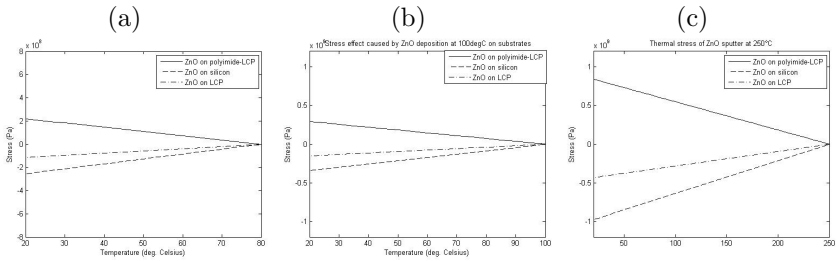


Figure 7.5: Thermal-induced stresses for ZnO initial deposition temperature at a)80°C (temperature induced by the plasma sputtering procedure) b) 120°C c)250°C.

From table 7.1 and figures 7.5 we can see why the use of temperatures $\succ$100°C in the processing are not desired as they introduce high stresses in the ZnO ceramic film. The stresses were evaluated comparatively to ZnO fracture strength 2.68GPa. Traditional ZnO sputtering at 250°C introduced high stresses, however, without reaching the material's fracture stress. By applying less heat at 100°C and 80°C (plasma temperature) during ZnO RF sputter, the thermally-induced stresses were reduced.

The compressive stress on ZnO deposited on Si/SiO_2 and LCP substrates is justified by the fact that the substrates has a smaller TCE than the thin film, therefore more constraint is exerted against the expansion of the thin film. Because of this, the thin film experiences compressive stresses at the interface and it expands more along the z direction to relieve these stresses [321]. The tensile nature of the stresses caused by the polyimide substrate, on the other hand, were caused by the higher TCE of the polyimide compared to that of the ZnO. The high tensile stress of ZnO on polyimide explains the ceramic's occasional brittle cracking after deposition and cooldown (see figure 7.3 shown later in section 7.2).

Stress becomes more of a problem for compliant substrates such as LCP and polyimide as opposed to standard rigid substrates with high Young's modulus. This is because their flexibility causes them to undergo large strains and deformation in order to relief the stress. However we noticed that, due to the higher TCE mismatch among layers, ZnO thermal stresses on Si/SiO_2 were much greater in magnitude than on LCP. This adds to the argument that LCP can make a very good candidate as an organic substrate for ZnO ceramic integration.

The presence of Au reduced ZnO stress for the silicon substrate case as the TCE mismatch between ZnO and Au (16ppm/°C) is lower than ZnO and Si (29.45ppm/°C), leading to smaller deformations and hence less film stress. Au presence increased stresses (although very slightly) in the LCP substrate case, because the TCE mismatch between ZnO and Au (16ppm/°C) is slightly higher than that of ZnO and LCP (13ppm/°C). ZnO on polyimide yielded tensile stresses which were higher in magnitude (almost twice) and opposite in mode than those of ZnO on LCP. Thermal analysis showed that ZnO on LCP yielded the lowest thermal-induced film stresses.

7.3.2 As-deposited ZnO total stresses: experimental and numerical validation

In the above section we numerically calculated the thermal stresses caused by the ZnO deposition temperature. However, thermal stresses are only part of the total stress a thin film experiences. In this section we calculate the total stress of the multilayer after measuring the wafer's radius of curvature.

LCP/ZnO multilayer

As-deposited stresses on ZnO interface were calculated after measuring the curvature with a Dektak surface profiler. Initial substrate curvature was 0.173m^{-1} while the final curvature 0.045m^{-1}. To attain the stress values of ZnO from the curvature measurements, the numerical models from section 2.6.3 were encoded into Matlab® and the results were then compared to one another. The scope of this analytical comparison was to find the most suitable equation for describing thin film stresses on compliant substrates as this is a very new field. Note that wherever intrinsic stress was considered (Y.C.Tsui and S.Wagner methods), a value of 2.5GPa was given [295]. Results for these numerical studies are given in table 7.2.

Table 7.2: ZnO interface stresses on LCP (ignore Au layer effect).

Numerical method	**Stress on ZnO (MPa)**
Stoney	- 529.7 (compressive)
K.S. Chen	-26.2 (compressive)
S. Wagner	-55.8 (compressive)
Y. G. Tsui	-27.8 (compressive)
J.I. Han	-21.5 (compressive)

The results obtained by the experimental curvature method were an order of magnitude smaller than the thermal results found in section 7.3.1. The reason could lie behind the fact that, in the thermal analysis, the intrinsic stresses ($\sim$2.5GPa) were ignored along with lateral geometric considerations.

From the description of Stoney's equation given in section 2.6.3 and the results in table 7.2, we can conclude the validity of Stoney's formula does not hold for ZnO on LCP. This is both because the film rigidity is higher than the substrate's and also because substrate undergoes very large deflections. Stoney's equation works only if rigidity of film is much less than rigidity of substrate which, for our case, is not true as 1μm ZnO film has rigidity $1.9826\text{e}^3\text{GPaKg}m^2$ while 100μm LCP has rigidity $1.0165\text{e}^3\text{GPaKg}/m^2$. Furthermore, the stress results derived by SToney's formula deviated largely from those given by the other models. For the calculation of ITO stresses on PET, however, Wong et al. [300] did employ Stoney's formula.

From previous literature, the stress of ZnO on stiff substrate was found to be in the -1000 to -200MPa region [45]. The stress results we attained for ZnO on LCP were at least four orders of magnitude smaller. This is because the stresses within a thin film deposited on a compliant substrate are reduced (usually by a factor of about 2) compared to those of a stiff substrate [235].

We can conclude that the stresses of ZnO after deposition on LCP were far from the ZnO fracture strength threshold limit of ∼2.68GPa (or 0.412-9.53GPa [210], Agrawal et al. [6]). This meant that after deposition and cool-down, the ZnO did not fracture as also noticed by the ZnO on LCP (or Au/LCP) not flaking off or cracking after deposition.

LCP/polyimide/ZnO multilayer

As we have seen, ZnO did not crack after deposition on LCP due to the stress being lower than its threshold fracture strength. However, when deposited at 100°C on LCP/polyimide, ZnO did flake off in some areas straight after sputtering. Stress effects for this multilayer case are examined in more detail by comparing the measured stress (thermal and intrinsic) with the simulated ones (thermal).

Table 7.3: Validation LCP/polyimide/ZnO multilayer stress (given R=126) with J.I.Han method.

	Simulations using thermal equation	**Calculations using J.I.Han numerical method**
ZnO thin film stresses on LCP/polyimide (MPa)	794.2	295.3

The offset between experimental and theoretical values can be explained by the simulations only accounting for thermally-induced stresses (ignoring intrinsic ones). The second reason for experimental offset from simulations is due to the measurement methods not being adequate enough as the x-ray diffraction demands macroscopic isotropy from the specimen [198] (see section 5.7.5 for explanation), while our LCP/polyimide/ZnO sample curled up when deformed (see figure 5.42in section 5.7.5).

According to the results in table 7.3, the ZnO stress (whether 794.2 from simulations or 295.3 from experiments) was below the ZnO fracture strength of 2.68GPa found from tensile testing. ZnO flaking from LCP/polyimide can, therefore, be explained by poor adhesion between the materials caused by the polyimide's low surface energy.

7.3.3 Multilayer parametric studies on ZnO stress

We have seen that stresses on as-deposited ZnO do not exceed the threshold value of 2.68GPa. Now it is important to find the effect of independent variables (i.e. substrate bow) on the ZnO state. In order to do this ANSYS Workbench was employed for parameteric studies, whereby different parameters were purposely changed to see their effect on ZnO stress. This parametric investigation is important as it allows the future MEMS developer to match appropriate parameter values to their needs.

LCP substrate bow effect on ZnO stresses

A parametric study of ZnO stress as a function of substrate bowing is important for both fabrication and application purposes. Fabrication involves handling of the substrate which, occasionally, bends. Application motives are also critical, since part of the reason for polymer-based MEMS fabrication is for applications that require the substrates to bend, fold and be shaped so that they can physically fit into different locations. In fact, a main reason for which polymers are considered to be candidate substrates is because of their flexibility. Their ability to, therefore, eventually mould around their surroundings without the metal and the ceramic failing is essential. The studies were carried out on a 10μm thick LCP with a 1μm ZnO film.

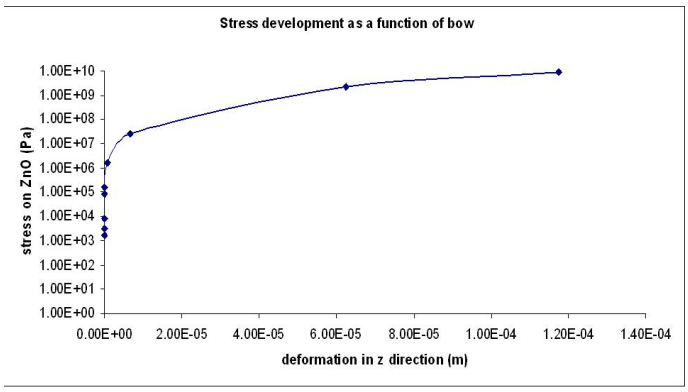


Figure 7.6: Stress on ZnO film as a function of substrate deformation.

As substrate bowing increased, stress increased in a logarithmic manner (figure 7.6). This means that the initial bowing magnitudes had more effect on ZnO stress than the final ones. We can see that up to a substrate deflection of 60μm the stress experienced on the ZnO was still below the fracture threshold of ~2.68GPa. Past this value, the ZnO can be at risk of failing.

Notice that the thicker the substrate, the less bowing it can undergo if it is to safeguard the ZnO from reaching the fracture strength parameter. This is because, as the thin film position moves further from the neutral axis, the stresses it will experience, given the same deflection (or bow), will be higher. The concept can be better understood with equation 7.1 [279], where N is the neutral axis position and it depends on thickness (t), Young's Modulus (E), Poisson's ratio (v) coordinate distance normal to linear composite dimension (γ).

$$N = \frac{t}{2} - (\sum_{i} \frac{E_i \gamma_i (t_i/2)}{\sum_i E_i t_i}) \tag{7.1}$$

Maximum substrate bending before ZnO breaks

The literature suggests that a standard Si substrate has a bow of ∼1mm [98], [306]. But, as the LCP is a material with lower Young's modulus (therefore, lower stiffness), the bow is expected to be different. I analysed the maximum bending LCP could withstand before ZnO failure. The parameter considered for bending analysis was the bow, defined by equation 2.38.

Simulations were carried out in Matlab using Tsui and Clyne [280] method shown in equation 2.39 integrated with equation 2.38. However all the temperature-related variables were taken out for this analysis. Thermal effects are not relevant due to the nature of our scope which is purely mechanical: to discover the amount of physical bending the substrate can undergo before ZnO failure.

It was found that before the ZnO interfacial stress reached critical yield stress of 2.68GPa the maximum bow of the multilayer before ZnO fracture was 7.62mm. This maximum substrate bending value before ZnO failure is close to the bow value of 5.9mm found experimentally after ZnO deposition at 100°C.

LCP substrate thickness effect on ZnO stresses

Because microsystems production might require substrates of various thicknesses (normally between 25μm and 500μm) depending on their application, an assessment of the substrate thickness variation effect on ZnO interfacial stresses is desired. Simulations were carried out with ANSYS Workbench given a constant downwards pressure of 500Pa.

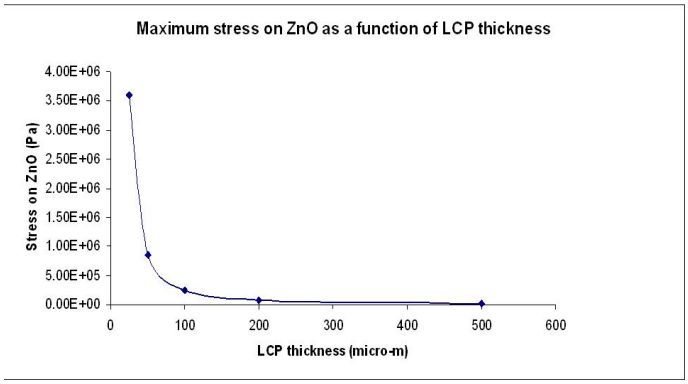


Figure 7.7: ZnO stress variation as a function of LCP thickness given specific load.

As the thickness increased for a given load, the stress experienced by ZnO decreased. This is because the substrate became more rigid and, therefore, bent less making the ZnO experience less stress. Graph 7.7 shows a logarithmic decrease of ZnO stress with respect to LCP thickness.

Presence of Au effect on ZnO stresses

Since on the substrate some of the ZnO was deposited on Au and the rest directly on LCP, ANSYS simulations were conducted for a comparative study of the stress on ZnO, given a load of 5N, with and without Au at the interface.

Table 7.4: Results on ZnO(1μm) stresses given an applied downward force of 5N on LCP(10μm) with and without intermediate Au(100nm)layer.

Multilayer	**Max strain on ZnO**	**Max stress on ZnO (Pa)**
ZnO on LCP	1.18e-02	1.9e12
ZnO on Au/LCP	3.66e-08	5.86e6

From table 7.4 we can see that given the same force (5N) applied in the z direction, the maximum deformation and, therefore, strain experienced by the ZnO film was greater in the case without 100nm Au. The presence of Au, however, slightly decreased the strain undergone at the ZnO interface due to the additional Au stiffness and overall rigidity. This lead to higher stress experienced by the ceramic thin film in the case of ZnO on LCP than with ZnO deposition

of Au/LCP.

Another reason for the ZnO on Au/LCP bending less is that, with the presence of Au, the plane at which the load is applied is further relative to the neutral axis position (N) (see table 7.5) by about $\sim$15μm. It is well known that, for a given curvature, the stress experienced by a layer is grater the further away it is from the neutral axis. The reverse argument can be given: in order to deflect a composite which has a further stress plane from N, more pressure (or load) must be applied. The neutral axis and the distance of this from the layers can be calculated through equation 7.1 [279].

Table 7.5: Results of neutral axis position of LCP/Au/ZnO and LCP/ZnO.

Multilayer	**ZnO plane position relative to neutral axis position (m)**
LCP/Au/ZnO	1.98e-5
LCP/ZnO	1.96e-5

7.3.4 Observations on fabrication and multilayer mechanical reliability

After carrying a comparative simulation of the as-deposited thin film stresses, it was found that when Au/ZnO were deposited on LCP, the combination yielded the lowest stresses compared to the other two substrate options: Si and LCP/polyimide. This is because LCP/Au/ZnO provided the smallest TCE mismatch compared to the other multilayer structures (Si/Au/ZnO and LCP/polyimide/Au/ZnO). Thermal stress analysis showed that stresses of ZnO on LCP and Si were compressive, while those on polyimide were tensile. Furthermore the presence of Au did not seem to provide a major effect on the stresses.

As part of the as-deposited ZnO stress studies, after employing the substrate curvature technique, some numerical approaches were compared to each other. First of all Stoney's formula inadequacy for thin film stress measurements on flexible substrates was proven. Other methods (employed by Chen and Ou [36], S. Wagner [235], Tsui and Clyne [280] and Han [86]), however, validated each other yielding ZnO stress values in the same order of magnitude 20-56MPa (compressive). Furthermore we used J.I.Han method [86] to prove that the stresses of as-deposited ZnO on LCP (-21.5MPa) were smaller than those of ZnO on LCP/polyimide (295.3MPa) and opposite in sign.

In all cases the discrepancies between the thermal model and the experimental validation (with appropriate numerics), were due to the fact that thermal stresses are only part of the total stresses found in the experiments as they make up total stresses only in conjunction with intrinsic stresses.

The LCP/Au/ZnO bowing yielded after processing was calculated to be 5.9mm, which was close to the maximum allowed substrate bending of 7.62mm before ZnO reaches its fracture strength (2.68GPa). ZnO stress was shown to increase logarithmically as a function of bow.

The substrate thickness and the presence of an intermediate gold layer also showed to have some effect on the stress experienced by ZnO. A thicker substrate or one with the presence of a metal layer, added rigidity to the composite, therefore meaning that the substrate required more force to bend. This was explained both by a higher substrate rigidity and by the neutral axis position being further from the given stress layer.

In conclusion we can say that for LCP/ZnO the as-deposited ZnO stresses were below the ceramic thin film's threshold fracture strength value of 2.68GPa. Furthermore, the reliability of a multilayer made up of ZnO ceramic, Au metal and an LCP substrate it was proven. Hence, the multilayer combination can be used for device production with only minor reliability concerns.

7.4 Device reliability

Mechanical reliability is essential for the study of MEMS as the physical behaviour of these devices must be consistent. Mechanical reliability of both multilayer and eventual device is affected by stress and strain parameters. For the device reliability analysis the scope is to quantify the stress limit (maximum stress that can be applied) of the device by verifying that the yield or fracture strengths of the individual materials (LCP, Au and ZnO) are larger than the stress applied in real-world applications. For these studies, the device refers to the resonating structure part.

First static loads are considered where the ceramic/polymer combination reliability is analysed. Here, for given loads, the stress parameters of ZnO are compared to its fracture strength ∼2.68GPa. Then cyclic loading effect on ceramics within polymeric devices is investigated. Cyclic (or fluctuating) loads are comparatively small relative to the mean load (high stress ratio) and tend to be neglected. Finally, novel device designs will be proposed in order to relieve the stress from the ZnO ceramic by concentrating it on specific areas (or links) that act as stress absorbers of the overall device.

The simulations are carried out assuming no initial stress in the system. This stress free initial state is assumed for two reasons:

1. Ease of modeling.
2. Because we are interested in knowing the effect of the substrate only on the device performance and compare the silicon with the polymer.

Although the polymer mechanical parameters (i.e. Young's modulus) used in the simulations are those of LCP, it is important to remember that they are similar for most polymers.

7.4.1 Static loading device reliability comparison

A stress analysis of the ZnO ceramic on the LCP-based device substrate is needed in order to know whether the ZnO fracture strength is reached. The analysis was comparative as it involved simulation of force effects on the LCP-based devices and their comparison with their counterpart Si-based MEMS. Hence the force applied was arbitrary, given for comparative reasons. Cantilever and FBAR membrane structures were considered. Static loading was applied in various directions to assess the effects of device under tension, compression and flexion. This compared the effect of external forces applied on the resonating structure.

Given the use and application of the devices, which might require the substrate to be folded, chances for the substrate to flex are greater than for it to compress or be pulled. However all three effects were considered and a total force of 10N was applied in the following directions:

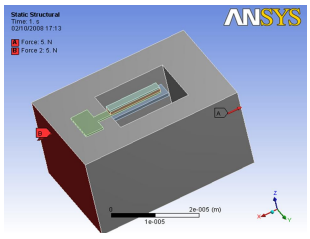
1. Tensile load on two sides - tension effect.
2. Compressive load on two sides - compression effect.
3. Momentum about the y-axis (downwards force) - flexural bending effect.

It is important to keep in mind that the 10N value was not indicative of the actual static loading forces a device undergoes, but simply employed for comparative reasons. Another fact to consider is that viscoelastic effects were not accounted for as they are generally not known to affect stress result outputs for static loading cases (they are, however, employed later in the cyclic loading case).

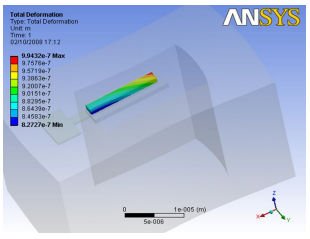
Cantilever

Pulling substrate with force

(a)



(b)



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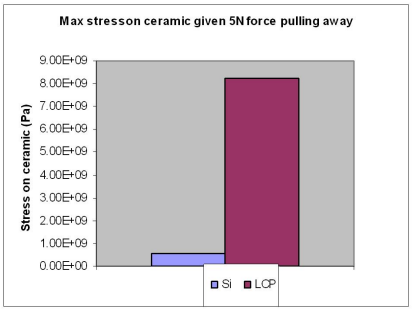
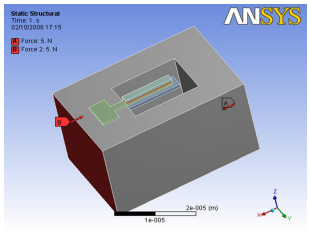


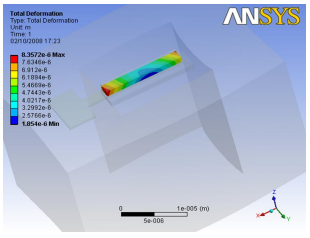
Figure 7.8: a)Boundary conditions, b)stress on ZnO, c)ZnO stress results of Si VS LCP.

Pushing substrate with force

(a)



(b)



(c)

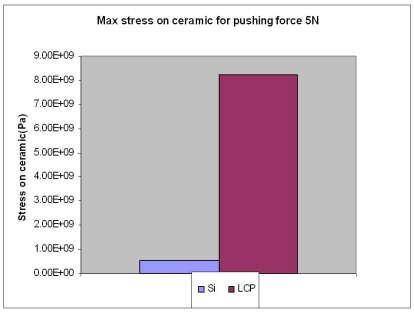
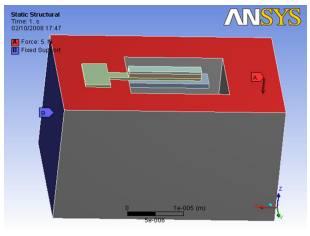


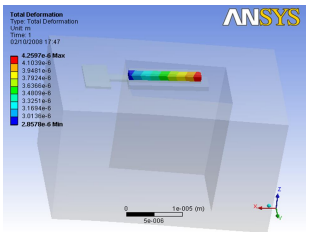
Figure 7.9: a)Boundary conditions, b)stress on ZnO, c)ZnO stress results of Si VS LCP.

Downwards force on substrate

(a)



(b)



(c)

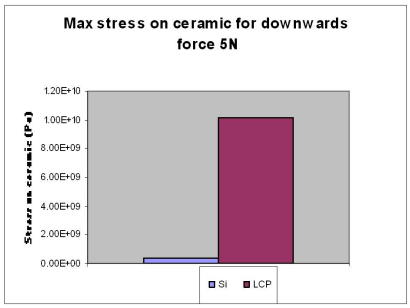
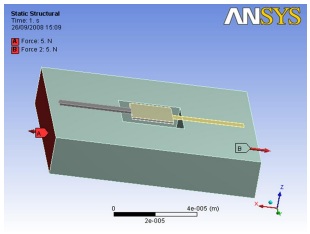


Figure 7.10: a)Boundary conditions, b)stress on ZnO, c)ZnO stress results of Si VS LCP.

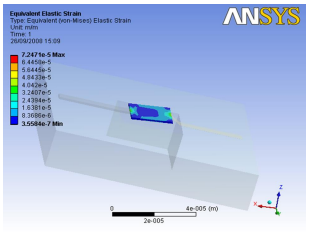
FBAR

Pulling substrate with force

(a)



(b)



(c)

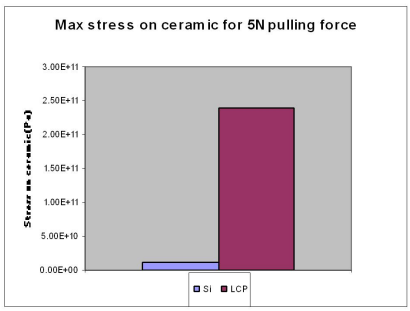


Figure 7.11: a)Boundary conditions, b)stress on ZnO, c)ZnO stress results of Si VS LCP.

Pushing substrate with force

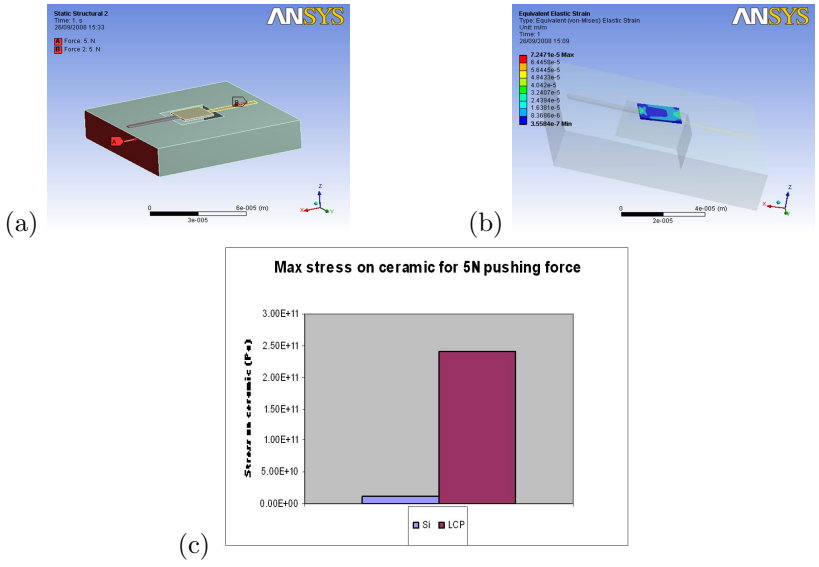


Figure 7.12: a)Boundary conditions, b)stress on ZnO, c)ZnO stress results of Si VS LCP.

Downwards force on substrate

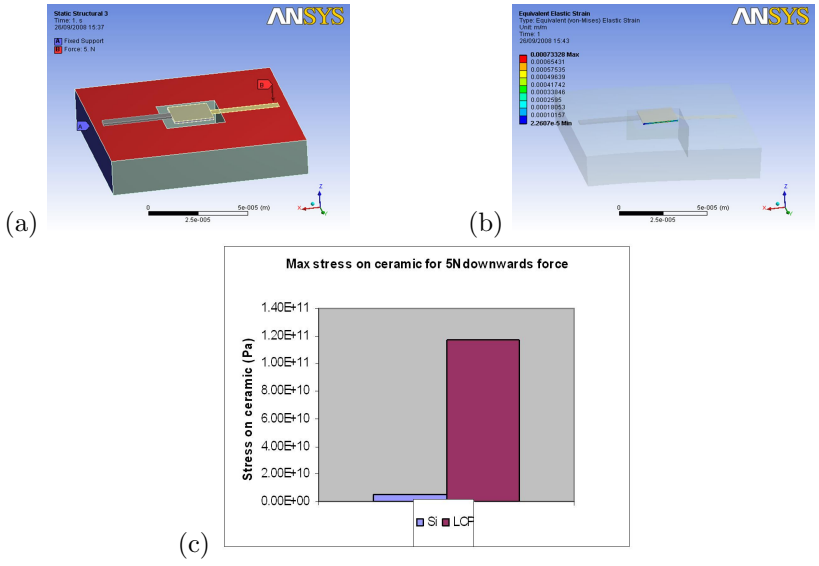


Figure 7.13: a)Boundary conditions, b)stress on ZnO, c)ZnO stress results of Si VS LCP.

Observations on static loading device reliability comparison

From the simulation results, for all three loading cases (compressive, tensile and bending), shown in figures 7.8, 7.9, 7.10 and 7.11,7.12, 7.13 it is evident

that, given the same applied load of 5N, ZnO experienced more stress for the LCP-substrate case compared to the Si one. This was for both the cantilever and the FBAR structures. If the excessive stress is greater than ZnO fracture strength of 2.68GPa, it can lead material failure. As we will see later device design configurations can be used to overcome this limitation.

7.4.2 Cyclic loading device reliability comparison

Cyclic (or dynamic) loading is a phenomenon occurring at high frequencies. Resonance is considered to induce cyclic loading effects, accumulating large numbers of cycles in short periods of time [196]. Fatigue studies induced by cyclic loading in MEMS are of particular interest in RF devices which operate at microwave frequencies (kHz to GHz).

The high frequencies of operation can cause behavior evolution over just a few cycles due to strain hardening or softening which, in turn, causes device performance to change well before failure is reached [286]. Cyclic loading effect analysis on ZnO stress are invaluable for the study of ceramic/polymer multilayer device behaviour assessment.

The cyclic loading evaluation is important especially for the cases where the ductile, viscoelastic polymer is combined with the active component of the structure since ductile materials are susceptible to fatigue under cyclic loading. Both mechanical and thermal dissipation of energy can happen in viscoelastic materials jeopardizing the frequency of the polymer-based vibrating structure, its functionality over number of cycles and the ceramic stress.

Due to the viscoelastic nature of polymers, some strain (a type of potential) energy is dissipated under cyclic loading [299] in the form of heat. This is because of the viscoelastic phase lag (hysteresis) under cyclic loading and unloading, which leads to dissipation of mechanical energy [167] and, hence, decrease in frequency. The cantilever structure is used in order to show what effect viscoelasticity has when the polymer is employed as a functional part of the device.

In this section we studied the effect of cyclic loading on the ZnO stress at the device's exact frequency of operation. To this end we simulated the structures of interest (cantilever and FBAR) using harmonic analysis with force for cyclic loading. Forces were applied instead of voltages due to ease of modeling. Voltages were converted into the approximate force on electrodes through force sensitivity values 100-540V/N [57]. These force sensitivity values yielded loads between 0.0002N-0.1N. Both thermal and mechanical loss effects of the LCP on ZnO stress were accounted for.

Cantilever

Cantilever makes use of the viscoelastic polymer (LCP) as the structural part. Forces were applied at the tip of the cantilever in the z-direction and the harmonic frequency was set at the device's operational frequency. Hence for LCP cantilever f=3.16MHz, for Si cantilever f=3.42MHz.

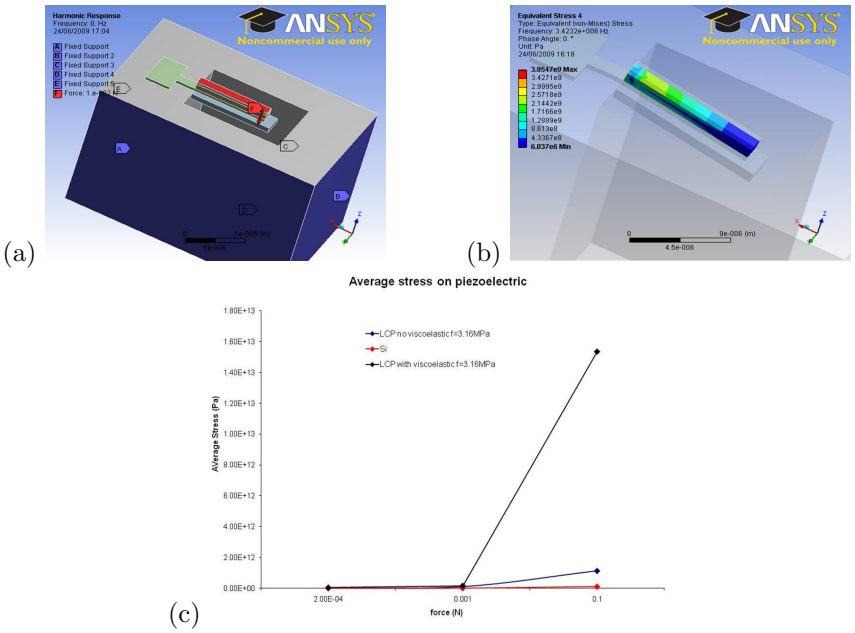
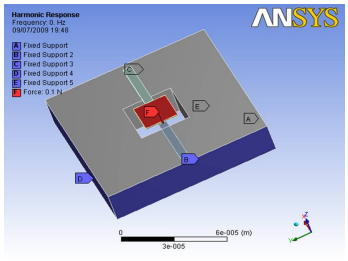


Figure 7.14: a)Boundary conditions for simulation, b) stresses on ceramic, c) average ZnO stress results of Si VS LCP.

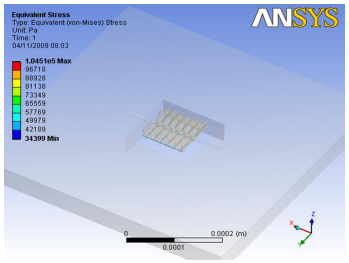
FBAR

Unlike the cantilever, the FBAR structure does not have LCP as the active device part, so in theory the cyclic loading stress of FBAR on LCP and Si should be similar. Forces were applied in the centre of the FBAR in the z-direction at the FBAR's main operational frequency of 1.5GHz (for both LCP and Si), hence cyclic loading stress simulations were carried out with harmonic analysis about this frequency.

(a)



(b)



(c)

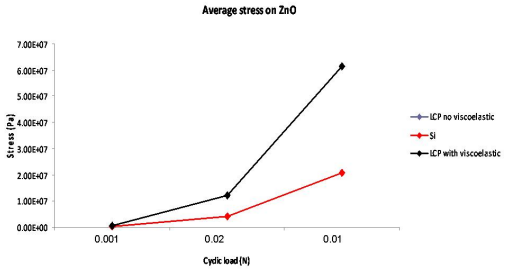


Figure 7.15: a)Boundary conditions for simulation, b) stresses on ceramic, c) average ZnO stress results of Si VS LCP.

Observations on cyclic loading device reliability comparison

From figures 7.14 and 7.15 we derive that the stress experienced by ZnO was larger for the cantilever case than for the FBAR for all given applied forces. This is because LCP makes up part of the active vibrating structure and, therefore, its effect is greater.

For the cantilever case (see figure 7.14 c)) we can notice that, when the viscoelasticity effect was taken into account, the stress experienced by the ZnO was larger than when the loss modulus was not considered. This is because loss modulus causes thermal dissipation. Furthermore, for both cases (with and without viscoelasticity effect) the ZnO experienced more stress for the LCP than for the Si-based cantilever. This is because of the LCP having lower stiffness than silicon.

For the FBAR device (see figure 7.15 c)) the viscoelasticity of the LCP did not

have any apparent effect on the stress experienced by the ZnO. This is because the LCP is not part of the functioning multilayer resonator. However there was a slightly higher ZnO stress outcome with LCP used as substrate instead of Si. This can be explained by the fact that the edges, to which the active FBAR component is clamped, had a slight indirect effect on the device's mechanical characteristics.

Considering cyclic loading with the given actuation loads and frequencies (which were realistic for the device actuation regime) the stresses experienced by ZnO were below its threshold fracture strength value of 2.68GPa for both LCP-based cantilever and FBAR. However, when considering the viscoelastic effect, the ZnO stress value exceeded its fracture stress for a force of 0.1N (voltage of 5.4kV).

The cyclic loading results of LCP-based devices were overall reassuring as the stress results did not deviate largely from those of standard devices. In conclusion, the use of LCP-based devices is reliable and promising.

7.4.3 Novel structural configuration for device stress relief

We saw in section 7.4.1, for the static device analysis, that LCP-based structures cause the ceramic to undergo more stress for a given amount of load than Si-based structures. Given the same load, stresses on ZnO were higher for the LCP-based devices than for the silicon-based ones as they underwent more deformation due to the LCP compliance (low stiffness). One solution to reduce the mechanically-induced stresses on ZnO for the LCP-based devices, is to change the device geometry.

Stress-relieving methods from the ceramic, aimed at reducing the initial stress on the ceramic at the production level, are discussed. Since we are concerned with application-induced stresses, we tackle the stress-relieving issue through the use of a suitable device configuration. This is a new approach which has not yet been found in the literature.

As we are dealing with ceramic (brittle material) integration with polymer (flexible material), a novel approach of geometric modification aimed at stress relief within the active piezoelectric component could be beneficial. Stress on the piezoelectric ZnO ceramic causes reliability concerns both at the production and application levels. The substrate is eventually man-handled, curved and bent, which can cause large stresses on the ZnO leading to the possibility of material failure (i.e. fracture). We are particularly interested in the single FBAR configuration improvement for a low stress ceramic, but the proposed designs can be applied to various devices.

Strain is a means of stress relief through deformation. The larger the strain the more stress is relieved. Because LCP is a low E material, when applying a load, it deforms greatly leading to ZnO strain, hence, stress relief and fracture. The principle was to use structures' links to absorb the stress so that the ZnO would not suffer excessive strain and, therefore, stress. LCP's compliance was

employed to our advantage, as a stress-damping element, through the creation of links to drive away the stress from the ZnO. In order to achieve large strain on the structure, this was made more compliant through area reduction, hence why the creation of thin links. The simple stress-strain relationship shows how this works: σ=F/A=Eϵ, where F and E are assumed constants, and σ (stress) and ϵ (strain) change as a function of A.

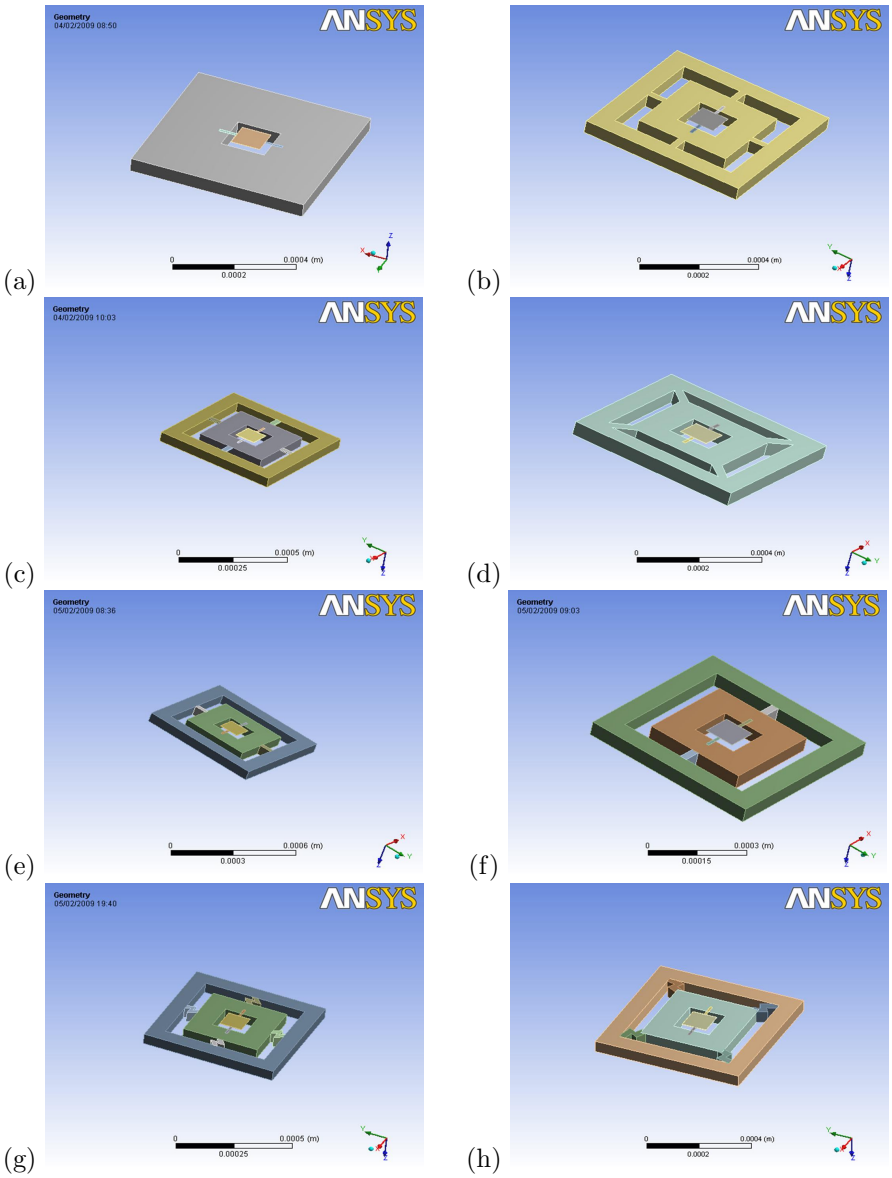


Figure 7.16: Device configurations: a)standard, b)modified 1, c)modified 2, d)modified 3, e)modified 4, f)modified 5, g) modified 6, h) modified 7.

Moment and compression were applied in order to study the stresses respectively

with flexural and compressive conditions. These simulated real-life situations in which the component is employed. For example, the substrate can be bent to be fitted in an electronic device, or it might experience compression due to packaging etc.

Apply moment

Moment about x axis was applied with 500Pa Pressure. Figure 7.17 shows the stress values on the ZnO, while figure 7.18 highlights the structures with highest stress.

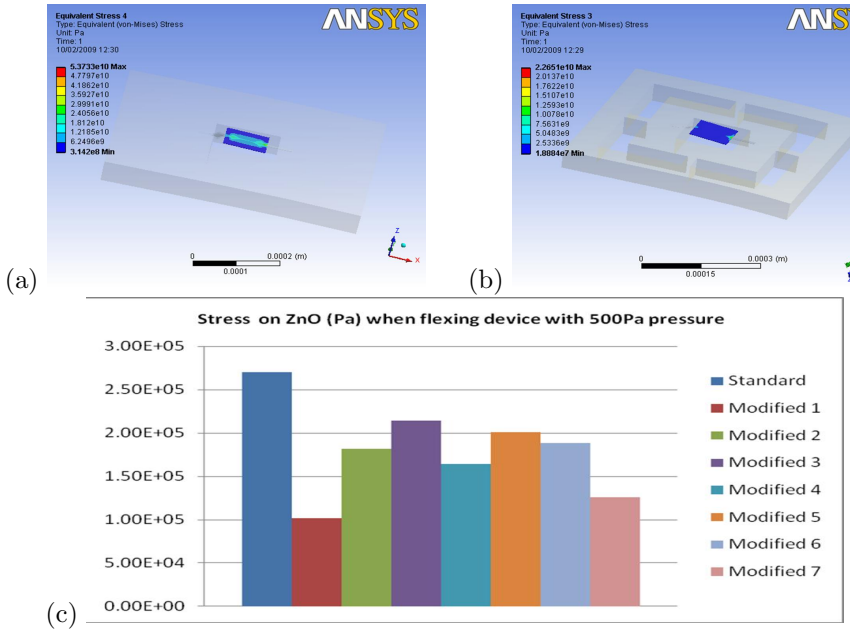


Figure 7.17: Stress on ZnO when applying moment: a) standard device, b) modified 1, c) ZnO stress analysis and configuration comparison for applied flexural pressure of 500Pa.

Figures 7.17 a) and b) show the stress on ZnO with flexed substrate and a pressure of 500Pa for the standard and the Modified 1 devices respectively. Graph 7.17 c) represents all the results from which it is evident that Modified 1 yielded the lowest ZnO stress. The stresses on the ZnO were greater for the standard substrate than any of the others. This is explained by the links of the structure in the other configurations 'absorbing' the stresses.

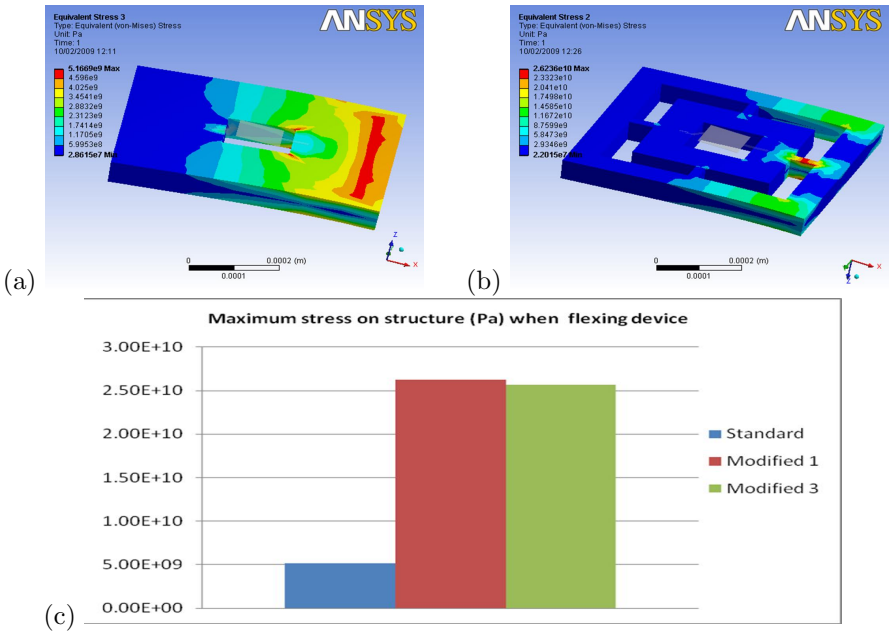


Figure 7.18: Stress on structure when applying moment: a)for standard device b) for Modified 1 c) structure stress analysis and configuration comparison for applied flexural pressure of 500Pa.

Figures 7.18 a) and b) show the stress absorbed by the structure, respectively, for the standard and the modified 1 structures. Graph 7.18 c) represents the stress results on the structure where we can notice that for Modified 1 and Modified 3 this value was higher. The structure for Modified 1 and 3 deviated the stresses away from the central ZnO ceramic. The other modified structures were not represented as the stress for these was in the same order of magnitude as that of the standard case.

Apply compression

Compression was applied with 500Pa pressure in the x axis direction.

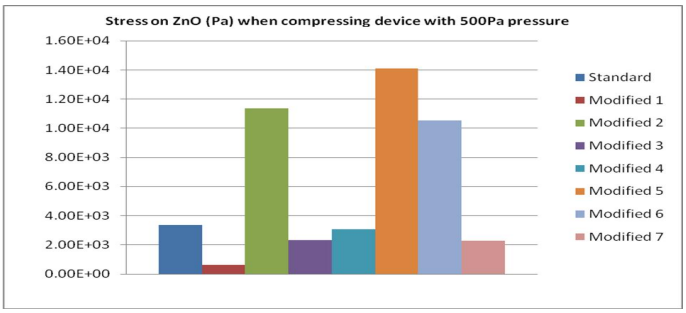


Figure 7.19: ZnO stress analysis and configuration comparison for applied compression of 500Pa.

From figure 7.19 we can derive that under compression the lowest stress experienced by ZnO was for Modified 1. Modified 2, Modified 5 and Modified 6 showed a higher stress on ZnO given the same amount of pressure under compression possibly because of the configuration's connection links being too compliant. For Modified 2 the links were very thin making the connection strain too much, hence, causing large displacement and stress of the device area. Modified 5 had the same configuration as Modified 1 on the load side, however it lacked connections perpendicular to the load direction (side connections), again making the structure too compliant. In Modified 6 the connection on the load side was zig-zagged which, in theory, should have a positive effect as it translates into compliance, however, because the side connections were also zig-zagged, this caused greater device displacement and stress than desired.

From these results we notice that substrate compliance is sought for through the creation of thin links. However there is a limit for this as the consequence can be high device displacement, leading high stress experienced on the device and ZnO. For applications that require compressive stresses, the connections must have the right amount of compliance.

Observations on novel structural configuration for device stress relief

The geometrical design studies allowed an evaluation of the stresses caused by substrate deformations on the ZnO ceramic for fabrication and application purposes. It can be concluded that a compliant design made the stresses concentrate elsewhere on the structure (i.e. the connections) as opposed to the mechanically sensitive ZnO. A structure with too high a compliance (with thin or zig-zagged links), though, caused the device area to undergo large deformations and stresses, compromising the mechanical integrity of the ZnO.

Both flexural and compression studies showed that Modified 1 design, with four straight links on the sides, yielded the lowest stress effects on ZnO. Possible disadvantages of the new configuration and general considerations include signal transmission. The main thing to worry about in these configurations is getting the signals in and out across the very compliant suspensions as the wave propagation mode and RF/electronic implications for the new layout have not been

studied here but this is suggested as part of the future work.

7.4.4 Observations on device reliability

Brittle ZnO ceramic integration with flexible, viscoelastic LCP caused some concerns both at the production (fabrication) and application (eventual flexed component, device performance etc.) levels. The necessity of studies aimed at device reliability were carried out to analyse the impact of substrate deformation (static analysis) and high frequency device performance (cyclic analysis, resonant actuation) on the ZnO layer.

Static loading studies simulated the stresses experienced by the device during substrate handling for post-processing application purposes. For static loading analysis ZnO experienced more stress, given the same load, when on LCP than on Si. The stresses experienced by ZnO were, however, found to be below ZnO threshold limit (fracture strength 2.68GPa) for both compression and flexion of devices subjected to 500Pa pressure (12.5N given area=500x500μm^2 in simulation). To relieve these stressed from the ceramic, optimal device configurations was also investigated.

Cyclic loading simulations were used to model the device under operation. Here we saw that, given the same load, LCP-based devices caused the piezoelectric ceramic to experience more stress than the silicon-based ones. However the stresses were still below the ZnO fracture strength, which is reassuring in terms of device operational reliability. The higher operational stresses on the ZnO in the LCP-based devices can be used to an advantage as it would mean that a lower operational voltage would be required to actuate the components.

Structural modification and configuration analysis were carried out after the static loading analysis findings where ZnO on LCP experienced more stress than on standard silicon. The idea of this novel geometrical device configuration used the LCP's compliance to its advantage, whereby suspended structure links were created to easily strain and, hence, to absorb the stresses, deviating them from the ZnO. Modified 1 configuration showed excellent outcomes in terms of low ZnO stress achievement for both flexural and compressive loading cases. The study's success and originality could lead to future devices using this geometry modification principle for stress-reducing effects on the active ceramic component of the MEMS.

7.5 Packaging reliability

One of the reasons for using LCP as a substrate is the ease by which it can be packaged, hence packaging reliability should be examined. LCP's excellent thermal performance (including high melting temperature) facilitates cooling for a package and improves package performance at higher temperatures.

Packaging has desirable effects such as protecting features, creating vacuum (therefore increasing the resonance frequency of the device), and minimizing viscous or squeeze film damping effects. Packaging is a crucial step as both dust particles and the atmosphere in which the device operates can impact on the characteristics and functionality of a MEMS component [232].

In microelectromechanical systems (MEMS), the packaging determines the reliability, long-term stability and the total cost of the system. Since MEMS structures are movable and fragile, they can be easily damaged during manufacturing processes such as dicing and wire-bonding [42]. Traditional packages can be all-ceramic, ceramic with a glass lid, all-silicon or many more.

Packaging stresses impact the performance of the transducer [236], however, the use of LCP substrate in packaging would have the advantage of bonding through lamination, therefore avoiding the use of any bonding layers which cause excessive interfacial stresses and lead to debonding or breakage of the bonded wafers [42]. LCP offers the possibility of adhesiveless packaging through lamination and a variety of advantages including: overall thinness, light weight, flexibility and greater thermal stability [308].

Reliability issues for packages are: hermeticity, moisture resistance, thermal shock and mechanical shock. Since we already know that LCP-LCP lamination would provide hermetic and water resistant packages, we are interested in simulating the mechanical shock effects under static and cyclic loading conditions. The models assume high bonding strength, thus no number of defects/voids in the bonding interface. The interfacial stress results are evaluated as this is where the delamination occurs in a package. Both shear and tensile loads are applied to study the effect of external force on the interfacial stress and assess whether this surpasses the critical LCP yield stress value of 200MPa [46]. Finally the results of the all-LCP package are compared with those of a standard all-silicon package.

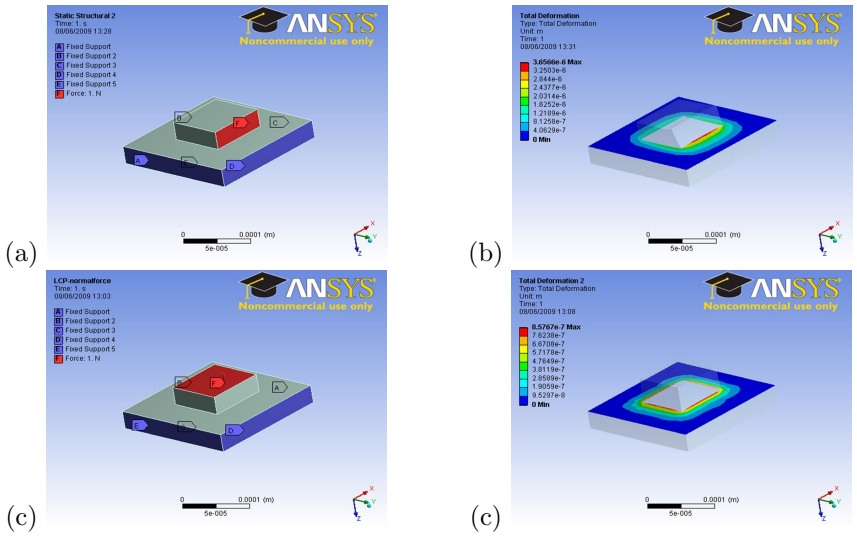


Figure 7.20: Shear load: a)boundary conditions, b)interfacial stress. Pulling load: c)boundary conditions, d)interfacial stress.

Figures 7.20 show the interfacial stresses when the package is subjected to shear load (a and b) and tensile force (c and d).

7.5.1 Static and dynamic analysis

Static analysis, representing a mechanical shock, gives the stress value for a given instant load. However if the package undergoes continuous loading as a result of external factors, the structure experiences cyclic loading. It is well known that cyclic loading leads to more rapid failure of solids compared to static loading at the same magnitude. This is because of the constant action of a load [153].

For both static and dynamic analysis, the simulations included pulling the package upwards for tension and pushing laterally for shear stress with loads from 0.1N to 100N. For the dynamic analysis a frequency of 1.5GHz was considered as this is the working frequency of a standard 250x250μm FBAR.

(a) (b)

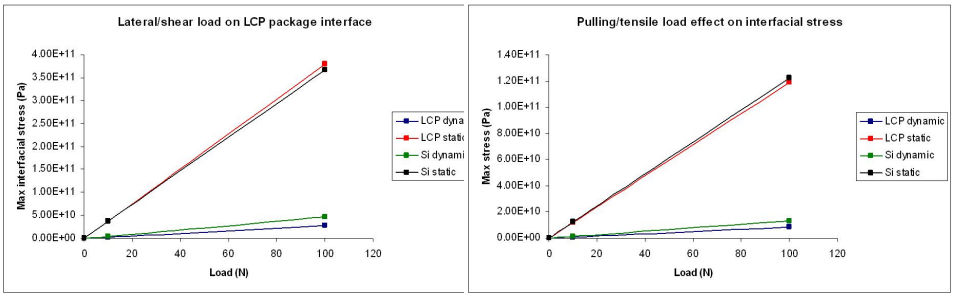


Figure 7.21: Static and dynamic loading comparisons for: a)shear load, b)tensile load.

Static analysis (figure 7.21) shows that stresses experienced on LCP and Si interface were similar both for shear and tensile loading cases. Shear load maximum applied before reaching interfacial stress equivalent to LCP yield strength threshold (200MPa) was 0.7N. While tensile (pulling) load maximum applied before reaching 200MPa was 1.81N.

From figure 7.21 we can also see that given the same load and frequency of occurrence on the packaging structures, the stress experienced on the LCP interfacial package was less than that experienced at the Si interface for both shear and tensile cases. This can be explained by heating usually associated with cyclic loading and LCP, being a thermal insulator, not experiencing the stress-inducing temperature rise at the interface. The maximum shear cyclic force that the all-LCP package withstood before reaching 200MPa yield strength was 0.73N, while a maximum tensile force of 2.36N was applied before attaining 200MPa stress.

7.5.2 Observations on packaging reliability

Static loading studies showed no major differences between the all LCP and the all Si packages. The maximum loads applied on an all-LCP package before it reached the yield stress LCP threshold value of 200MPa were between 0.7-1.81N (depending on the load direction).

For the cyclic loading cases the all-LCP package showed less stress at interface than its all-Si counterpart. This means that the use of LCP package would provide a more reliable solution for future device applications. Maximum cyclic loads that were applied to the all-LCP package before the interface reacheed LCP yield strength were between 0.73-2.36N (depending on the load direction).

The simulations showed that an all-LCP package is an ideal solution as it experiences stresses within the same range as an all-Si package with added advantages such as adhesiveless bonding, hermeticity and low moisture adsorption.

7.6 Electrical reliability

RF losses in a substrate cause quality and frequency limitations [227] hence, in this section, electrical reliability is discussed in these terms. Electric signals provide temperature rise and power loss since the average heat generated is equivalent to the electrical power loss [101]. Low power loss means high power efficiency while high temperature rise means high power consumption.

The heat generated by electronic devices and circuitry leads to failure. Part of this heat is caused by electromagnetic effects such as radiation while the rest is induced by the current which passes through contacts. The motivation for the magnetostatic analysis of metal CPW on the substrates is to quantify electromagnetic effects (i.e. radiation) which cause parasitic charging effects on RF MEMS [273] and lead to heat generation and eventual device failure.

In recent years the use of relatively thin dielectric interface layers on silicon has been proposed as a possible solution to overcome the substrate loss due to the low resistivity and to minimize the electromagnetic field interaction of the passive structures with the silicon substrate [150]. The role of low dielectric constant substrates is, here, assessed for electromagnetic applications since it is known to allow a reduction in power consumption, cross talk and interconnection delay [117].

7.6.1 CPW electro-thermal signal response

Coplanar waveguides (CPW) are widely used in RF MEMS (such as FBARs) due to their simplicity of fabrication and ability to carry high frequencies. Electro-thermal power loss and efficiency is a concern in transmission lines as it causes reliability issues. The substrate upon which the CPW are deposited affects the electromagnetic response, which leads to parasitic charging. Studies were carried out to assess and compare power loss when an AC signal passes through metal track on LCP insulator and on high resistivity Si semiconductor.

LCP is an insulator and an ideal material used for high frequency PCB use. As an insulator, it has very high resistivity, which can be defined as the measure of resistance to the conduction of current. As a consequence of its high resistivity, its dielectric loss due to AC signals is very small. Dielectric loss (or dissipation factor), is the measure of the amount of electrical energy converted to heat in the dielectric [100]. This means that LCP experiences low energy loss and small temperature rise.

Electromagnetic energy can be scattered, reflected or transmitted, but also dissipated into other microscopic motions within the matter, coming to thermal equilibrium and manifesting itself as thermal energy in the material [278]. Even small electrical losses can cause significant temperature rise in microscopic parts [101]. Power loss of CPWs causes heat flow and temperature rise. For these reasons, in the electrical reliability studies, the thermal aspect was discussed.

In the simulations I talked about heat flux and flux density and it is important

to keep in mind that flux density (B) is proportional to current density (J) and power loss is:

$$PL = \frac{J^2}{2}\rho \tag{7.2}$$

Where ρ is the resistivity. This means that flux density (B) is proportional to power loss (PL). Power loss proportionality to heat flux density was also mentioned by Blundell and Overshott [16] and Lee et al. [149]. Power loss is proportional to the square of the current density [101].

A magnetostatic analysis in ANSYS® was carried out for the CPW (frequency∼60Hz built in the EMAG analysis of the software). However, it is important to keep in mind that at higher frequencies (GHz range) electrostatic effects dominate over electromagnetic ones. Material parameters used for the CPW model are shown in the Appendix A..2, resistivity of LCP is $10^{19}\Omega$·m, while that of high resistivity Si is $1.2\text{x}10^{6}\Omega$·m.

Electromagnetic analysis ANSYS

The simulation conditions on the signal line were set with either constant current and varying voltage or constant voltage and varying current. The effects of the electromagnetic activities of the metal tracks in LCP and Si were then compared.

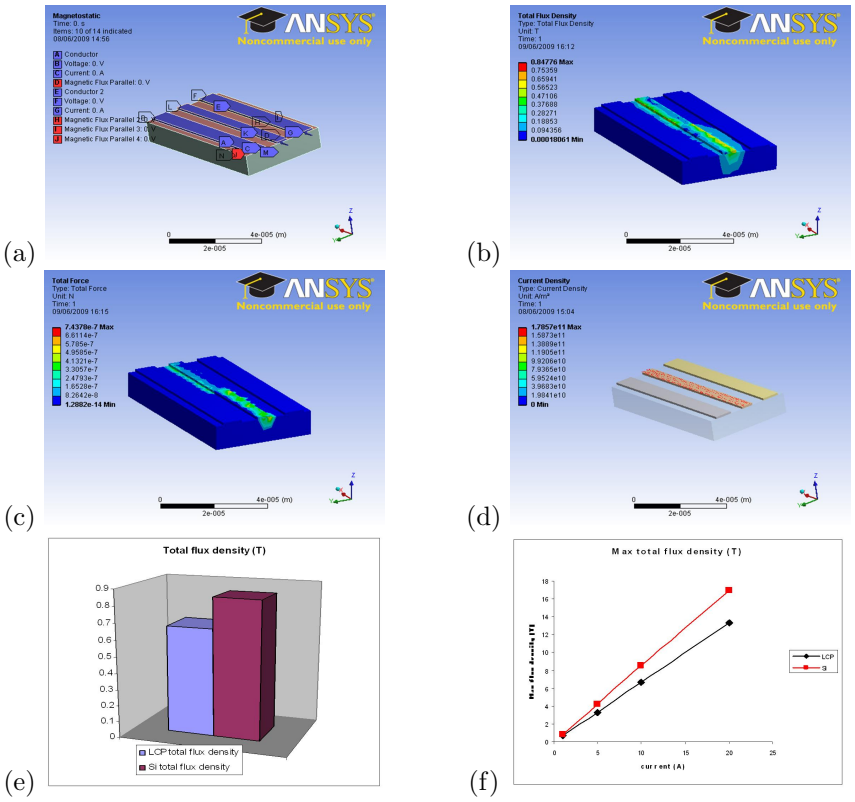


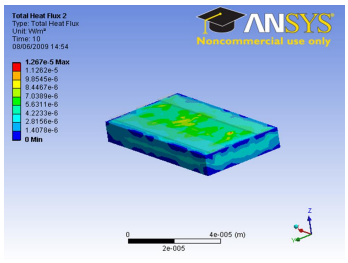
Figure 7.22: a)Boundary conditions, b)total flux density, c)total force, d)current density, e) total flux density with steady current, f) total flux density with steady voltage.

Figure 7.22 e) shows what happened when a steady current of 1Amp was applied with a voltage varying from 5V-50V. Change in voltage did not affect flux density. The results show that the total flux density on Si was greater than on LCP. Figure 7.22 f) represents what happened when a steady voltage of 5V and changing current varying from 1 - 20Amp was applied. We can see that total flux density and force increased with respect to current. Also here it was evident that the total flux density on Si is greater than on LCP. From both figures 7.22 e) and f) we derive that there was more loss of energy for metal tracks on Si than on LCP due to the former having lower resistivity.

Transient thermal analysis ANSYS

For direct heat flux analysis transient thermal simulation was also carried out where the temperature was set at 22°C, the voltage at 20V and current at 1A.

(a)



(b)

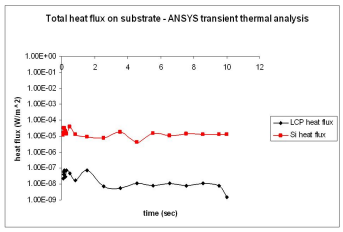


Figure 7.23: a)Total heat flux image, b) total heat flux VS time (transient analysis).

LCP has higher specific heat than Si which means that it is more capable of stabilising temperature. LCP temperature changes less when it absorbs or loses a given amount of heat. Since the heat flux of LCP was less than that of Si, less power was lost in this than in standard Si substrates.

Conclusion on CPW electro-thermal signal response

By simulating the effect of CPW electrical activity on LCP and Si we can conclude that, given the same boundary conditions, the heat flux experienced by the LCP substrate was less than that of high resistivity Si. CPW electrical activity on LCP proved to produce less heat, meaning that its electrical activity caused less power dissipation.

We can conclude that lower flux density and, hence, power loss were experienced when using LCP instead of Si substrate (flux density and power loss are directly proportional see equation 7.2). The higher efficiency of CPWs on LCP was proved to be due to both LCP's higher resistivity and its higher specific heat.

Chapter 8

Concluding remarks and future work

8.1 General conclusions

Low cost and high performance FBARs are necessary for integration with existing passive and active components. The creation of resonators or filters directly on organic substrates would mean that integration of packaged digital components with active devices could be carried out easily through lamination, thus, eliminating the use of un-matching layers, extra adhesives and wiring which can contribute to reliability issues such as outgassing, stress-induced delamination or circuit parasitics. Hence, the development of low cost and low loss passive components on polymers to combine with active devices, would lead to overall performance improvement and reduction in interconnection and packaging problems. The integration of FBAR devices directly on a single flexible RF chip could allow the replacement of discrete components, offering the above-mentioned features.

The goal of producing FBARs on LCP with MEMS processing techniques and appropriate pre-processing steps has been achieved. The knowledge of fabrication methods for FBAR creation directly on LCP will widen the knowledge of passive RF MEMS production in the field of flexible circuits since so far only active devices (switches [290], antennae [53], cantilevers and membranes (for pressure/tactile sensors) [292]) have been created. Our project faced the creation of FBARs on LCP for the first time.

The topic of polymer-based FBARs is of interest as the literature is very limited. Furthermore ZnO ceramic deposition on LCP has never been carried out. The combination of a microwave substrate like LCP used in conjunction with a piezoelectric material like ZnO provides high potential for the creation of high efficiency RF devices for resonance and filtering applications.

For the fabrication, first of all pre-processing was carried out where the LCP was safely backed to silicon in order to undergo standard MEMS processing. We found that the best backing method for the achievement of low waviness

and high radius of curvature was with the home-made vacuum bonding equipment with 1μm black wax used as the adhesive layer. While waviness was mainly influenced by the rigidity of the composite, the radius of curvature of this multilayer was shown to be affected by both rigidity and thermal mismatch parameters.

Both Cu-clad and unclad LCP present an undesired surface roughness which must be reduced for successful functional material growth and crystallization. Hence, the next step was to reduce the roughness of the LCP. The preferred smoothing method was found to be CMP carried out at Tyndall National Institute (Cork, Ireland) using alumina slurry, polishing time of 20min and pressure of 3.45N/cm^2. The only drawback of CMP was that it caused sporadic striations on the surface of the LCP, which affected subsequent thin film layer deposition quality. The solution suggested is to use slurry-free CMP pads (future work).

CMP allowed low roughness achievement without causing major surface stresses. Polyimide coating, on the other hand, introduced high surface stresses making the substrate curl up, therefore, hard to process and less reliable for ZnO ceramic integration. Another disadvantage of using polyimide smoothing method is that, through the use of polyimide, the essential LCP properties (high chemical resistance, low moisture absorption, low dielectric loss) are masked.

Metal deposition was tested both through sputtering and evaporation. Sputtering is a better option than evaporation as it tends to generate uniform, void-free thin metal layers. For sputtered metals, the quality was shown to depend on the substrate roughness. As the roughness decreased, the Au <111> orientation improved.

ZnO growth quality on LCP was assessed as a function of initial substrate roughness and deposition temperature. It was found that c-axis orientation of the piezoelectic largely depended on the LCP substrate roughness. The deposition temperature yielding the highest ZnO <002> peak was 200°C. However, at this temperature the ZnO delaminated and cracked in certain areas due to thermally-induced surface stresses. A deposition temperature of 100°C was, hence, chosen as it showed an appropriate balance between high quality and low surface stresses. Electrical results were taken for ZnO deposition at 100°C which had values very close to those of standard ZnO and an appropriate capacitive behaviour. The slight discrepancies were thought to be a result of the slight remaining roughness of the LCP (5nm). Both surface smoothness and deposition temperature were seen to be essential parameters for acceptable ZnO growth on LCP.

ZnO/Au/LCP multilayer mechanical analysis was carried out after deposition in order to find the properties of each material layer. The properties derived from the measurements were very close to what was expected (wherever possible to compare). The results were used as references to provide threshold value limits for the stress simulation analysis of the devices.

For the photolithographic process we concluded that the best solution for bottom electrode patterning was to avoid bi-layer and lift off but, instead, to carry

patterning and etching after blanket metal deposition. This was in order to avoid unwanted effects, such as LCP/photoresist interaction during curing and UV exposure.

Misalignment of the devices, caused the sides of some FBARs to be clamped, therefore, damping their resonance and Q. Alignment accuracy depended on one or a combination of more of the following factors: LCP dimensional stability (parameter over which we had no control), substrate curvature and waviness. Substrate bow and waviness, which were induced by thin film stresses and the manufacturing process, were parameters easy to control through appropriate backing. The alignment accuracy was optimised with high quality substrate backing method in order to minimise waviness and increase radius of curvature.

LCP etching was carried out through RIE using oxygen gas. While high power (150W) favoured high etch rate, high etch pressures (>100mTorr) were proven to work in favour of high material selectivity. The LCP oxygen etch at high pressures (∼200mTorr) provided the highest LCP to Au selectivity. Straight walls were noticed after LCP RIE etch, this would lead to smaller device sizes, 3D MEMS production and, therefore, overall space savings. Furthermore, because LCP was etched with oxygen gas only, there was no need for a buffer layer (Si_3N_4 or SiO_2) as for the Si-based fabrication technology. Both size reduction (through vertical wall achievement) and elimination of buffer layer would lead to higher device frequencies. The former would allow this because of device size reduction, while buffer layer elimination would eliminate the mass-loading effect of this additional layer. However it is important to note that, some residues were found at the back of the LCP even at pressures up to 200Torr. Excimer laser could eventually be used to selectively remove the residues in particular locations with high ablation rates (0.13μm/pulse for 300 mJ/cm^2 for photoresist ablation [118]).

FBAR performance is known to depend on many factors including LCP substrate smoothness and ZnO sputtering conditions. In my project I achieved the desired FBAR resonance and k^2_{eff}, however the Q factor was very low even after de-embedding, meaning that the effect of the fixtures was not relevant in the as-measured devices. Low Q was thought to be a consequence of one or more of the following: LCP roughness still existing (5nm), and LCP back residues. Hence, although FBAR device RF performance was improved throughout the studies, there is room for Q improvement through further LCP roughness reduction and total elimination of back residues.

While some devices showed FBAR-like behaviour, others failed. Some of the major reasons for device failure were mentioned and analysed. Causes for poor device performance, assessed both theoretically and experimentally, were thought to be: mass-loading, electrical shorts and opens, acoustic losses, electrical losses and contact failure problems during measurement.

The mass-loading effect, whether caused by back LCP residues or by edge clamping, was shown to decrease the resonant frequency and Q of the FBAR. Some fabrication process effects such as defective ZnO material growth or over-etching of metal track, showed to lead to open and short circuits respectively. ZnO sur-

face roughness proved to yield, besides poor piezoelectric characteristics, power loss through acoustic and electrical mechanisms.

The success of FBAR microwave measurement was proven to rely, to some extent, on the physical contact made between probe and metal. Contact quality was measured in terms of contact resistance through s-parameters determination and conversion into resistance. A high track resistance meant higher power loss. The causes for high track resistance were substrate waviness and roughness, which caused low contact area, and probe-induced strain. Hence, for low track resistance, the need for a flat, smooth substrate was seen with a good balance between high probe/substrate contact area and low probe-induced strain.

Stress analysis of the multilayer for device applications is very important since, besides leading to material and device failure, stresses can affect the electromechanical response due to initial stress levels. Simulations were, hence, carried out in order to assess the reliability of the LCP-based devices. This was done through stress analysis validation against critical values such as ZnO fracture strength. Both fabrication and application-induced stresses were analysed.

From the simulation results in the fabrication reliability we found that as-deposited thin films on LCP had less stress within than when deposited on stiff silicon. The presence of an extra polyimide (if used as a smoothing method) in the multilayer brought an increase in ZnO thin film stresses from up to ∼500MPa on LCP/polyimide. The stresses of ZnO on LCP were below 200MPa (less than the critical value of 2.68GPa of ZnO) meaning that, after high temperature deposition, the ZnO was not strained enough to reach its critical fracture strength value. From the multilayer reliability studies of the as-deposited ZnO we concluded that the ceramic/metal/polymer combination, given the fabrication parameters used, was reliable for device production.

For the device reliability we saw that with the application of a static external force to the LCP-based device, the stress experienced by the ZnO was greater than when using the same force on standard silicon substrates. This was given by the LCP substrate liability to higher deformation. Furthermore, cyclic analysis simulations of the FBARs under high frequency operation were carried out from which we concluded that, given the same conditions (frequency and force), the LCP-based device experienced slightly higher stress than the Si-based FBAR. However this was considered an advantage as it would mean that the actuation voltage (force) of FBARs on LCP could be less in the future.

In order to avoid unnecessary stresses for the static device loading case, novel device layouts were proposed whereby we saw the reduction of stresses within the critical ZnO through the use of appropriate geometry. The novel configurations proved the validity of this theory as, for some of the new geometries, stress was absorbed by the LCP suspended links and, therefore, relieved from the ZnO. However studies on the signal transmission when using these geometries must be carried out as part of the future work.

From the packaging reliability simulations we derived that all-LCP packages experienced slightly lower stresses than an all-silicon one with added features

such as adhesiveless bonding, hermeticity and low moisture absorption.

Electrical reliability was assessed in terms of power loss (proportional to heat flux) for CPW on LCP and Si. Simulations showed that signal transmission was more efficient (less heat flux, more efficiency) for CPW metal tracks on LCP than on Si. This is due to LCP having having higher resistivity and specific heat than silicon. The conclusion to these studies was that LCP caused less power consumption than Si leading to more electrically reliable devices.

In this project I attained an improvement in control of front and back processing for FBAR production on LCP through appropriate pre-processing steps followed by standard MEMS techniques. Performance yield improved by a factor of 40 (compare Sample 9 and Sample 21). FBAR process flow on LCP was very different to that of FBAR on Si as we can see in Appendix A..3. It can be noticed that FBARs on LCP required more steps than traditional silicon-based ones. This is a disadvantage of LCP-based MEMS as the process variabilities increase and, from equation 2.34, we can notice that the yield decreases with respect to an increase in the number of manufacturing steps.

Process development was one of the focuses of my research, whereby I investigated how to achieve high quality thin films on a non-standard substrate and safely integrate ZnO ceramic with flexible LCP. Furthermore I assessed the reliability outcome of such a combination and analysed the final devices. In conclusion I showed that, with appropriate substrate pre-processing (rigid backing and smoothing) and tailored MEMS fabrication steps, LCP was a viable substrate for complex RF MEMS device geometry production such as FBARs.

8.2 Advantages and disadvantages of FBAR on LCP

Advantages of using LCP

The main advantages of polymer-based FBARs are:

- Low cost of LCP makes it attractive over the current silicon use.
- Overall size reduction. The use of a flexible substrate would mean lighter and smaller components as the light polymer can be folded and bent.
- Lower transmission losses for RF components due to LCP lower dielectric constant, lower dielectric loss and higher resistivity than Si/SiO_2 substrate.
- Low moisture absorption which means more frequency stability in device operation.
- High melting point compared to other polymers (315°C).
- High temperature stability of LCP: i.e. dielectric loss does not change when LCP is subjected to high temperatures [276].

- Excellent chemical resistance (i.e. HF and KOH) and biocompatibility of LCP which will allow the FBARs to be used in harsh environments.
- Eventual higher FBAR frequencies given by: elimination of buffer layer (hence of mass-loading), and realisation of vertical back-etched walls (therefore device size reduction).
- Less required actuation voltage (force) to actuate LCP-based devices. This is explained by applying the same force on both LCP and Si-based devices and getting a larger stress on the LCP-based ones (see section 7.4).
- Ease of assembling and packaging the LCP-based FBAR through lamination at relatively low temperatures providing better polymer/polymer adhesion instead of the eutectic or adhesive bonding currently used for standard MEMS. An all-LCP device and package would eliminate the material TCE mismatch problem leading to package delamination such as that occurring in adhesive-bonded assemblages.
- Direct 3D integration with PCB and other components (i.e. antenna) for the duplexer creation.

Disadvantages of using LCP

- More fabrication steps are, so far, required for LCP-based FBARs compared to Si ones. This leads to lower device yield. Extra steps included flattening and roughness reduction pre-processing stages.
- LCP still has high roughness which causes FBAR low Q factor achievement.
- RIE etch leaves residues on the back of the device. For FBAR, this can lead to lower frequencies and Q factor.

8.3 Future work

Future work will need to concentrate on the following aspects:

- Optimization of roughness reduction process and rigidity enhancement for more homogeneous ZnO growth, Q and FBAR performance.
- As part of the roughness reduction optimisation, the use of slurry-free CMP pads would have advantages such as producing scratch-free LCP surfaces.
- Back FBAR residue elimination to allow higher frequency and Q. Residue elimination could be done in various ways: polishing of the LCP backside prior to RIE, use of excimer laser or optimization of the RIE etching conditions to achieve high selectivity and no back residues.
- Reduction of the number of fabrication steps for FBAR production on flexible LCP to increase the device yield per wafer.

- Use of different thin film materials such as Aluminium Nitride (AlN) for piezoelectric and Molybdenum (Mo) for electrodes could be a way forward. AlN has high acoustic velocity which will allow high FBAR frequencies, while Mo is a very light metal hence leading to smaller mass-loading of the resonator.
- Implementation of new device geometries for reduced stress effect on the ceramic.
- Carrying out signal transmission analysis of the FBARs when the new stress-relieving geometries are employed.
- Investigation of transient-thermal reliability of device operation. Since LCP is a viscoelastic material which can lead to dimensional changes, component mismatch and failure [220] caused by time and temperature can occur.

8.4 Events and publications

Events
Flexidis Workshop - Cambridge, 29th 30th March 2007.
Micro Nano Engineering (MNE) conference 2008, Athens.
Eurosensors conference 2009, Lausanne, Switzerland.

Publications
"Suitability of Liquid Crystal Polymer Substrates for High Frequency Acoustic Devices", Ghazal Hakemi, Robert Wright, Paul Kirby, Colin Colinge, Alan Blake, Elsevier Procedia Chemistry, Volume 1, Issue 1, Proceedings of the Eurosensors XXIII conference, August 2009, Edited by Juergen Brugger and Danick Briand, Pages 72-75.

Chapter 9

Contribution to knowledge

Gaps in the state of the art and contribution to knowledge of this thesis include:

MEMS processing methods on LCP

Development of MEMS processing methods directly on LCP was carried out. At the start of the project it was not known whether the creation of back-etched free-standing FBARs on LCP was possible. Standard fabrication methods were employed to produce front and back processed devices.

- With appropriate substrate pre-processing (rigid backing and smoothing) LCP has proven to be a viable substrate for metal deposition and piezoelectric thin film growth.
- The knowledge that CMP process can be used to smooth LCP to a sufficient extent to develop a device processing technique.
- It is possible to use a wafer bond technique as a means of front and back processing on flexible substrates using common photolithographic techniques.
- Photolithographic conditions for acceptable patterning have been established (i.e. avoid using bi-layer and lift off).
- Ideal fabrication process flow has been developed for front-and-back processed device.

ZnO growth on LCP

The knowledge of ZnO thin film growth on LCP is novel both in terms of growth quality and reliability. In this project the conditions for appropriate ZnO growth on LCP have been given. ZnO quality is assessed in terms of c-axis orientation intensity followed by mechanical analysis giving ZnO fracture strength limit.

- Dependance of ZnO degree of c-axis orientation (high intensity required for FBARs) on the roughness of the underlying LCP.
- Determination of the correlation between ZnO c-axis intensity and growth temperature on LCP.

- Given appropriate LCP surface texture and ZnO RF sputtering conditions, possibility of high c-axis ZnO deposition on LCP. The ZnO showed appropriate electrical characteristics including the capacitive behaviour.
- Determination of ZnO fracture strength on LCP which can be employed for reliability studies of the ceramic/metal/polymer multilayer.

LCP-based FBAR production, yield and performance

There is no previous work on LCP-based free-standing FBARs, hence performance results are novel.

- The possibility to achieve a fully free-standing device with no etch stop layer (i.e. SiN_x or SiO_2) has been proven.
- It has been proven that the devices produced also act like FBARs with high ${k_{eff}}^2$ (however Q is still low). The devices have the desired FBAR resonance and electromechanical coupling coefficient, however the Q factor is low. This is thought to be a consequence of the LCP still being too rough, therefore causing acoustic loss. The performance can be improved through further LCP roughness reduction.
- An assessment of device failure mechanisms has been carried out. The conclusions of this assessment are useful as they allow troubleshooting of the issues.

ZnO/LCP integration and reliability

Multilayer and device reliability analyses, considering the ceramic/polymer integration, are carried out in terms of the ZnO fracture strength.

- Stresses caused by FBAR fabrication on LCP (especially high temperature ZnO deposition) do not exceed the ZnO fracture strength threshold limit. The multilayer combination does not exceed the critical ceramic fracture value at the fabrication level. On the contrary, stresses of as-deposited ZnO on LCP have been proven to be lower than as-deposited ZnO on Si.
- Substrate bow negatively affects the stress experienced by the ZnO. Substrate thickness and presence of Au, however, reduce the stress experienced by the ZnO due to an increase in neutral axis distance from the ZnO/LCP interface (increase in rigidity).
- Device reliability studies show that for a given load on the structure, the LCP-based FBAR leads to larger ZnO stresses. Hence, the simulated effect of novel geometries on the stress experienced by the ZnO ceramic has been carried out. It has been shown that some of these configurations have a stress-relieving effect.
- A device created on LCP is more power-efficient than one on Si due to the former having both higher resistivity and specific heat.
- An LCP-based FBAR is also more power efficient as it needs less actuation voltage to operate.

Appendix A

APPENDIX

A..1 Standard and modified processing methods and conditions

Photolithography

STANDARD PHOTOLITHOGRAPHY

Table A.1: Standard photolithography procedure.

Process	Condition	Time
Deposit S1818	spin 4000rpm	30s
Baking	115 °C	30s
Exposure (with mask)	100mJ (time=mJ/intensity)	22s
Develop	MF319	30-45s

IMAGE REVERSAL PATTERNING

Table A.2: Process conditions for photolithography using AZ5214 as a negative photoresist.

Process	Condition	Time
Deposition AZ5214	4000rpm	30s/60s
Bake	90 °C	2min
Exposure (with mask)	100mJ	25s
Wait	Nitrogen disperses in photoresist	30min
Bake	115 °C	3min
Flood exposure	500mJ	110s
Develop	MF319	30-45s

STANDARD METAL BILAYER and LIFT-OFF

Table A.3: Bilayer and lift-off photolithography procedure.

Process	**Condition**	**Time**
Deposit LOR2A	spin 3000rpm	30sec
Bake LOR2A	115°C	5min
Deposit S1818	spin 3000rpm	45sec
Bake S1818	115°C	90sec
Expose	100mJ (time=mJ/intensity)	25s
Develop	MF319	30-45s
Deposit Metal	-	-
Lift-off	Put sample in acetone	10min-5hrs

MODIFIED METAL BILAYER and LIFT-OFF

This is done since the adhesive deposited to keep LCP attached to the rigid Si substrates was, in some cases, affected and dissolved by acetone. This mainly happened for samples that where lift-off did not happen within the first hour, but took longer.The following process offers the possibility of using MF319 instead of acetone for the lift-off step.

Table A.4: Modified bilayer and lift-off photolithography procedure.

Process	**Condition**	**Time**
Deposit LOR2A	spin 3000rpm	30sec
Bake LOR2A	115°C	5min
Deposit S1818	spin 3000rpm	45sec
Bake S1818	115°C	90sec
Expose	100mJ (time=mJ/intensity)	25s
Develop	MF319	30-45s
Flood exposure	100mJ	25s
Deposit Metal	-	-
Lift-off	Put sample in acetone	10min-5hrs

BACK PHOTOLITHOGRAPHY FOR SILICON DRIE ETCH

Table A.5: Using AZ4562 as mask

Process	**Condition**	**Time**
Spin AZ4562	500rpm	30s (for 16μm AZ4562)
Bake AZ4562	90°C	30min
Expose AZ4562	500mJ	102s

Table A.6: Using Al as mask

Process	**Condition**	**Time**
Reverse photolithography for bi-layer	See "Image reversal patterning"	
Sputter Al	500nm	20min
Lift-off Al	Put sample in acetone	2-5hrs

Sputtering

Table A.7: Metal sputtering conditions - Nordiko.

	Gold (Au)	**Platinum (Pt) DC**	**Titanium (Ti)**	**Chromium (Cr)**	**Aluminium (Al)**
Argon flow (sccm)	45	45	45	45	45
Power (W)	100	-	300	200	200
Voltage (V)	-	475	-	-	-
Current (Amps)	-	0.7	-	-	-
Sputter rate (nm/sec)	0.48	2.05	0.33	0.3	0.41
Chamber pressure (mTorr)	5e-3	5e-3	5e-3	5e-3	5e-3

Table A.8: ZnO sputtering conditions to achieve 1μm thickness - Balzers.

Power (W)	**Pressure (mtorr)**	**Gas mixture (O_2/Ar)**	**Temperature (°C)**	**Time (min)**	**Thickness yielded (μm)**
250	25	10/90	250	120	1-1.5

For ZnO sputter, a 30min pre-sputtering is necessary. The temperature was varied between a range of: room temperature up to 250°C.

Electroplating

Table A.9: Ni electroplating tested conditions for 8x8cm and 4inch diameter wafer.

Deposited thickness (μm)	**Solution temperature(°C)**	**Current (mAmp)**	**Time (hr)**
1	50	38 (0.53mA/cm^2 current density)	1
50	50	100 (1.4mA/cm^2 current density)	19
100	50	100 (1.4mA/cm^2 current density)	38

Etching

CHEMICAL ETCHING

Au etch: in gold etchant TFA (contains 8 wt% Iodine, 21 wt% Potassium Iodide, 71 wt%water) etch rate of 200nm/min. Au etchant also affects Cu after one minute dip due to the development of an oxide layer on the copper; the average etch rate of Cu in Au etchant was 10.3μm/min.

Cr etch: in cerium ammonium nitrate+acetic acid solution with an etch rate of 0.3μm/sec.

Cu and Ni are etched in ferrochloric acid ($FeCl_3$).

DRY ETCHING

Table A.10: Dry etching of standard materials.

Etched material	**Power (W)**	**Pressure (torr)**	**Gas mixture**	**Etch rate (μm/min)**
Ti (RIE)	100	20	CHF_3	0.0016
Si (DRIE)			SF_6+CHF_4	2.4

Pickling

Nitric acid (HNO_3) (Johnson Matthey 69%) is slowly added to DI water were to make a 200cc solution of HNO_3:DI=1:3. The acid is added to the water and not the other way around because, as a general principle, it is known that the reaction produces heat. By preparing the solution this way, the heat produced can be better controlled. The sample is then dipped in the solution for 10sec followed by rinse in DI water.

Polyimide coating and removal

Coating with Pyrolin Supelco PI2555 polyimide

1. deposit 2mil polyimide (PI2555 Supelco) (with dynamic viscosity (μ) 1.34Pa·s, and max. operating temperature=350C.) at (4000) 2000rpm for (45) 30s, Polyimide PI2555 sealing resin.
2. bake for 24hrs at 90°C.

Coating with Durimide 7020 polyimide

1. 2mil polyimide (Durimide 7020), with dynamic viscosity (μ) 5.2Pa·s, was deposited on at 4000rpm for 45s (spun for longer time because more viscous than PI2555), it was then left to
2. bake for 24hrs at 90°C.

Polyimide removal To remove PI [71].

1. Dip sample for 5 minutes in the ultrasonic bath at 55°C temperature in NMP (N-mthyl-pyrrolidinone)
2. Dip sample in PI developer QZ3501 in ultrasonic bath at 55°C for 5min.
3. Dip sample in NMP at room temperature for another 5min.

An alternative to NMP is to use Microposit remover.

A..2 Material properties

Table A.11: General material properties used for simulations

Material	Thermal expansion coefficient(ppm/°C)	Young's modulus(Pa)	Poisson's ratio	Emissivity ($\frac{mJ}{cm^2}$)	Surface energy
Si	0.55e-6	150e9	0.17	3.9	-
LCP	17e-6	2.255e9	0.3	2.9	41.04
Au	14.1e-6	78e9	0.44	-	-
ZnO	30.02e-6	108e9	0.25	-	-
Polyimide	27e-6 or 54e-6	3.5e9	0.35	-	18.9
Cu	16.6e-6	115e9	0.32	0.05	-
Ni	13e-6	200e9	0.31	-	-

Table A.12: Material properties used for 1-D Mason Model electro-acoustic FBAR simulations

ZnO thickness(μm	1
Au density(kg/m^3)	19300
LCP density(kg/m^3)	1400
ZnO density(kg/m^3)	5700
Au acoustic velocity (m/s)	3210
LCP acoustic velocity (m/s)	2500
ZnO acoustic velocity ((m/s)	6039

Table A.13: Material properties used for CPW model

LCP resistivity	10^{19}
Si resistivity	1200000
LCP dissipation factor	0.02
Si dissipation factor	0.001
LCP specific heat	1.41J/g/°C
Si specific heat	0.7J/g/°C

A..3 FBAR fabrication process flows

Standard FBAR process flow

1. Bi-layer for bottom electrode.
2. Bottom electrode deposition (sputtering with Nordiko) and lift-off.
3. ZnO deposition.
4. Photolithography and alignment for ZnO via patterning.
5. Photoresist development in MF319 and ZnO pattern etch in 25% acetic acid for 1-3min.
6. Bi-layer photolithography and alignment for top electrode.
7. Top electrode deposition and lift-off.
8. Back-side AZ4562 photoresist deposition or Al metal sputtering for back masking.
9. Front-to-back alignment of masks for etching back features. Development of AZ4562 or lift-off Al back features.
10. DRIE etch of silicon (thickness $\sim 500\mu$m in SF_6)for 3 hours.

Process Flow 1: FBAR on ULTRALAM3850 with silicon backing

1. Spin photoresist on one side of Cu-LCP-Cu sample.
2. Etch front side of Cu clad.
3. Attach Si with to back with black wax.
4. LCP front roughness reduction: lap polish or polyimide spin.
5. Bi-layer for bottom electrode.
6. Bottom electrode deposition (sputtering with Nordiko) and lift-off. At this stage LCP can detach from Si.
7. ZnO deposition.
8. Photolithography and alignment for ZnO patterns/vias.
9. Photoresist development in MF319 and ZnO pattern etch in 25% acetic acid for 1-3min.
10. Bi-layer photolithography and alignment for top electrode.
11. Top electrode deposition and lift-off.
12. Back-side AZ4562 photoresist deposition or Al metal sputtering for back masking.
13. Front-to-back alignment of masks for etching back features. Development of AZ4562 or lift-off Al back features.

14. DRIE etch of silicon (thickness $\sim 500\mu$m in SF_6)for 3 hours.
15. Cu features etched with $FeCl_3$ and black wax adhesive layer removed with toluene.
16. RIE etch of LCP back to release Au/ZnO/Au membrane.
17. Removal of Si substrate and Cu layer (if necessary). Former carried with acetone dip while the latter is done thorugh $FeCl_3$ etch with appropriate protection of front features (especially since ZnO is affected by the acid).

Process flow for ULTRALAM3800 is the same except for the initial and final Cu clad etch steps.

Process Flow 2: FBAR on ULTRALAM3850 with Cu (or Cu-Ni) backing

1. Spin photoresist on one side of Cu-LCP-Cu sample.
2. Etch front side of Cu clad with ferrochloric acid $FeCl_3$ while leaving back Cu clad.
3. If electroplating, then attach Si on front LCP side to keep sample planar for Ni electroplating.
4. Electrodeposition of Ni and Si detachment with acetone.
5. Roughness reduction: lap polishing or polyimide deposition.
6. Photolithography of back of wafer (for membrane features) using S1818 photoresist followed by bi-layer for of front of wafer (for bottom electrode features) using LOR2A and S1818.
7. Pattern using front-to-back alignment: front (bottom electrode features) and back (membrane etch features) masks are aligned in double sided mask aligner, Karl Suss MJB21, intensity 12.2 J, exposure time 9s, development time 45s in MF319 alkali solution.
8. Etch patterned back Cu (or Ni-Cu) features so that during lift-off of bottom electrode in acetone, the back patterns remain.
9. Deposit bottom electrode: Nordiko sputtering (Ti-Au).
10. Lift-off in acetone .
11. RIE etch of LCP followed by complete Cu (or Cu-Ni) removal in $FeCl_3$.
12. Deposition of $\sim$1-2μm ZnO with: Power=250W, time=2hrs, T=20-250°C (preferably 100°C due to thermal-induced stresses caused by TCE difference between polyimide and Au), pressure=25-30mtorr.
13. Photolithography and alignment for ZnO patterns/vias. Alignment gap of single sided mask aligner is increased to maximum 247.5μm or 99 steps (each step=2.5μm) from usual 17.5μm or 7 steps; this is to allow for small substrate warpage not to interfere and cause friction with the mask during alignment.

14. Photoresist development in MF319 and ZnO pattern etch in 25% acetic acid for 1min.

15. Bi-layer, alignment and development for top electrode.

16. Top electrode deposition and lift-off in acetone.

17. Back side etch of FBAR in RIE .

18. Cu/Ni removal, if necessary, from back with $FeCl_3$ with appropriate protection of front features.

Process Flow 3: Alternative FBAR on ULTRALAM3850 with Cu (or Cu-Ni) backing

1. Spin photoresist on one side of Cu-LCP-Cu sample.

2. Etch front side of Cu clad while leaving back Cu clad.

3. Attach Si on front LCP side to keep sample planar for electroplating.

4. Electroplate Ni on back side and detach supporting Si wafer with acetone.

5. Roughness reduction: lap polish, polyimide spin.

6. Bi-layer for bottom electrode on LCP side and pattern back side of Cu.

7. Back-to-front alignment of front (bottom electrode) and back (membrane feature etch) masks with double mask aligner (Karl Suss MJB21)intensity 12.2J, exposure time 9s, development time 30s. Follow with development of patterned features.

8. Etch patterned Cu (or Ni-Cu) back in $FeCl_3$) so that during bottom electrode lift-off the back patterns remain.

9. Bottom electrode deposition (sputtering or evaporation) and lift-off in acetone.

10. RIE etch for back side of FBAR.

11. Cu clad (or Cu-Ni) removal from back in $FeCl_3$.

12. Deposit $\sim$ 1-2μm ZnO.

13. Photolithography and alignment for ZnO patterns/vias. Alignment gap of single sided mask aligner is increased to maximum 247.5μm or 99 steps (each step=2.5 μm) from usual 17.5 μm or 7steps; this is to allow for small substrate warpage not to interfere and cause friction with the mask during alignment.

14. Photoresist development in MF319 and ZnO pattern etch in 25% acetic acid for 1min.

15. Bi-layer, alignment and development for top electrode.

16. Top electrode deposition and lift-off in acetone.

Process flow schematics

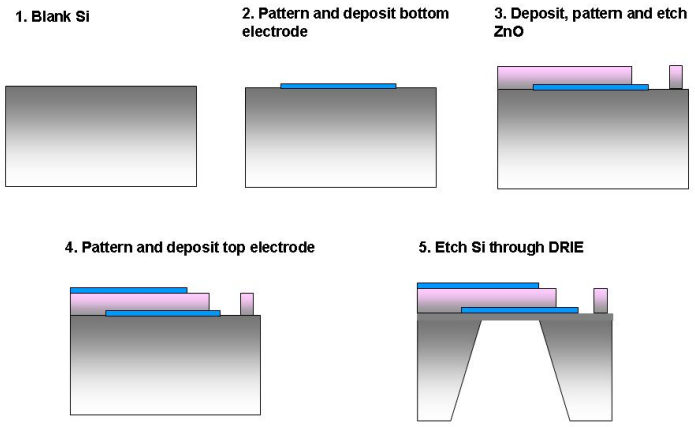


Figure A.1: Standard FBAR fabrication process flow.

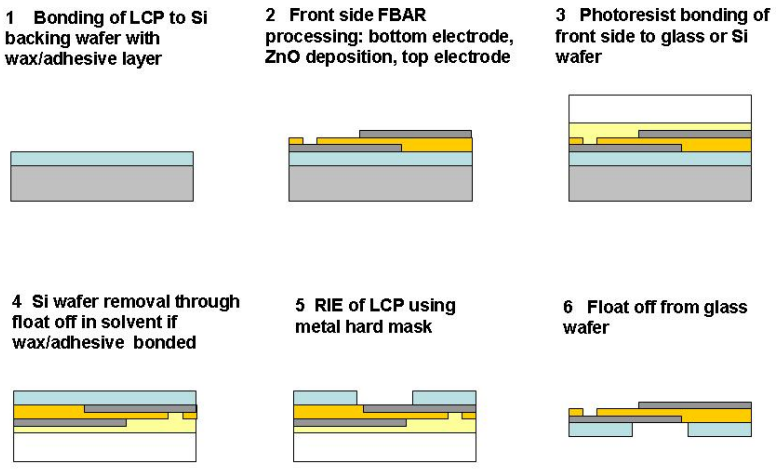


Figure A.2: Main FBAR production process flows on LCP without silicon backing.

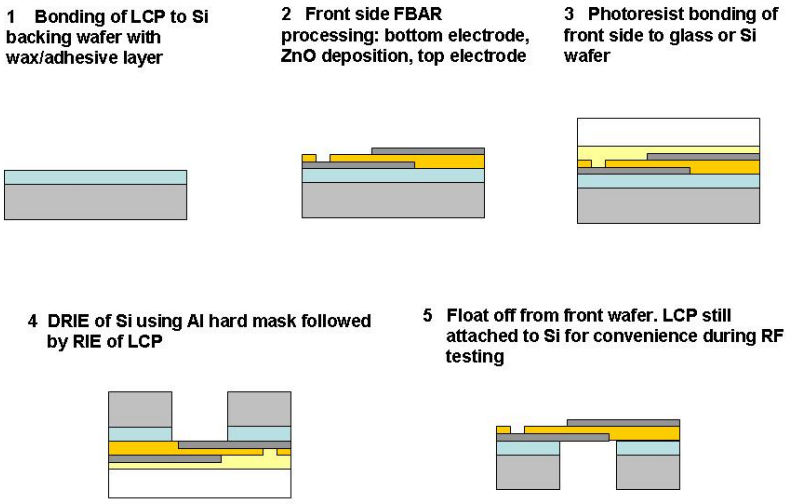


Figure A.3: Preferred FBAR production process flow on LCP. Notice that silicon backing is best to be kept until the end for RF measurement.

A..4 Sample list with methods

Table A.14: List of samples and methods used. N.B.: A=ULTRALAM3850 (Cu-cladded), B=ULTRALAM3800 (unclad).

Sample name	**Reference substrate**	**Backing method**	**Backing substrate**	**Adhesive**	**Smoothing method**	**Mask for back etch**
Sample 1	A	None	Cu	None	None	NA
Sample 2	A	None	Cu	None	CMP	NA
Sample 3	A	None	Cu	None	CMP	NA
Sample 4	A	None	Cu	None	polyimide	NA
Sample 5	A	Electroplate	Cu-Ni	None	CMP	NA
Sample 6	A	Electroplate	Cu-Ni	None	polyimide	NA
Sample 7	A	Hotplate	Si	S1818	polyimide	NA
Sample 8	A	Hotplate	glass	S1818	polyimide	NA
Sample 9	A	Electroplate	Cu-Ni	None	CMP	Cu-Ni
Sample 10	B	Hotplate	Si	AZ4562	polyimide	NA
Sample 11	B	Hotplate	glass	AZ5462	CMP	Au
Sample 12	B	Vacuum oven	Si	AZ4562	CMP	Si/photoresist
Sample 13	A	Hotplate	Si	AZ5462	CMP	NA
Sample 14	B	Vacuum oven	Si	black wax	CMP	Au
Sample 15	polyimide	Vacuum oven	Si	black wax	polyimide	Si/photoresist
Sample 16	B	Tailored vacuum bonding	Si	black wax	CMP	Si/Al
Sample 17	A	Tailored vacuum bonding	Si	black wax	CMP	Si/photoresist
Sample 18	A	Tailored vacuum bonding	Si	black wax	CMP	Si/Al
Sample 19	B	Tailored vacuum bonding	Si	black wax	CMP	NA
Tyndall 1 (sample 20)	A	Tailored vacuum bonding	Si	black wax	CMP	Si/photoresist
Tyndall 2 (sample 21)	B	Tailored vacuum bonding	Si	black wax	CMP	Si/Al
Tyndall 3 (sample 22)	A	Tailored vacuum bonding	Si	black wax	CMP	NA
Tyndall 4 (sample 23)	B	Tailored vacuum bonding	Si	black wax	CMP	NA

A..5 FBAR MASK

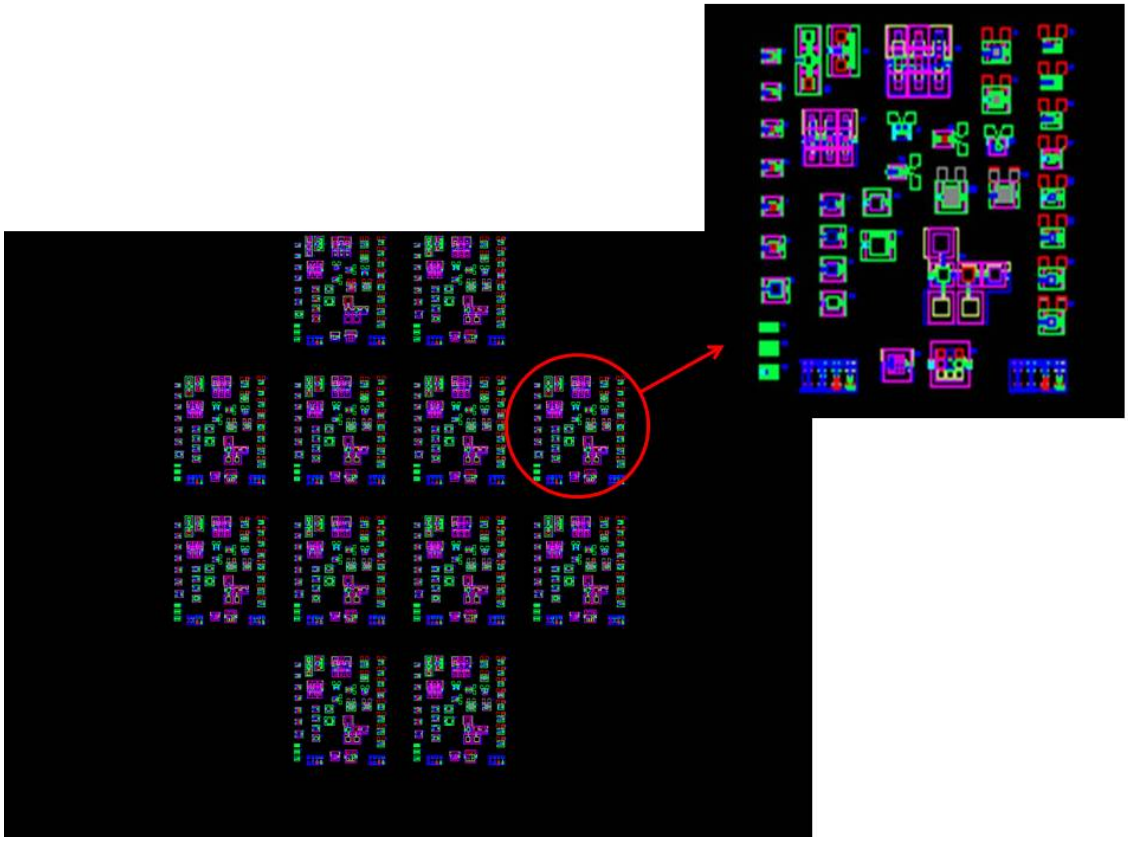


Figure A.4: FBAR mask employed.

A..6 Capacitance and dielectric constant extraction from S-parameters

Capacitance

$$C = \frac{1}{Z(j \cdot \omega + \omega \cdot tan\delta)} \tag{A.1}$$

Where:
Z is the impedance.

$$Z = \frac{(100 - 100 \cdot S_{21})}{S_{21}} \tag{A.2}$$

$$Z = \frac{1}{j\omega C} \tag{A.3}$$

ω is the angular frequency.

$$\omega = 2 \cdot \pi \cdot f; \tag{A.4}$$

tanδ dielectric loss of ZnO.

$$tan\delta = 1\omega \cdot C \cdot R; \tag{A.5}$$

Dielectric constant

$$\varepsilon = \frac{C \cdot t}{\varepsilon_0 \cdot A} \tag{A.6}$$

Where: ε_0=8.8x10^{-12} is permittivity of free space, A is the area C is the capacitance and t is the ZnO thickness.

A..7 Track resistance method

Because a new substrate with different properties and topography is used, the measurement of the metal resistance is crucial prior to device fabrication. Substrate properties such as roughness, dielectric loss etc., in fact, greatly contribute to signal transmission line characteristics (track resistance). These transmission characteristics, as we will later see, are measured with electro-acoustic scattering parameters. A method to extract and calculate track resistance of a transmission line experimentally and estimate it theoretically is here overviewed.

Experimental extraction of track resistance from S-parameters

Consider two-port circuit for thru-line as shown in figure A.5.

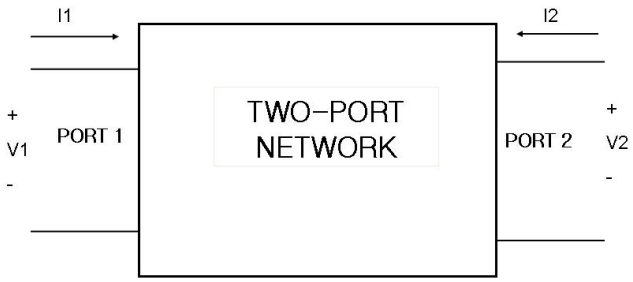


Figure A.5: Two port network representation.

1. Measure S-parameters (transmission loss) of CPW with the VNA.
2. Convert S-parameter to ABCD matrix.

$$\text{ABCD(S,Z}_0\text{)}=\begin{vmatrix} \frac{(1+S_{11})(1-S_{22})+S_{12}\cdot S_{21}}{2\cdot S_{21}} & Z_0\cdot\frac{1+S_{11})(1-S_{22})-S_{12}\cdot S_{21}}{2\cdot S_{21}} \\ \frac{1}{Z_0}\cdot\frac{(1-S_{11})(1-S_{22})-S_{12}\cdot S_{21}}{2\cdot S_{21}} & \frac{(1-S_{11})(1+S_{22})+S_{12}\cdot S_{21}}{2\cdot S_{21}} \end{vmatrix}$$

3. Re-arrange the equations to find B and C matrix parameters

$$\begin{pmatrix} A=cosh\cdot\beta l & B=Z_c sinh\cdot\beta l \\ C=\frac{sinh\beta l}{Z_c} & D=cosh\cdot\beta l \end{pmatrix}$$

   where l is transmission line length (1000μm) and β=propagation constant. If βl is small, then: sinh(βl) $\sim$ βl, cosh(βl)$\sim$ 1

4. Find propagation constant β through equation:

$$\beta=\frac{(2\pi freq)}{(c/(\epsilon^{0.5}))} \tag{A.7}$$

   where c=speed of light, ϵ=dielectric constant of substrate. The lower the dielectric constant the better.

5. Calculate transmission line impedance Z0:

$$Z0=\sqrt{\frac{B}{C}} \tag{A.8}$$

6. Find experimental track resistance from the following equation $\text{R}_{experimental}$= abs(β*Z0) , where Z0 has been extracted from the S-parameters.

The track resistance depends, not only on the S-parameters, but also on the dielectric loss of the substrate through equation A.7.

Theoretical model of track resistance

Frequency-dependent R for a metal slab, including the skin effect, should be :

$$R = \frac{\rho \cdot l}{((2 \cdot (2\rho/(2 \cdot \pi \cdot f \cdot 4\pi \cdot 10^{-7}))^{0.5}) \cdot w} \tag{A.9}$$

Where ρ is resistivity of the metal, l is the length, f is the frequency and w is the track width.

Skin effect

Track resistance tends to increase with frequency as a result of the skin effect. Skin depth, or the distance an alternating current can penetrate beneath the surface of a conductor, tends to decrease at high frequencies (see equation A.10), which means that less current passes through the conductor and, by Ohm's law V=I*R, leading to an increase in conductor resistance.

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \tag{A.10}$$

Track resistance values used

Table A.15: Values used for track resistance calculations of Au on LCP

Length of transmission line (μm)	1000
Thickness of metal slab (μm)	0.1
Width of metal slab (μm)	20
Resistivity Au (Ohm-m)	$2.44*10^{-8}$
Permeability Au (A/m^2)	999960
Permeability of free space(A/m^2)	125660
Speed of light (m/s)	299792458

A..8 Matlab codes

Thermal stress

```
%Importance of TCE mismatch in thin film stresses

%Stress when depositing ZnO - example
Es1=150e9 ;   %Young s modulus of Si
Es2=2.255e9;    %Young s modulus of LCP
Ef=108e9;     %Young s modulus of thin film ZnO
vs1=0.27;    %Poisson's ratio of Si
vs2=0.3;    %Poisson's ratio of LCP (G.Zou 2004)
vf= 0.25;    %Poisson's ratio of thin film ZnO
Ys1=Es1/(1 - vs1);
Ys2=Es2/(1 - vs2);
Yf=Ef/(1-vf);
alpha1=2.5e-6;     %TCE of Si
alpha2=17e-6;    %TCE of LCP
alphaf=30.02e-6; %TCE of ZnO=30.02e-6
tf=1e-6;     %thickness film
ts=500e-6;     %thickness substrate: assume tLCP=tSi
T0=200;  %initial temperature (depends on deposition conditions)
T=20;    %final temperature
R0=183500000;   %this value was taken from experimental measurement of R of Si
R02=1000;

%solve:
strain1=(alphaf - alpha1)* (T-T0)
strain2=(alphaf - alpha2)* (T-T0)

R1=ts / ( 6 * (Yf/Ys1) * (tf/ts)*strain1 ) ;
                        %Si curvature from G. Zou et al 2004
R2= ts / ( 6 * (Yf/Ys2) * (tf/ts) * strain2); %LCP curvature

sigma1=Ys1 * ((1/R1)-(1/R0)) * (ts^2 / tf);
     %Stoney's equation thin film stress caused by substrate
sigma2=Ys2 * ((1/R2)-(1/R0)) * (ts^2 / tf);
```

Rigidity

```
ELCP=2.255e9;
ECu=110e9;
ENi=200e9;
ESi=150e9;
EZnO=108e9;

hLCP=400e-6;
hCu=18e-6;
hNi=100e-6;
hSi=400e-6;
hZnO=1e-6;
```

```
mLCP=1400*2.545e-6;    %(kg/m^3)*(m^3)
mCu=8960*1.145e-7;  %(kg/m^3)*(m^3)
mNi=8902*6.36e-7;    %(kg/m^3)*(m^3)
mSi=2330*2.545e-6;    %(kg/m^3)*(m^3)
mZnO=5700*6.3617e-009;

r=0.045; %m

ILCP=(1/12)*mLCP*(3*(r^2) + (hLCP^2))   %inertia of a solid cylinder
ICu=(1/12)*mCu*(3*(r^2) + (hCu^2))
INi=(1/12)*mNi*(3*(r^2) + (hNi^2))
ISi=(1/12)*mSi*(3*(r^2) + (hSi^2))
IZnO=(1/12)*mZnO*(3*(r^2) + (hZnO^2))


rigidityLCP=ELCP*ILCP
rigidityCu=ECu*ICu
rigidityNi=ENi*INi
rigiditySi=ESi*ISi
rigidityZnO=EZnO*IZnO
```

Stress compensation scheme 1 - Nickel

```
%Ni backing "Stress compensation scheme" for ZnO-coated LCP
%assume 0 initial stress with: LCP/Cu. Therefore treat Cu as a seed layer

alphaCu=17e-6;
alphaNi=13e-6;
alphaZnO=4.3e-6;
alphaLCP=17e-6;
ECu=115e9;
ENi=200e9;
EZnO=108e9;
vNi=0.31;
vCu=0.32;
vZnO=0.35;
NielectrodepStress=-100e6;

Tf=10:5:200; %this is the annealing temperature
T0=10; %this is ambient temperature

for i=1:1:size(Tf,2)
    sigmaZnOLCP(i)=(EZnO/(1 - vZnO) )* (alphaLCP - alphaZnO) * (Tf(i)-T0);
    %consider Ni electrodeposition stress=
            %-100MPa for current density of ~1.4mA/cm^2 J.K.Luo et al(2006)
    sigmaNiLCP(i)=NielectrodepStress+((ENi/(1-vNi))*(alphaLCP-alphaNi)*(Tf(i)-T0));
    sigmaCuLCP(i)=((ECu/(1-vCu))*(alphaLCP-alphaCu)*(Tf(i)-T0));
    sigmatotalBACK(i)=sigmaNiLCP(i)+ sigmaCuLCP(i);
```

```
    stresscomp(i)=sigmaZnOLCP(i)-sigmatotalBACK(i);
end

figure(1)
plot(Tf,sigmaZnOLCP, Tf,sigmatotalBACK, Tf,stresscomp);
legend('ZnO on LCP','Cu-Ni on LCP', 'stress-compensation effect of Ni');
xlabel('Temperature (deg. Celsius)');
ylabel('Stress (Pa)');
title ('Ni backing stress compensation scheme ZnO');
```

Stress compensation scheme 2 - Silicon

```
%Si backing "Stress compensation scheme" for ZnO-coated LCP

alphaCu=17e-6;
alphaSi=3.2e-6;
alphaZnO=4.3e-6;
alphaLCP=17e-6;
ECu=115e9;
ESi=150e9;
EZnO=108e9;
vCu=0.32;
vSi=0.27 ;
vZnO=0.35;

Tf=10:5:300; %this is the annealing temperature
T0=10; %this is ambient temperature

for i=1:1:size(Tf,2)
    sigmaZnOLCP(i)=(EZnO/(1 - vZnO) )* (alphaLCP - alphaZnO) * (Tf(i)-T0);
    sigmaCuLCP(i)=((ECu/(1-vCu))*(alphaLCP-alphaCu)*(Tf(i)-T0));
    sigmaSi(i)=((ESi/(1-vSi))*(alphaLCP-alphaSi)*(Tf(i)-T0));
    sigmatotalBACK(i)=sigmaSi(i)+ sigmaCuLCP(i);
    stresscomp(i)=sigmaZnOLCP(i)-sigmatotalBACK(i);
end

figure(1)
plot(Tf,sigmaZnOLCP,Tf,sigmatotalBACK,Tf,stresscomp);
legend('ZnO on LCP','Si on LCP', 'stress-compensation effect of Si');
xlabel('Temperature (deg. Celsius)');
ylabel('Stress (Pa)');
title ('Si backing stress compensation scheme ZnO');
```

Curvature of multilayer - numerical analysis

```
%wafer bonding validation of measurement LCP/black wax/glass find curvature
%[P. H. Townsend 1987]

%Material properties
```

```
alphaSi=3e-6;
alphaCu=17e-6;
alphaGlassPyrex=3e-6;
alphaLCP=17e-6;
alphaBlackwax=52e-6;

ESi=150e9;
ECu=115e9;
EGlassPyrex=64e9;
ELCP=2.255e9;
EBlackwax=5e9 ;

vSi=0.27;
vCu=0.32;
vGlassPyrex=0.2;
vLCP=0.3;
vBlackwax=0.33;

tSi=500e-6;
tCu=25e-6;
tGlassPyrex=500e-6;
tLCP=100e-6;
tBlackwax=2.7e-6;
t=tGlassPyrex+tBlackwax+tCu+tLCP; %total thickness of composite


ds=0.084 ; %length of the substrate
di=0.084;  %length of the layers

T0=100; %this is the annealing temperature
Tf=20; %this is ambient temperature


%Theoretical prediction of curvature of a composite structure:

%--------------------------------------------------------------------
%SILICON BACKING and BLACK WAX

%Coordinate distance normal to the linear dimension of the composite:
base=0;
ziSi=tSi;  %DISTANCE FROM COMPOSITE BASE TO UPPER SURFACE OF LAYER i
zi0Si=base; %DISTANCE FROM COMPOSITE BASE TO LOWER SURFACE OF LAYER i
zpSi=tSi+tBlackwax ; %DISTANCE FROM COMPOSITE BASE TO UPPER SURFACE OF Black wax LAYER
zp0Si=tSi; %DISTANCE FROM COMPOSITE BASE TO lower SURFACE OF Black wax LAYER
zmSi=tSi+tBlackwax+tCu;%DISTANCE FROM COMPOSITE BASE TO UPPER SURFACE OF Cu LAYER
zm0Si=tSi+tBlackwax;%DISTANCE FROM COMPOSITE BASE TO lower SURFACE OF Cu LAYER
zlSi=tSi+tBlackwax+tCu+tLCP;%DISTANCE FROM COMPOSITE BASE TO UPPER SURFACE OF LCP LAYER
zl0Si=tSi+tBlackwax+tCu;%DISTANCE FROM COMPOSITE BASE TO lower SURFACE OF LCP LAYER

gammaSi=t - (ziSi + zi0Si);
```

```
gammaBlackwax= t - (zpSi + zp0Si);
gammaCu=t - (zmSi + zm0Si);
gammaLCP=t - (zlSi + zl0Si);

%Position of neutral plane:
NSi=(t/2) - ((ESi*gammaSi*(tSi/2)) + (EBlackwax*gammaBlackwax*(tBlackwax/2)) +
      (ECu*gammaCu*(tCu/2))+(ELCP*gammaLCP*(tLCP/2))) / ((EGlassPyrex*tGlassPyrex)+
                                        (EBlackwax*tBlackwax)+(ECu*tCu)+(ELCP*tLCP));

numSi= ((ESi*gammaSi*(tSi/2) * (-alphaSi + (((ESi*tSi*alphaSi)+
       (EBlackwax*tBlackwax*alphaBlackwax)+(ELCP*tLCP*alphaLCP)+(ECu*tCu*alphaCu))
                     /((ESi*tSi)+(EBlackwax*tBlackwax)+(ECu*tCu)+(ELCP*tLCP))))));

numBlackwax= ((EBlackwax*gammaBlackwax*(tBlackwax/2) * (-alphaBlackwax + (((ESi*tSi*
         alphaSi)+(EBlackwax*tBlackwax*alphaBlackwax)+(ECu*tCu*alphaCu)+(ELCP*tLCP*
            alphaLCP))/((ESi*tSi)+(ECu*tCu)+(EBlackwax*tBlackwax)+(ELCP*tLCP))))));

numCu= ((ECu*gammaCu*(tCu/2) * (-alphaCu + (((ECu*tCu*alphaCu)+(EBlackwax*
         tBlackwax*alphaBlackwax)+(ELCP*tLCP*alphaLCP))/((ECu*tCu)+(EBlackwax*
                                                  tBlackwax)+(ELCP*tLCP))))));

numLCP= ((ELCP*gammaLCP*(tLCP/2) * (-alphaLCP + (((ESi*tSi*alphaSi)+(EBlackwax*
        tBlackwax*alphaBlackwax)+(ECu*tCu*alphaCu)+(ELCP*tLCP*alphaLCP))/((ESi*tSi)
                                + (ECu*tCu)+(EBlackwax*tBlackwax)+(ELCP*tLCP))))));


num1=numSi+numBlackwax+numCu+numLCP;

denSi=(ESi*tSi)*  ((((NSi*t)/2 - (t^2)/3)+ (t-NSi)*(gammaSi/2) -
                                          (1/12)*(3*gammaSi^2+tSi^2-t^2)));

denBlackwax=(EBlackwax*tBlackwax)* ((((NSi*t)/2 - (t^2)/3)+ (t-NSi)*
           (gammaBlackwax/2) - (1/12)*(3*gammaBlackwax^2+tBlackwax^2-t^2)));

denCu=(ECu*tCu)*  ((((NSi*t)/2 - (t^2)/3)+ (t-NSi)*(gammaCu/2) -
                                          (1/12)*(3*gammaCu^2+tCu^2-t^2)));

denLCP=(ELCP*tLCP)*((((NSi*t)/2 - (t^2)/3)+ (t-NSi)*(gammaLCP/2) -
                                        (1/12)*(3*gammaLCP^2+tLCP^2-t^2)));

den1=denSi+denBlackwax+denCu+denLCP;

%ELASTIC RELATION FOR COMPOSITE OF MATERIALS WITH
%DIFFERENT ELASTIC MODULI+TCE EFFECT
Ktot1=((Tf-T0) * num1)/(den1)
Rtot1=1/Ktot1


%--------------------------------------------------------------------%
%GLASS and BLACK WAX
```

```
%Coordinate distance normal to the linear dimension of the composite
base=0;
zi=tGlassPyrex;  %DISTANCE FROM COMPOSITE BASE TO UPPER SURFACE OF LAYER i
zi0=base; %DISTANCE FROM COMPOSITE BASE TO LOWER SURFACE OF LAYER i
zp=tGlassPyrex+tBlackwax ; %DISTANCE FROM COMPOSITE BASE TO UPPER SURFACE
                                                        %OF Black wax LAYER
zp0=tGlassPyrex; %DISTANCE FROM COMPOSITE BASE TO lower SURFACE
                                                        %OF Black wax LAYER
zm=tGlassPyrex+tBlackwax+tCu;%DISTANCE FROM COMPOSITE BASE TO UPPER SURFACE
                                                        %OF Cu LAYER
zm0=tGlassPyrex+tBlackwax;%DISTANCE FROM COMPOSITE BASE TO lower SURFACE
                                                        %OF Cu LAYER
zl=tGlassPyrex+tBlackwax+tCu+tLCP;%DISTANCE FROM COMPOSITE BASE TO UPPER SURFACE
                                                        %OF LCP LAYER
zl0=tGlassPyrex+tBlackwax+tCu;%DISTANCE FROM COMPOSITE BASE TO lower SURFACE
                                                        %OF LCP LAYER

gammaGlassPyrex=t - (zi + zi0);
gammaBlackwax= t - (zp + zp0);
gammaCu=t - (zm + zm0);
gammaLCP=t - (zl + zl0);

%Position of neutral plane
N=(t/2) - ((EGlassPyrex*gammaGlassPyrex*(tGlassPyrex/2)) + (EBlackwax*gammaBlackwax*
                 (tBlackwax/2)) + (ECu*gammaCu*(tCu/2))+(ELCP*gammaLCP*(tLCP/2)))/
            ((EGlassPyrex*tGlassPyrex)+(EBlackwax*tBlackwax)+(ECu*tCu)+(ELCP*tLCP));

numGlassPyrex= ((EGlassPyrex*gammaGlassPyrex*(tGlassPyrex/2)*(-alphaGlassPyrex +
                 (((EGlassPyrex*tGlassPyrex*alphaGlassPyrex) +(ECu*tCu*alphaCu)+
                      (EBlackwax*tBlackwax*alphaBlackwax)+(ELCP*tLCP*alphaLCP))/
                   ((EGlassPyrex*tGlassPyrex)+(EBlackwax*tBlackwax)+(ELCP*tLCP)
                                                          +(ECu*tCu))))));

numBlackwax2= ((EBlackwax*gammaBlackwax*(tBlackwax/2) * (-alphaBlackwax +
    (((ESi*tGlassPyrex*alphaGlassPyrex)+(ECu*tCu*alphaCu)+(EBlackwax* tBlackwax
              *alphaBlackwax)+(ELCP*tLCP*alphaLCP))/((EGlassPyrex*tGlassPyrex)
                          +(EBlackwax*tBlackwax)+(ELCP*tLCP)+(ECu*tCu))))));

numCu= ((ECu*gammaCu*(tCu/2) * (-alphaCu + (((ECu*tCu*alphaCu)+(EBlackwax*tBlackwax*
          alphaBlackwax)+(ELCP*tLCP*alphaLCP)) /((EGlassPyrex*tGlassPyrex)+(ECu*tCu)
                                        +(EBlackwax*tBlackwax)+(ELCP*tLCP))))));

numLCP2= ((ELCP*gammaLCP*(tLCP/2) * (-alphaLCP + (((ESi*tGlassPyrex*alphaGlassPyrex)+
       (EBlackwax*tBlackwax*alphaBlackwax)+ (ECu*tCu*alphaCu)+(ELCP*tLCP*alphaLCP))
       /((EGlassPyrex*tGlassPyrex)+(EBlackwax*tBlackwax)+(ELCP*tLCP)+(ECu*tCu))))));

num2=numGlassPyrex+numBlackwax2+numCu+numLCP2;
```

```
denGlassPyrex=(EGlassPyrex*tGlassPyrex)*  ((((N*t)/2 - (t^2)/3)+
    (t-N)*(gammaGlassPyrex/2) - (1/12)*(3*gammaGlassPyrex^2+tGlassPyrex^2-t^2)));

denBlackwax2=(EBlackwax*tBlackwax)*   ((((N*t)/2 - (t^2)/3)+
          (t-N)*(gammaBlackwax/2) - (1/12)*(3*gammaBlackwax^2+tBlackwax^2-t^2)));

denCu=(ECu*tCu)*  ((((N*t)/2 - (t^2)/3)+ (t-N)*(gammaCu/2) -
                                              (1/12)*(3*gammaCu^2+tCu^2-t^2)));

denLCP2=(ELCP*tLCP)*((((N*t)/2 - (t^2)/3)+ (t-N)*(gammaLCP/2) -
                                            (1/12)*(3*gammaLCP^2+tLCP^2-t^2)));

den2=denGlassPyrex+denBlackwax2+denCu+denLCP2;

Ktot2=((Tf-T0) * num2)/(den2);
Rtot2=1/Ktot2;   %radius of curvature
```

K.S.Chen method

```
% Non-linear thin film stress related to substrate deformation
% K.S.Chen et al 2002

ds=100e-6;
df=1e-6;
Ef=108e9;
Es=2.255e9;
vs=0.3;
L=0.045;   %wafer radius
R=0.173 ;  %radius of curvature
T1=100;
T2=25;
alphas=17e-6;
alphaf=30.02e-6;

Kst= (Es * (ds^3))/(3*(1-vs) * L^2 * df^2 * (1+ (ds/df)));
                                                    %conversion factor
Bow=(L^2)/(2*R);  %where L is wafer radius, R is radius of curvature
Bowb=-(3/4) * (Ef/Es) * (df/ds) * (alphas - alphaf)
                                              * (2*L)^2 * (T2-T1);
sigmaf= Bow * ( (Kst * (1 +  ( 1.12 * ((Ef/Es)^(1/5))
                 * ((df/ds)^(1/3)) * ((Bow^2)/((ds+df))^2)))));
stressf= Bowb * Kst * (1 +   1.12* ((Ef/Es)^(1/5))
                     * ((df/ds)^(1/3)) * ((Bow/(ds+df))^(2)));
```

Y.C.Tsui method

```
%Y.C.Tsui et al 1997
%Drawback intrinsic stress is assumed

b=0.045;     %edge length/radius of sample
H=100e-6;    %substrate thickness
w=1e-6;      %layer 1 thickness
Es=2.255e9;
TCE_s=17e-6;
Ed=108e9;
T2=25;        %room temperature (deg C) after deposition of ZnO
T1=100;       %ZnO deposition temperature (degC)
delta1=(w^2 * Ed -H^2*Es) /(2*(w*Ed+H*Es));
                    %distance from neutral axis with layer 1
delta2=((2*w)^2 * Ed - H^2 * Es)/(2*((2*w) *
    Ed +H*Es)); %distance from neutral axis with layer1 and 2

deltan=  ((w^2 * Ed) - (H^2 * Es))/(2*(w*Ed + H* Es));
k1=4.5e-2;    %curvature
k2=0.173;
```

```
k_thermal= (6*Ed*Es*w*H*(w+H)*(TCE_s*(T2-T1)))/(Ed^2 * w^4 +
   4*Ed*Es*w^3*H + 6*Ed*Es*w^2*H^2  +  4*Ed*Es*w*H^3 + Es^2*H^4);
                              %kc-kn=k_thermal  thermal curvature

sigma_q= 2.5e9;    %from S.Kuroda et al. 1995

stiff_total= (b * Ed * w)*((w^2/3)-(w*deltan)+ (deltan^2) ) +
                  (b*Es*H)*((H^2/3) +(H*deltan) + (deltan^2));
                                 %stiffness of composite beam

Fcte=(2 * (k_thermal) * stiff_total)/(w+H);
F1= sigma_q * b* w* ((H*Es)/((H*Es) +(w*Ed)));
          %where sigma_q is the intrinsic or quenching stress
F2=sigma_q*b*w*((H*Es + w*Ed)/(H*Es + 2*w*Ed));

%Total stress on top surface =stress_noCTE + stress_CTEonly
Stress_total_ManyLayer=  (((-Es * F1)/(b*(H*Es + (2-1)*w*Ed)))+
   Es*(k2-k1)*delta1)  -  (Fcte/(b*H))  +  (Es*(k_thermal)*deltan);

Stress_total_TwoLayer=(-F1/(b*H)) +  (Es * k1 * delta1)  -
           ((Es*F2)/(b *(H*Es + w*Ed)))  +  Es* (k2 - k1) * delta2;
            %Stress_total_TwoLayer does not consider thermal stresses

Stress_total_Twolayer_midpoint= (F1/b*w) - (Ed*k1*(w/2  - delta1))-
         ((Ed*F2)/(b*(H*Es + w*Ed)))  -  Ed*(k2-k1) * ((w/2)-delta2) -
                              (Fcte/(b*H))  +  (Es*(k_thermal)*deltan);

Stress_total_Twolayer_midpoint2=(F2/b*w) - Ed*(k2-k1) * ((3*w)/2 - delta2);
```

S.Wagner method

```
%S.Wagner et al 2005

ds=100e-6;
df=1e-6;
Ef=108e9;
Es=2.255e9;
vs=0.3;
vf=0.3;  %from H.K.Yoon et al. 2005
T1=100;
T2=25;
alphas=17e-6;
alphaf=30.02e-6;
% K=0.173;

Es_bi=Es/(1-vs^2);
Ef_bi=Ef/(1-vf^2);

eintrinsic=0.0231; %because= 2.5e9/108e9
```

```
ethermal=(alphas - alphaf) * (T2-T1);
e=eintrinsic+ethermal;

stress_f=(e*Ef_bi) /(1+(Ef_bi*df)/(Es_bi*ds)); %film stress
```

J.I.Han method

```
% J.I. Han 2005

ts=100e-6 ;     %substrate thickness
tf=1e-6;        %layer 1 thickness
Es=2.255e9;
Ef=108e9;
R=1730;

%For two layers
sigmaf=  (Es *ts^2)  / (6*R*tf*(ts+tf))
```

Strain-induced track resistance

```
% Track resistance
Es=2.255e9;
Ef=78e9;
vs=0.3;  %LCP
vf=0.42;  %Au
stress=1e9; % the probe/substrate contact pressure
e=stress/Es;
% e=0.2;

%Importing VNA measured *.S2P files
num=1601;

%Read Files
load Z:\PhD\Experiments\experiments_6_device\S-parameters
   \FBARsample9\FBARsample9n2\8micrombacketch\CopyFBARB2.mdf
load Z:\PhD\Experiments\experiments_6_device\S-parameters
   \CPW-TrackResistance\CPW_standard\CPW_Standard.s2p

%Extract LCP CPW Parameters
freq=CopyFBARB2(:,1);
S11R=CopyFBARB2(:,2);
S11I=CopyFBARB2(:,3);
S21R=CopyFBARB2(:,4);
S21I=CopyFBARB2(:,5);
S12R=CopyFBARB2(:,6);
S12I=CopyFBARB2(:,7);
S22R=CopyFBARB2(:,8);
S22I=CopyFBARB2(:,9);
```

```
%Extract standard CPW Parameters
freqa=CPW_Standard(:,1);
S11Ra=CPW_Standard(:,2);
S11Ia=CPW_Standard(:,3);
S21Ra=CPW_Standard(:,4);
S21Ia=CPW_Standard(:,5);
S12Ra=CPW_Standard(:,6);
S12Ia=CPW_Standard(:,7);
S22Ra=CPW_Standard(:,8);
S22Ia=CPW_Standard(:,9);

%Conversion in dB
%it should be absolute value , not dB (as it is in this case)
S11dB=complex(S11R+S11I);
S21dB=complex(S21R+S21I);
S12dB=complex(S12R+S12I);
S22dB=complex(S22R+S22I);

S11dBa=complex(S11Ra,S11Ia);
S21dBa=complex(S21Ra,S21Ia);
S12dBa=complex(S12Ra,S12Ia);
S22dBa=complex(S22Ra,S22Ia);

%Thru-transmission line
Z0=50; %ohm
l=1*10^-3; %(m) length of TL
mu=1.2566*10^-6;%permeability of free space
t=100*10^-9; %tickness of Ti-Au TL metal
w=20*10^-6;  %width of metal TL
omega=2*pi*freq;  %angular frequency
resistivityAu=2.44*10^-8;
conductivityAu=45210000;
permeabilityAu=0.99996;

%Find Z0 - transmission line impedance
%For LCP
B=50 .* (((1+S11dB).*(1+S22dB)-S12dB
                        .*S21dB)./(2.*S21dB));
C=(1/50).*(((1-S11dB).*(1-S22dB)-S12dB
                        .*S21dB)./(2.*S21dB));
Z0=sqrt(B./C);

%For SiO2
Ba=50 .* (((1+S11dBa).*(1+S22dBa)-S12dBa
                      .*S21dBa)./(2.*S21dBa));
Ca=(1/50).*(((1-S11dBa).*(1-S22dBa)-S12dBa
                      .*S21dBa)./(2.*S21dBa));
Z0a=sqrt(Ba./Ca);
```

```
% A=((1+S11dB).*(1-S22dB)+S12dB.*S21dB)
                                  /(2.*S21dB);
%propagation constant
%for LCP
beta=(2.*pi.*freq)./(299792458/((0.0025)^0.5));
%for Si
betaa=(2.*pi.*freqa)./(299792458/((0.0009)^0.5));

R_experimental=abs(beta.*Z0); %LCP resistance
R_experimentala=abs(betaa.*Z0a); %Si resistance

%Find resistance without strain effect
%for LCP
R0= R_experimental  * (((1-vs)*(1-vf))/ (1+e));
%for Si
R0= R_experimental  * (((1-vs)*(1-vf))/ (1+e));

figure(1)
plot(freq,R_experimental, freqa,R0)
title('Comparison of actual track resistance on LCP')
legend('Measured resistance with pressure-induced strain effect',
            'Resistance without pressure-induced strain effect')
ylabel('Resistance (Ohms)')
xlabel('Frequency (Hz)')
```

FBAR Mason Model - with viscosity term

```
% Translated from Mathcad Mason model
%Carlos 12/11/08, Modified by Ghazal 20/01/09

% Densities
dens_Si=2340;
dens_SiO=3000;
dens_Au=1.93*1e4;
dens_LCP=1400;
dens_ZnO=5700;
dens_Ti=4.5*1e3;

G_LCP=3*1e9 ; %(Pa) complex viscoelastic quantity

% Capacitor dimensions
d1=200*1e-9;    % Top electrode thickness
d2=1*1e-6;      % ZnO thickness
d3=100*1e-9;    % Bottom electrode thickness
wd=200*1e-6;    % Side length of capacitor
d4=0;           % no buffer layer for LCP
d41=0.2*1e-6;
d42=0.5*1e-6;
d43=0.8*1e-6;
d44=1*1e-6;
d45=10*1e-6;

% Acoustic velocities m/s
V_Si=8433;  % Si acoustic velocity now revised
V_SiO=5900;
V_Au=3.21*1e3;
V_LCP=2500;  % LCP acoustic velocity [L. El Fissi]
V_ZnO=6039;
V_Ti=6130;

% Electromechanical coupling coefficients for piezoelectrics
K_eff=0.06;  %for my sample on LCP Ra~50nm K_eff=0.3
k_ZnO=sqrt(K_eff);

% Dielectric Constants
e0=8.854*1e-12;
e_ZnO=8.8;

%Acoustic Attenuation (Np/m) frequency dependent
%(8.7dB/m=1Np/m)
nn=0;
% Work out Qa '1 Hz' attenuation
% Nepers/meter=(20/ln10dB)/meter
Ha_Si=(100*((1*1e9)^nn));
Ha_SiO=(500*((1*1e9)^nn));
```

```
Ha_ZnO=(2148*((1*1e9)^nn));
Ha_Au=(120*((1*1e9)^nn));
Ha_Ti=(500*((1*1e9)^nn));
%viscoelastic materials have higher damping
%and higher acoustic attenuation:
Ha_LCP=(8000*((1*1e9)^nn));

% Capacitance
Cp=((e0*e_ZnO*(wd^2))./d2);

% Acoustic Impedances
Z_SiO=dens_SiO*V_SiO;
Z_Si=dens_Si*V_Si;
Z_LCP=dens_LCP*V_LCP;
Z_Ti=dens_Ti*V_Ti;
Z_Au=dens_Au*V_Au;
Z_ZnO=dens_ZnO*V_ZnO;sqrt(K_eff);

% Range of frequencies in GHz to scan
start_freq=from;
stop_freq=up_to;
points=1601;
sstep=(stop_freq-start_freq)/points;
n=[0:(points-1)];
freq=start_freq+n*sstep;

% Calculate frequency dependent attenuation
%Ha is acoustic attenuation constant
Fqa_SiO=Ha_SiO./((freq*1e9).^nn);
Fqa_Si=Ha_Si./((freq*1e9).^nn);
Fqa_LCP=Ha_LCP./((freq*1e9).^nn);
Fqa_Ti=Ha_Ti./((freq*1e9).^nn);
Fqa_Au=Ha_Au./((freq*1e9).^nn);
Fqa_ZnO=Ha_ZnO./((freq*1e9).^nn);
h_ZnO=(1./(2*Fqa_ZnO));

%FREQUENCY DEPENDENT ATTENUATION
w=2*pi*freq;
Fa_SiO=(w*1e9)./(2*V_SiO*Fqa_SiO);
Fa_Si=(w*1e9)./(2*V_Si*Fqa_Si);
Fa_LCP=(w*1e9)./(2*V_LCP*Fqa_LCP);
Fa_Ti=(w*1e9)./(2*V_Ti*Fqa_Ti);
Fa_Au=(w*1e9)./(2*V_Au*Fqa_Au);
Fa_ZnO=(w*1e9)./(2*V_ZnO*Fqa_ZnO);

% Calculate wavenumber in the different layers at each frequency
k1=w*(1e9/V_Au);
k2=((w*1e9)./(V_ZnO)).*(1-0.5*j*h_ZnO);
k3=w*(1e9/V_Au);       %  Bottom electrode
k4a=w*(1e9/V_SiO);     %  Buffer Layer
```

```
k5a=w*(1e9/V_Si);
k5b=w*(1e9/V_LCP);

%Acoustic impedance from top
Z1=Z_Au.*tanh((Fa_Au+j*k1)*d1);

%silicon
Z5a1=Z_Si.*tanh((Fa_Si+j*k5a)*d41);

Z4a1=Z_SiO.*((Z5a1.*cosh((Fa_SiO+j*k4a)*d41)+Z_SiO.*
   sinh((Fa_SiO+j*k4a)*d41))./(Z_SiO.*cosh((Fa_SiO+j*k4a)
                      *d41)+Z5a1.*sinh((Fa_SiO+j*k4a)*d41)));

%Si SiO2 dependent
Z3a1=Z_Au.*((Z4a1.*cosh((Fa_Au+j*k3)*d3)+Z_Au.*
   sinh((Fa_Au+j*k3)*d3))./(Z_Au.*cosh((Fa_Au+j*k3)*
               d3)+Z4a1.*sinh((Fa_Au+j*k3)*d3)));

%LCP
Z5b1=Z_LCP.*tanh((Fa_LCP+j*k5b)*d41);

%LCP dependent
Z3b1=Z_Au.*((Z5b1.*cosh((Fa_Au+j*k3)*d3)+Z_Au.*
    sinh((Fa_Au+j*k3)*d3))./(Z_Au.*cosh((Fa_Au+j*k3)*
         d3)+Z5b1.*sinh((Fa_Au+j*k3)*d3)));

Y_all_Si1=(Z_ZnO.*(Z1+Z3a1).*(cos((k2.*d2)/2).^2)+(Z_ZnO).^2.*
     sin(k2.*d2)*j)./(Z_ZnO.*(Z1+Z3a1).*cos(k2.*d2)+(((Z_ZnO).^2)+
                                        (Z1.*Z3a1)).*sin(k2.*d2)*j);

Y_all_LCP1=(Z_ZnO.*(Z1+Z3b1).*(cos((k2.*d2)/2).^2)+(Z_ZnO).^2.*
     sin(k2.*d2)*j)./(Z_ZnO.*(Z1+Z3b1).*cos(k2.*d2)+(((Z_ZnO).^2)+
                                        (Z1.*Z3b1)).*sin(k2.*d2)*j);

ke_ZnO=sqrt(((k_ZnO)^2)/(1+(k_ZnO)^2));

Zsys_Si_a1=(-j.*(1-(((((ke_ZnO)^2).*(tan((k2.*d2)./2))
                     ./((k2.*d2)./2)))).*Y_all_Si1))./(w*1e9.*Cp);

Zsys_LCP_b1=(-j.*(1-(((((ke_ZnO)^2).*(tan((k2.*d2)./2))
                 ./((k2.*d2)./2)))).*Y_all_LCP1))./(w*1e9.*Cp);


% Resistances
R1=1.8;          % Electrode Resistance
tand=0.02;
R2=1./(w.*1e9*tand.*Cp); %ZnO resistance
Z_total_Si_a1=R1+((Zsys_Si_a1.*R2)./(R2+Zsys_Si_a1));
Z_total_LCP_b1=R1+((Zsys_LCP_b1.*R2)./(R2+Zsys_LCP_b1));
Z_LCP_viscous1=j * Z_LCP*tan(w*(sqrt(d41 * (dens_LCP/G_LCP))));
```

```
Z_total_LCP1=Z_total_LCP_b1 + Z_LCP_viscous1;
Loss_model_Si1=abs(real(Z_total_Si_a1)./imag(Z_total_Si_a1));
Loss_model_LCP1=abs(real(Z_total_LCP_b1)./imag(Z_total_LCP_b1));

% S-parameters
%mass-loading+viscous effect
S11dB_model_Si1=20*log10(abs(Z_total_Si_a1./(100+Z_total_Si_a1)));
S11dB_model_LCP_b1=20*log10(abs(Z_total_LCP_b1./(100+Z_total_LCP_b1)));
S11dB_model_LCP1=20*log10(abs(Z_total_LCP1./(100+Z_total_LCP1)));

%mass-loading+viscouseffect
S21dB_model_Si1=20*log10(abs((100./(Z_total_Si_a1+100))));
S21dB_model_LCP_b1=20*log10(abs((100./(Z_total_LCP_b1+100))));
S21dB_model_LCP1=20*log10(abs((100./(Z_total_LCP1+100))));
```

FBAR Mason Model -with roughness consideration

```
% Tailored roughness because: roughness of the piezoelectric
% material affects: coupling coefficient and acoustic wave loss.
% Attenuation increases with roughness.
% Energy scattering on surface roughness equation was suggested
% by A.A. Shirakawa et al 2006
% Attenuation=alpha_rough=Ha=247.47 * ((d * f^2)/(dpiezo*Va))

% Densities
dens_Si=2340;
dens_SiO=3000;
dens_Au=1.93*1e4;
dens_LCP=1400; %ref [Rogers corporation]
dens_ZnO=5700; %ref [http://www.mt-berlin.com/frames_cryst
                                    %/descriptions/substrates.htm]
dens_Ti=4.5*1e3;

% Define range of frequencies in GHz to scan over
start_freq=from;
stop_freq=up_to;
points=1601;
sstep=(stop_freq-start_freq)/points;
n=[0:(points-1)];
freq=start_freq+n*sstep;

% Capacitor dimensions
d1=100*1e-9;    % Top electrode thickness
d2=1*1e-6;      % ZnO thickness
d3=100*1e-9;    % Bottom electrode thickness
wd=200*1e-6;    % Side length of capacitor
d4=0.2*1e-6;    %Si case
d5=0.2*1e-6;    % LCP case
```

```
% Acoustic velocities
V_Si=8433;  % Si acoustic velocity
V_SiO=5900;
V_Pt=3.26*1e3;
V_Au=3.21*1e3;
V_LCP=2500;
% V_LCP=5000% LCP acoustic velocity [L. El Fissi]
V_ZnO=6039 ; %m/s
V_Ti=6130;

%Surface roughnesses (as measured)
RaSi=0.045 * 1e-9;
RaLCP=50 * 1e-9;
RaZnOa=8 *  1e-9;  %roughness of ZnO on Si
RaZnOb=200 * 1e-9;

% Electromechanical coupling coefficients for piezoelectrics
K_eff=0.06;  %for my sample on LCP Ra~50nm K_eff=0.3
k_ZnO=sqrt(K_eff);

% Dielectric Constants
e0=8.854*1e-12;
e_ZnO=8.8;

%Acoustic Attenuation (Np/m) frequency dependent so estimate
%(8.7dB/m=1Np/m)
nn=0;
%Material-dependent acoustic attenuation
Ha_Si_ac=(100*((1*1e9)^nn));
Ha_SiO_ac=(500*((1*1e9)^nn));
Ha_LCP_ac=(8000*((1*1e9)^nn));
Ha_ZnO_ac=(2148*((1*1e9)^nn));  %Cranfield
Ha_Au_ac=(120*((1*1e9)^nn));
Ha_Ti_ac=(500*((1*1e9)^nn));

%Roughness-dependent acoustic attenuation
Ha_Si_ra=247.47 .* ((RaSi .* freq.^2)/(d2 .* V_Si))  ;
Ha_LCP_ra=247.47 .* ((RaLCP .* freq.^2)/(d2 .* V_LCP));
Ha_ZnOa_ra=247.47 .* ((RaZnOa .* freq.^2)/(d2 .* V_ZnO));   %Silicon
Ha_ZnOb_ra= 247.47 .* ((RaZnOb .* freq.^2)/(d2 .* V_ZnO));  %LCP


%Total acoustic attenuation: Roughness-dependent + Material-dependent
Ha_Si=Ha_Si_ac+Ha_Si_ra;
Ha_SiO=Ha_SiO_ac;
Ha_LCP=Ha_LCP_ac+Ha_LCP_ra;
Ha_ZnOa=Ha_ZnO_ac+Ha_ZnOa_ra;      %Silicon
Ha_ZnOb=Ha_ZnO_ac+Ha_ZnOb_ra;       %LCP
Ha_Au=Ha_Au_ac;
Ha_Ti=Ha_Ti_ac;
```

```
% Capacitances
Cp=((e0*e_ZnO*(wd^2))/d2);

% Acoustic Impedances
Z_SiO=dens_SiO*V_SiO;
Z_Si=dens_Si*V_Si;
Z_LCP=dens_LCP*V_LCP;   %Z in viscoelastic materials is low
Z_Ti=dens_Ti*V_Ti;
Z_Au=dens_Au*V_Au;
Z_ZnO=dens_ZnO*V_ZnO;sqrt(K_eff);

% Calculate frequency dependent attenuation
w=2*pi*freq;

Fqa_SiO=Ha_SiO./((freq*1e9).^nn);  %Ha is material acoustic attenuation constant
Fqa_Si=Ha_Si./((freq*1e9).^nn);
Fqa_LCP=Ha_LCP./((freq*1e9).^nn);
Fqa_Ti=Ha_Ti./((freq*1e9).^nn);
Fqa_Au=Ha_Au./((freq*1e9).^nn);
Fqa_ZnOa=Ha_ZnOa./((freq*1e9).^nn);
Fqa_ZnOb=Ha_ZnOb./((freq*1e9).^nn);

%FREQUENCY DEPENDENT ATTENUATION
Fa_SiO=(w*1e9)./(2*V_SiO*Fqa_SiO);
Fa_Si=(w*1e9)./(2*V_Si*Fqa_Si);
Fa_LCP=(w*1e9)./(2*V_LCP*Fqa_LCP);
Fa_Ti=(w*1e9)./(2*V_Ti*Fqa_Ti);
Fa_Au=(w*1e9)./(2*V_Au*Fqa_Au);
Fa_ZnOa=(w*1e9)./(2*V_ZnO*Fqa_ZnOa);
Fa_ZnOb=(w*1e9)./(2*V_ZnO*Fqa_ZnOb);

h_ZnOa=(1./(2*Fqa_ZnOa));
h_ZnOb=(1./(2*Fqa_ZnOb));

% Calculate wavenumber k in the different layers at each frequency
k1=w*(1e9/V_Au);
k2a=((w*1e9)./(V_ZnO)).*(1-0.5*j*h_ZnOa);    %ZnO on Si
k2b=((w*1e9)./(V_ZnO)).*(1-0.5*j*h_ZnOb);    %ZnO on LCP
k3=w*(1e9/V_Au);     %Bottom electrode
k4a=w*(1e9/V_SiO);   %Membrane Layer
k5a=w*(1e9/V_Si);
k5b=w*(1e9/V_LCP);

%Acoustic impedance from top
Z1=Z_Au.*tanh((Fa_Au+j*k1)*d1);

%Acoustic impedance from bottom

 %silicon
```

```
Z5a=Z_Si.*tanh((Fa_Si+j*k5a)*d5);

Z4a=Z_SiO.*((Z5a.*cosh((Fa_SiO+j*k4a)*d4)+Z_SiO.*
      sinh((Fa_SiO+j*k4a)*d4))./(Z_SiO.*cosh((Fa_SiO+j*k4a)*
                              d4)+Z5a.*sinh((Fa_SiO+j*k4a)*d4)));

%Si SiO2 dependent
Z3a=Z_Au.*((Z4a.*cosh((Fa_Au+j*k3)*d3)+Z_Au.*
      sinh((Fa_Au+j*k3)*d3))./(Z_Au.*cosh((Fa_Au+j*k3)*
                              d3)+Z4a.*sinh((Fa_Au+j*k3)*d3)));

%LCP
Z5b=Z_LCP.*tanh((Fa_LCP+j*k5b)*d5);

%LCP dependent
Z3b=Z_Au.*((Z5b.*cosh((Fa_Au+j*k3)*d3)+Z_Au.*
      sinh((Fa_Au+j*k3)*d3))./(Z_Au.*cosh((Fa_Au+j*k3)*
           d3)+Z5b.*sinh((Fa_Au+j*k3)*d3)));

%Admittances
Y_all_Si=(Z_ZnO.*(Z1+Z3a).*(cos((k2a.*d2)/2).^2)+(Z_ZnO).^2.*
       sin(k2a.*d2)*j)./(Z_ZnO.*(Z1+Z3a).*cos(k2a.*d2)+(((Z_ZnO).^2)
                                          +(Z1.*Z3a)).*sin(k2a.*d2)*j);

Y_all_LCP=(Z_ZnO.*(Z1+Z3b).*(cos((k2b.*d2)/2).^2)+(Z_ZnO).^2.*
       sin(k2b.*d2)*j)./(Z_ZnO.*(Z1+Z3b).*cos(k2b.*d2)+(((Z_ZnO).^2)
                                          +(Z1.*Z3b)).*sin(k2b.*d2)*j);

ke_ZnO=sqrt(((k_ZnO)^2)/(1+(k_ZnO)^2));

%Total impedance
Zsys_Si_a=(-j*(1-(((((ke_ZnO).^2).*(tan((k2a.*d2)/2))
                           .//((k2a.*d2)/2)))).*Y_all_Si))./(w*1e9*Cp);

Zsys_LCP_b=(-j*(1-(((((ke_ZnO).^2).*(tan((k2b.*d2)/2))
                          .//((k2b.*d2)/2)))).*Y_all_LCP))./(w*1e9*Cp);

% Resistances
R1=1.8;             % Electrode Resistance
tand=0.02;
R2=1./(w.*1e9*tand*Cp); %ZnO resistance
Z_total_Si_a=R1+((Zsys_Si_a.*R2)./(R2+Zsys_Si_a));
Z_total_LCP_b=R1+((Zsys_LCP_b.*R2)./(R2+Zsys_LCP_b));

Loss_model_Si=abs(real(Z_total_Si_a)./imag(Z_total_Si_a));
Loss_model_LCP=abs(real(Z_total_LCP_b)./imag(Z_total_LCP_b));

% S-parameters
S11dB_model_Si=20*log10(abs(Z_total_Si_a./(100+Z_total_Si_a)));
S11dB_model_LCP=20*log10(abs(Z_total_LCP_b./(100+Z_total_LCP_b)));
```

```
S21dB_model_Si=20*log10(abs((100./(Z_total_Si_a+100))));
S21dB_model_LCP=20*log10(abs((100./(Z_total_LCP_b+100))));
```

FBAR Mason Model Ladder filter- with viscosity term

```
%FBAR Ladder filter model from Qingxin Su 2000
% Translated from Mathcad Mason model

% Densities
dens_Si=2340;
dens_SiO=3000;
dens_Au=1.93*1e4;
dens_LCP=1400;
dens_ZnO=5700;
dens_Ti=4.5*1e3;

G_LCP=3*1e9 ; %(Pa) complex viscoelastic quantity

% Define range of frequencies in GHz to scan over
start_freq=from;
stop_freq=up_to;
points=1601;
sstep=(stop_freq-start_freq)/points;
n=[0:(points-1)];
freq=start_freq+n*sstep;

% Capacitor dimensions
d1=100*1e-9;    % Top electrode thickness for series FBARs
d1p=120*1e-9;   % Top electrode thickness for parallel FBARs
d2=1*1e-6;      % ZnO thickness
d3=100*1e-9;    % Bottom electrode thickness
wd1=80*1e-6;    % Side length of capacitors
wd2=200*1e-6;
wd3=60*1e-6;
d4=0.2*1e-6;    %Si case
d5=0.2*1e-6;    % LCP case

% Acoustic velocities
V_Si=8433;
V_SiO=5900;
V_Au=3.21*1e3;
V_LCP=2500;  % LCP acoustic velocity [L. El Fissi]
V_ZnO=6039 ; %m/s
V_Ti=6130;

%Surface roughnesses (as measured)
RaSi=0.045 * 1e-9;
RaLCP=50 * 1e-9;
```

```
RaZnOa=8 *  1e-9;  %roughness of ZnO on Si
RaZnOb=200 * 1e-9;

% Electromechanical coupling coefficients for piezoelectrics
K_eff=0.06;  %for my sample on LCP Ra~50nm K_eff=0.3
k_ZnO=sqrt(K_eff);

% Dielectric Constants
e0=8.854*1e-12;
e_ZnO=8.8;

%Acoustic Attenuation (Np/m) frequency dependent
% so estimate (8.7dB/m=1Np/m)
nn=0;
%Material-dependent acoustic attenuation
Ha_Si_ac=(100*((1*1e9)^nn));
Ha_SiO_ac=(500*((1*1e9)^nn));
Ha_LCP_ac=(8000*((1*1e9)^nn));
Ha_ZnO_ac=(2148*((1*1e9)^nn));
Ha_Au_ac=(120*((1*1e9)^nn));
Ha_Ti_ac=(500*((1*1e9)^nn));

%Roughness-dependent acoustic attenuation
Ha_Si_ra=247.47 .* ((RaSi .* freq.^2)/(d2 .* V_Si))  ;
Ha_LCP_ra=247.47 .* ((RaLCP .* freq.^2)/(d2 .* V_LCP));
Ha_ZnOa_ra=247.47 .* ((RaZnOa .* freq.^2)/(d2 .* V_ZnO));  %Silicon
Ha_ZnOb_ra= 247.47 .* ((RaZnOb .* freq.^2)/(d2 .* V_ZnO)); %LCP

%Total acoustic attenuation: Roughness-dependent + Material-dependent
Ha_Si=Ha_Si_ac+Ha_Si_ra;
Ha_SiO=Ha_SiO_ac;
Ha_LCP=Ha_LCP_ac+Ha_LCP_ra;
Ha_ZnOa=Ha_ZnO_ac+Ha_ZnOa_ra;  %Silicon
Ha_ZnOb=Ha_ZnO_ac+Ha_ZnOb_ra;  %LCP
Ha_Au=Ha_Au_ac;
Ha_Ti=Ha_Ti_ac;

% Capacitances
Cs=((e0*e_ZnO)*(wd1^2))/d1;
Cp=((e0*e_ZnO*(wd2*wd3))/d2);

% Acoustic Impedances
Z_SiO=dens_SiO*V_SiO;
Z_Si=dens_Si*V_Si;
Z_LCP=dens_LCP*V_LCP;
Z_Ti=dens_Ti*V_Ti;
Z_Au=dens_Au*V_Au;
Z_ZnO=dens_ZnO*V_ZnO;sqrt(K_eff);

% Calculate frequency dependent attenuation
```

```
%Ha is material acoustic attenuation constant
w=2*pi*freq;
Fqa_SiO=Ha_SiO./((freq*1e9).^nn);
Fqa_Si=Ha_Si./((freq*1e9).^nn);
Fqa_LCP=Ha_LCP./((freq*1e9).^nn);
Fqa_Ti=Ha_Ti./((freq*1e9).^nn);
Fqa_Au=Ha_Au./((freq*1e9).^nn);
Fqa_ZnOa=Ha_ZnOa./((freq*1e9).^nn);
Fqa_ZnOb=Ha_ZnOb./((freq*1e9).^nn);

%FREQUENCY DEPENDANT ATTENUATION
Fa_SiO=(w*1e9)./(2*V_SiO*Fqa_SiO);
Fa_Si=(w*1e9)./(2*V_Si*Fqa_Si);
Fa_LCP=(w*1e9)./(2*V_LCP*Fqa_LCP);
Fa_Ti=(w*1e9)./(2*V_Ti*Fqa_Ti);
Fa_Au=(w*1e9)./(2*V_Au*Fqa_Au);
Fa_ZnOa=(w*1e9)./(2*V_ZnO*Fqa_ZnOa);
Fa_ZnOb=(w*1e9)./(2*V_ZnO*Fqa_ZnOb);

h_ZnOa=(1./(2*Fqa_ZnOa));
h_ZnOb=(1./(2*Fqa_ZnOb));

% Calculate wavenumber in the different layers at each frequency
k1=w*(1e9/V_Au);
k2a=((w*1e9)./(V_ZnO)).*(1-0.5*j*h_ZnOa);    %ZnO on Si
k2b=((w*1e9)./(V_ZnO)).*(1-0.5*j*h_ZnOb);    %ZnO on LCP
k3=w*(1e9/V_Au);    % Bottom electrode
k4a=w*(1e9/V_SiO);  % Membrane Layer
k5a=w*(1e9/V_Si);
k5b=w*(1e9/V_LCP);

%Acoustic impedance from top
Z1=Z_Au.*tanh((Fa_Au+j*k1)*d1);
Z1p=Z_Au.*tanh((Fa_Au+j*k1)*d1p);

%Acoustic impedance from bottom
%silicon
Z5a=Z_Si.*tanh((Fa_Si+j*k5a)*d5);

Z4a=Z_SiO.*((Z5a.*cosh((Fa_SiO+j*k4a)*d4)+Z_SiO.*sinh
             ((Fa_SiO+j*k4a)*d4))./(Z_SiO.*cosh((Fa_SiO+j*k4a)*d4)
                                    +Z5a.*sinh((Fa_SiO+j*k4a)*d4)));

%Si SiO2 dependent
Z3a=Z_Au.*((Z4a.*cosh((Fa_Au+j*k3)*d3)+Z_Au.*sinh((Fa_Au+j*k3)*d3))./
               (Z_Au.*cosh((Fa_Au+j*k3)*d3)+Z4a.*sinh((Fa_Au+j*k3)*d3)));

%LCP
Z5b=Z_LCP.*tanh((Fa_LCP+j*k5b)*d5);
```

```
%LCP dependent
Z3b=Z_Au.*((Z5b.*cosh((Fa_Au+j*k3)*d3)+Z_Au.*sinh
                        ((Fa_Au+j*k3)*d3))./(Z_Au.*cosh((Fa_Au+j*k3)*d3)
                                +Z5b.*sinh((Fa_Au+j*k3)*d3)));

ke_ZnO=sqrt(((k_ZnO)^2)/(1+(k_ZnO)^2));

% Resistances
sigma=0.02 ; %(ohm m)^-1 , conductivity ZnO thin film
alpha=0.002;
R1altern=(((pi./2).^2 .*alpha)./(ke_ZnO.^2.*2.*pi.*10^9.*Cs))+0.5;
R1=1.8;             % Electrode Resistance
R2=1.5*1e6;
tand=0.02;
R2altern=(((pi./2).^2 .*alpha)./(ke_ZnO.^2.*2.*pi.*10^9.*Cp))
                                              + 0.5;  %ZnO resistance
R1p=d2/(sigma.*wd1^2);
R2p=d2/(sigma*wd2*wd3);

%series FBAR
Y_all_Si=(Z_ZnO.*(Z1+Z3a).*(cos((k2a.*d2)/2).^2)+(Z_ZnO).^2.*sin
                           (k2a.*d2)*j)./(Z_ZnO.*(Z1+Z3a).*cos(k2a.*d2)
                              +(((Z_ZnO).^2)+(Z1.*Z3a)).*sin(k2a.*d2)*j);

Y_all_LCP=(Z_ZnO.*(Z1+Z3b).*(cos((k2b.*d2)/2).^2)+(Z_ZnO).^2.*sin
                            (k2b.*d2)*j)./(Z_ZnO.*(Z1+Z3b).*cos(k2b.*d2)
                              +(((Z_ZnO).^2)+(Z1.*Z3b)).*sin(k2b.*d2)*j);


Zsys_Si_a=(-j*(1-(((((ke_ZnO).^2).*(tan((k2a.*d2)./2))
                                ./((k2a.*d2)/2)))).*Y_all_Si))./(w*1e9*Cp);

Zsys_LCP_b=(-j*(1-(((((ke_ZnO).^2).*(tan((k2b.*d2)./2))
                                ./((k2b.*d2)/2)))).*Y_all_LCP))./(w*1e9*Cp);

Zs_Si_s=((Zsys_Si_a .*R1p)./(Zsys_Si_a+R1p))+R1altern;
Zs_LCP_s=((Zsys_LCP_b .*R1p)./(Zsys_LCP_b+R1p))+R1altern;

%Viscous model for series
Z_LCP_viscous=j * Z_LCP*tan(w*(sqrt(d4 * (dens_LCP/G_LCP))));
Z_total_LCP_viscous_s=Zs_LCP_s + Z_LCP_viscous;

%parallel FBAR
Y_all_Sip=(Z_ZnO.*(Z1p+Z3a).*(cos((k2a.*d2)/2).^2)+(Z_ZnO).^2.*sin
                           (k2a.*d2)*j)./(Z_ZnO.*(Z1p+Z3a).*cos(k2a.*d2)
                              +(((Z_ZnO).^2)+(Z1p.*Z3a)).*sin(k2a.*d2)*j);

Y_all_LCPp=(Z_ZnO.*(Z1p+Z3b).*(cos((k2b.*d2)/2).^2)+(Z_ZnO).^2.*sin
                            (k2b.*d2)*j)./(Z_ZnO.*(Z1p+Z3b).*cos(k2b.*d2)
                              +(((Z_ZnO).^2)+(Z1p.*Z3b)).*sin(k2b.*d2)*j);
```

```
Zsys_Si_ap=(-j*(1-(((((ke_ZnO).^2).*(tan((k2a.*d2)./2))
                                ./((k2a.*d2)/2)))).*Y_all_Sip))./(w*1e9*Cp);

Zsys_LCP_bp=(-j*(1-(((((ke_ZnO).^2).*(tan((k2b.*d2)./2))
                                ./((k2b.*d2)/2)))).*Y_all_LCPp))./(w*1e9*Cp);

Zp_Si_p=((Zsys_Si_ap .*R2p)./(Zsys_Si_ap+R2p))+R2altern;
Zp_LCP_p=((Zsys_LCP_bp .*R2p)./(Zsys_LCP_bp+R2p))+R2altern;

%Viscous for parallel
Z_total_LCP_viscous_p=Zp_LCP_p + Z_LCP_viscous;

%FINAL SERIES FBAR
Z_total_Si_a=R1+((Zsys_Si_a.*R2)./(R2+Zsys_Si_a));
Z_total_LCP_b=R1+((Zsys_LCP_b.*R2)./(R2+Zsys_LCP_b)); %With viscous effect
Loss_model_Si=abs(real(Z_total_Si_a)./imag(Z_total_Si_a));
Loss_model_LCP=abs(real(Z_total_LCP_viscous_p)./imag(Z_total_LCP_viscous_p));

%FINAL PARALLEL FBAR
Z_total_Si_ap=R1+((Zsys_Si_ap.*R2)./(R2+Zsys_Si_ap));
Z_total_LCP_bp=R1+((Zsys_LCP_bp.*R2)./(R2+Zsys_LCP_bp));
Loss_model_Sip=abs(real(Z_total_Si_ap)./imag(Z_total_Si_ap));
Loss_model_LCPp=abs(real(Z_total_LCP_bp)./imag(Z_total_LCP_bp));

%Ladder FBAR
%From H.J.Zhao et al. 2002
% S-parameters series
S11dB_model_Si=20*log10(abs(Z_total_Si_a./(100+Z_total_Si_a)));
S11dB_model_LCP=20*log10(abs(Z_total_LCP_viscous_s./(100+Z_total_LCP_viscous_s)));
                                                        %With viscous effect
S21dB_model_Si=20*log10(abs((100./(Z_total_Si_a+100))));
S21dB_model_LCP=20*log10(abs((100./(Z_total_LCP_viscous_s+100))));
                                                        %With viscous effect

% S-parameters parallel
S11dB_model_Sip=20*log10(abs(Z_total_Si_ap./(100+Z_total_Si_ap)));
S11dB_model_LCPp=20*log10(abs(Z_total_LCP_viscous_p./(100+Z_total_LCP_viscous_p)));
S21dB_model_Sip=20*log10(abs((100./(Z_total_Si_ap+100))));
S21dB_model_LCPp=20*log10(abs((100./(Z_total_LCP_viscous_p+100))));

%Ladder filter
%Silicon
for a=1:1601
A_Si=[1,Zs_Si_s(a);0,1];
B_Si=[1,0;(1./Zp_Si_p(a)),1];
C_Si=[1,(-i./(2*pi*freq(a)*10^9*Cs));0,1];

M_Si=A_Si* B_Si *C_Si *A_Si *B_Si;
```

```
M_Si1=M_Si(1,1);
M_Si2=M_Si(1,2);
M_Si3=M_Si(2,1);
M_Si4=M_Si(2,2);
S2_Si=100./((50 .* M_Si1) + (M_Si2)  +(M_Si3 .*50^2) + 50.*(M_Si4));
S21_Si=20*log10(abs(S2_Si));
SA21_Si=20*log10(abs(S21_Si));
S21_SiC(a)=S21_Si;
SA21_SiC(a)=SA21_Si;
end

%LCP
for a=1:1601
A_LCP=[1,Z_total_LCP_viscous_s(a);0,1];
B_LCP=[1,0;(1./Z_total_LCP_viscous_p(a)),1];
C_LCP=[1,(-i./(2*pi*freq(a)*10^9*Cs));0,1];

M_LCP=A_LCP* B_LCP *C_LCP *A_LCP *B_LCP;

M_LCP1=M_LCP(1,1);
M_LCP2=M_LCP(1,2);
M_LCP3=M_LCP(2,1);
M_LCP4=M_LCP(2,2);
S2_LCP=100./((50 .* M_LCP1) + (M_LCP2)  +(M_LCP3 .*50^2) + 50.*(M_LCP4));
S21_LCP=20*log10(abs(S2_LCP));
SA21_LCP=20*log10(abs(S21_LCP));
S21_LCPC(a)=S21_LCP;
SA21_LCPC(a)=SA21_LCP;
end
```

A..9 Stress compensation scheme

Thin film stresses causing to substrate curling can be counteracted so that the manhandling and/or high temperature effects during the fabrication stage are minimised. We have seen that through an appropriate backing the substrate's tendency to deform can be counteracted. This step is essential as substrate bowing can cause both fabrication and material reliability (i.e. ZnO cracking) issues. Hence the stress compensation scheme suggested, based on the previously employed backing methods, is here analysed more in depth.

Stress compensation scheme is based on balancing the stresses on the front of wafer through backing and introducing stresses at the back of the wafer. Crawford [49] already proposed a stress compensation scheme whereby an additional layer with appropriate Young's modulus is deposited on the opposite side of the polymer substrate.

In this study, multilayer rigidity and thermal mismatches are the most important parameters. From table 4.1 in section 4.3.1 we can see that the stiffest combination is provided by the LCP/Cu/Si combination with a rigidity of $5.1152e^5$ GPaKg/m^2. However, in our stress compensation scheme, we simply consider the thermal effect on ZnO/LCP interfacial stresses, which can cause cracking of the ceramic, and how these are relieved through appropriate backing during processing. Through a stress analysis we will study how a backing wafer (Si) or electroplated metal (Ni) can increase the rigidity of the multilayer making it resistant against bowing.

To assess the stress compensation scheme we used the thermal equation 2.43 from section 2.6.3 for calculating front stresses caused by Au and ZnO and back stresses caused by the backing, and the stress compensation overall effect (see figure A.6) given various ZnO deposition temperatures.

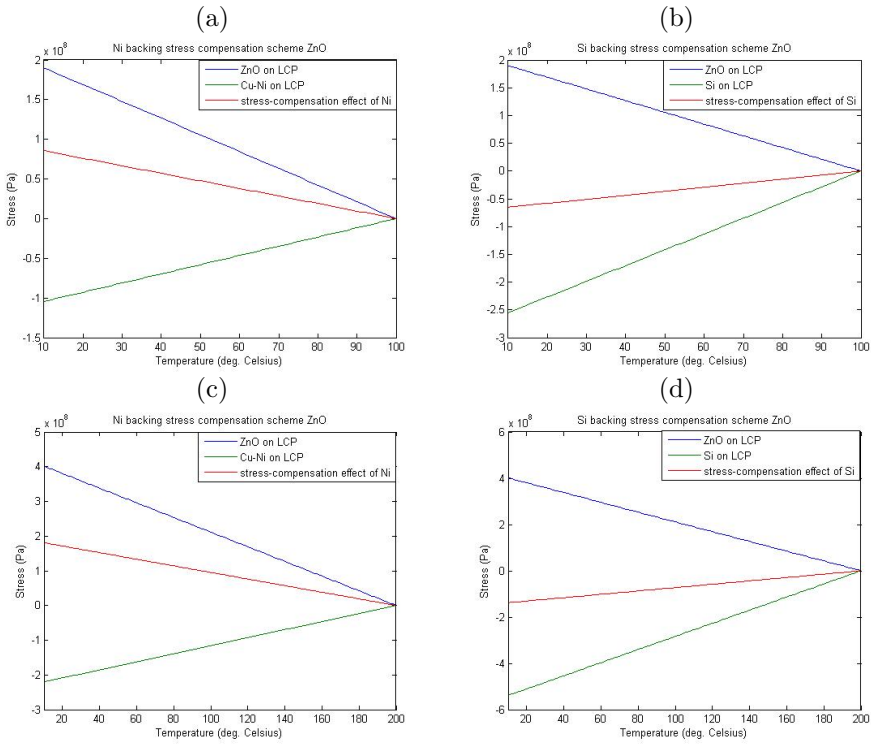


Figure A.6: Stress compensation scheme of ZnO growth at a)100°C with Ni backing , b)100°C with Si backing, c)200°C with Ni backing, d)200°C with Si backing.

For a ZnO processing temperature of 100°C the compensation scheme shows that the thermal effect of the combination yields compressive stress on ZnO film once it cools down for Si and tensile for the Ni backing case (see figures A.6 a) and b)). This is because the compressive stress provided by the backing is higher for the Si case, therefore balancing the front ZnO stress more. The overall compressive stress for the Si backing case is smaller in magnitude (-65MPa) than the overall tensile stress in the Ni backing case (86MPa).

For a ZnO processing temperature of 200°C the compensation scheme we see again that the higher compressive stress value provided by the silicon backing translates into an overall stress of ZnO of the compressive kind, while for the Ni backing this is tensile (see figures A.6 c) and d)). The magnitude of the ZnO stresses is higher in the Ni-backed case (179MPa) than in the Si case (-136MPa).

From the results shown in figure A.6, we can conclude that Si is a better backing substrate than Ni (even when thickness is not considered) since the thermal stresses generated on the ZnO film are smaller for Si-backing than for Ni backing. Another drawback of using Ni is the smaller electroplated material thickness (max. 100μm) than that of the thicker silicon wafer (500μm), leading to less substrate rigidity and, therefore, more proneness to curling.

A..10 Heat transfer considerations: conduction theory and heat sink principle

An issue to consider is heat transfer which can affect the fabrication in various stages such as: the photolithographic and material growth. Processing, which encompasses photolithography and material deposition, requires relatively temperatures up to at least 100°C. The concern arises as LCP is a thermal insulator and, therefore, has very low conductivity compared to silicon (see table A.16). Due to the lower heat flux and thermal conductivity, thermal conduction through LCP (insulator) is less than through silicon substrate. This could consequently affect processes of sputtering and photolithography, where after photoresist spinning, the sample is placed on a hotplate for baking.

Although we have not had any major problems in adapting traditional processing methods to LCP for MEMS production, an in-depth knowledge of the heat transfer process during photolithography can give us reassurance and insight. Some stages might need to be tailored in the future to suit the particular LCP case. These stages are primarily any of those which require the bottom of our samples to be in touch with a hot surface (i.e. photolithography) or when sample is inside a heated vacuum chamber (i.e. ZnO sputtering). Thermal consideration is important for both functional material grain growth and photolithographic processes.

Substrate thicknesses and heat conduction parameters affect the photoresist curing and grain growth. The heating and cooling ratse of ZnO on LCP is higher than on silicon and the phenomenon can be explained through the thermal conduction theory and heat sink principle: the thickness of LCP/Cu/Si sample being larger than that of the standard sample, and the overall thermal conductivity of LCP/Cu/Si being greater than Si alone. I have considered the substrate to be a heat sink and applied the heat dissipation principle. A heat sink is an object (substrate) with high conductivity, which uses thermal contact to absorb and dissipate heat from another object (i.e. grown ZnO). The heat conduction principle is based on the equation A.11:

$$H = \frac{\Delta Q}{\Delta T} = k \cdot A \cdot \frac{\Delta T}{x} \tag{A.11}$$

Where $\frac{\Delta Q}{\Delta T}$is the rate of heat flow, k is the thermal conductivity, A is the total cross sectional area of conducting surface, ΔT is temperature difference and x is the thickness of conducting surface Cengel and Boles [33]. Thermal conductivity is directly proportional to heat conduction, meaning that a high k will lead to a higher rate of heat flow. On the other hand, the thickness of the substrate slows down the rate of heat flow. Using equation A.11 we get the heat conduction values in table A.16. Note that for these analyses the adhesive was not considered as an essential contributor to heat dissipation (this layer is very thin 1-3μm).

Table A.16: List of material properties

Substrate	**Thermal conductivity(k)** $(\frac{\mathbf{W}}{\mathbf{cm°C}})$	**Substrate thickness** $(\mu\mathbf{m})$	**Area of substrate** $(\mathbf{m^2})$	**ΔT** $(°\mathbf{C})$	**Heat conduction (H)(J/s)**
LCP	0.002	50	0.008	57	18.5
Cu	4.01	25	0.008	57	74123.6
LCP/Cu	4.21	75	0.008	57	24720.2
Silicon	1.3	400	0.008	57	1502
LCP/Si	1.5	450	0.008	57	1337
LCP/Cu/Si	5.51	475	0.008	57	5168

For LCP/Si only (ULTRALAM3800) the heat conduction is less than on standard silicon, therefore the need higher temperatures or longer times for fabrication purposes might arise: photolith, ZnO deposition etc. This can explain why bad photolithography might have occurred (i.e. bad bilayer features in section 5.5) and can be solved through an increase in curing times. However, the LCP-Cu (ULTRALAM3850) on Si has a higher heat conduction than standard Si. Thermal conductivity of LCP in series (added to) Cu and Si allows faster heat dissipation, higher cooling rates and smaller ZnO grain sizes, and this is due to the Cu metal having a very high heat conduction, which is a characteristic of metals. This high heat dissipation rate in ULTRALAM3850 can explain the good ZnO grain sizes on LCP since, to attain small-grained crystals, a rapid cool-down is needed.

Furthermore it is important to compare the heat conduction differences, within a same sample, due to the patterned mask (whether it is Cu or Si mask). The difference in heat conduction through a sample can cause issues on the top features in the photolithographic process for example. We will consider both bare LCP with back Cu metal mask as an example to compare the heat flux (heat Flux=heat conduction/area) on the area with and the one without Cu backing. The following simulations carried out with ANSYS transient thermal analysis consider: 25μm Cu, 100μm LCP, temperature 100°C.

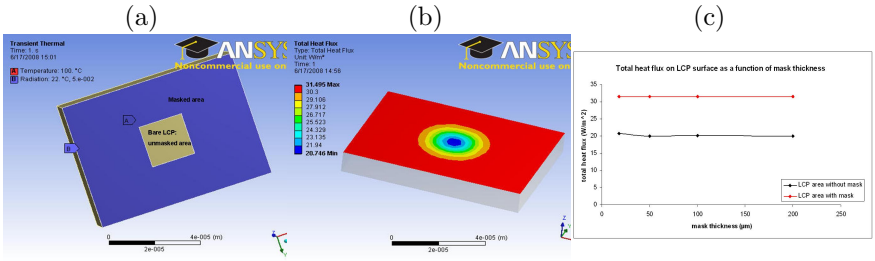


Figure A.7: ANSYS simulations: a) initial conditions, b) total heat flux result, c) heat flux as a function of mask thickness.

As evident from figure A.7, the heat flux to the top of the sample is greater in

the areas where the mask ($31.495 W/m^2$) is present at the back thanks to the added conductivity the mask provides compared to the front area that does not have a mask at the back ($20.746 W/m^2$). For curiosity a study of the effect of mask thickness on heat flux was also carried out leading to the conclusion that mask thickness does not contribute to heat flux through the front of the sample.

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