CRANFIELD UNIVERSITY

MACIEJ SZYMON BENDYK

ADVANCED CONTROL OF A MULTI-SOURCED MULTI-LEVEL VOLTAGE SOURCE INVERTER SYSTEM FOR HIGH PERFORMANCE ELECTRIC VEHICLES

SCHOOL OF WATER, ENERGY AND ENVIRONMENT

PhD Thesis
Academic Year: 2016

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This thesis is submitted in partial fulfilment of the requirements for the degree of Doctor of Philosophy

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ABSTRACT

At present, electric vehicles are getting very popular and there is a high demand for related technologies. Therefore, car manufacturers are looking for cost-effective solutions to improve the efficiency and performance of drive trains. One of the biggest challenges is to create an efficient, reliable and robust system architecture integrated with energy management systems to maximize its performance. Thus, in the last decade technologies started evolving towards use of higher voltage levels with multiple energy sources, which involve complex control and power electronics capable of performing sophisticated functions.

In the quest for a new electric drive-train technology, a system architecture together with power and energy management has been identified as a key area of research. This work investigates problems related to the complexity of energy management for power-limited energy sources to improve performance in the whole operation envelope. The widely accepted solution of using multiple energy storage systems is discussed and found to relate to more complicated and expensive power electronic hardware. Furthermore, to achieve high power with reasonable efficiency it is necessary to use high voltage, which is difficult to attain.

This work proposes an electrical system with integrated motor control and energy flow management between multiple electric sources with the aim to increase the power capability of an electric drive train. To reach good performance and high efficiency the multilevel, cascaded Voltage Source Inverter with multiple sources is introduced to provide instantaneous proportional power split and to boost voltage for the electric motor at the same time. Whilst there are existing examples of multilevel inverters with electric motor drives, none of them has successfully found their way to mainstream vehicles due to the intricacy and many unresolved technical challenges.

This thesis contributes to the field of power electronics in the following areas. Firstly a detailed mathematical analysis of hybrid cascade multilevel inverter

with variable voltage ratio between sources has been performed to find its operational limitations and to establish the power-sharing relationship between the sources. Secondly, based on the derived equations a new multilevel inverter control and modulation strategy to increase the transient power capability by distributing power between the battery and ultracapacitors has been developed. The method has been validated first through a simulated model in Matlab/Simulink and subsequently by experimental work on a specifically designed and built hardware platform. The results showed that the proposed architecture with modest increase in complexity can markedly improve the system's transient power capability, and contribute to higher maximum output voltage availability and at the same time minimize Total Harmonic Distortions and switching losses.

Keywords:

Multilevel inverter, multisource, switching strategy, power management, drivetrain, space vector modulation.

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I would like to express my sincere gratitude to my advisor Prof. Patrick Chi Kwong Luk for the continuous support of my PhD study and related research. His guidance helped me throughout my research and the writing of this thesis. I could not have imagined having a better advisor and mentor for my PhD study.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF EQUATIONS

LIST OF ABBREVIATIONS

AC	Alternating Current
BMS	Battery Management System
DC	Direct Current
DCI	Diode Clamped Inverter
DOD	Depth Of Discharge
DTC	Direct Torque Control
ESR	Effective Series Resistance
EV	Electric Vehicle
EDLC	Electric Double-Layer Capacitors
EMF	Electromagnetic Force
EMI	Electromagnetic Interference
FPGA	Field Programmable Gate Array
FOC	Filed-Oriented Control
FCI	Flying-Clamped Inverter
HES	Hybrid Energy Storage
HV	High Voltage
IHBI	Insulated-H-Bridge-Inverters
IGBT	Insulated Gate Bipolar Transistor
IPMSM	Internal Permanent Magnet Synchronous Motor
LED	Light Emitting Diode
Li-Ion	Lithium–ion batteries
LC	Inductance Capacitance
LPF	Low Pass Filter
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MMF	Magneto-Motive Force
MMC	Modular Multilevel Converter
MTPA	Maximum Torque Per Ampere
NPC	Neutral Point Clamped
Ni-MH	Nickel–Metal Hydride Battery
NN	Neural Networks
PES	Power Electronic Shell
PF	Power Factor

PI	Proportional Integral
PMSM	Permanent Magnet Synchronous Motor
PWM	Pulse Width Modulation
RAM	Random Access Memory
RMS	Root-Mean-Square value
SOC	State Of Charge
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
UC	Ultracapacitor
VSI	Voltage Source Inverter

NOMENCLATURE

a	Phase rotation operator
I_{bat_max}	Battery maximum current limit
I_{bat_min}	Battery charging current limit
C	Capacitance
C_{UC}	Ultracapacitor capacitance
ΔE_{UC}	Energy stored in capacitor
$E_{reg,Max}$	Maximum energy to recuperate
$E_u(V_{dr})$	Energy stored in capacitor
$E_{pr}(V_{dr})$	Unified energy
F_{mA}	Magneto-motive force
I	Current vector
I_{bat}	Battery current
I_{max}	Maximum motor current
$I_{A,}\ I_{B,}\ I_C$	Phase currents
$I_{uc\_A,}I_{uc\_B,}I_{uc\_C}$	Average UC DC current in phase A,B and C
$i_{uc\_A,}i_{uc\_B,}i_{uc\_C}$	Instantaneous currents seen by the UC in phases A, B and C
I_{dx}	Stator current in d axis
i	Current in time domain
i_{dse}^*	Reference current in d frame
i_{dse}	Synchronous current in d frame
i_{qse}	Synchronous current in q frame
J	Moment of inertia
k	Space vector generally
L_d	d axis inductance
L_q	q axis inductance
N	Non active power
M	Mass
p	Number of magnetic poles
$p_{A,}\ p_{B,}\ p_C$	Instantaneous active power in phase A,B and C
$p_{uc\_A,}\ p_{uc\_B,}$ p_{uc_C}	Instantaneous UC active power in phase A,B and C
α	Modulation switch angle

ϕ	Phase angle
P	Active power
P_{bat}	Active power delivered by battery
P_{UC}	Total active power delivered by three capacitors
$P_{A,}P_{B,}P_{C}$	Active power in phase A,B and C
$P_{x}*$	Reference active power
R_{s}	motor phase resistance
S	Apparent power
Q	Reactive power
Q_{x}^{*}:	Reference passive power
T_{e}	Electromagnetic torque
Ψ_{s_α}	Stator flux in α plane
Ψ_{s_β}	Stator flux in β plane
Ψ_{qse}	flux linkage in q axis
Ψ_{dse}	flux linkage in d axis
Ψ_{PM}	permanent magnet flux linkage in synchronous frame
Ud	Source voltage
v	Voltage in time domain
V_{as}	Output waveform
V_{ag}	Bulk inverter voltage
V_{agx}	Conditioning inverter
V_{dcx}	Capacitor voltage
${v_{qsx}}^{s*}$	Reference voltage in q axis
${V_{dsx}}^{s*}$	Reference voltage in d axis
V_{dr}	Proportional discharge
$V_{an,}\ V_{bn,}\ V_{cn}$	Phase voltages
$V_{AB,}\ V_{BC,}\ V_{CA}$	Phase to phase voltages
V_{α}	Voltage in α plane
V_{β}	Voltage in β plane
V_{UC_ref}	Ultracapacitor reference voltage
V_{ref_α}	Reference voltage in α plane
V_{ref_β}	Reference voltage in β plane
V_{ref_d}	Reference voltage in rotary d plane

V_{ref_q}	Reference voltage in rotary q plane
v	Velocity
V_{UC}	Ultracpacitor voltage
V_{uc_avg}	Average capacitance of three Ultracpacitor voltages
V_{cap}	Capacitor voltage
V_{UC_Max}	Maximum capacitor voltage
V_{dse}	Voltage in d axis synchronous frame
V_{sup}	Supply voltage
V_{qse}	Voltage in q axis synchronous frame
V_{ref}	Reference voltage
V_{bat}	Battery voltage
V_{UC_A}	H-Bridge capacitor voltage in phase A
V_{UC_B}	H-Bridge capacitor voltage in phase B
V_{UC_C}	H-Bridge capacitor voltage in phase C
$V_{MI\_max,min}$	Maximum, minimum inverter output voltage in MODEI
$V_{MII\_max,min}$	Maximum, minimum inverter output voltage in MODEII
$V_{MIII\_max,min}$	Maximum, minimum inverter output voltage in MODEIII
$V_{MIV\_max,min}$	Maximum, minimum inverter output voltage in MODEIV
$V_{MV\_max,min}$	Maximum, minimum inverter output voltage in MODEV
$V_{MVI\_max,min}$	Maximum, minimum inverter output voltage in MODEVI
χ	Phase shift angle
γ_{Ψ}	Flux angular position
ω_r	Motor angular velocity

CHAPTER 1 INTRODUCTION

1.1 Overview of Electric Vehicle technology

Electric vehicles (EV) have gained great popularity over recent years, and more car manufacturers are introducing models with an electric drivetrain. The technology is now widely accepted as consumers have become more aware of the greenhouse gasses that affect climate change as well as the issue of air pollution from combustion engines. Concerns surrounding the depletion of oil reserves and the security of its supply mean governments are encouraging motorists to switch from fossil fuels to electrical energy. The examples of Tesla, BMW and Nissan prove that EV that combine practical design, great performance and reasonable range are in high demand. The global market for EV is growing fast. In the year 2015 alone the number of EV on the road exceeded one million, and that is expected to rise exponentially (Slowik, Pavlekno and Lutsey, 2016). In many countries EV have become a significant part of market share, with Norway leading, having reached 23% (International Energy Agency, 2016). Nonetheless, the percentage of EV still comprises just a fraction of cars with combustion engines currently on the road. The barriers limiting the market growth of EV include a smaller range than for conventional vehicles, their charging time and their high purchase price. The crucial problem with EV is the battery bank, which has limited energy and power density, and a high cost per kilowatt-hour (kWh) (Whittingham, 2012). Battery technologies are seeing constant growth and development, with a huge number of patents being registered in the last decade. Yet breakthroughs appear still to be far off (Lin et al., 2013). Because battery technologies represent a compromise between available power and available energy, one solution to improve the energy-storage performance and extend the life of the battery is to combine batteries with different types of energy storage technology (Shen, Dusmez and Khaligh, 2014). Another way to extend the range and performance of EV is to improve its efficiency and kinetic energy recovery capability. Advancements in power train, power electronics, energy management, aerodynamic and lightweight materials are key elements in achieving increased efficiency of EV. Attention is not

always paid to the power electronic, but this element accounts for a significant share of the total EV price and is almost as important as the battery or electric motor. The power electronics is the intermediary between the battery and the AC motor, and allows power distribution between voltage sources. Thanks to advancements in modern-day electronics and control methods AC motors with high power density, good reliability and superior performance have become the most popular drivetrain structure (Mahmoudzadeh Andwari et al., 2016). Nowadays electronics can achieve high efficiency, typically within the range of 95-98%, but power losses increase with multiple voltage conversion stages. By combining the right drivetrain architecture with power management and power electronic control, the efficiency, performance and cost of EV can be significantly improved (Anwar et al., 2016), (Chen et al., 2016). One of the most useful benchmarks for the electric powertrain is the Formula E racing championship that began in 2014 and has brought huge attention from the automotive industry, including Jaguar, Renault, Audi, BMW and DS. Since its second season in 2015 the regulations have allowed manufacturers to develop new powertrains, including electric motors, inverters and gearboxes, while the chassis and battery stay the same (Biesbrouck, 2015). The 2015-16 championship saw many new drivetrain architectures with different motor and inverter types and configurations, and with more regenerative breaking capabilities (current-e, 2016). The results prove that that the right powertrain architecture, together with good control software and strategies, is the key to achieving the best performance and efficiency and to extend range (FIA Formula E, 2016) (TECH TALK, 2016).

1.2 Research problem - review

The research on EV can be divided into the few main topics with the biggest interest dedicated to energy-storage technologies (batteries, UC) and design of Battery Management System (BMS). Because range is the key problem for EV, the vehicle charging topics become also very popular. The other elements of EV development are electric motors, power electronic for DC/AC and DC/DC inverters, control algorithms for electric motor and power and energy

management. The area of energy storage has been widely researched since there is a huge need for technical improvements, not only for EV but for other applications such as mobile devices. Voltage sources, such as lithium batteries and their variations, have seen major improvements in terms of their price, safety management, charging time and capacity (Lu et al., 2013). Nevertheless, the gap between the expected energy density for EV and what current batteries can offer is still large and seems unlikely to change soon (Lin et al., 2013) (Yong et al., 2015). To improve batteries' characteristics, the concept of hybridizing them with high-power capacitors (UC) has become popular in the last decade (Khaligh and Li, 2010). The Hybrid Energy Storage (HES) technology is proving to be promising and solves many problems, but because of the increased cost and complexity the solution has not been widely adopted within (EV) (Ju et al., 2014). At the same time the electric motor's need for higher voltage with low harmonics has made multilevel inverter structures a subject of interest for EV (Vasiladiotis and Rufer, 2015) (Gholinezhad and Noroozian, 2013). The multilevel inverter has proven to be a high-performance and efficient solution for electric propulsion where multiple energy sources can be accommodated.

The research in this thesis focuses on the design of an innovative topology for an electric drivetrain with multiple electric energy sources. The scope of this work includes power electronic hardware design, the development of a control algorithm for instantaneous energy transfer between energy sources, and vector control for the electric motor. Figure 1-1 presents a summarised scope of the research. The deliverable of this project will be a drivetrain system consisting of a multilevel inverter where the battery is the primary form of energy storage and the UCs are the secondary power source. To meet vehicle load demands, the control algorithm will provide vector control for the electric motor with simultaneous energy/power transfer control. The battery will operate under controlled load conditions when the UCs provide peak power consumption and energy recuperation.

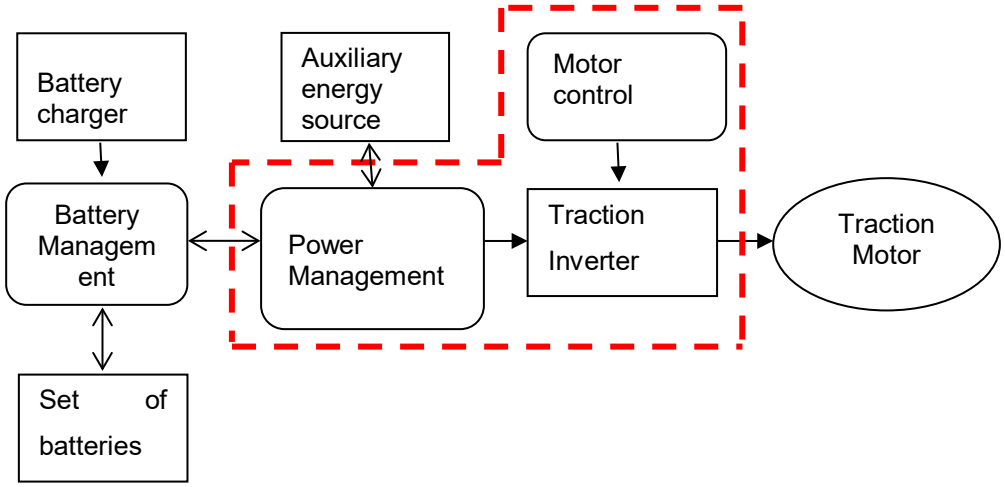


Figure 1-1 Scope of the research on EV drivetrain

1.3 Aims and objectives

This research project aims to contribute to the development of new technology to increase the transient power capability of the electric drivetrain by sharing power between multiple sources, thereby protecting the primary source against overloads during transients and increasing regenerative breaking ability. In addition to extending the drivetrain's power capability the work also aims to improve its efficiency by minimising Total Harmonic Distortions (THD) and switching losses. The resulting system should also have a simplified and cost-effective structure.

The first objective of this research is to perform a detailed analysis of multilevel multisource systems and discover their operational limitations. The next objective is to define a strategy for power and energy sharing for the proposed structure that could at the same time provide the best inverter performance. The key objective is to design, analyse and implement an innovative control algorithm for power sharing together with a modulation strategy. Finally an experimental platform will be developed in order to test the performance of the proposed hardware and control system architecture. The performance of the new system shall be measured against existing solutions in terms of its achievement of the goals such as reduction of voltage and current ripples at low and high speed and improvement of transient response. The system is

expected to have THD in the range of 5-10% and low switching losses and switching stress. Also the expected unit cost should not increase drastically when new functionality of instantaneous power transfer between sources and extended performance at high speed is implemented.

1.4 Approach and methodology

The starting point of this work is to identify a system architecture that is able to meet the goal of the research. The first step is to review existing multisource drivetrain structures in literature to select the appropriate technology and understand its physical and operating constraints. To fully understand the architecture being examined, a basic analysis and simulations of the system elements are required. Firstly, fundamental studies on the energy sources used are necessary to distinguish their operating modes. Understanding the properties of the system is crucial in verifying the proposition of implementing a multilevel voltage source inverter in configuration with a dual energy source (batteries and ultracapacitors). The current literature provides only limited information on this type of structure; therefore, a detailed analysis and state modelling will be performed.

Having identified the complete architecture, the next step is to investigate a suitable control method that will enhance the performance of the electric drivetrain. Because the proposed topology functions as a power/energy distributor between the sources, and as a traction inverter, the control algorithm will have to manage the energy sharing and torque control of the electric motor at the same time. Furthermore, as variable UC voltage does not allow the implementation of the traditional method of Space Vector Modulation (SVM), it will be necessary to research and develop a new modulation method.

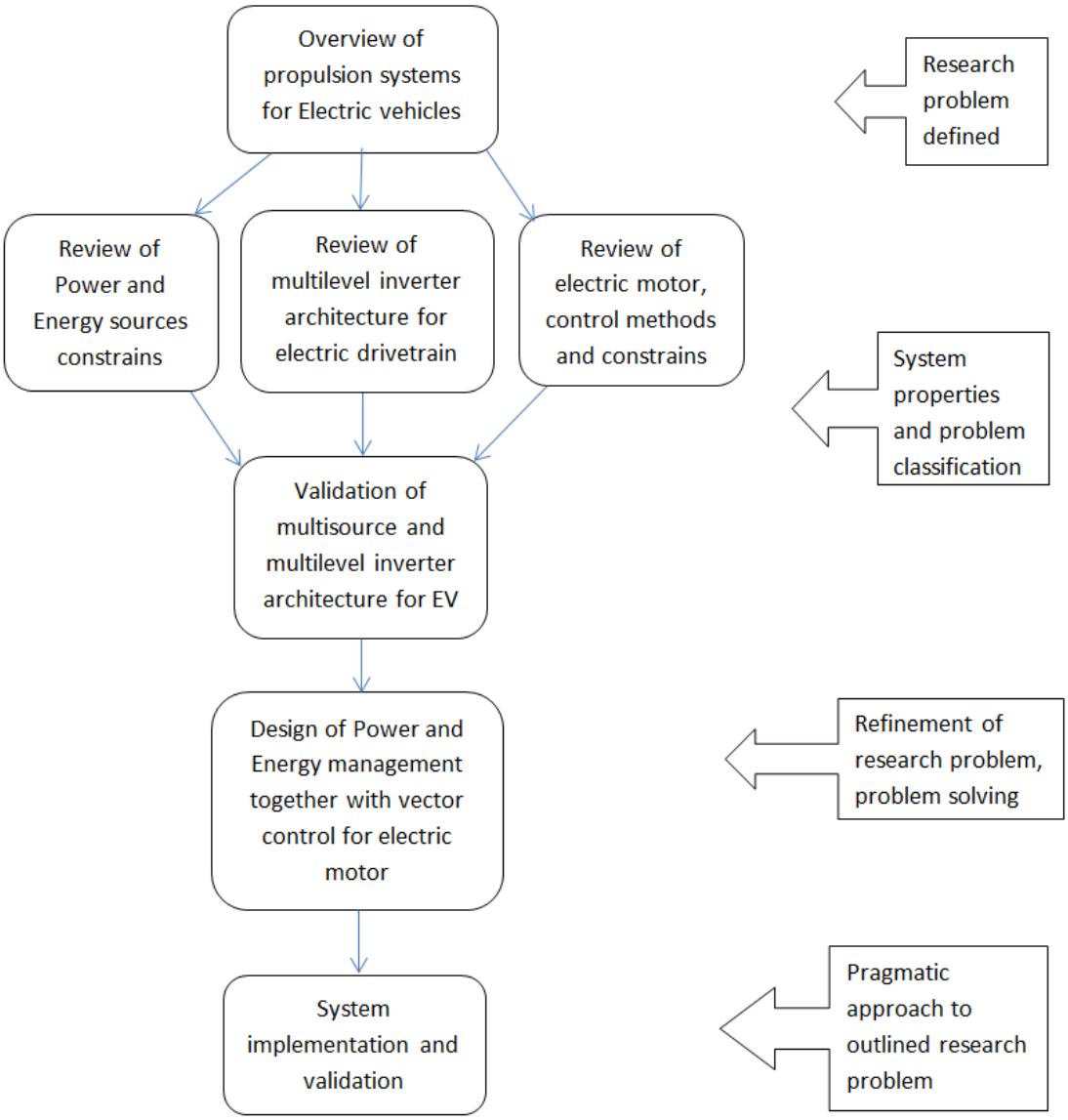


Figure 1-2 Research methodology

The next step of the research is to apply a numerical computing environment to simulate the proposed system. For this application the MATLAB/Simulink software was selected. The simulations should provide verification of the control algorithm and at the same time help design logic that can be used as software for the physical model.

The final step is to design and build a working prototype of the system as described. The platform shell is then tested by experimental measurements against previously simulated results. The system's performance will also be compared with multisource solutions existing in literature. In the case of

significant variation between the results and the predicted outcome, investigation of the discrepancy will be undertaken. Figure 1-2 presents a summary of the research framework.

1.5 Thesis structure

Chapter 2 begins with an introduction of the energy sources for EV (batteries and ultracapacitors) and reviews power management architectures for multisource systems. This chapter later analyses the electric motor and its control methods. Multilevel inverter structures are also reviewed and a mathematical description of the space vector concept is presented.

Chapter 3 establishes a mathematical approach for a hybrid cascade multilevel inverter under conditions where the sources have variable voltage amplitude. An inverter analysis is performed to find modulation limits, and a strategy to control energy flow is derived. The chapter also discusses ultracapacitor reference voltage in contexts of kinetic energy and inverter output voltage. The last section reviews further possible inverter modifications that could improve its performance without a significant increase in cost.

Chapter 4 describes the control strategy that was formulated based on the analysis in Chapter 3. The structure of the developed algorithm and its main elements, such as power management, motor control and the space vector modulator for the proposed inverter are presented.

Chapter 5 is an overview of the Matlab/Simulink model of the proposed system, with a discussion of the results of numerical calculations.

Chapter 6 presents the design of the experimental platform that was developed and reviews the results that were extracted during drivetrain operation. The results are also compared with the simulated inverter model.

Chapter 7 analyses the results of the work and presents the conclusions of the thesis, including recommendations for further work.

The Appendix section provides details of the simulated model, the control hardware build and the control program design, including block diagrams of the LabView program that was developed.

CHAPTER 2 OVEVIEW OF ELECTRIC VECHICLE PROPULSION TECHNOLOGY

In this chapter, a broad survey on elements of electric propulsion system is presented. First an overview of energy sources (batteries and UC) for EV is introduced and later the multisource system architectures are reviewed. The principles of power management for hybrid systems are studied as well representation of the space vector is outlined for further discussion. The final section review multilevel inverters to find best suited structure for the multisource system. Also an electric motor together with its control is examined.

2.1 Energy sources for EV

The key element of each EV vehicle is the energy storage that is responsible for providing power to drivetrain and additionally to recover kinetic energy from breaking. Currently there is many solutions to store energy but none is ideal since there is always compromise between energy density, power availability and cost. The most well-known solution is battery but since energy is stored through electrochemical reactions the response time especially during charging is slow. In case of UC the energy is stored through the static charge and since energy is in the same form, the charging and discharging rates can be high. However UC energy density is around ten times lower than battery and for this reason UC require to be complementary to batteries.

2.1.1 Battery technologies

Technology advancement in recent decades brought many new battery types that vary between price, energy density and management complexity. Typical battery consists of anode and cathode, and electrolyte material that has a function to transport energy through ion migration between electrodes. Because the reaction during charging is different from discharging the time required to recharge or release energy might be also different. Base on electrode and electrolyte type we can distinguish four main technologies that found applications in the EV (Sun et al., 2008).

The most well-known battery type that was traditionally used in combustion engine vehicle is a lead-acid type. This technology is well developed and relatively cheap however is very limited because of its low energy density and short life. For those reason lead acid batteries are only used in very small electric vehicles such as golf carts (Mahmoudzadeh Andwari et al., 2016). Nowadays the common replacement of lead-acid battery technology becomes lithium-ion that found applications not only in EV but also is used in many mobile devices. Because of rapid development of lithium technology, currently we can distinguish number of types and subtypes of those batteries including lithium-Ion and lithium-ion polymer, and variants with nickel, cobalt, manganese and iron (Lin et al., 2013). The lithium batteries offer currently the best power density but their biggest problem is high cost and sensitivity to operating conditions. In order to facilitate the safe use of batteries it is require to use a protection circuit against short-circuit, overcharge, deep discharge and temperature.

We can also distinguish Nickel Metal Hydride batteries that become popular solution in automotive market because of their lower than lithium cost and around twice energy density in comparison to lead acid batteries. The limit of Nickel battery technology has been reached and capacity is still unsatisfactory to become energy source for the EV. The last technology that is worth to mention is Sodium Metal Chloride battery (Zebra) as this type has very long life cycle, good energy density, low cost and is relatively safe to use. But since sodium batteries have low power density there is a need to combine them with other sources type (Catenacci et al., 2013).

To operate batteries safely there is usually imposed maximum current limit (I_{bat_max}) that is related with electrodes current conducting ability and battery safe operation conditions. Also because battery state of charge has influence on its internal resistance, the maximum output voltage will decrease at low state of charge, consequently the maximum output power become reduced in addition to current constrain. In case of charging the power is further reduced by the maximum cell charging voltage specific for each battery type and relate with its

state of charge. For this reasons the charging current (I_{bat_min}) has to be smaller than the maximum discharge current. All above parameters are additionally related with battery temperature (Lu et al., 2013).

Since high voltage for electric motor is needed the number of individual cells has to be connected in series where each cell voltage might vary and the weakest cell can reduce performance of complete battery. The overvoltage can easily damage batteries and in case of lithium batteries can cause fire. This makes unit operations within range challenging and require to implement additional Battery Management System (BMS) that balance voltages and provide its safe use (Affanni et al., 2005). The process of equalising individual cells voltage has also additional effect on extending battery charging time (Gao, Tian and Chen, 2009).

2.1.2 Ultracapacitors

Supercapacitors, also known as ultracapacitors (UC) are increasingly used in the automotive market. Those devices are Electric Double-Layer Capacitors (EDLC) and derive high capacitance from the porous carbon-based electrode material. The carbon-based electrode material allows creating a surface area reaching 2000 square meters per gram. Thanks to increased surface area and thin charge separation in comparison to standard capacitors that use flat films, the stored energy can be much higher. Since there is no chemical reaction the energy can be released or captured instantaneously and the cycle can be repeated millions of times. Compared with batteries, which are traditionally used in EV and have ten times higher energy density, the supercapacitors have the following advantages: more charge/discharge cycles, higher power density, higher cycle efficiency, longer lifetime, lower toxicity of material used, and easier State Of Charge (SOC) estimation.(Maxwell Technologies, 2014). Because of those reasons the UCs did not find many applications as an individual energy source but become suitable as assistance to smooth power variations. Thanks to advancement in power electronics the combination of high energy battery and high power capacitors become very popular solution. The power oscillations decoupling through UC prove that the efficiency of the drive

train can be improved thanks to higher kinetic energy recuperation and higher acceleration can be achieved since available power is higher (Miller, 2009). Also amount of power dissipated in battery become lower as well temperature so the battery lifetime can be extended (Miller et al., 2009). Especially integration of low power and low cost Zebra batteries with UC provide promising results but because of limited UC capacity there is always limitation in case of a long breaking (Dixon et al., 2010). Consequently there is a need to find best UC size to achieve longest battery cycle without significantly increasing system cost and size (Shen, Dusmez and Khaligh, 2014).

The justification of using UC for EV is very well described in H. Douglas and P. Pillay's publication (Douglas and Pillay, 2005) . The UC technology has been commercially available for over two decades. The energy that can be stored in them is much higher than for conventional capacitors and the available sizes are up to 4000F with voltage ratings of up to 3V per cell. The discharge or charge is much faster than batteries and delivered power can be 10-20 times higher than in conventional voltage sources. Lead acid and Ni-MH batteries are capable of delivering short bursts of power; however operating them under extreme discharging conditions dramatically reduces their life. The comparison between batteries, UC and conventional capacitors is presented in Table 2-1.

Table 2-1 A comparison of battery, ultracapacitors and conventional capacitors performance (Douglas and Pillay, 2005)

Available Performance	Lead Acid Battery	Ultracapacitor	Conventional Capacitor
Charge Time	1 to 5 hrs	0.3 to 30s	10^{-5} to 10^{-6} s
Discharge Time	0.3 to 3 hrs	0.3 to 30s	10^{-3} to 10^{-6} s
Energy (Wh/kg)	10 to 100	1 to 10	<0.1
Cycle Life	1000	>500 000	>500 000
Specific Power (W/kg)	<1000	<10 000	<100 000
Charge / Discharge efficiency	0.7 to 0.85	0.85 to 0.98	>0.95

Unlike batteries, the voltage of UC varies dramatically depending on the energy stored. Often, there is a DC-DC converter between the UC and inverter to provide constant voltage for the inverter to drive the electric machine.

In his presentation about Maxwell UC, John M. Miller (Miller, 2007) predicts that in the next few years the power and energy density of UC will double (Figure 2-1). The author also pointed out that despite the higher performance and better availability of lithium-ion batteries, the UC would still remain the product that has to be used due to the high power level that is maintained across the full temperature range. Batteries slow down when cold because of redox reaction and become too reactive when hot.

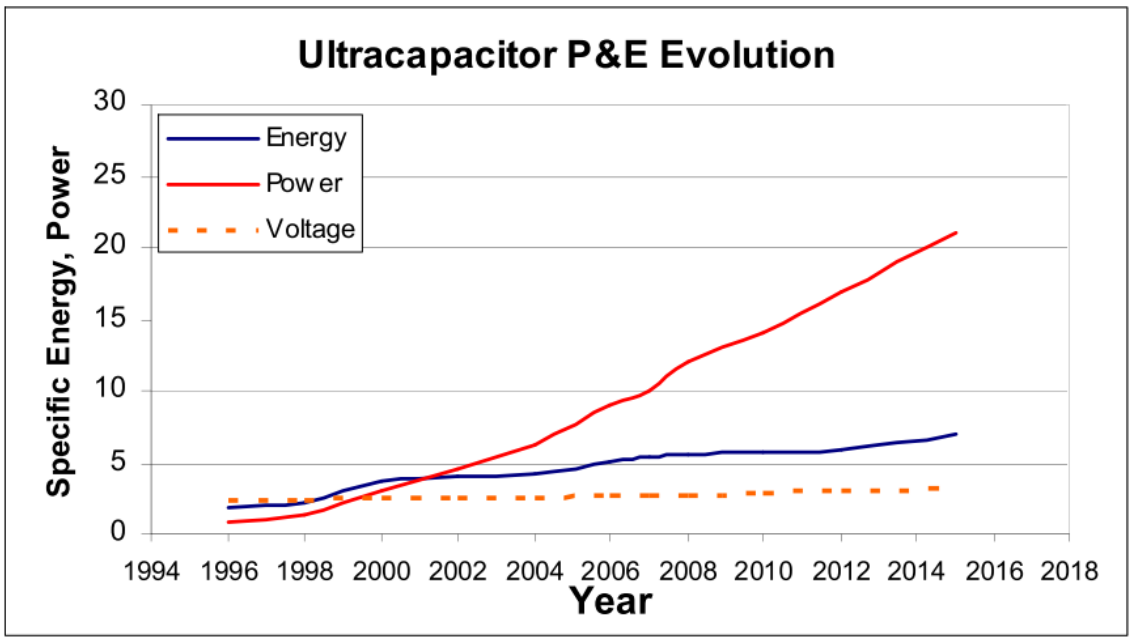


Figure 2-1 Evolution of Ultracapacitors Power and Energy (J. Miller, 2008)

The combination of UC with lithium–ion batteries was very accurately summarized in another work by John M. Miller (J. Miller , 2008) where the many issues related with lithium-ion batteries were presented. The biggest problem remains a cost factor as it is still too high on a power basis ($/kW), also performance at cold temperatures, especially for discharge power, remains poor and fades with ageing. Temperature goals for lithium-ion are -30°C to +65°C. The cycle life is close to meeting target expectations but calendar life remains elusive, especially for 15 year life in power assist. Lithium batteries today are

limited to 20% and 30% loading factors, or state of charge (SOC) window, because deep cycling significantly reduces life. For instance, a lithium-ion battery capable of 2,600 cycles to 30% depth of discharge (DOD) would only be capable of 1,000 cycles at 80% DOD. Loading factors must increase from 80% to 90% for electric vehicles to be feasible. Additionally tolerance to abuse: short circuit, over voltage, over temperature, rapid discharge and charge, and crush tolerance remain particularly problematic in the lithium-ion cell. This entails strong reliance on proper charge/discharge controls, and energy management is necessary.

On the other hand UC offer many advantages that complement the lithium-ion weaknesses with the most important low cost on a power basis since UC are power-dense components. Performance at cold temperatures, in both discharge and charge, is strong and very efficient, the cycle life is high, in the one million cycles at 75% to 80% of SOC. Also calendar life is high because the UC does not wear out; it stores energy in the same form as it will be used (as electrons), meaning there is no electrical-to-chemical energy conversion as takes place in a battery. UC have very fast responses and can deliver very high pulse power virtually instantaneously. Therefore, the UC must be handled carefully when charged because of its exceptional power density. Proper controls and energy management are essential.

There is growing perception that lithium technology has shortcomings when a long-term charge operation is demanded that has superimposed the shallow power cycling characteristic of charge remaining. Issues with SOC window, charge acceptance above 80% SOC and discharge performance below 30% SOC, along with poor pulse power performance at low temperatures, are cause intense research into advanced lithium chemistries, such as the lithium-ion cathode and non-graphitic, lithium-titanate anode designs.

UC offer new opportunities when combined with fast dynamic DC-DC converters. The combination of UCs and DC-DC converters shows the promise of the composite energy storage system delivering power and energy at greater

than 90% efficiency over the high dynamic working range of application power levels (Lu et al., 2007b).

2.1.3 Review of multisource energy storage systems

A concept to combine multiple sources with different performance is well known and many authors proposed different architectures and strategies.

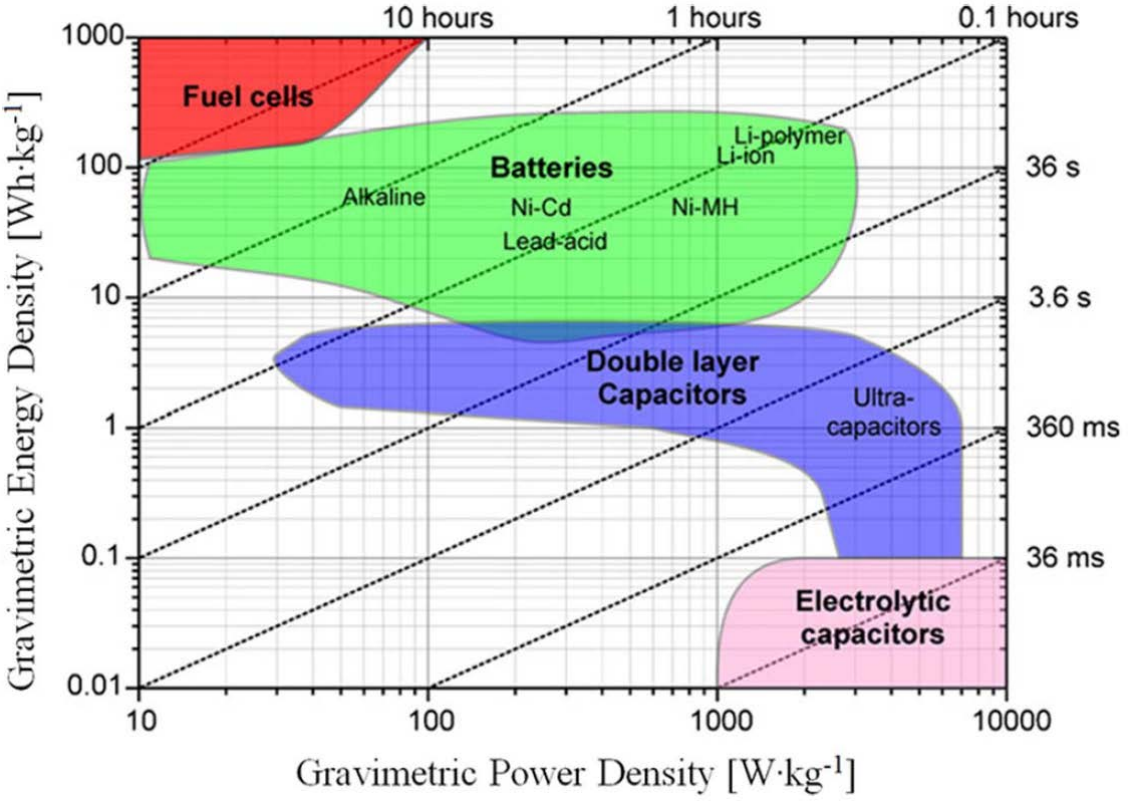


Figure 2-2 The relation between power and energy for different energy sources (Aharon and Kuperman, 2011)

An overview of powertrain architectures with multiple energy sources is well presented by Aharon and Kumperman (Aharon and Kuperman, 2011). To aid understanding of Gravimetric the Power and Energy graph, density has been presented in Figure 2-2. It shows the variation of energy density with power density for different storage technologies. It is clear that to create a system that can be characterized with long range and high power the hybridization of technologies is needed. To achieve best battery and UC performance different

configurations of hybrid systems have been used. The typical topologies can be qualified as:

The passive hybrid - The most common battery, UC hybridization is studied by many researchers and employed in commercial products. In the passive hybrid topology, the battery and UC packs are connected in parallel directly to the DC link (Figure 2-3). The obvious advantages of this topology are its simplicity, the lack of power electronics and control circuitry, reducing the overall energy, and power density. The main disadvantage is the uncontrolled current flow, determined only by the sources impedances and low utilization of the UC.

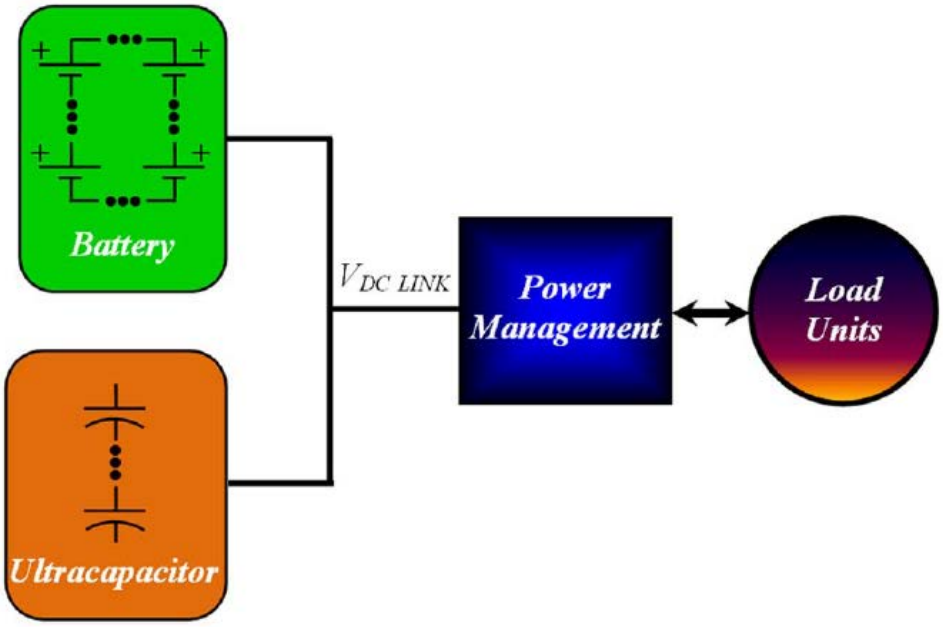


Figure 2-3 Passive hybrid topology (Aharon and Kuperman, 2011)

Parallel Semi-active Hybrid (Figure 2-4) - This configuration improves the passive hybrid topology by satisfying the voltage requirement of the load by maintaining the DC-link voltage at its nominal value despite variations in the battery/UC voltage. In addition, it allows a mismatch between the battery voltage (and hence, the UC voltage rating) and the load. Nevertheless, it does not change the fact that the battery supplies part of the dynamic current and the UC available energy is still limited. Another drawback is the need for a full rating DC–DC converter.

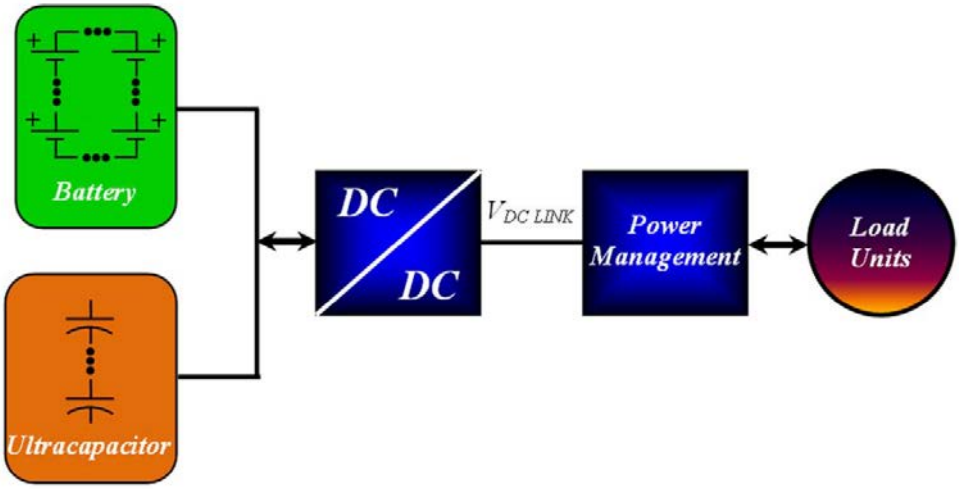


Figure 2-4 Parallel semi-active hybrid energy storage powertrain (Aharon and Kuperman, 2011)

Capacitor Semi-active Hybrid (Figure 2-5) - This topology allows decoupling between the UC and the DC-link voltages, thus improving the utilization of the UC energy.

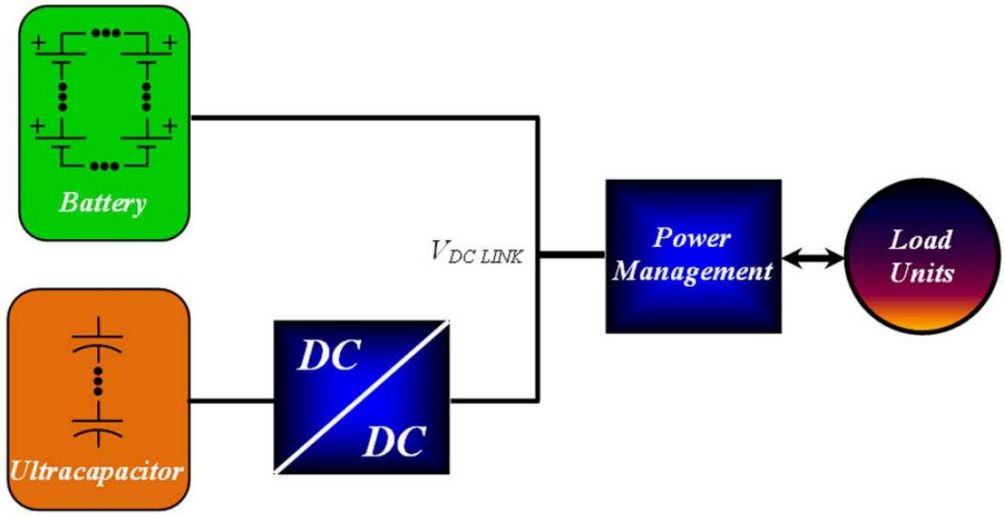


Figure 2-5 Capacitor semi-active hybrid energy storage powertrain (Aharon and Kuperman, 2011)

The topology is useful in vehicles with a large amount of regenerative braking. The energy range is 50% to 100% of its rated voltage, allowing utilization of 75% of the overall available energy. The main disadvantages of the approach

are the high rating of the DC-DC converter and the fact that the battery still supplies part of the dynamic currents in some cases.

Battery Semi-active Hybrid (Figure 2-6) - The main advantage of such a topology is the ability to maintain the battery current at a near constant value despite the load current variations. This allows significant improvement of the battery performance in terms of life, energy efficiency, and temperature. In addition, the voltage matching between the battery and the DC link is no longer required (Guidi, Undeland and Hori, 2007), (Guidi, Undeland and Hori, 2009).

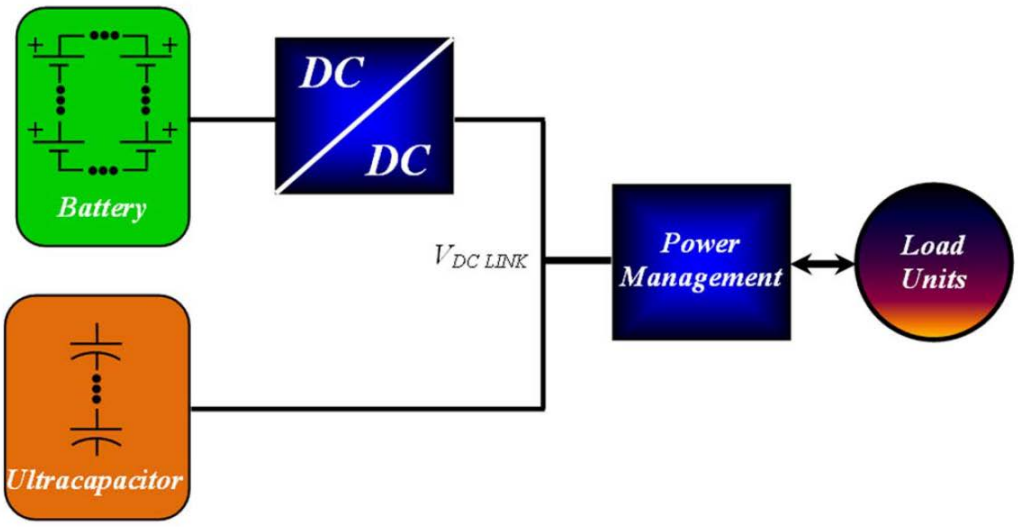


Figure 2-6 Battery semi-active hybrid energy storage powertrain (Aharon and Kuperman, 2011)

Series Active Hybrid (Figure 2-7) - This solves the problems of UC voltage variation and matching by placing an additional DC–DC converter between the UC and the DC link. The main disadvantages of the topology are the addition of a full rating DC-DC converter and reduced efficiency, since there are two conversion stages between the battery and the DC link.

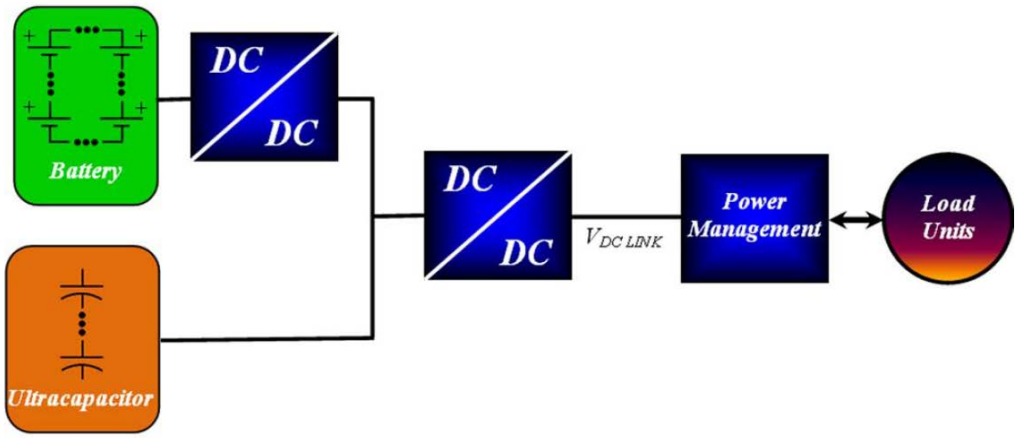


Figure 2-7 Series active hybrid energy storage powertrain (Aharon and Kuperman, 2011)

Parallel Active Hybrid - This topology is, by far, the most advantageous active hybrid, reported in literature. It solves the problems of UC voltage variations and matching by placing a DC–DC converter between the UC and the DC link. In addition, it allows a near constant current flow from the battery as well as voltage mismatch between the battery and the DC link by placing a DC-DC converter between the battery and the DC link. The topology is shown in Figure 2-8.

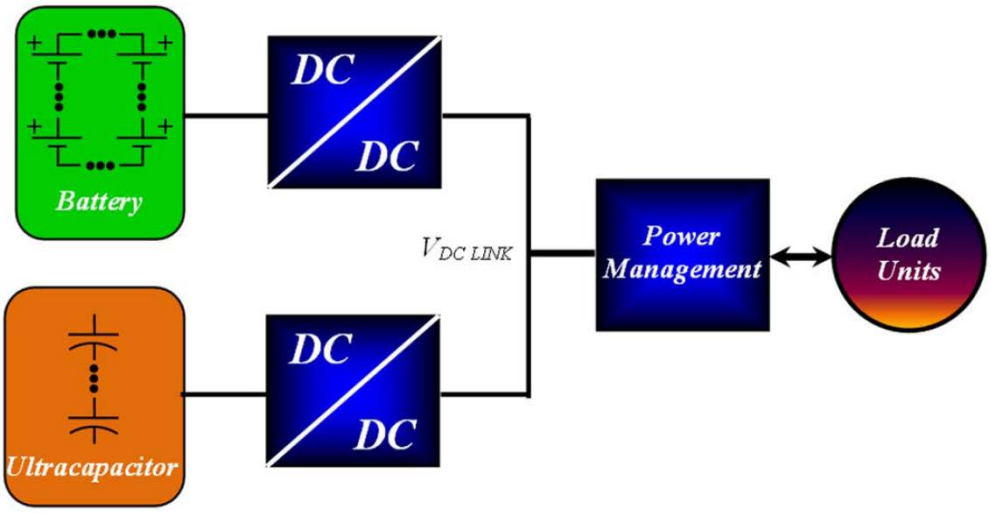


Figure 2-8 Parallel active hybrid energy storage powertrain (Aharon and Kuperman, 2011)

The main disadvantage of the topology is the utilization of two DC-DC converters, one rated at the load average power and another rated according to the dynamic peak power, bringing complexity, control effort, and additional losses into the system.

Research carried out by A. L. Allegre and R. Trigui (Allègre, Trigui and Bouscayrol, 2013) concerns an Electric Vehicle (EV) with Hybrid Energy Storage (HES) batteries and UC using an active association with two choppers in parallel, as shown in Figure 2-9. Four elaborated strategies have been studied with their systems sharing the power demand between batteries and UC. For each strategy the EV with HES is compared with an EV with battery only. It appears that the use of HES is interesting for the electric consumption, the size and the expected life of the batteries. Each strategy presents different results for the same sizing.

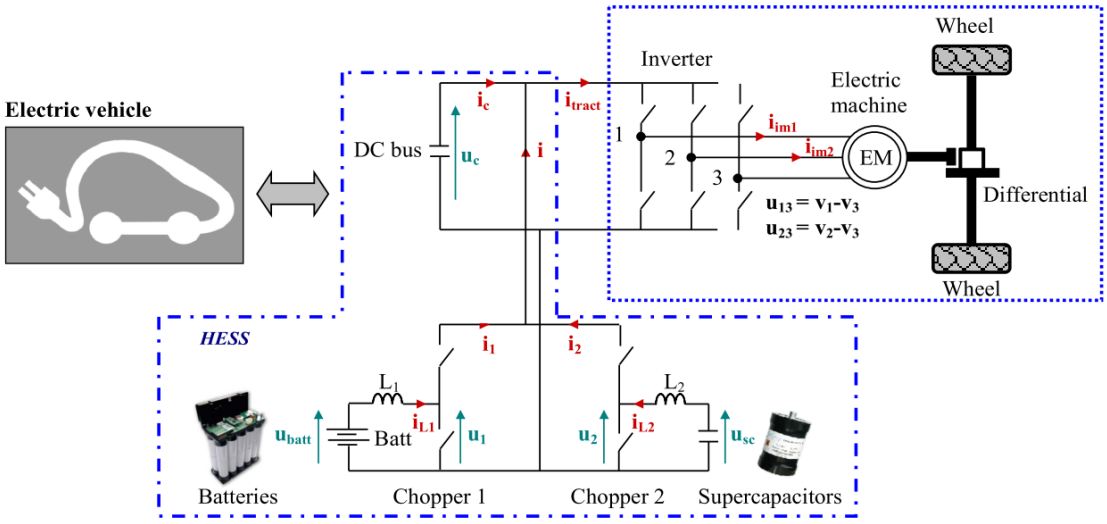


Figure 2-9 Studied EV with multiple sources (Allègre, Trigui and Bouscayrol, 2010)

The authors found that adding an additional energy source in the form of an UC can bring benefits in terms of lower power consumption, longer battery life, and smaller battery sizing (Figure 2-10). On the other side the system can be criticized for amount of additional power conversion stages and its control complexity.

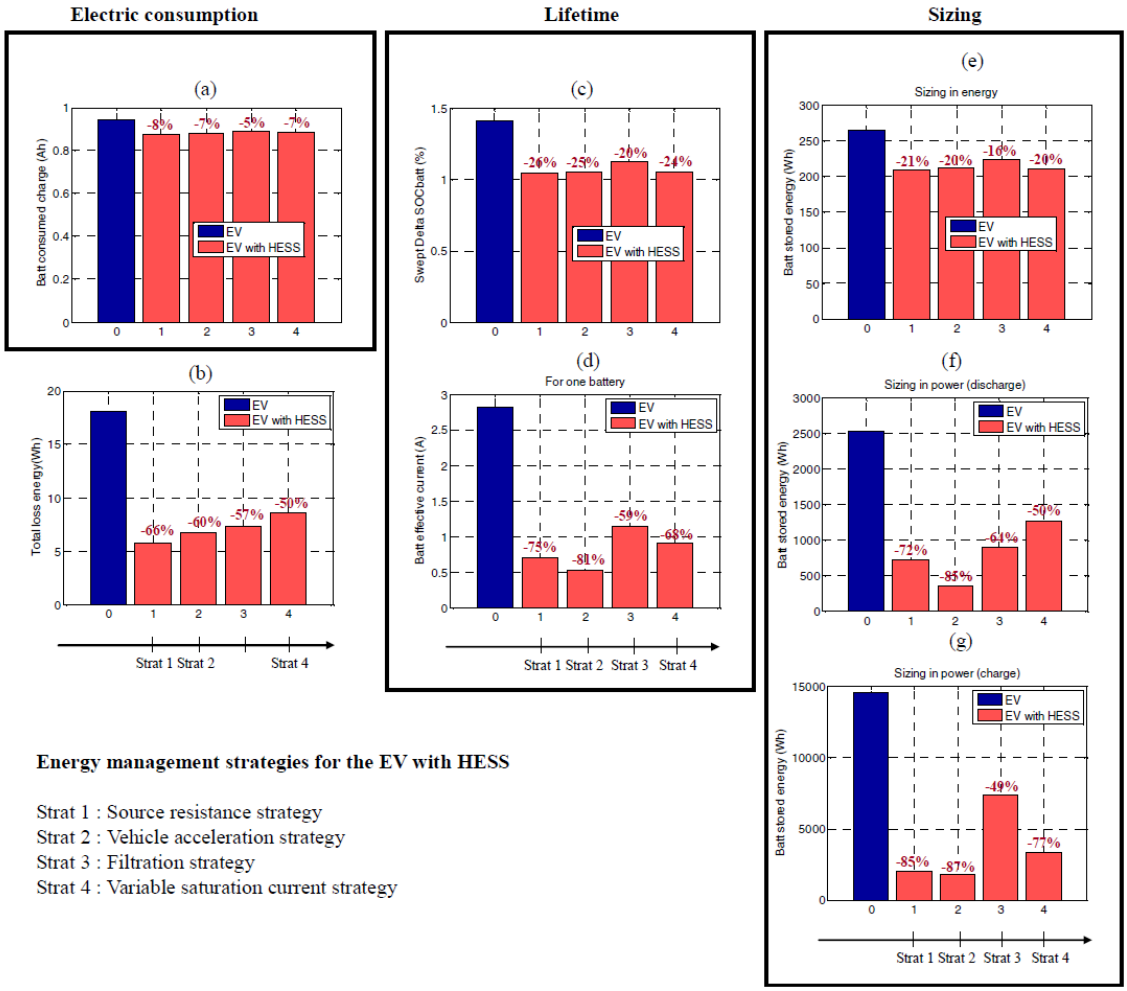


Figure 2-10 Comparison of the performances of the EV and the EV with Hybrid energy sources (Allègre, Trigui and Bouscayrol, 2010)

Work by R. Carter and A. Cruden (Carter and Cruden, 2008), (Carter, Cruden and Hall, 2012), has also proven that multisource systems with the right control strategy can extend battery life and system efficiency. The system being tested consisted of the parallel connection of the batteries and UC, where energy transfer was controlled by DC/DC inverters for each source as shown in (Figure 2-11). The authors tested two different strategies for this vehicle system. One was fine-tuned for maximum vehicle efficiency and the other was to reduce battery current and extend battery life. It was possible to improve 7.6% of vehicle efficiency as well as reducing battery currents up to 72%. It was also evident that a specific drive cycle has a significant effect on battery efficiency and current. As one of the parameters, either battery life or vehicle efficiency,

has to be given priority over the other it was clear that optimization to reduce battery current would also decrease efficiency.

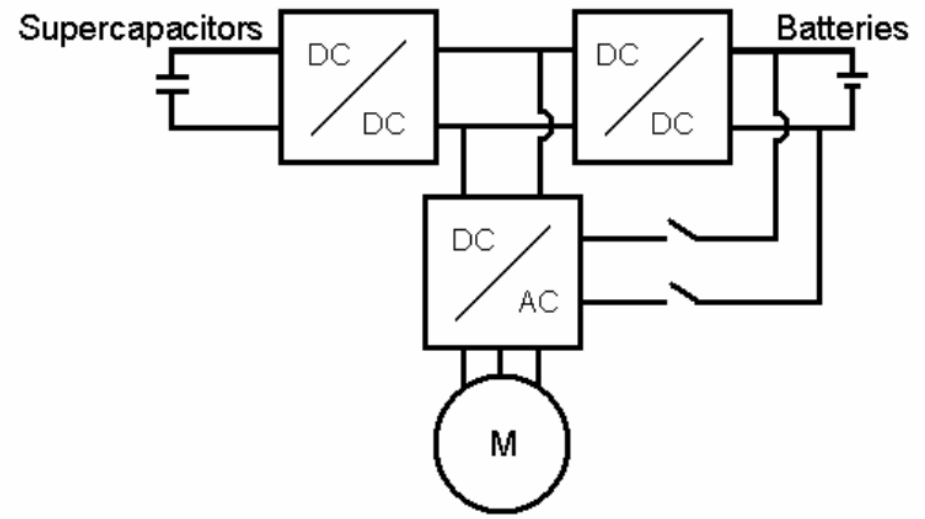


Figure 2-11 Platform used for strategy verifications (Carter and Cruden, 2008)

The drive train was controlled using the flow chart as shown in Figure 2-12.

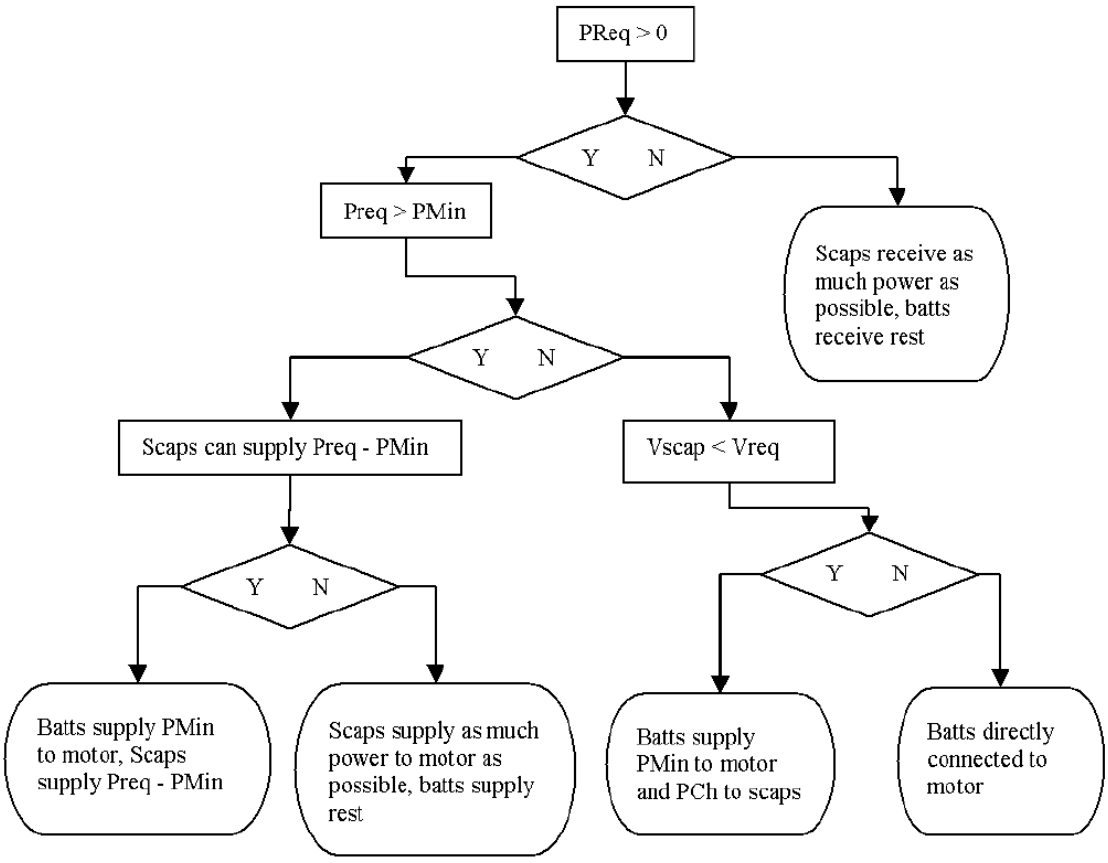


Figure 2-12 Control logic for multisource system (Carter and Cruden, 2008)

The control logic show general principle of multisource system where there has to be compromise between requested and available power from battery and how to keep UC at right voltage reference. Because driving cycle is usually very complex the above solution might not always provide best power capture and source capability.

Jorge Moreno and Micach E. Ortuzar (Moreno et al., 2006) propose a different high-efficiency energy-management system for EVs. They use neural networks (NN). Their system minimizes the energy requirement of the vehicle and is able to work with different primary power sources, such as fuel cells, micro-turbines, zinc-air batteries, or other power supplies with a poor ability to recover energy from regenerative braking, or with a low power capacity for fast acceleration. The experimental EV that was used in their work included lead-acid batteries, an UC bank, and a brushless DC motor (Figure 2-13).

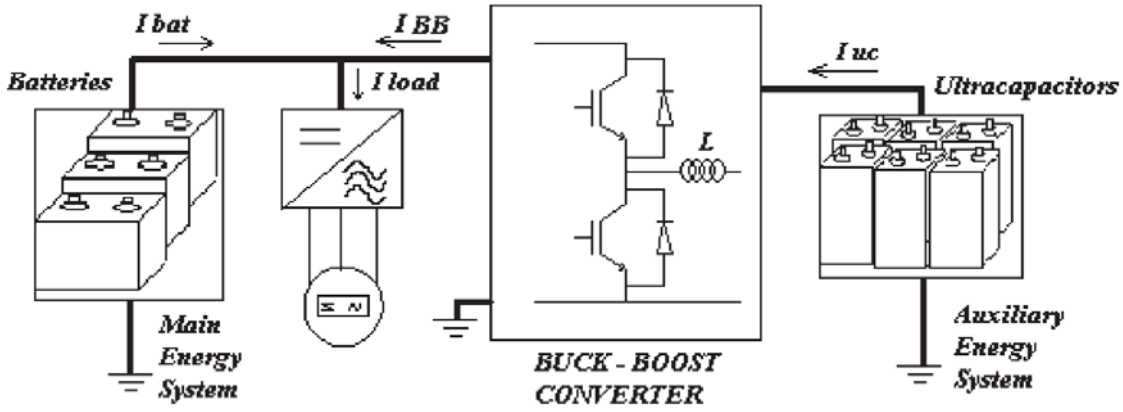


Figure 2-13 Schematic of hybrid system used to verify neutral network algorithm (Moreno et al., 2006)

Figure 2-14 presents the control system based on primary-source voltage, car speed, instantaneous currents, and actual voltage of the UC. When the system included UC, the increase in range was around 5.3% in city tests. However, when optimal control with NN was used, this figure increased to 8.9%.

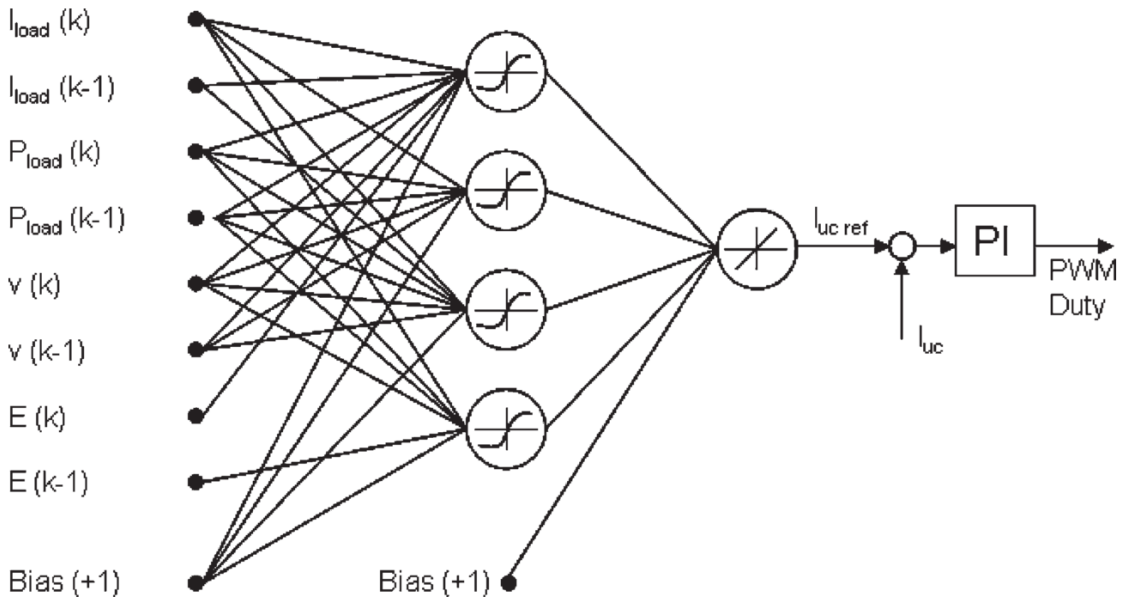


Figure 2-14 Schematic of neutral network used by J Moreno to improve efficiency in multisource system (Moreno et al., 2006)

R. Schupbach and J. Baldda (Schupbach and Balda, 2003) used a different approach for their UC system.

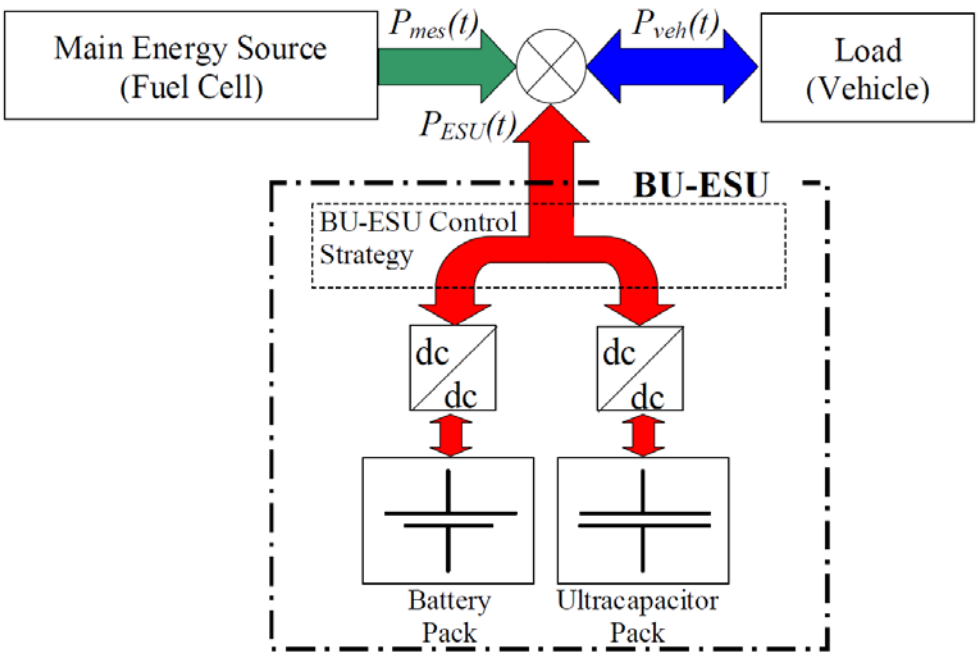


Figure 2-15 Hybrid system with three different sources:, battery, ultracapacitor and fuel cell (Schupbach and Balda, 2003)

Their strategy was elaborated based on the efficiency characteristics of the Auxiliary Energy Source confirmed by UC and a buck-boost converter, where, in order to control energy flow, an optimal-control model was formulated (Figure 2-15). Their system achieved an efficiency improvement of 4.9% from the basic strategy based on UC SOC.

In their work on the Power and Energy Management Structure for Dual Energy Source EV, L. Rosario and P. C. K Luk (Rosario et al., 2006) introduced a modular approach as a hierarchical decision process. The Energy Management Shell provides a prescription for action to the Power Management Shell policy, which in turn generates the feed forward reference power trajectories to the Power Electronic Shell (PES). Outputs of the PES are Pulse Width Modulation (PWM) signals to the power electronic converter.

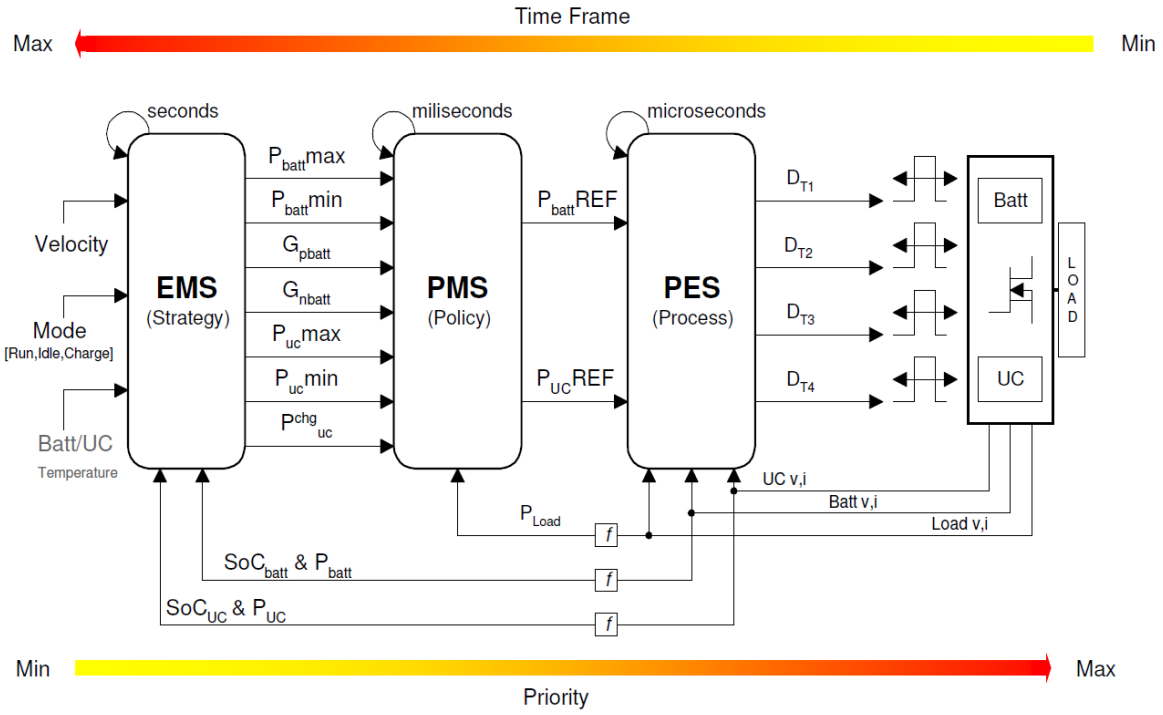


Figure 2-16 Structure of modular Power Energy Management System (Rosario et al., 2006)

The structure presented in Figure 2-16 summarizes the modular structure where:

Energy Management Shell – Is a long term process responsible for strategy, decision epoch in terms of seconds – period dictated by the energy storage system and vehicle dynamics.

Power Management Shell – Is a medium term process responsible for policy, decisions epochs in terms of milliseconds – period dictated by the power demand dynamics.

Short/Immediate term – Power Electronics shell – Process, Decision epochs in terms of microseconds – period dictated by the power electronics converter topology and dynamics.

The research demonstrated that the problem of managing power and energy can be broken down in such a way that three major processes, and the links between them, can be identified. The results obtained from the prototype EV demonstrated the capability of determining the power delivery and energy expenditure of multiple energy systems, as presented in Figure 2-17.

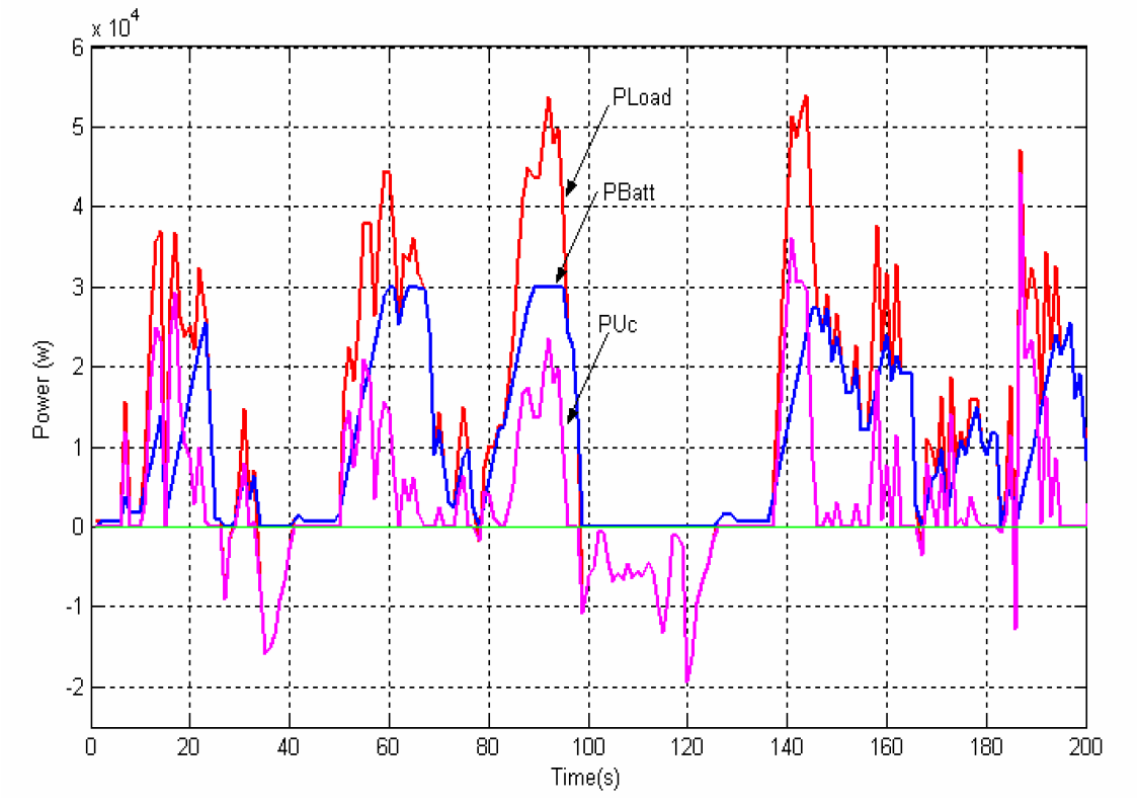
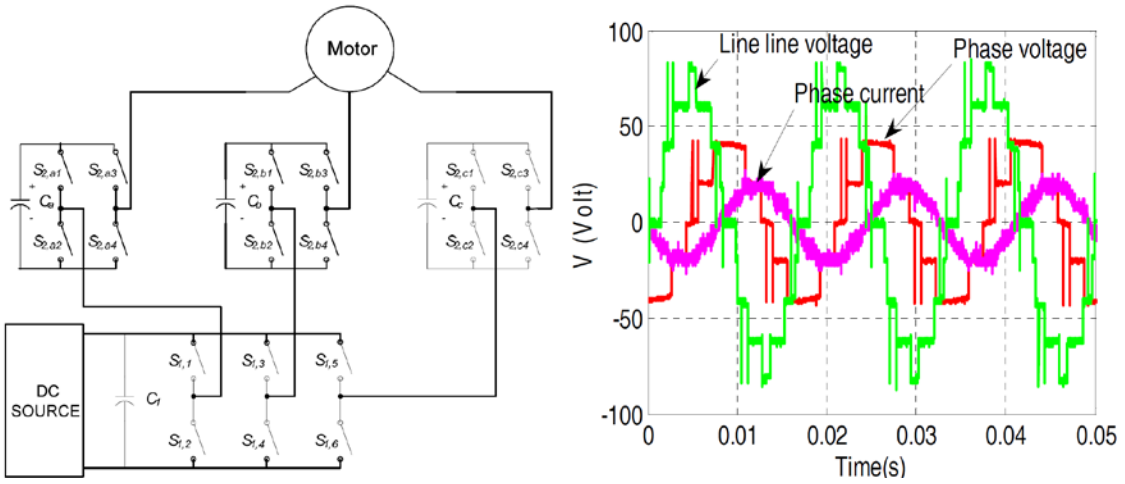


Figure 2-17 Superimposed load power demand (P_{load}) and Batt (P_{bat})- UC (P_{Uc}) power split (Rosario, 2007)

Du, Zhong .(Du et al., 2007) proposed different concept of converter structure for a multisource system to increase voltage amplitude without use of inductors by use of multilevel inverter architecture. Because most EV traction drives require bulky inductors that significantly increase the weight and cost of the system, the H-bridge multilevel boost inverter for EV was introduced. The cascaded boost inverter they proposed uses a standard three-leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg, which uses a capacitor as the DC power source (Figure 2-18).



(a) Multilevel Inverter schematic

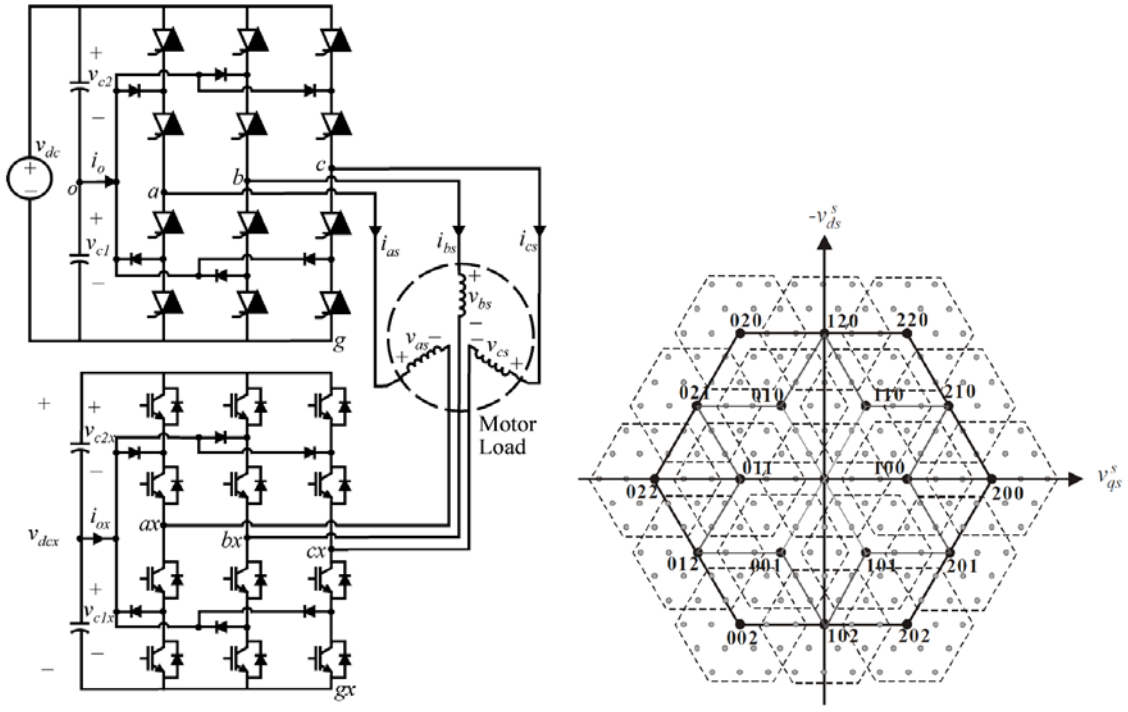
(b) Line to line voltage, phase current and voltage

Figure 2-18 Proposed three-phase boost inverter and its performance (Du et al., 2007)

The method consists of monitoring the output current and the capacitor voltage, so that during periods of zero voltage output, either the switches S2a1, S2a4, and S1, 2 are closed or the switches S2, a3, S2, a4, and S1, 1 are closed, depending on whether it is necessary to charge or discharge the capacitor. It is this flexibility in choosing how to make that output voltage zero that is exploited to regulate the capacitor voltage. Experimental results proved that this type of DC/AC inverter structure is able to boost voltage without using inductors (Du et al., 2007.). The authors did not analyse energy transfer in this system, concentrating on boosting voltage alone. Also the inverter switching was limited

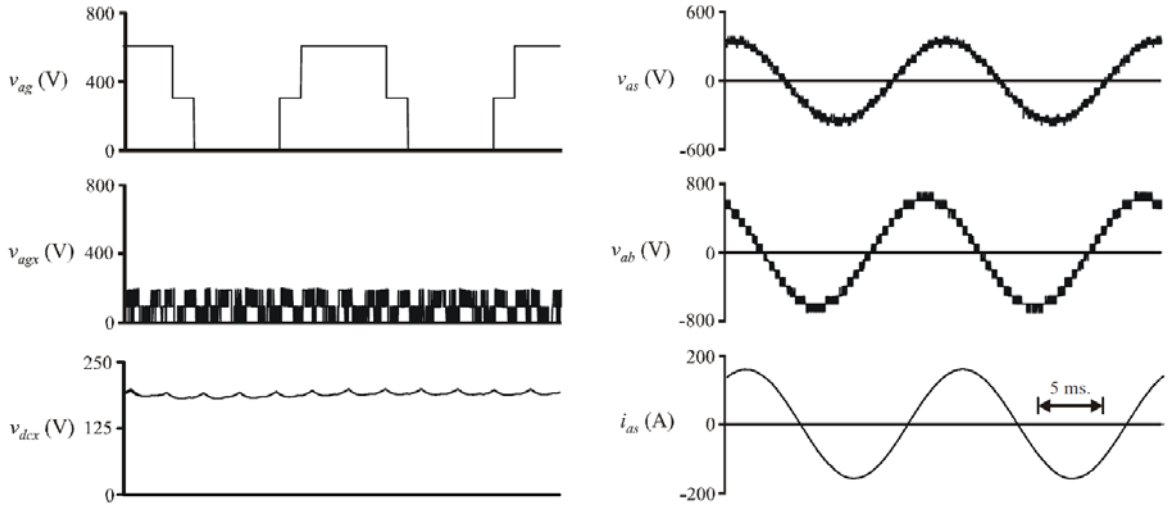
to fundamental frequency without utilizing potential to minimize harmonic content.

Shuai Lu, Keith A. Corzine, and Tom H. Fikse, in their work “Advanced Control of Cascaded Multilevel Drives Based on P-Q Theory” (Lu et al., 2007a)(Lu et al., 2007c) present research on new control methods of cascade multilevel-inverter that consist two sections. The bulk inverter is controlled with fundamental frequency and the conditioning inverter controls real and reactive power flow based on P-Q theory. The conditioning inverter can be set up with zero real power, meaning that load can be supplied solely from a main source. The structure of the multilevel inverter is presented with output waveforms of bulk $V_{ag}(V)$, conditioning inverter $V_{agx}(V)$ and capacitor voltage $V_{dcx}(V)$ (Figure 2-20). It shows in Figure 2-20 that the capacitor voltage is stable, the bulk inverter is switched with fundamental frequency, and the conditioning inverter with high-frequency switching allows output waveform $V_{as}(V)$ to build with very low Total Harmony Distortion (THD).



(a) Multilevel inverter schematic (b) Space vectors coordinates

Figure 2-19 The structure of multilevel inverter for multisource system and its output voltage vectors (Lu et al., 2007a)



(a) Voltage outputted by main and auxiliary section and capacitors voltage

(b) Output voltage and current

Figure 2-20 The structure of multilevel inverter for multisource system and its performance (Lu et al., 2007a)

To control power shearing between sources authors developed the control algorithm as shown in Figure 2-21 for the conditioning inverter based on active power P and reactive Q from P-Q theory (2-1),(2-2):

$$\mathrm{P} = \frac{3}{2}\left(v_{qs}^{s} i_{qs}^{s} + v_{ds}^{s} i_{ds}^{s}\right) \tag{2-1}$$

$$\mathrm{Q} = \frac{3}{2}\left(v_{qs}^{s} i_{ds}^{s} + v_{ds}^{s} i_{qs}^{s}\right) \tag{2-2}$$

Giving auxiliary inverter section reference voltage $v_{qsx}^{s\,*}$ and $v_{dsx}^{s\,*}$ base on product of auxiliary inverter active P_x^* and reactive power Q_x^*:

$$v_{qsx}^{s\,*} = -\frac{2}{3}\left(\frac{P_x^* i_{qs}^{s} + Q_x^* i_{ds}^{s}}{i_{qs}^{s\,2} + i_{ds}^{s\,2}}\right) \tag{2-3}$$

$$v_{dsx}^{s\,*} = -\frac{2}{3}\left(\frac{P_x^* i_{ds}^{s} + Q_x^* i_{qs}^{s}}{i_{qs}^{s\,2} + i_{ds}^{s\,2}}\right) \tag{2-4}$$

It was proven that it is possible to use a multilevel inverter together with an UC and batteries where instant control of real power between the battery, UC, and motor is performed. The power electronic needed for proposed become much

more complicated and expected high cost doesn't make this system commercially attractive for EV. The other disadvantage of the proposed inverter architecture is complex design of modulation scheme (Lu et al., 2010).

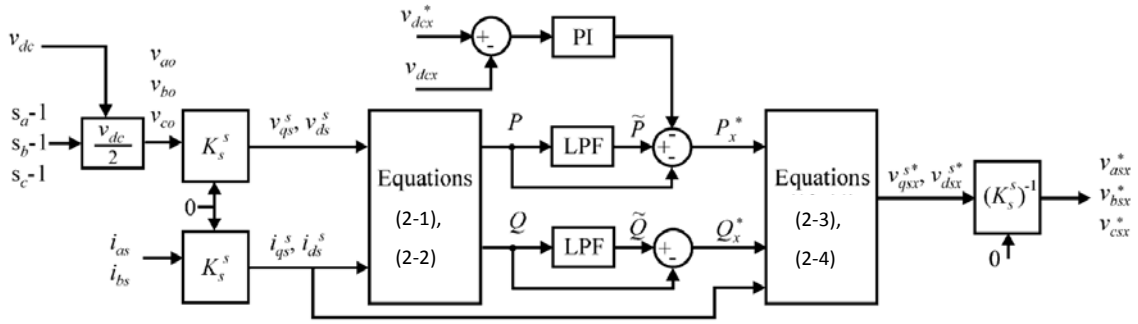


Figure 2-21 Block diagram of P-Q conditioning inverter controller (Lu et al., 2007a)

Implementation of the multilevel inverter with battery and UC continues to get a lot of attention for various power conversion systems. Especially the structure of Modular Multilevel Converter (MMC) with multiple sources becomes popular topic for renewable energy conversion applications (Mathe et al., 2016).

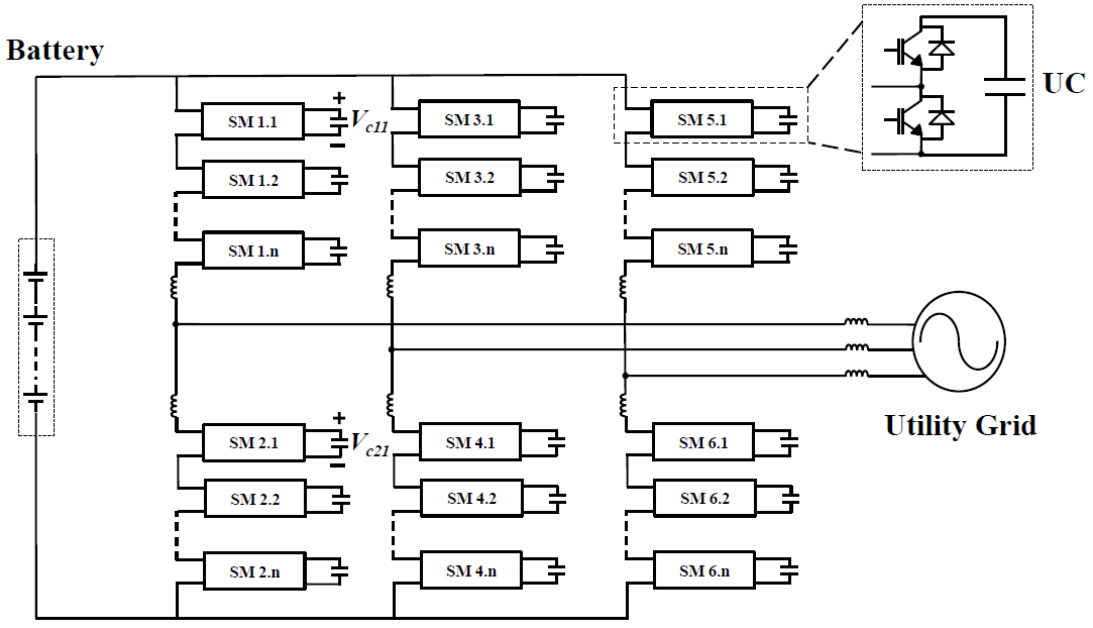


Figure 2-22 Modular Multilevel Converter (MMC) with multiple sources (Guo and Sharma, 2015)

Example of such a system propose F. Guo and R. Sharma (Guo and Sharma, 2015). The topology presented in Figure 2-22 prove to improve efficiency, reduce harmonics and has good reliability. Because this structure type require high number of components it is unlikely that it will become popular in EV because impact on vehicle price (Quraan, Yeo and Tricoli, 2016), (Zheng et al., 2014).

2.1.4 Power Management for multisource systems

The main purpose of the multi-sourced system is to extend the capability of the motor drive by adding sources with high power density that can compensate limitations of the main high-energy source (Allègre, Trigui and Bouscayrol, 2013). The high power source should be able to capture most of the available kinetic energy during breaking and supply high power to meet the additional demand during acceleration (Grbovic, P.r et al., 2011). There are many methods found in literature that based on sophisticated relation are able to find best reference voltage to improve efficiency and battery lifetime. As an example its worth to mention methods that use Neural Networks (Zgheib and Al-Haddad, 2015), (Moreno et al., 2006), Model Predictive Control (Mane et al., 2016),(Bordons et al., 2010) and control directly in reference to vehicle kinetic energy (Loukakou et al., 2010), (Rosario et al., 2006). The last solution is briefly described in this section to present relation between simple UC reference voltage and vehicle kinetic energy and how in simple way utilize UC (Burke and Miller, 2011).

The vehicle's kinetic energy available for regeneration can be simply described as:

$$E_{\mathrm{Re}g,Max} = \frac{1}{2} M v^2 \tag{2-5}$$

M-vehicle mass, v- vehicle velocity

On the other hand, in systems that use UC, the amount of energy that can be regenerated is related with voltage squared and is represented by:

$$\Delta E_{UC} = \frac{1}{2} C_{UC} \left(V_{UC\_Max}^2 - V_{UC}^2 \right) \tag{2-6}$$

C_{UC} - ultracapacitor capacitance, V_{UC_Max} - maximum capacitor voltage, V_{UC} - UC voltage

This means that to regenerate the most kinetic energy, the UC voltage should be controlled at the reference set point that meets the following equation:

$$V_{UC}(v) \leq \sqrt{V_{UC_{Max}}^2 - \frac{M}{C_{UC}} \cdot v^2} \tag{2-7}$$

M - vehicle mass, v - speed, C - capacitance

The relation above is often found in the literature as a one of the simplest solution for Electric Vehicles. Because the scope of this research is focused mainly on system architecture, this dependency is implemented into the system based on existing research without detailed evaluation. The control system for the above relation is presented in Figure 2-23 where additionally Battery Power Limit module protect battery against operation outside nominal power.

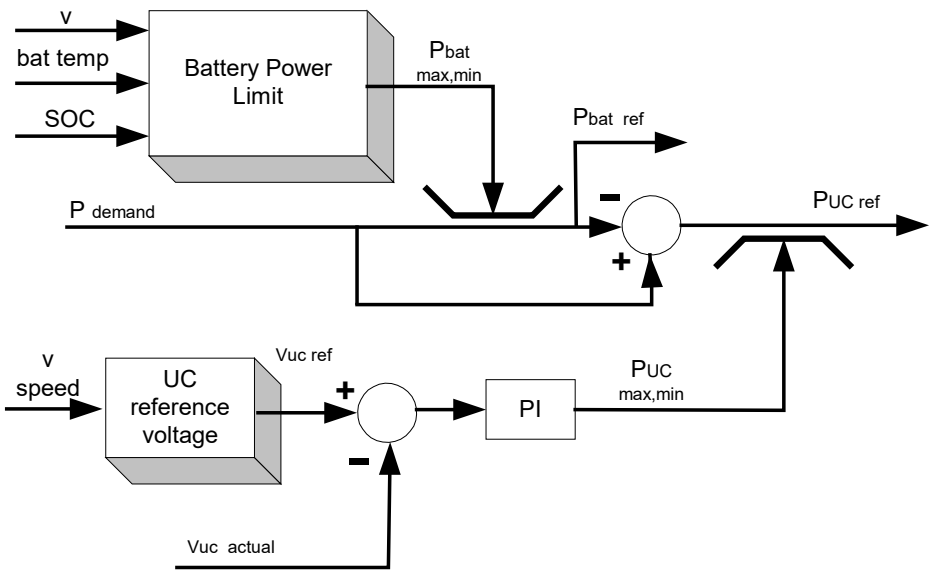


Figure 2-23 Control for power sharing between battery and UC

The proposed system provides reference power for the UC that will share power with the battery in such a way that the battery will not exceed the set power levels in regenerative and motoring modes and the UC voltage level will allow the capture of maximum kinetic energy.

The square relation between the energy stored and the UC state of charge (2-6) means that to utilize the most capacitor energy it is not necessary to operate with a large difference between the minimum and maximum voltage. From the calculations (2-8) it can be seen in Figure 2-24 that with a 30% voltage drop almost 50% of the stored energy can be utilized.

$$E_{pr}(V_{dr}) = \frac{E_u(V_{dr})}{E_u(1)} \tag{2-8}$$

Where

$$E_u(V_{dr}) = \frac{1}{2} C\, V_{Max}^2 \left[1 - \left(\frac{V_{dr}}{100}\right)^2\right] \tag{2-9}$$

and

$$V_{dr} = \frac{V_{Min}}{V_{Max}} \tag{2-10}$$

V_{dr} - proportional discharge, $E_u(V_{dr})$ – energy stored in capacitor, $E_{pr}(V_{dr})$ - unified energy

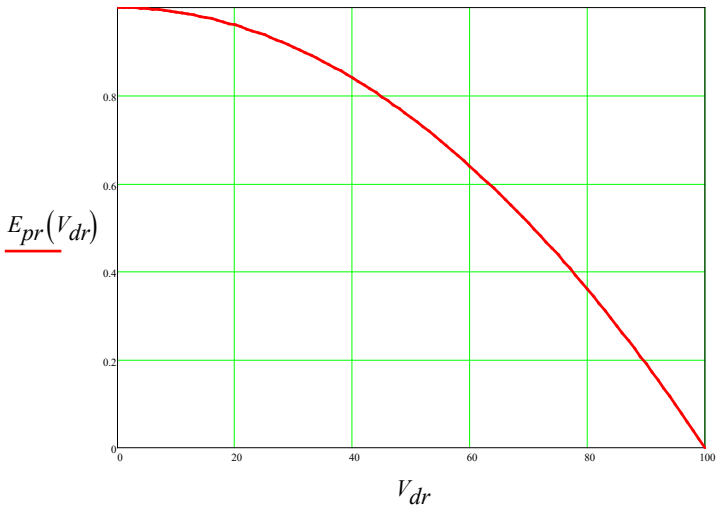


Figure 2-24 Relationship between capacitor voltage V_{dr} and stored energy E_{pr}

This relation show that to use most UC energy it is not needed to completely discharge the UC. In cases where there is imposed limit on the minimum UC voltage it could be possible to additionally use their voltage as an additional passive source for example to compensate a non-active power.

2.2 Space vectors and their representation in the coordinate system

Most of EV available on the market in their drive train use an AC electric motor. There are many types of AC motors depending on rotor type additionally there is also many variants with different phase numbers (Subotic et al., 2013). Still the most common configuration is motor supplied by three-phases. To simplify calculations there is widely known method to convert phase current, flux and voltage into rotating space vector (Álvarez et al., 2011). In this part the theoretical background is overviewed to help reader easier understand further chapters . Presented analysis provide summary of M. Kazmierkowski and H. Tunia work on Control of Converter-Fed drives (Każmierkowski M. P., 1994).

2.2.1 Physical basis

The magneto-motive force (MMF) induced by the current in a solenoid coil, which may represent, for example, phase A of a three-phase motor stator is given by the formula.

$$F_{mA} = z_A I_A \tag{2-11}$$

This magneto-motive force has a precisely defined direction in space, which lies along the magnetic coil axis. It can therefore be treated as a vector (Figure 2-25).

$$\boldsymbol{F}_{mA} = z_A \boldsymbol{I}_A \tag{2-12}$$

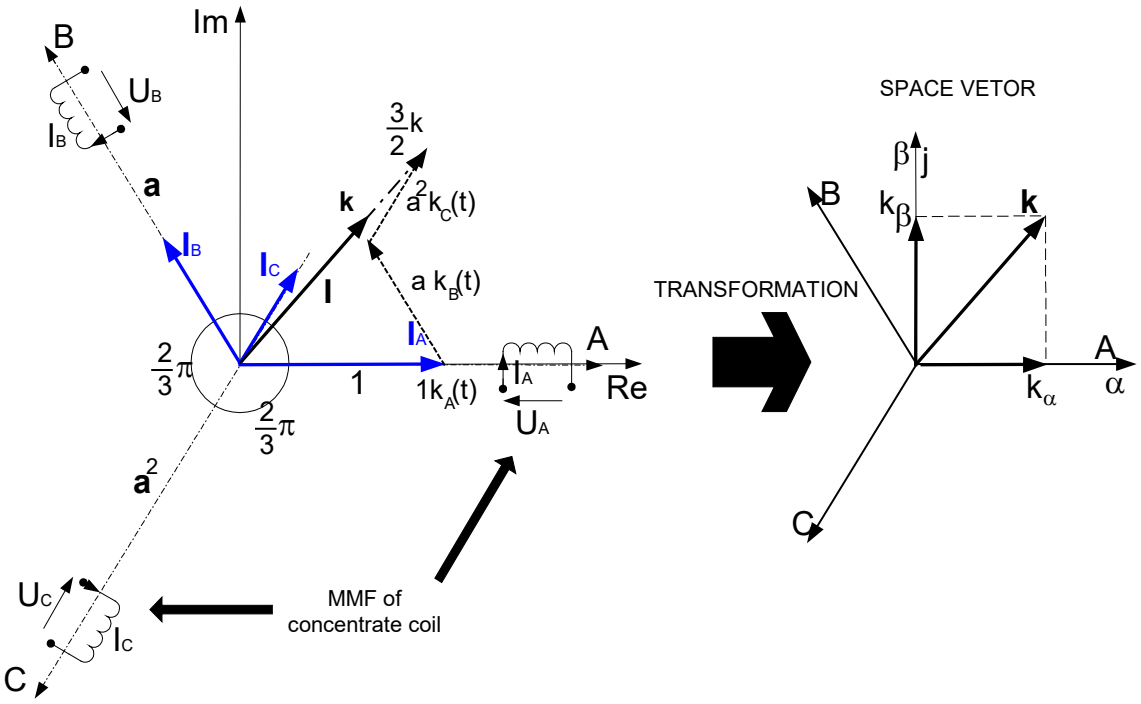


Figure 2-25 Construction of resultant space vector k of three-phases motor stator current and its representation in stator-fixed rectangular system of coordinates

Furthermore, the current $\boldsymbol{I}_A$ can be treated as a vector. Thus conceived, the vector $\boldsymbol{I}_A$ is collinear with the magnetic axis of the coil, thanks to which its spatial position is unequivocally defined by the position of the coil. Its amplitude, on the other hand, is equal to the instantaneous value of the current flowing in the coil. It is worth pointing out that this current may have any wave form. The phase winding B and C of the motor stator can be ascribed phase current vectors $\boldsymbol{I}_B$ and $\boldsymbol{I}_C$, respectively (2-13). Vector summation yields.

$$\boldsymbol{I} = \boldsymbol{I}_A + \boldsymbol{I}_B + \boldsymbol{I}_C \tag{2-13}$$

Vectors $\boldsymbol{I}_A$, $\boldsymbol{I}_B$, $\boldsymbol{I}_C$ lie in the plane of the stator cross-section perpendicular to the motor shaft axis. The resultant vector $\boldsymbol{I}$ is coplanar with vectors $\boldsymbol{I}_A$, $\boldsymbol{I}_B$, $\boldsymbol{I}_C$. Its amplitude and position depend on the instantaneous values of phase current $\boldsymbol{I}_A$, $\boldsymbol{I}_B$, $\boldsymbol{I}_C$.

If the (Gaussian) complex plan is positioned in such a way that real axis coincides with the magnetic axis of the phase winding (2-14)-(2-16), one can write.

$$\boldsymbol{I}_A = 1\, I_A \tag{2-14}$$

$$\boldsymbol{I}_B = I_B\, e^{j\,2\pi/3} = \boldsymbol{a}\, I_B \tag{2-15}$$

$$\boldsymbol{I}_C = I_C\, e^{j\,4\pi/3} = \boldsymbol{a}^2\, I_C \tag{2-16}$$

Where

$$\boldsymbol{a} = e^{j\,2\pi/3} = -1/2 + j\,3^{-2}/2 \tag{2-17}$$

$$\boldsymbol{a}^2 = e^{j\,4\pi/3} = -1/2 - j\,3^{-2}/2 \tag{2-18}$$

Hence, equation (2-13) takes the complex calculus form

$$\boldsymbol{I} = 1\, I_A + \boldsymbol{a}\, I_B + \boldsymbol{a}^2\, I_C \tag{2-19}$$

This resultant vector $\boldsymbol{I}$ given by equation (2-13) or (2-19) is called the space vector.

The space vector concept can be extended to other quantities describing electric motors, such as voltages or flux linkages. Let it be pointed out that the term “space vector“ does not denote a physical vector quantity because voltage and current, for example, are not vectors, strictly speaking. It is, nevertheless, an analytical quantity that refers to a plane and obeys the laws of vector algebra.

2.2.2 Definitions and basic properties

A three-phase symmetric system represented in natural coordinate system by phase quantities, such as voltages, currents or flux linkages, can be replaced by one resultant space vector of, respectively, voltage, current and flux linkage. If $k_A(t),\ k_B(t),\ k_C(t),$ denote arbitrary phase quantities in a system of natural coordinates (A,B,C) satisfying the condition.

$$k_A(t) + k_B(t) + k_C(t) = 0 \tag{2-20}$$

Then a space vector is defined as

$$\boldsymbol{k} = 2/3[\boldsymbol{1}\, k_A(t) + \boldsymbol{a}\, k_B(t) + \boldsymbol{a}^2\, k_C(t)] \tag{2-21}$$

Thus defined, a space vector is a complex quantity, the factor 2/3 in the definition equation (2-20) being the normalization factor (generally: 2/ms, where "ms" is the number of phases of a multiphase system). The factor 2/3 adopted in (2-20) guarantees, for the case of sinusoidal waves, equality of the space vector amplitude and the amplitude of instantaneous per phase waves. This is especially convenient in the analysis and synthesis of converter drives.
An example of space vector construction in accordance with definition (2-21) is shown in Figure 2-25.

2.2.3 Space vectors in coordinate system

An important advantage of space vectors as a mathematical tool applied to the analysis of electric machines is that they can be represented in various systems of rectangular coordinates.

Introducing a stator-fixed system of rectangular coordinates such that $\boldsymbol{\alpha}$ is the real axis and $\boldsymbol{\beta}$ the imaginary axis, and resolving the space vector $\boldsymbol{k}$ into its real and imaginary parts, yields (Figure 2-25)

$$\boldsymbol{k} = k_\alpha + j\, k_\beta \tag{2-22}$$

Where

$$k_\alpha = Re\, \boldsymbol{k} = Re\, 2/3[\boldsymbol{1}\, k_A + \boldsymbol{a}\, k_B + \boldsymbol{a}^2\, k_C] = 2/3[\boldsymbol{1}\, k_A(t) - 1/2(k_B + k_C)] \tag{2-23}$$

If condition $k_A(t) + k_B(t) + k_C(t) = 0$ is satisfied, obtain $k_\alpha = k_A$

Similarly,

$$k_\alpha = Re\, \boldsymbol{k} = Re\, 2/3[\boldsymbol{1}\, k_A + \boldsymbol{a}\, k_B + \boldsymbol{a}^2\, k_C] = 2/3[\boldsymbol{1}\, k_A(t) - 1/2(k_B + k_C)] \tag{2-24}$$

2.3 Multilevel Voltage Source Inverters

2.3.1 Introduction

High power and efficiency requirement of modern day drive train push power electronic development towards more sophisticated solutions. The high voltage become a standard for current EV what combined with high frequency switching creates many issues such as Electromagnetic Interference (EMI) and components stress. Also high switching losses require better components and good thermal management. The other solution is to use more advance voltage converter structures that will better balance thermal and electrical stresses. In particular, multilevel inverters for adjustable speed drive applications not only effectively reduce harmonics content and EMI problems, but also avoid possible high frequency switching dv/dt induced motor failure an might reduce switching losses (Kazmierkowski et al., 2011),(Lai, Member and Peng, 1996). Results from many authors confirm that implementation of multilevel inverter for drives and increased number of levels improve the system total efficiency. (Krug, Bernet and Fazel, 2007) (Papastergiou, Wheeler and Clare, 2008). The better efficiency of multilevel inverters is related with lower THD and lower switching losses since multiple sources that are switched have smaller amplitude (Qashqai, Sheikholeslami and Vahedi, 2016) (Jalili et al., 2005).

Contemporary topologies of multilevel inverters are based on four basic solutions: (Rodríguez, Member and Lai, 2002) (Hartman M., 2006)

- Neutral-point-clamped inverters
- Flying-capacitor inverters
- Diode-clamped inverters
- Insulated-H-Bridge-inverters

2.3.2 Neutral-point-clamped inverters

The concept of a three-phase inverter with neutral point clamped (NPC) is based on the artificial division of voltage of circuit intermediary Ud on two values of Ud/2 with the help of the capacitive divisor (Orfanoudakis et al., 2013). The

midpoint of connection of both condensers is the potential of reference output voltage. An example of NPC converter in single phase system is presented in Figure 2-26. This type of structure become very popular since it requires only one source separated in middle point. Because using only NPC inverter doesn't allow utilizing multiple sources this structure is not investigated further. A three-phase NPC converter requires 12 switches and six additional diodes to achieve five levels at the output. The other disadvantage of this inverter is that most of the time inverter will conduct through diode's what additionally increases conducted losses (Zheng, 2009).

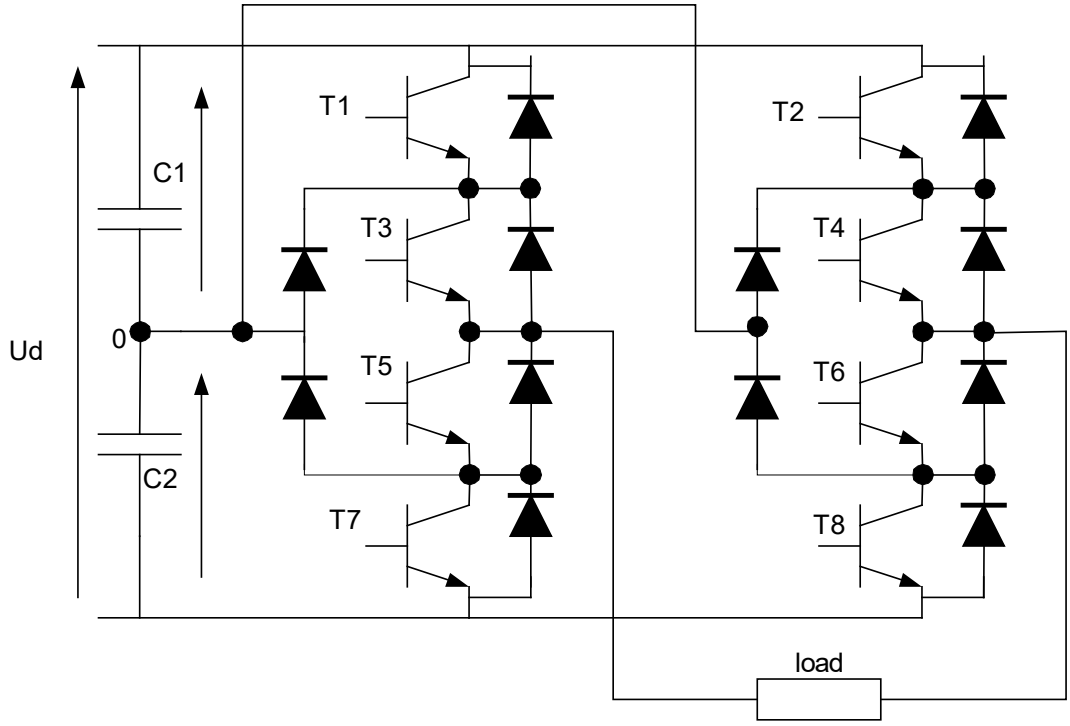


Figure 2-26 Basic one phase NPC inverter

2.3.3 Flying-capacitor inverters

The topology introduced by Meynard and Foch in 1992 is a very popular structure and is constantly evolving with different multicellular architectures (Meynard et al., 2002). The typical flying capacitor inverter includes two serial capacitors C connected parallel to DC voltage source Ud which is divides, and a series of capacitors connected by inverter switches to a load circuit (Figure 2-27). As the clamps of the capacitors are not directly connected to the voltage source, their potential is variable (hence the name flying-clamped inverter FCI).

The basic structure of the inverter for a single phase is presented in Figure 2-27. In one-phase FCI inverter capacitors C connected to source voltage Ud divides this voltage on Ud/2. Capacitors C1, C2, and C3 connected to the inverter switches must first be charged to the right voltage. The most common values are Uc1=1/4Ud; Uc2=1/2Ud; Uc3=3/4Ud. These capacitor-voltage values give the same blocking voltage of all switches T1-T8. The proper switching sequence is able to form output voltage from values: -Ud/2; -3/8Ud; -1/4Ud; -1/8Ud; 0; 1/8Ud; 1/4Ud; 3/8Ud; Ud/2.

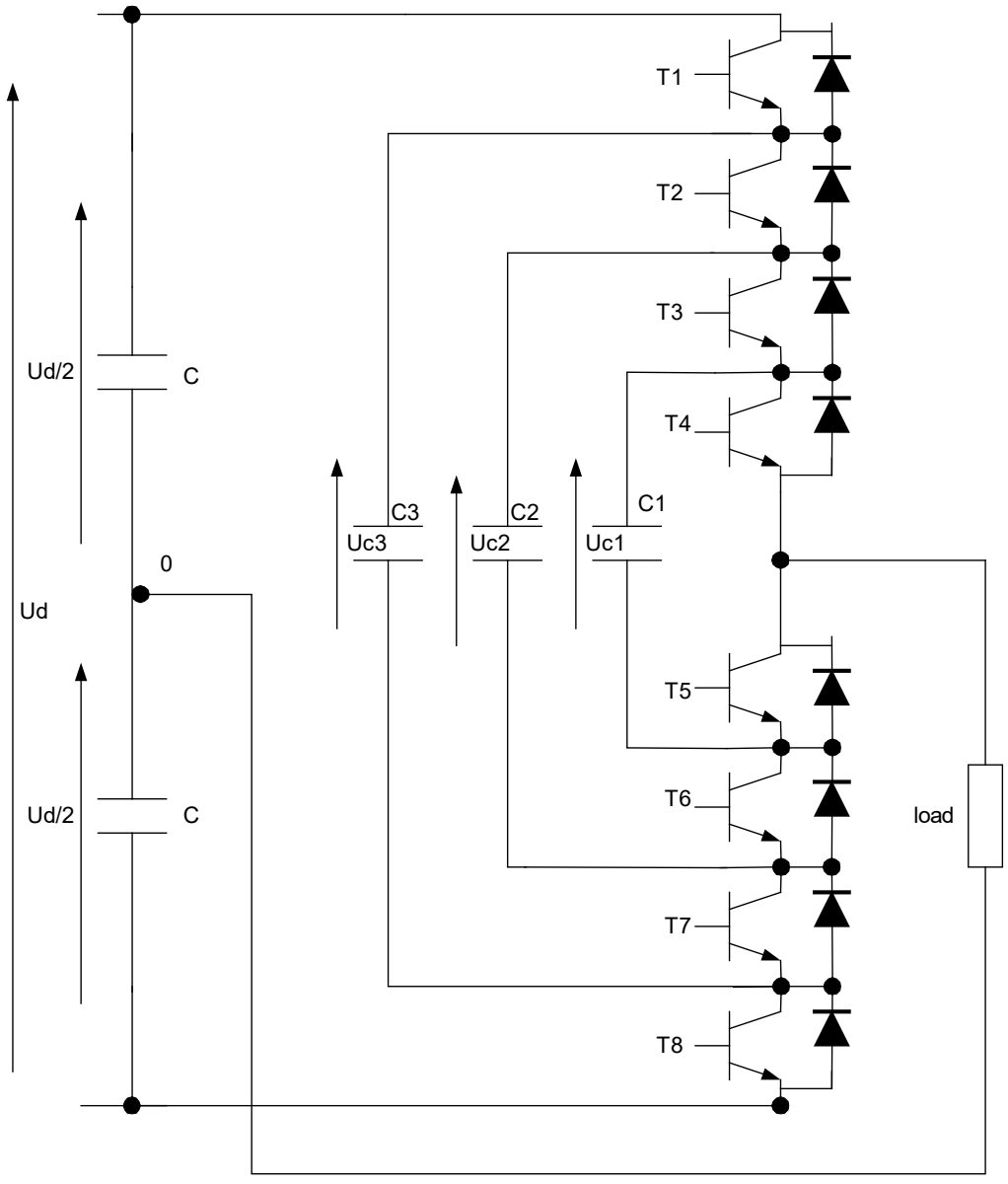


Figure 2-27 Basic one-phase FCI inverter

The main advantage of a flying-capacitor multilevel voltage source inverter is that it include large amount of storage capacitors what provides extra ride through capabilities during power outage. The structure also provides switch combination redundancy for the balancing of different voltage levels. Since the number of output voltage level can be expanded it is possible to reach the sufficient number of levels to minimise the harmonic content low enough to avoid passive filters. Additionally the real and reactive power flows can be controlled, making converter a possible candidate for high voltage DC transmissions. The disadvantages of this topology is an excessive number of storage capacitors that is required to achieve high number of converter levels. High-level systems are more difficult to package and more expensive with the required bulky capacitors. The inverter control is usually very complicated, and the switching losses are high for real power transmission (Ghias et al., 2016). Because the maximum output voltage is equal to main voltage source Ud it mean that in this structure it is impossible to boost inverter output voltage what could be desire for high speed electric motor drive.

2.3.4 Diode-clamped inverters

The Diode-Clamped Inverter DCI topology use diodes for clamping different levels of voltage (Figure 2-28). Thus, not only the waveform quality is improved but also the switching devices voltage stress is reduced by a (m-1) factor, where m denotes the number of levels. However, the clamping diodes stress can vary among the levels (Jayasinghe et al., 2011). Also, the DC-link capacitors balance can be difficult to achieve, especially for high level number in active power applications (Lee, 2009). Similarly to FCI inverters the main advantages of diode-clamp multilevel voltage source inverters is possibility to expand number of levels at the output to the state where harmonic content is low enough so the passive filters are not needed. Reaching high number of output level allow to additionally increase efficiency by switching devices at fundamental frequency.

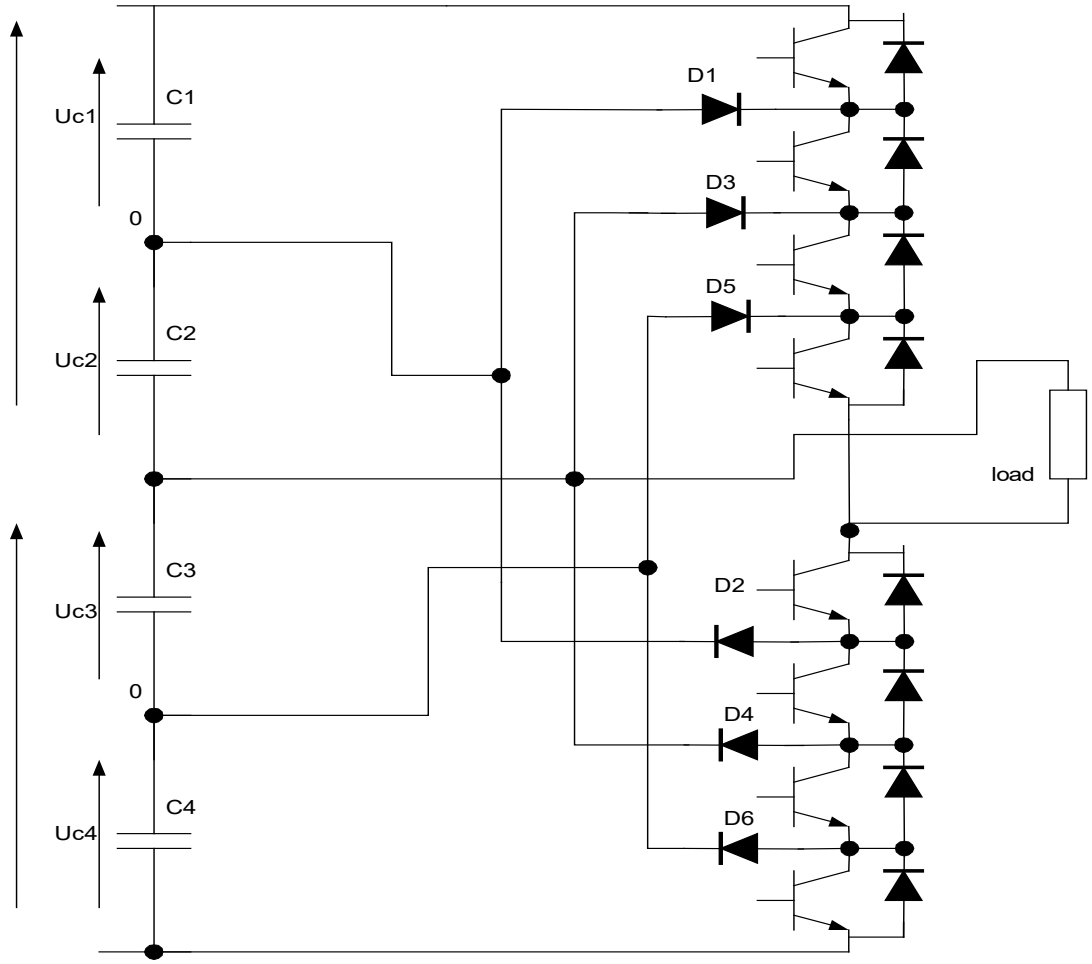


Figure 2-28 Basic one phase DCI inverter

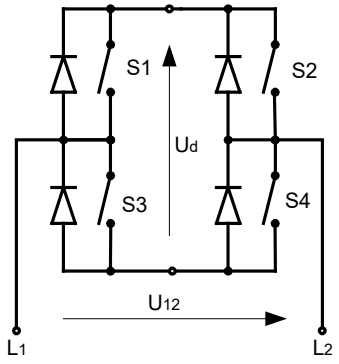
The main disadvantage of this topology is excessive number of clamping diodes needed when the number of levels is high. The real power flow is difficult to control but power shearing between sources can be achieved without a need of additional DC/DC converters. The power flow control requires complicated modulation strategy to balance DC link voltages (Jayasinghe et al., 2011).

2.3.5 Insulated H-Bridge inverters

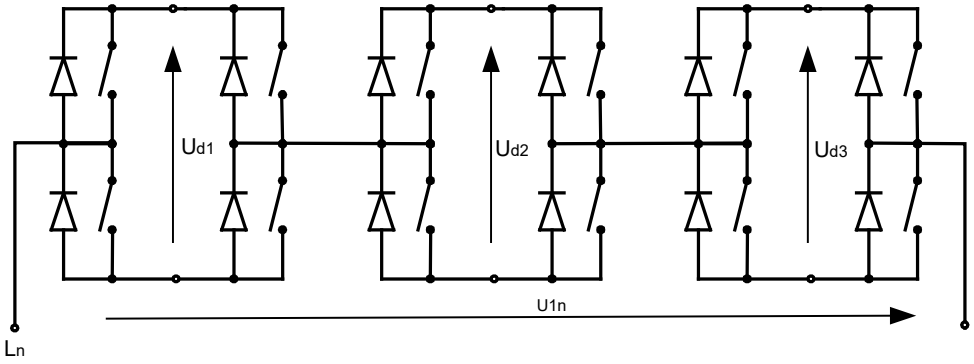
The commercial application of multilevel, inverters is frequently reduced to Insulated-H-Bridge-Inverters (IHBI) topology especially for photovoltaic power converters (Yu et al., 2016). The IHBI topology is based on the commonly known Graetz's bridge, which serves the role of the switch in the constant current to alternating current transformation (DC/AC) (Figure 2-29). The switches S1-S4 are connected in pairs. When S1,S4 are on (S2,S3 off) the

positive voltage +Ud is connected to line L1 and when. S2, S3 are on (and (S1,S4 are off) the L1 has the negative voltage –Ud. To receive zero voltage on line L1 either pairs S1,S2 or S3,S4 have to be on. Therefore, a single Greatz's bridge can generate output voltage waveform of maximum three levels of voltage: +Ud,0,-Ud.

The ease with which to generate waveforms of three-phase output voltage by a single inverter cell has served as a basis for combining single inverters into a chain of inverters as shown in Figure 2-29. This combination of inverters is known as a cascade or chain. The output voltage is the sum of the individual cell voltages. In the case of same cells (Ud=Ud1=Ud2=Udn) the output voltage waveform is a level waveform (2n+1) of the maximum value of voltage of Um=nUd. Each cascade cell plays a part in modifying the value of the output voltage for a definite period of time as a result of the control strategy.



(a) Single Greatz's bridge



(b) Cascade of "n" one phase Greatz's bridges

Figure 2-29 One-phase Insulated H-Bridge inverter

In conclusion, the main advantage of IHBI multilevel voltage source inverter is the least number of components among all multilevel converters to achieve the same number of voltage levels. The modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage-balancing capacitors, which gives the flexibility to expand the number of levels easily without introducing undue complexity in the power circuit. Additionally the soft-switching can be used in this structure to avoid bulky resistor capacitors diode snubbers. The main disadvantage is that there is a need of separate DC sources for real power conversions, and thus its applications are somewhat limited. In case of multisource systems the need of isolated sources can be advantage.

2.3.6 Modified three-phase cascade of two inverters

Contemporary research has focused on two fields: First, it seeks new inverter structures or modifies the existing ones in order to gain better technical and technological qualities. Second, it searches for new solutions to inverter control to enhance their electrical parameters. To minimise inverters cost approach to reduce device count in multilevel topologies become very attractive. In literature there is many examples of inverter modification where part number was reduced at compromise of loss modularity, more complex architecture and modulation scheme (Gupta, Ranjan and Bhatnagar, 2016). One of the concepts of modifying two single cascade inverters with a three-phase cascade is to replace three single cells with one three-phase bridge (Figure 2-30) (Suh B.S., 1999).

The operational principle of the inverter set shown in Figure 2-30 takes account of a one- and a three-phase Graetz's bridge operation. The line-to-line voltage among A, B, and C meet the typical waveform requirements in three-phase circuits. The output voltage waveform (line-to-line) will depend on the correlation between the voltage of isolated sources: U_d, U_{d1}, U_{d2} and U_{d3}. For separate voltage sources which are in following relation: $1/2U_d = U_{d1} = U_{d2} = U_{d3}$, the proposed topology of the inverter can modify the phase voltage waveform by

five levels (+1U_d; 1/2U_d; 0; -1/2U_d; -U_d), whereas the line-to-line voltage is modified by a maximum of nine levels (Kot, 2003).

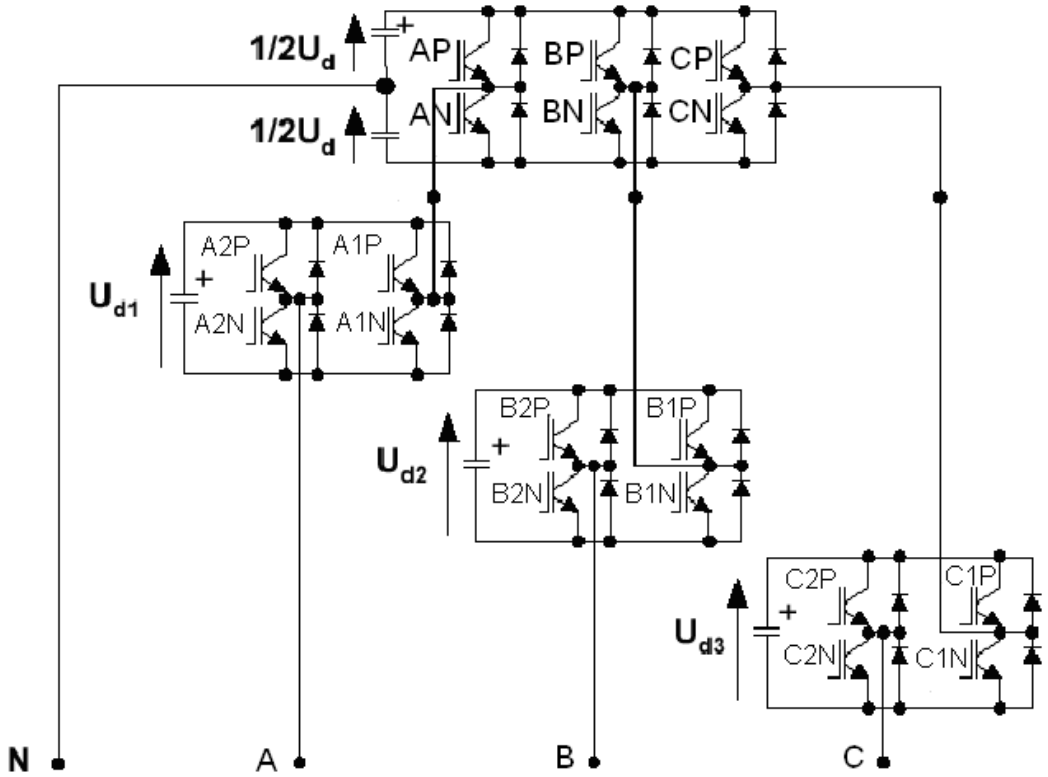


Figure 2-30 Modified three-phase voltage inverter in cascade topology

The topology can be expanded further to achieve more voltage levels by adding H-Bridges into phases. It was proven by authors (Mariethoz, 2013) that this structure can be supplied by only one active source and remaining H-Bridges can be supplied with passive capacitance. In such a case special modulation scheme has to be implemented that will select adequate sequence to control energy flow. The existing modulation schemes do not allow to control power independently to active and passive power variation at the output.

2.4 Electric Motor analysis

Currently the highest performance and efficiency from an electric motor are achieved by Permanent Magnet Synchronous Motors (PMSM). Of the many types of PMSM motor, that with internal permanent magnets (IPMSM) has additional reluctance torque, allowing an extension of the flux weakening region

and improving maximum speed (Wu, 2006). This becomes important aspect especially for drivetrain applications where gears are not used and high operational speed is required. The flux weakening method has been widely used for many types of AC motors such as Induction Motor (IM) and PMSM (Bernatt et al., 2007). The principles of this method are based on decreasing stator flux so the MMF is reduced and amplitude of motor voltage doesn't have to increase further (Lei, Xuhui and Shan, 2009). The limitation of this strategy is that the output torque becomes reduced. One of the most popular and effective methods to provide maximum torque capability for IPMSM is the MTPA strategy (Maximum Torque Per Ampere) that has been well analysed by authors (Howe, Chen and Zhu, 2000) and (Hoang, Zhu and Foster, 2012). The method in this section is analysed further to better understand the voltage, active power and passive power limitations. The principles of MTPA method are based on basic dynamic equations of IPMSM (Ko, Choi and Chung, 2006):

$$\frac{d\psi_{qse}}{dt} = V_{qse} - R_s i_{qse} - \omega_r \psi_{dse} \tag{2-25}$$

$$\frac{d\psi_{dse}}{dt} = V_{dse} - R_s i_{dse} + \omega_r \psi_{dse} \tag{2-26}$$

For

$$\psi_{qse} = L_q \cdot i_{qse} \tag{2-27}$$

$$\psi_{dse} = L_d \cdot i_{dse} + \psi_M \tag{2-28}$$

$$T_e = \frac{3}{4} p(\psi_{PM} i_{qse} + (L_d - L_q) i_{dse} i_{qse}) \tag{2-29}$$

Where

R_s - motor phase resistance

L_d - d axis inductance L_q- q axis inductance

ω_r - motor angular velocity

p- number of magnetic poles

T_e - Electromagnetic torque

i_{dse} – synchronous current in d frame

i_{qse} – synchronous current in q frame

V_{dse} - voltage in d axis synchronous frame

V_{qse} – voltage in q axis synchronous frame

ψ_{qse} - flux linkage in q axis

ψ_{dse} - flux linkage in d axis

ψ_{PM} - permanent magnet flux linkage in synchronous frame

By transforming above equations it is possible to find stator reference current depending on motor speed to achieve maximum torque. For operation below base speed the reference current i_{dse}* is selected by using the following equation (2-30) for maximum torque per ampere.

$$i_{dse}{}^{*}=\frac{-\psi_{PM}+\sqrt{\psi_{PM}{}^{2}+8(L_d-L_q)^2 I_S{}^{2}}}{4(L_d-L_q)} \tag{2-30}$$

For operations above base speed in filed weakening region the magnetizing current set point i_{dse}* can be selected by MTPA law under voltage and current constraints (2-31).

$$i_{dse}{}^{*}=\frac{\psi_{PM}L_d}{L_d{}^{2}-L_q{}^{2}}-\sqrt{\frac{L_q{}^{2}}{(L^2{}_d-L^2{}_q)^2}\psi^2{}_{PM}+\frac{\frac{V^2{}_{SC}}{\omega^2{}_r}-L^2{}_q I^2{}_s}{L_d{}^{2}-L_q{}^{2}}} \tag{2-31}$$

The voltage and current constraints from the inverter and motor determine the operating limits of a motor drive system and affect the maximum torque and power capabilities.

The maximum available torque current corresponding to the maximum transient available torque must be checked and modified to satisfy both voltage and current constraints:

$$I_s^{\,2} = I_{dse}^2 + I_{qse}^2 \le I_{con}^2 \text{ - current constraint} \tag{2-32}$$

$$V_s^{\,2} = V_{dse}^2 + V_{qse}^2 \le V_{con}^2 \text{ - voltage constraint} \tag{2-33}$$

For steady state the electrical equations of the machine are given as:

$$V_{qse} = R_s I_{qse} + \omega_r (\psi_{PM} + L_d I_{dse}) \tag{2-34}$$

$$V_{dse} = R_s I_{dse} - \omega_r L_q I_{qse} \tag{2-35}$$

In Figure 2-31, the relations described in the above equations are illustrated where, $I_q(I_{dx})$ is the nominal current constraint (red), $I_{gov}(I_{dx})$- maximum current constraint (blue dot), $I_{qu}(I_{dx})$- voltage constraint for low speed (green dot), $I_{qt}(I_{dx})$ constant torque curve (purple dot), $I_{qu2}(I_{dx})$- voltage constraint for high speed (brown dor), $I_{qm}(I_{dx})$ – Maximum Torque Per Ampere (blue).

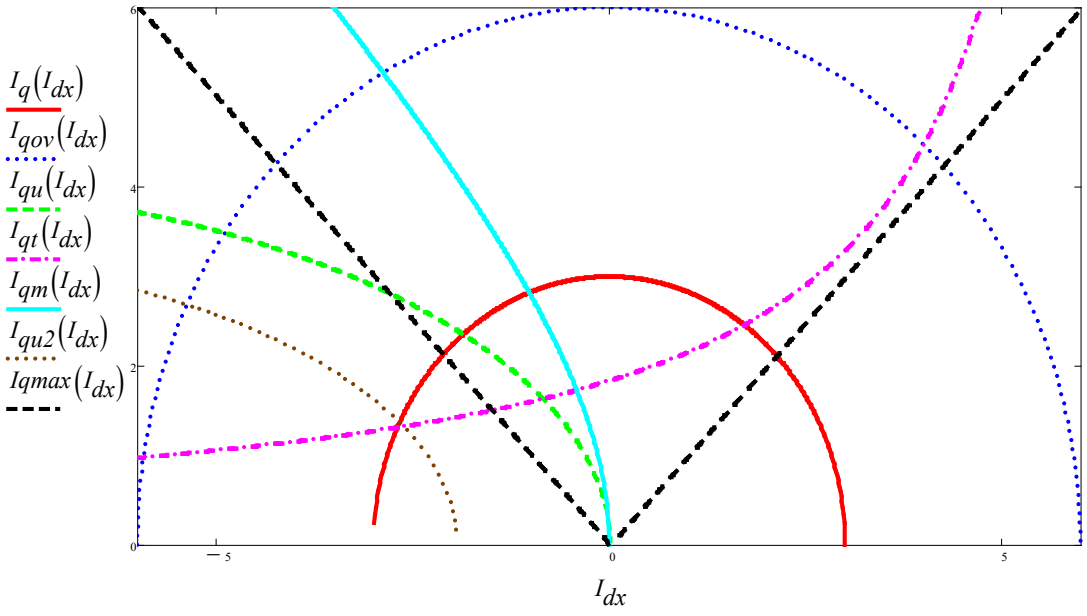


Figure 2-31 IPMSM control characteristics on d-q frame

It is possible to notice in above Figure 2-31 that available current is limited by current, voltage and torque curves and that to achieve higher speeds higher amplitude of stator current in d axis is needed (I_{dx}) (to be in envelope the I_{dx} current has to move into left direction).

To analyse the amount of passive power that could be compensated in our motor, the relation has been assessed between the power factor (cosα), the speed, and the current from the above equations (2-36).

$$\cos\left(\varphi(\omega)\right) = \tag{2-36}$$

$$= \frac{\left(R \cdot I_q + \omega \cdot L_{sd} \cdot I_d + \omega \cdot \psi_F\right) I_q + \left(R \cdot I_d - \omega \cdot L_{sq} \cdot I_q\right) I_d}{\sqrt{\left(R \cdot I_q + \omega \cdot L_{sd} \cdot I_d + \omega\psi_F\right)^2 + \left(R \cdot I_d - \omega \cdot L_{sq} \cdot I_q\right)^2} \cdot \sqrt{\left(I_q\right)^2 + (I_d)^2}}$$

It can be seen in Figure 2-32 that with high speed and low load the power factor can have a value of around 0.8 (blue curve), which means that it is possible to compensate circulating passive power and improve motor drive efficiency. This aspect shows that for operation at high speed with medium load it could be possible to use active source with smaller amplitude if additionally passive power source is available.

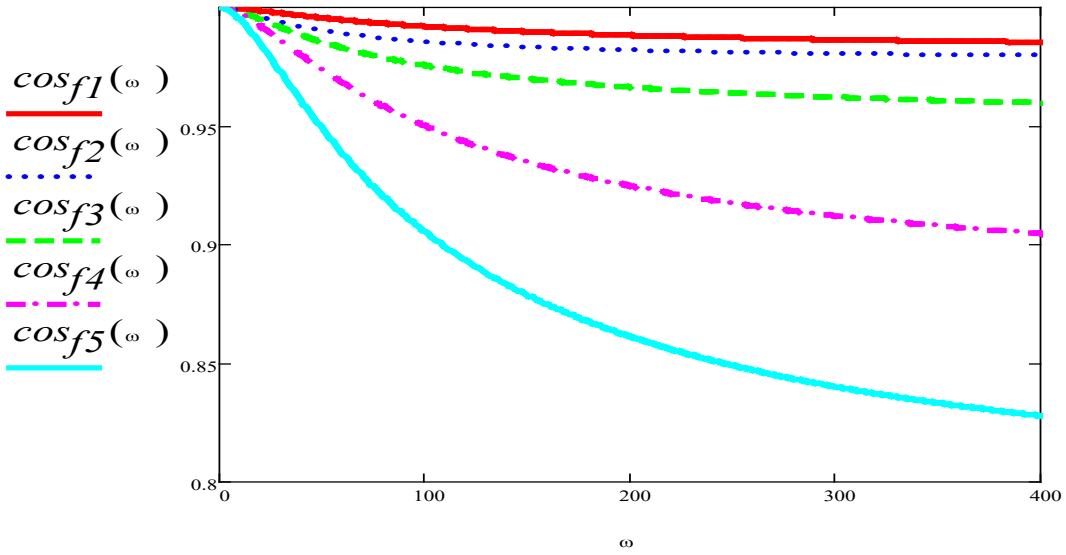


Figure 2-32 Relation between power factor and motor speed for Torque1 (cos_{f1}) > Torque2 (cos_{f2}) > Torque3 (cos_{f3}) > Torque4 >(cos_{f4}) > Torque5 > (cos_{f5})

For the typical electric motor it is also possible to achieve short overload with torque of twice the nominal value. Operations with much higher torque also mean that far greater current is required, which can be destructive to the battery as well as the motor. For these reasons during acceleration at low speed the UC are set to be mainly used and thermal linear degrade has to be implemented so torque will be limited when the motor reaches maximum temperature (Soong and Ertugrul, 2002).

2.5 Control for electric motor

To meet requirements of modern drive systems the control engineering developed number of methods to operate them. The main elements of the systems are flux and torque control loops, and sometimes speed estimation. The biggest popularity among many methods used for performance drivetrains have the linear torque controllers such as filed-oriented control (FOC), direct torque control (DTC) with voltage SVM or DTC with flux SVM (Kazmierkowski M. P., 2002).

The Direct Torque Control (DTC) system first presented by (Takahashi and Noguchi, 1986) deserves particular attention due to the many advantages that this drive features. The scheme has relatively simple control and require low computational time but provide nearly sinusoidal stator flux and current waveforms. The simplicity of control provides also reduced parameter sensitivity. This strategy has the excellent dynamic performance because of decoupled control of torque and flux and flux weakening strategy can be easily implemented. On the other hand, it is well known that DTC presents some disadvantages such as difficulty in controlling torque and flux at very low speed, and high current and torque ripples (Kazmierkowski et al., 2011).

2.5.1 DTC with multilevel inverter

The multilevel inverter has attracted great interest in high-voltage, high-power fields because of its less-distorted output voltage and lower switching frequency and losses. Once the three-level neutral-point-clamped (NPC) inverter was invented it was incorporated into the DTC strategy. In order to solve the intrinsic

problems of the NPC inverter, such as neutral-point-voltage imbalance, the DTC should be used with a special algorithm. One solution is to use the virtual-vector method (Figure 2-33) (Ngo and Foo, 2016).

In this method all the space voltage vectors are divided into large, medium and small vectors and synthesized into some virtual vectors fixed in twelve directions. This is useful to simplify the vector selection. By using the virtual-vector method, it is convenient to utilize the mature two-level DTC strategies in an NPC inverter. Furthermore, a new vector selection method can be derived from the scheme, and it may balance the neutral-point-voltage.

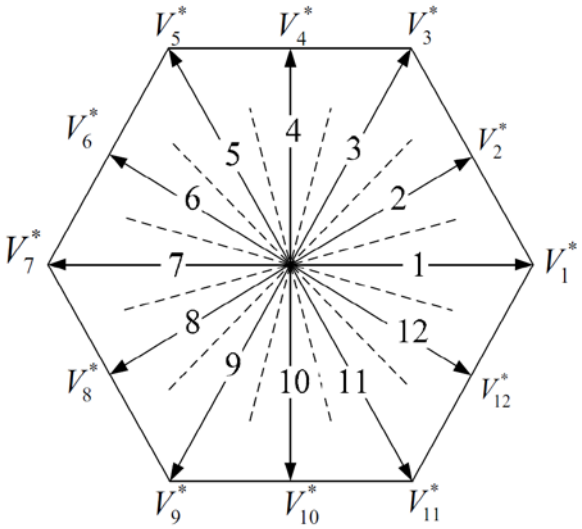


Figure 2-33 Virtual-vector in three-level DTC control (reproduced from (L. Hou, Y. Li, X. Feng, H. Cui, 2009))

The most important advantage of applying multilevel inverters in DTC systems is that in increasing the number of levels proportionally to the number of levels improves the torque quality, reducing ripple amplitude in the whole range of speed. This solution gives very good results and currently is the most popular in high power drives (Khoucha et al., 2010).

2.6 Summary

Presented review shows, that the addition of an UC can accomplish one or more of the following goals: Improve the overall efficiency of the vehicle, reduce long-term costs by extending the life of the batteries, improve the acceleration capabilities of the vehicle and reduce short-term costs by replacing some of the batteries. Elimination of the DC-DC converter in an EV application has the benefits of: better efficiency, better reliability, lower cost, smaller total component size, and lower total component weight. It was presented that combining multilevel inverter into drivetrain structure with batteries and UC can provide power sharing between multiple sources and at the same time improve its performance. Also the capability of multilevel inverter to compensate passive power can additionally increase voltage and extend motor operations at high speed.

CHAPTER 3 MATHEMATICAL ANALYSIS OF HYBRID MULTILEVEL CASCADE WITH TWO SOURCE TYPES AND VARIABLE VOLTAGE RATIO

In this chapter the mathematical model of the hybrid cascade inverter is presented and analysed to define its control strategy. The new modulation modes are establish for the variable voltage sources ratios. The modulation strategy is developed with aim to provide power sharing between sources and the lowest distortion at inverter output, and to achieve maximum output voltage. The theoretical model of the active power estimation from the power definition is derived for the proposed modulation strategy. Finally in this chapter the options to improve architecture of presented multilevel inverter are further discussed.

3.1 Introduction

In the previous chapter, the multilevel inverter was presented as one of the solutions for the high power and high voltage conversion systems in electric vehicles. Therefore, the research aims to find the best solution where instantaneous energy transfer is possible and at the same time harmonic distortions, EMI, and torque ripples can be significantly reduced. The Insulated H-Bridge Inverter (IHBI) was chosen because this is a popular DC/AC converter and has many advantages such as: low number of components or modularized circuit layout and packaging. The other main reason for choosing this topology was the need for separate DC sources that allow for the easy accommodation of batteries and UC into this multilevel structure. The IHBI concept to replace three single cells with one three-phase bridge (Figure 3-1) was found to be the most appropriate for the proposed drivetrain. It allows the use of a single main energy source such as a battery bank where UC as a second energy source can operate to reduce harmonics content and compensate passive power. Especially the aspect of low number of switches makes this topology attractive, as expected component number will be similar to traditional parallel multisource systems. The typical five-level cascade is composed of six cells or 24 switches, whereas this set has only 18 transistors, reducing the inverter cost by up to 25%. In comparison, the traditional bidirectional multisource system with two

DC/DC converters and DC/AC converter require around 14 switches and additional bulky inductors (Guidi, Undeland and Hori, 2008),(Guidi and Undeland, 2007) .

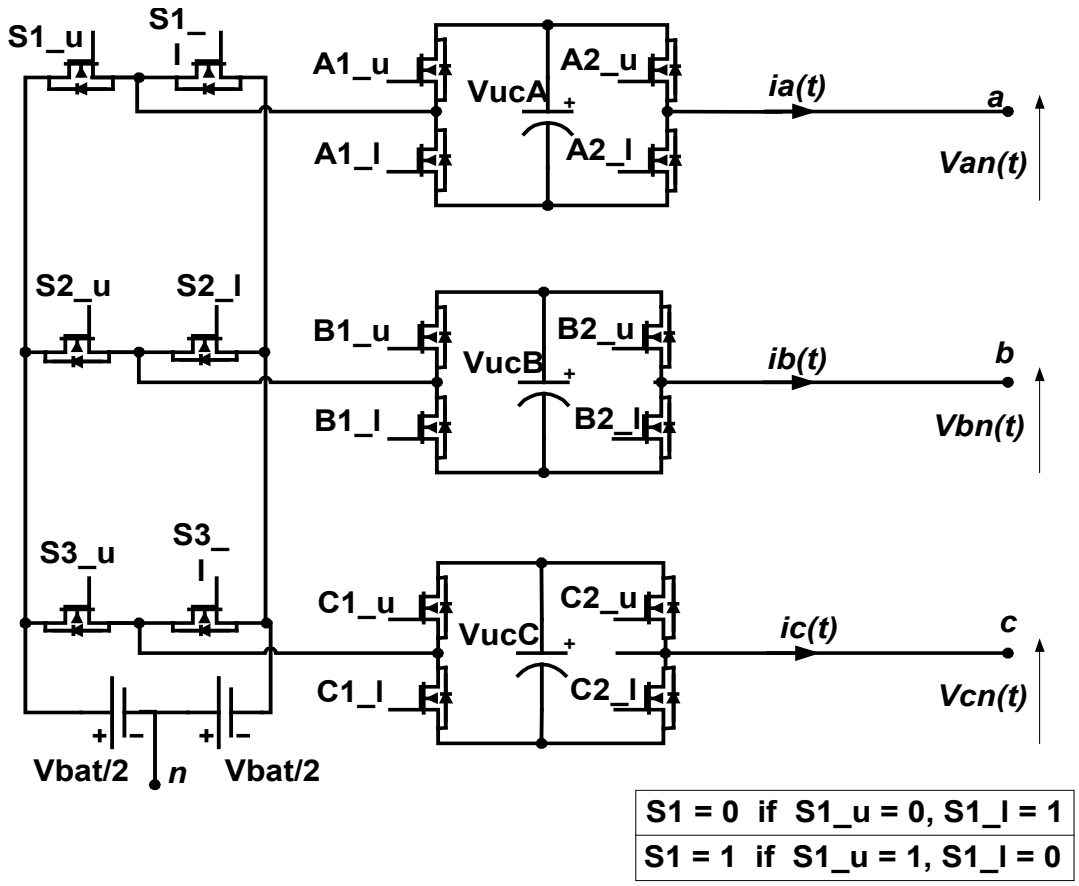


Figure 3-1 Modified cascade inverter consisting of three-phase inverter supplied by two batteries in series ($V_{bat}/2$) and three H-Bridges each supplied by same size UC ($V_{UC}\_A, V_{UC}\_B, V_{UC}\_C$)

To achieve low unwanted harmonics and to accomplish power sharing control the adequate modulation strategy has to be adopted for the above multilevel inverter. In the literature there are various modulation techniques such as PWM, SVM, harmonic control modulation, hysteresis or predictive control (Rodriguez et al., 2009). Those methods often get adjusted to specific system objectives. The most popular and well known method is PWM and is based on comparison of reference signal with triangular carrier waveform at higher frequency. This modulation strategy is very well analysed in literature (Holmes, 2003), the harmonic content is easy to predict and PWM can be extended into multilevel

structures (Mcgrath, Holmes, 2002). Since for some multilevel inverters it is possible to split reference voltage between various inverter section then the power sharing between sources can be archived (Pereda et al., 2009), (Ghias et al., 2016), (Rejas et al., 2016). The limitation of this strategy is that there will be a high number of switching events introducing noise. Also presented in literature solutions are targeting application where voltage ratio between inverter cells is constant (Zhang et al., 2013), (Das, Narayanan and Pandey, 2014). The SVM technique instead of handling triangle carrier use the vector representation and the output voltage is generated by three closest vectors. The main advantage is that the source voltage is better utilized and it is possible to minimise current ripple and switching losses. The SVM modulation is widely used for multilevel inverters where the main methods is stage by stage vector approximation (Mcgrath, Holmes and Lipo, 2003), (Menshawi, Kadir and Mekhilef, 2013). It can be also expanded for multilevel multiphase systems (Lopez et al., 2009). The main problem with this modulation is that there are no well define strategies to control voltage distribution between sources. Example that target this problem is work by M. N. A. Kadi, S.Mekhilef and H. W. Ping (Kadir, Mekhilef and Ping, 2010) where dual vector control strategy is splitting modulation on cells with different amplitude and maximize number of levels to avoid undesirable high switching frequency. In case voltage sources amplitude starts to vary then output voltage error can become significant and none of those methods become valid (Jayasinghe and Vilathgamuwa, 2011). By implementing harmonic control modulation it is possible to control harmonic content but it is required to have certain number of levels to achieve good results as inverter is switching at fundamental frequency (Du et al., 2009). Often this method is used for multi-cell modular converters since it is easier to integrate high number of cells (Sharifabadi, 2016). To control voltage balance between the cells, the phase shift method is used, where square waveform at fundamental frequency for particular cells are phase shifted (Farzaneh-fard, Beyragh and Adib, 2006), (Du, Liu and Liu, 2015). The main advantage of this method is that the switching losses are low in comparison to PWM (Sepahvand, Liao and Ferdowsi, 2011).

In this section the mathematical inverter model is analysed to find appropriate solution together with its limits for conditions where voltage sources have variable amplitude, as there is not much literature about this topic. The SVM that is derived is examined with standard active power equations to find active power estimation with aim to establish power flow control.

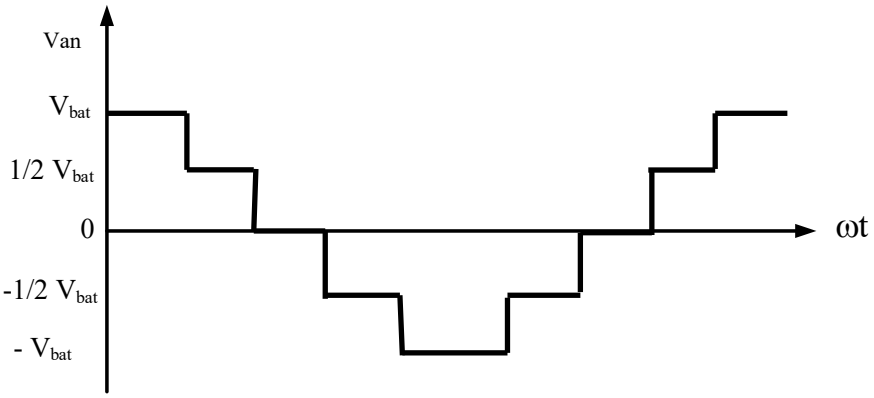
3.2 Structure of modified three-phase cascade of two inverters

The naming convention for switches from Figure 3-1 distinguishes the three-phase bridge with the letter “S” and the H-Bridge with the letters A, B, or C, depending on the phase. The switch pairs are identified by the letter “u“ for the upper switch and “l” for the lower switch. It is assumed that the upper switch is ON and lower switch OFF for switch pair logic state 1 and the opposite for switch pair state 0, as presented in Figure 3-2.

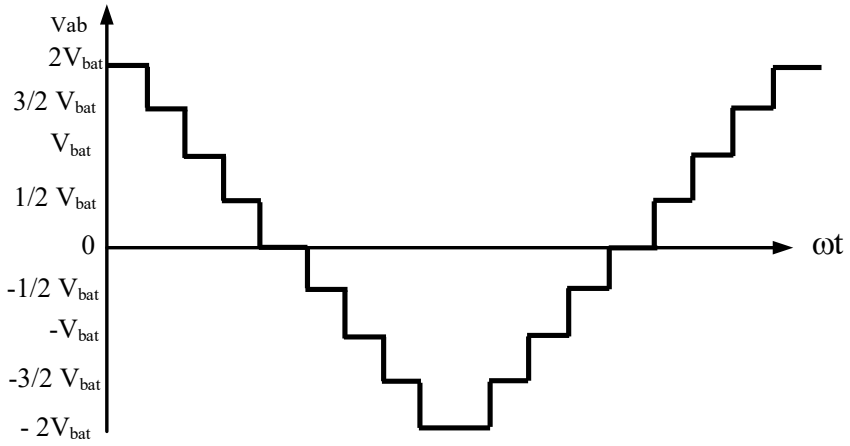
Figure 3-2 Switching pair naming and it’s logic states

The operational principle of the inverter set shown in Figure 3-1 takes account of a single- and a three-phase Graetz’s bridge operation. The line-to-line voltage among A, B and C meet the typical waveform requirements in three-phase circuits. The output voltage waveform (line-to-line) will depend on the correlation between the voltages of isolated sources. In the presented case the three-phase bridge is supplied by one source type consisting of two same-size batteries connected in series with their sources amplitude equal to V_{bat}/2. For H-Bridges second source type is used where phase A, B and C are supplied by separate UC with same capacitance and voltage amplitude equal to V_{UC_A}, V_{UC_B} and V_{UC_C} correspondently. For separated voltage sources which are in following the relation 1/2V_{bat} = V_{uc_A} = V_{uc_B} = V_{uc_C}, the discussed topology of

inverter can modify the phase voltage waveform by five levels (+1 V_{bat}; 1/2 V_{bat}; 0; -1/2 V_{bat}; -1 V_{bat}), whereas the line-to-line voltage is modified by a maximum of nine levels (Figure 3-3).



(a) Phase voltage (V_{an})

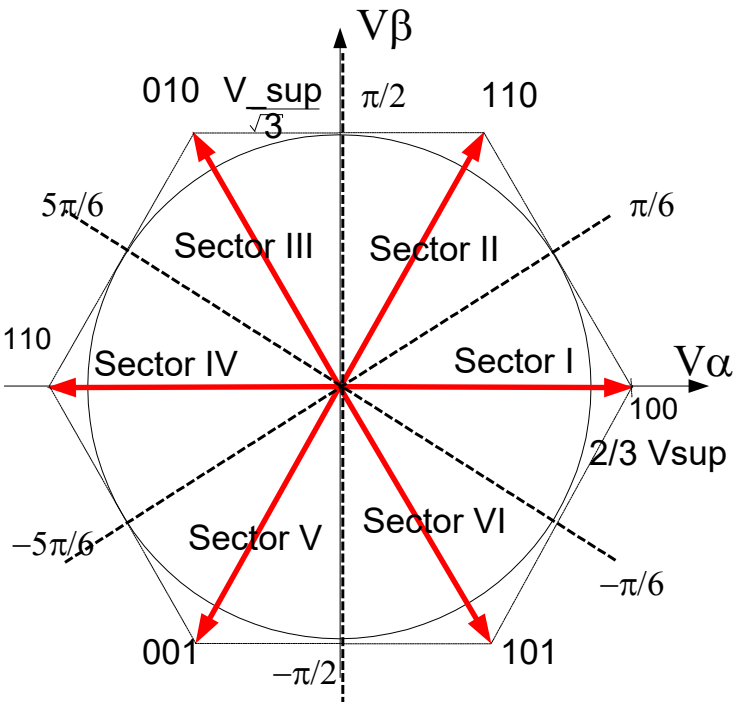


(b) Phase-to-phase voltage (V_{ab})

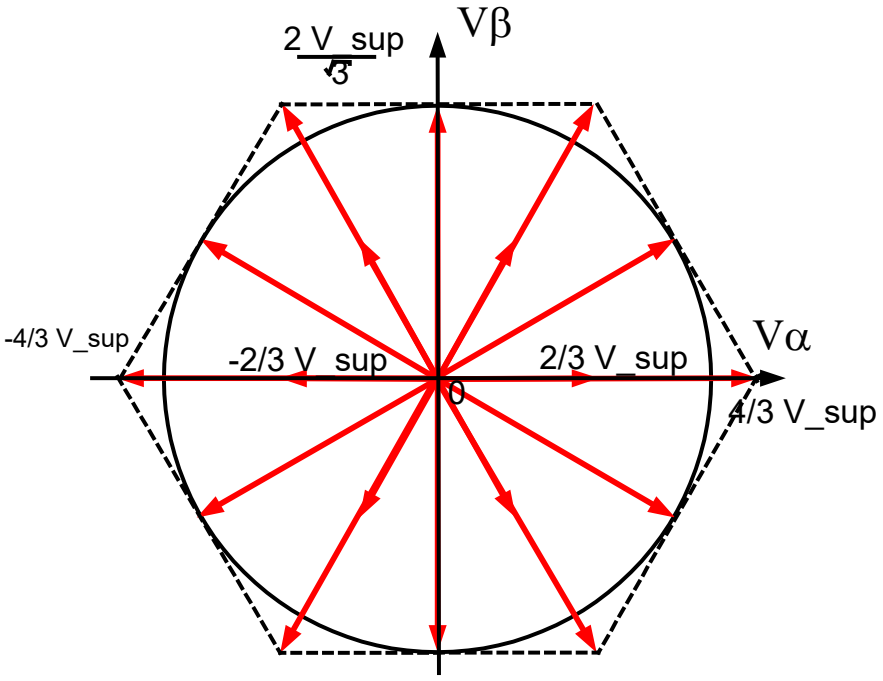
Figure 3-3 Inverter output time series for voltage ratio between amplitude of main source and auxiliary source equal to two

The best method for analysing this structure is to look at it as two separate inverters, so that the output voltage from inverter is a vectors sum of two inverter sections. In Figure 3-4 the set of space vectors in stationary α-β planes are presented for two inverter sections. Figure 3-4 (a) shows voltage vectors (red arrows) for a conventional three-phase bridge where there are six active voltage vectors with amplitude equal to two thirds of supply voltage (V_{sup}) and two zero vectors (000 and 111). Since in the three-phase system there are six

active voltage vectors separated by 60 degrees, the inverter envelope forms a hexagon where the maximum radius of the circle that can be inscribed inside the hexagon is equal to $V_{sup}/\sqrt{3}$.



(a) Voltage vectors produced by the three-phase bridge



(b) Voltage vectors produced by the cascade of three H-Bridges

Figure 3-4 Output voltage vectors for two sections of hybrid inverter

In the case of three H-Bridges forming three level inverters there are 64 possible combinations as there are six pairs of switches (2^6 = 64). From those 64 combinations it is possible to produce 18 active vectors (Figure 3-4 (b)) and ten zero vectors (two of those zero vectors combination “01 01 01” and “10 10 10” will transfer energy between cells depending on the phase currents). Because there are 54 possible switching combinations to produce 18 active vectors, some vectors have redundant switch states. Six active vectors with a maximum vector size equal to $4/3$ of a single-cell supply voltage are unique as they can be produced by only one switching configuration.

As mentioned earlier, the resulting vectors from the hybrid inverter are a sum of the vectors from two inverter sections and depend on the amplitude of their voltage sources. An example of how inverter vectors are added is presented in Figure 3-5, where the amplitude of the three-phase bridge (V_{bat}) is three times higher than the amplitude of the UC (V_{UC}). In presented figure we can find that vector coordinates represented as a sum of three-phase bridges and three H-Bridges produce 90 unique vectors positions. For this ratio (V_{bat}= $3V_{UC}$) it is possible to achieve the maximum number of voltage vectors with equal spacing between them. The three-phase bridge can generate seven different voltage vectors and each single Graetz’s bridge three voltage states, so for this topology there is a total of 189 different voltage vector combinations (7·3·3·3 = 189).

The output phase voltage (V_{an}, V_{bn}, V_{cn}) from the presented inverter (Figure 3-1) in reference to the centre point of the main voltage source called “n” can be described as the product of battery voltage (V_{bat}), ultracapacitors ($V_{uc\_A}, V_{uc\_B}, V_{uc\_C}$) and switch combinations (S1, S2, S3, A1, A2, B1, B2, C1, C2) which is summarised by the following equations (1- upper switch on, lower switch off, 0 – upper switch off, lower switch on) (3-1)-(3-3): (Rodriguez et al., 2003)

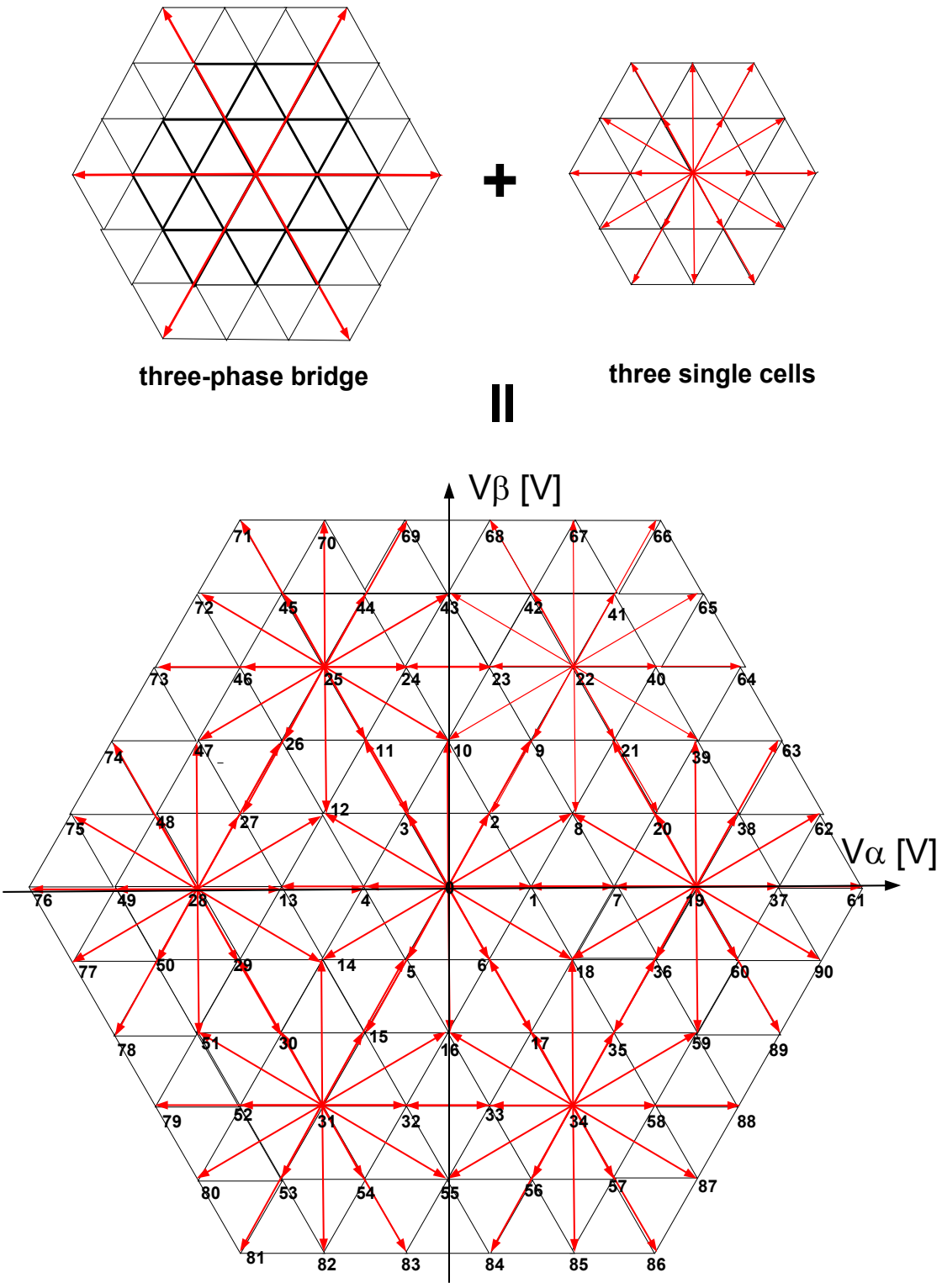


Figure 3-5 Analysis of multilevel cascade inverter as two spate sections with voltage ratio V_{bat}= 3V_{UC} in α-β plane

$$V_{an} = \frac{V_{bat}}{2}(2 \cdot S1 - 1) + V_{uc\_A}(A2 - A1) \tag{3-1}$$

$$V_{bn} = \frac{V_{bat}}{2}(2 \cdot S2 - 1) + V_{uc\_B}\ \ (B2 - B1) \tag{3-2}$$

$$V_{cn} = \frac{V_{bat}}{2}(2 \cdot S3 - 1) + V_{uc\_C}(C2 - C1) \tag{3-3}$$

Converting those three-phase voltages in time domain by Clark, α-β transformation into stationary space vectors two phase plane (V_α, V_β), it becomes possible to generate 512 switching combinations (for nine top and nine bottom switches there are 2^9 combinations). It was also assumed that all three UC banks would have the same voltage value.

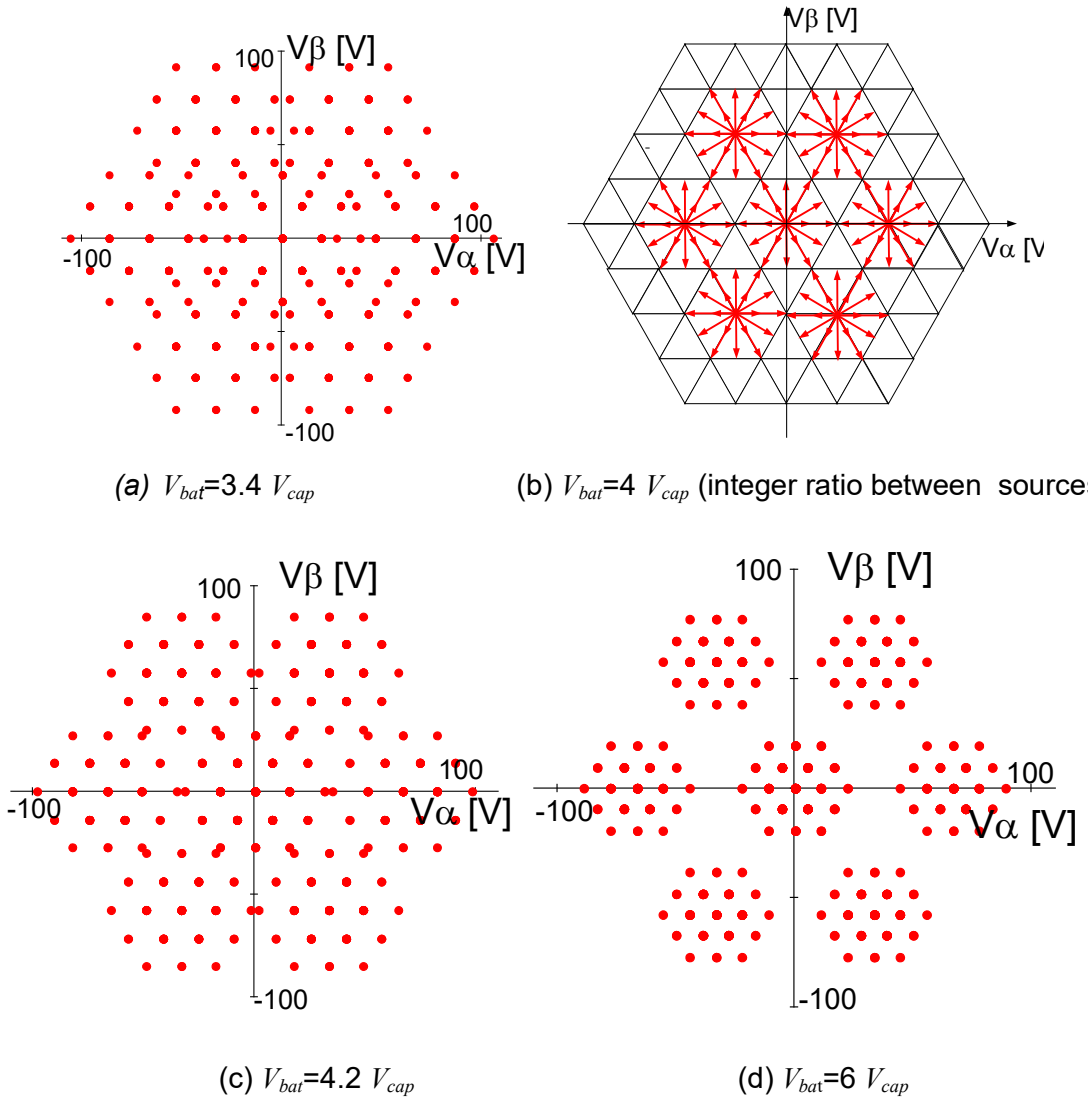
$$V_\alpha = \frac{2}{3}(V_{an} - \frac{1}{2}V_{bn} - \frac{1}{2}V_{cn}) \tag{3-4}$$

$$V_\beta = \frac{\sqrt{3}}{3}(V_{bn} - V_{cn}) \tag{3-5}$$

3.3 Space vectors of modified cascade with multiple source types and variable amplitude of its voltages

In standard applications of hybrid cascade multilevel inverters the voltage ratio between its sources is usually constant. Since the aim of the system is to directly integrate multiple source types into a multilevel inverter, it is expected that the amplitude of one source type will vary. The analysed architecture consists of two sources, where the amplitude of the first is constant or close to constant for longer periods. The second source is a high-power and low-energy type, such as UC or capacitors. Depending on sourced energy during acceleration or recuperated energy from braking, their voltage will vary. To illustrate the influence of H-Bridges voltage variation, based on equations (3-1) - (3-5), example coordinates of voltage vectors were calculated for the hybrid inverter (Figure 3-6) and presented as red dots or arrows. To simplify analysis it is assumed that the voltages on all three sources that supply H-Bridges are equal, since the regulator controls them to the same capacitor reference voltage. It can be noted that as the sources amplitude changes the distance

between vectors will vary. For voltage ratios between the main voltage source and UC (V_{bat}/V_{cap}) that are integer and if that ratio is lower than or equal to four, it is possible to achieve redundant vectors. For non-integer supply voltage ratios each vector is unique, since it can be generated by only one switching combination (without considering individual redundant switching states for H-Bridges and three-phase bridge) (Pereda and Dixon, 2013).



(a) V_{bat}=3.4 V_{cap}

(b) V_{bat}=4 V_{cap} (integer ratio between sources)

(c) V_{bat}=4.2 V_{cap}

(d) V_{bat}=6 V_{cap}

Figure 3-6 Set of available voltage vectors coordinates (red dots) calculated for different DC voltage ratios on stationary α-β plane base on equations (3-1) - (3-5)

It is evident in Figure 3-6 that with the increase of the voltage ratio between inverter sources the gaps between vectors hexagon envelope start to appear. This means that modulated reference voltage vector with circular trajectory that

have transitions through those areas will require changes in a high number of switching states at the same time in three-phase bridge and H-Bridges if the closest vectors are used. In Figure 3-7 an example of voltage vectors transition is presented where three-phase bridge change its state from 100 to 110 (red vectors) and in H-Bridges it is require to change four switches to remain close to reference. This type of vector change could cause high switching losses and large ripples in the output voltage, as transition through intermittent vectors is inevitable. Additionally, the modulation solution between the closest vectors may not provide the specified power share between sources. In the opposite situation, when the ratio between the sources decreases, the H-Bridges hexagons envelopes for closest vectors in the three-phase bridge start to overlap. In this case, depending on when the vector transition in the three-phase bridge occurs, and on the angle between the voltage and current vectors, the proportion of power delivered between the sources could be adjusted. In general, the variable sources voltages results that available voltage vectors are not constant and traditional Space Vector Modulation (SVM) for multilevel inverters cannot be implemented without modification.

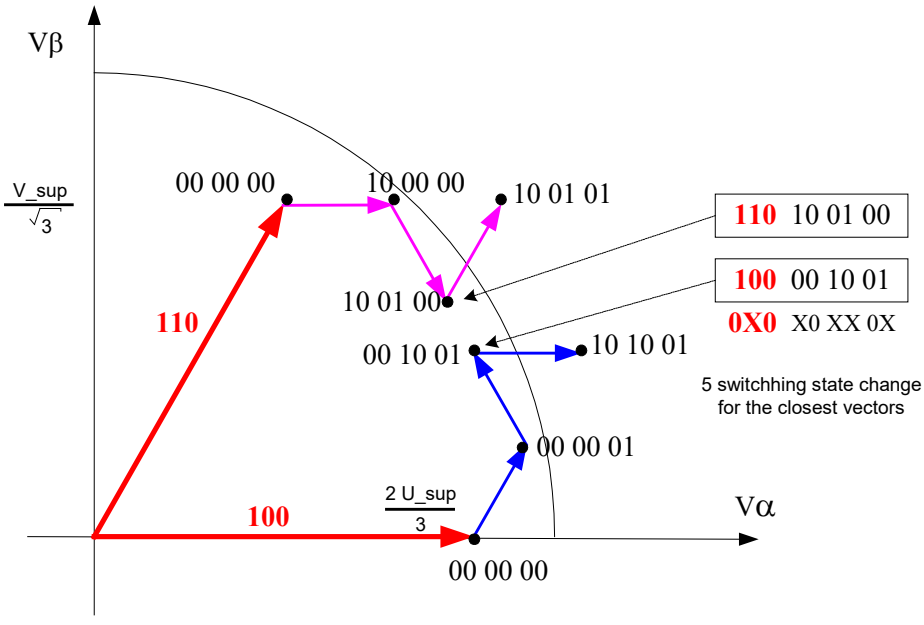
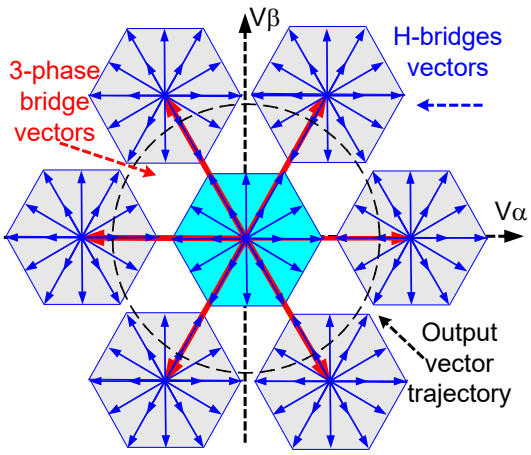
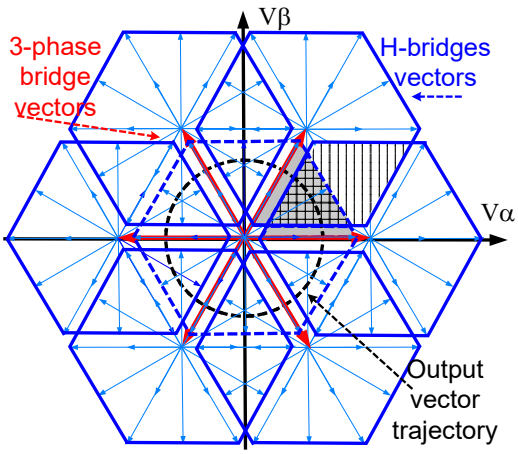


Figure 3-7 Number of switching states changes require to switch between vector coordinates when three-phase bridge vector change from 100 to 110

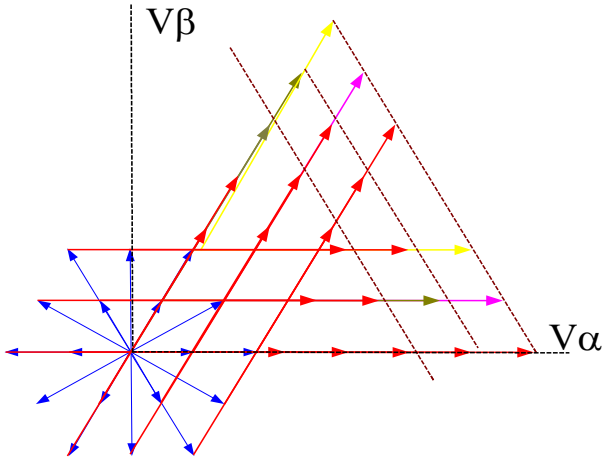
In Figure 3-8 (a) blue arrows represent combinations of voltage vectors for voltage ratio where the source supplying the three-phase bridge has much higher amplitude than the H-Bridge source. It is noticeable that for small amplitude of rotary reference voltage vector, the inverter is able to generate its output voltage by auxiliary inverter only (light blue hexagon). For higher amplitude of reference signal, only for part of the sector the output voltage can be generated without adjusting the switch configuration for the main and auxiliary inverter.



(a) Voltage ratio $V_{bat} = 6V_{uc}$



(b) Voltage ratio $V_{bat} = 2.1V_{uc}$



(c) Voltage ratio $V_{bat} = 6V_{uc}$ in first sector, blue vectors – vectors produced by H-Bridges, red vectors – vectors produced by three-phase bridge

Figure 3-8 Overlapping of voltage vectors from H-Bridges for different vectors from 3-phase bridge when the voltage ratio between the sources vary

In the next Figure 3-8 (b) vector diagram is presented for the condition where the sources voltage has very similar amplitude. For certain reference signal under these conditions it becomes possible to modulate the output voltage either by the auxiliary part of the inverter only or by a combination of a three-phase bridge switched at fundamental frequency and with H-Bridges minimising output voltage error (grey area). Additionally, overlapping area (hashed area) of H-Bridges hexagons shows that the angle where three-phase bridge active vector is switched can be selected. This could help to control the power transferred from the sources.

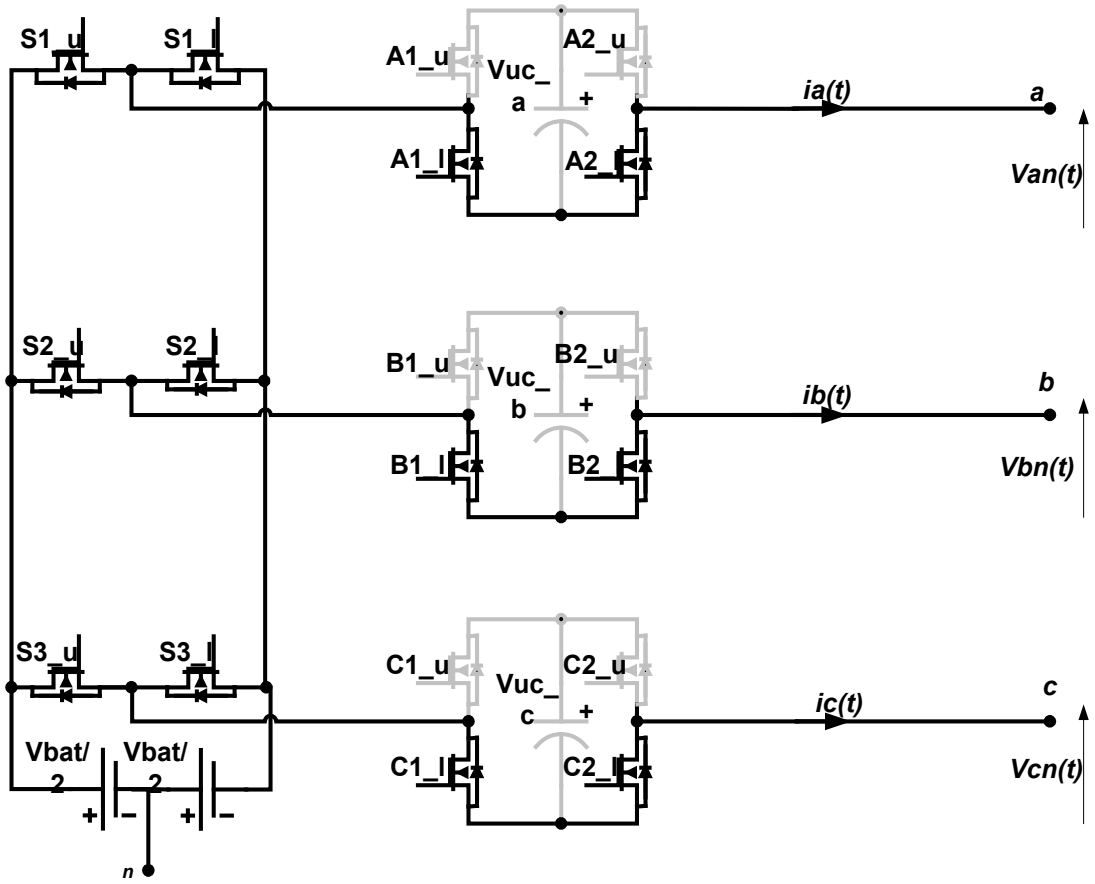
The Figure 3-8 (c) shows vector combinations for the first sector in a case when voltage cannot be produced by H-Bridges modulating in SVM. It is possible instead to switch an auxiliary inverter at fundamental frequency (blue arrows) with the main inverter modulating remaining voltage error (red arrows). In this case the area where it is possible to modulate voltage significantly increase for same voltage ratio as presented in Figure 3-8 (a). This helps to overcome the problem of non-uniform distribution of space vectors, but since the amplitude of the main inverter source is bigger, it is expected that voltage ripples will increase as well switching losses.

3.4 Voltage vectors modulation strategies for hybrid cascade inverter and its voltage limits

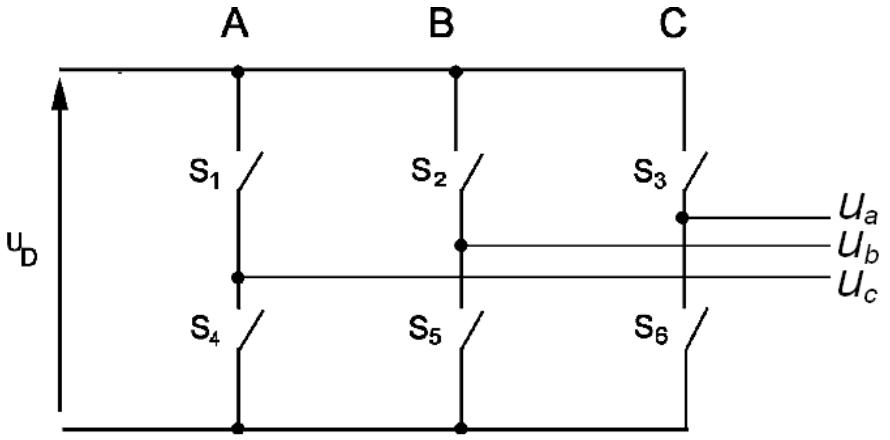
Based on the discussion above it can be concluded that to create a switching strategy for the presented hybrid cascade multilevel inverter, where the amplitude of the auxiliary voltage source varies from 5% up to 50% of the main voltage source, the possible operating modes of the inverter have to be identified. By finding the output voltage limitation for each mode and the expected output power it should be possible to select the best switching configuration during the entire operating range for various voltages of the UC. To simplify the calculation for the power distribution it was assumed that the motor current vector (I) seen by the inverter is ideally sinusoidal and the modulated vector has a circular trajectory.

MODE I: The simplest switching strategy for the discussed inverter is modulation, where a three-phase bridge operates in SVM in the same way as a standard three-phase voltage source inverter. The H-Bridges section will stay in the “00” position (all switches A1, A2, B1, B2, C1, C2 are “0”), meaning that only the lower switches are on (all the top switches for H-Bridges could be on if it is allowed to switch the upper-gate circuits for longer periods) (Figure 3-9). As presented in Figure 3-4 (a) for this switching strategy the inverter has only six active and two zero voltage vectors. The amplitude of the active vectors in stationary α-β coordinate system based on equations (3-1) - (3-5) is equal to two thirds of the supply voltage. For standard SVM in this mode without over-modulation the maximum amplitude of the rotary voltage vector is equal to the radius of the circle that can be inscribed inside the hexagon that is created by the inverter active vectors ($V_{MI\_max}=V_{bat}/\sqrt{3}$). The disadvantage of this switching method is that the main source has high voltage amplitude, which does not allows to exploit the benefit of the multilevel structure to reduce switching ripples and losses. The ability to use only one inverter section could increase the redundancy of the system. It also allows to output voltage from the inverter without depending on the capacitors’ state of charge.

MODE II: The main modulation strategy for the hybrid inverter is based on switching three-phase bridge at fundamental frequency and compensating the remaining voltage error with H-Bridges operating in SVM mode (or PWM). Each active vector of the three-phase bridge is switched on for one sixth of the reference voltage period forming a six-step waveform (Figure 3-10). The H-Bridges are used mainly to minimise voltage error (green trace), reduce harmonic content, and depending on the amplitude of reference voltage to sink or source energy.

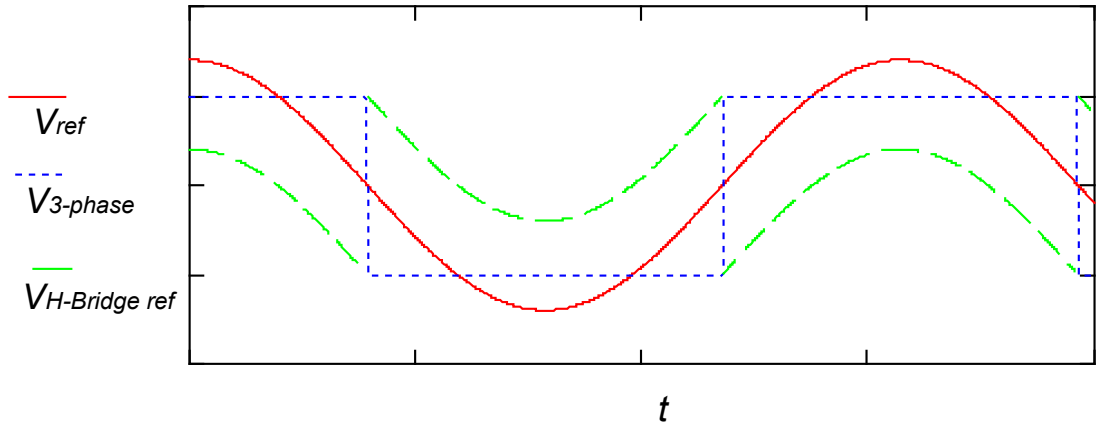


(a) Switch configuration with H-Bridges disable (grey inverter section)

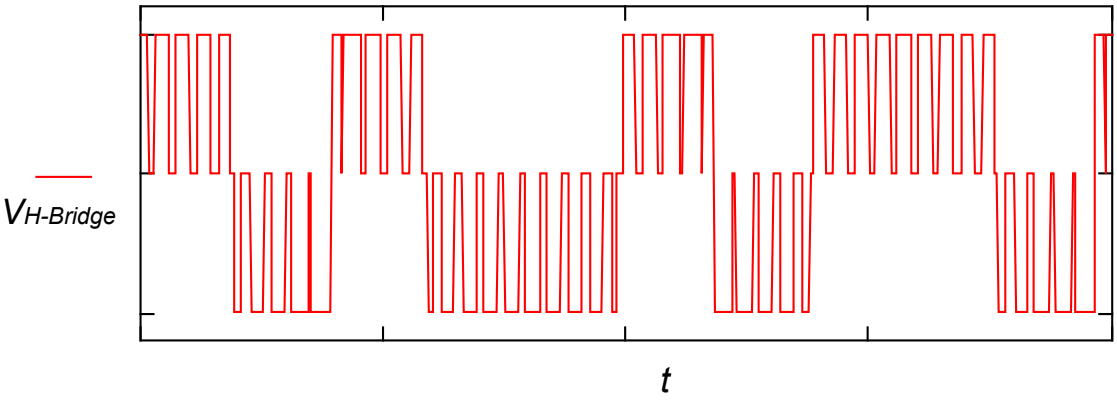


b) Simplified schematic for modulation strategy

Figure 3-9 Switch configuration for strategy with only three-phase bridge modulating output voltage,



(a) Reference voltage for three-phase bridge and remaining voltage error

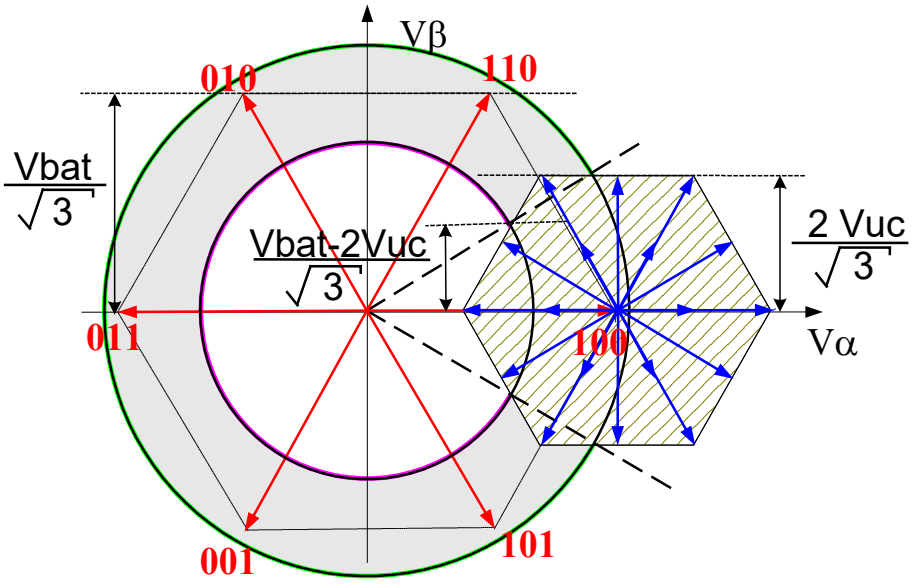


(b)Voltage generated by H-Bridge section

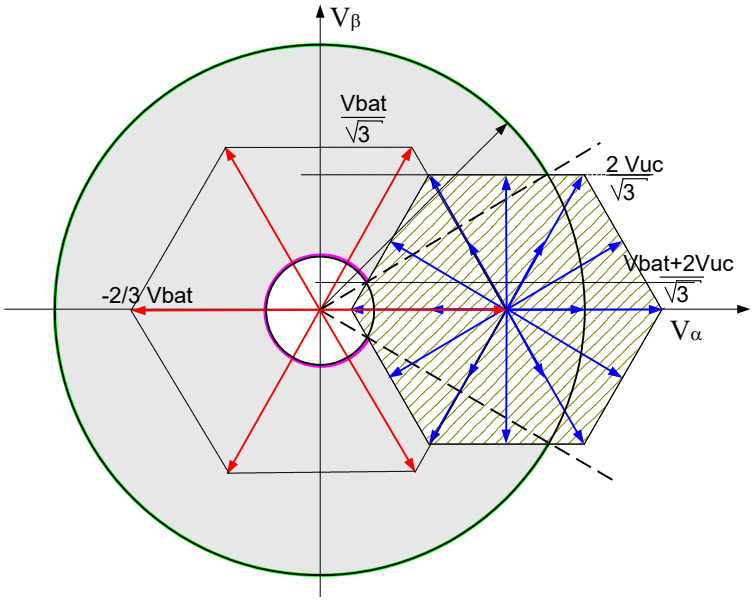
Figure 3-10 The modulation scheme in MODE II and reference voltage for H-Bridge inverter sections

As demonstrated in the previous paragraph, with the strategy when the amplitude of the H-Bridges sources drops it might be impossible to modulate the reference voltage for all coordinates. Figure 3-11 presents the graphs with the possible switching combinations for active voltage vector “100” (S1=1, S2=0, S3=0) in three-phase bridge and its limiting hexagon produced by H-Bridges. In this figure the red arrows represent voltage vectors from the three-phase bridge and blue arrows represent voltage vectors from H-Bridges in combination with “100” voltage vector. To better illustrate limiting boundary in MODE II the grey ring has been marked. The maximum output voltage vector that can be generated by this modulation is equal to $2(V_{bat} + 2V_{uc})/3$ (sum of voltage sourced for both sections), meaning that the maximum output voltage

has to be smaller than $V_{MII\_max} = (V_{bat} + 2V_{uc})/\sqrt{3}$. Additionally, the smallest output voltage vector in this configuration has to be higher than the difference between the inverter vectors $V_{II\_min} = 2/3(V_{bat} - 2V_{uc})$.



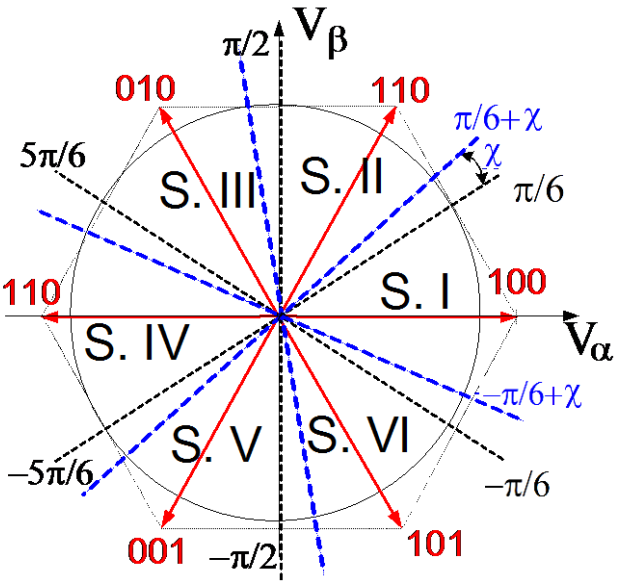
(a) Limiting boundaries for voltage ratio $V_{bat} = 3.5V_{uc}$



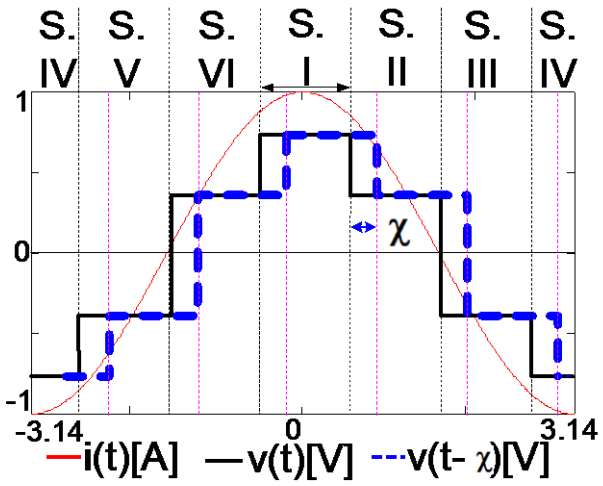
(b) Limiting boundaries for voltage ratio $V_{bat} = 2.3V_{uc}$

Figure 3-11 Modulation limits for strategy with three-phase bridge in six-step mode and H-Bridges in SVM (grey ring). Red vectors represents switching states for the three-phase bridge; blue vectors are switching states of three H-Bridges; grey ring represent amplitude of available voltage vector

In Figure 3-11 the grey ring marks the amplitude of the output voltage vector that can be generated through the whole first sector (- $\pi/6$, $+\pi/6$) when vector "100" is active in the three-phase bridge. For a set voltage reference within the grey ring it is possible to select at what angle the three-phase bridge changes its vector. In other words, phase shift angle ("χ") in reference to load current can be added or subtracted to the six-step waveform to either increase (only if $\cos(\emptyset) < 1$) or reduce the power delivered by the main source (Figure 3-12).



(a) Phase shift on complex plane (α-β)



b) Six-step voltage in time domain with phase-shift

Figure 3-12 The available voltage vectors for the three-phase bridge (red vectors) and corresponding sectors (S.) with phase shift in relation to load current (red)

The Figure 3-12 presents phase shift in relation to current waveforms, where black trace represent voltage before phase shift, blue dotted line represent output voltage after phase shift and red trace symbolize motor current. The maximum phase shift angle depends on the amplitude of the inverter sources and reference voltage. It can be calculated by solving a trigonometric equation using the height of the limiting hexagon. Since there are two possible solutions depending on the amplitude of the reference voltage, the results can be found as the smallest positive angle from the equations (3-6) and (3-7) .

$$\chi_1 = arcsin\left(\frac{2V_{uc}}{\sqrt{3}\,V_{ref}}\right) - \frac{\pi}{6} \tag{3-6}$$

$$\chi_2 = \frac{\pi}{6} - arcsin\left(\frac{V_{bat} - 2V_{uc}}{\sqrt{3}\,V_{ref}}\right) \tag{3-7}$$

By applying the above switching strategy it should be possible to minimise harmonics as the transitions between voltages levels should be smallest (equal to UC voltage) so the current ripples are expected to be reduced. The switching losses in the inverter are expected to be low as well, since the main inverter switches with the highest voltage are changed only six times during one period. Also for power factor close to one the voltage vectors from H-Bridges are almost orthogonal to current vector, meaning that the switched current will be very low, which should additionally reduce switching losses (low voltage and low current switched during SVM).

MODE III: Similarly to the first switching strategy it is possible to use the section with only the H-Bridges active in SVM and the three-phase bridge left continuously in zero state (“000” or “111”) (Figure 3-13). As all three auxiliary sources are expected to have very similar voltage amplitudes the inverter will be able to produce three levels of vectors: 0, V_{uc}, $2V_{uc}$ so the maximum amplitude of the rotary output voltage vector is limited to $V_{III\_max} = 2V_{uc}/\sqrt{3}$. The whole power required by the output is delivered by the UC and the amplitude of the voltage vectors will vary depending on the UC state of charge.

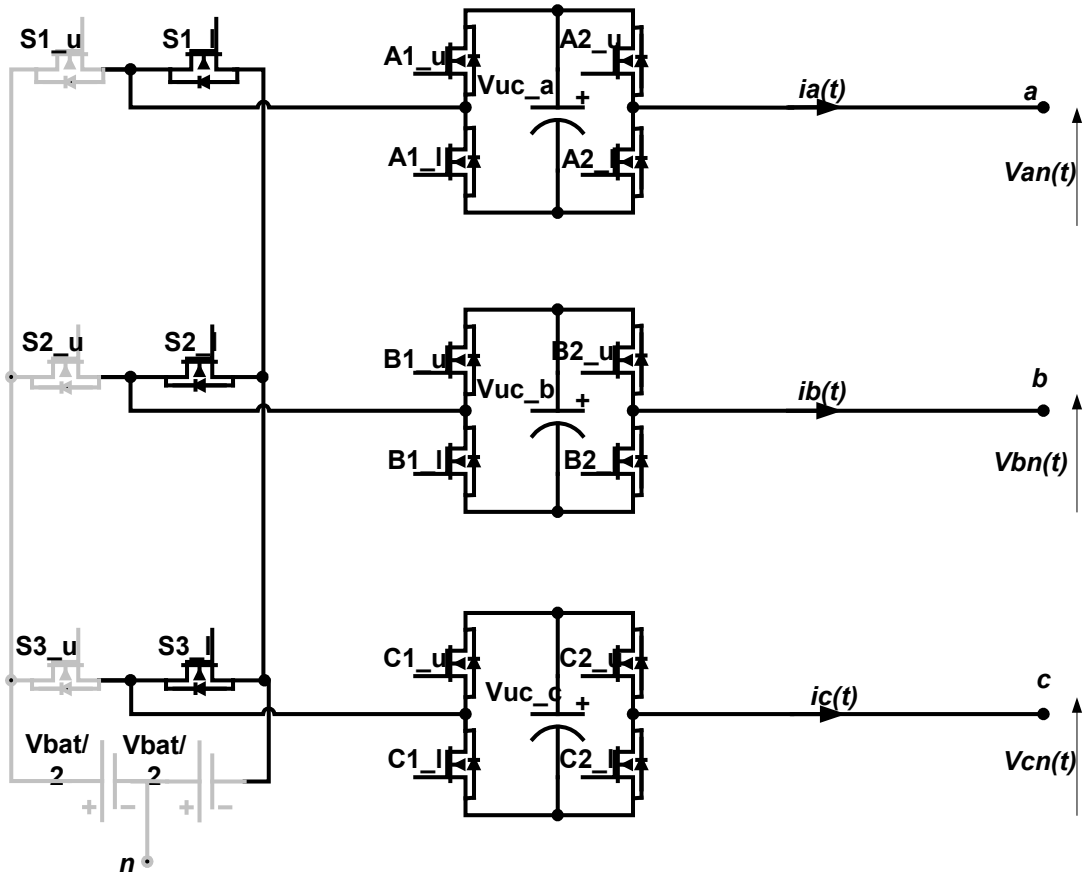


Figure 3-13 Switch configuration for strategy with only three H-Bridges modulating output voltage (MODE III) and three-phase bridge inactive (grey area)

MODE IV: Opposite to mode II the H–Bridges can be switched with a six-step mode and the three-phase bridge can source the remaining voltage error by Space Vector Modulation (Figure 3-8 (c)). Since the H-Bridges section is a three-level inverter it is possible to adjust the number of levels that are used for six-step switching. The first option is to switch with only two levels so only a single H-Bridge is active at a time (each H-Bridge active through a third of the period). The switching with a single vector from the H-Bridge and a vector from the three-phase bridge gives a maximum available output voltage in this configuration equal to $V_{IV\_max} = (V_{bat} + V_{uc})/\sqrt{3}$. Additionally, it is possible to change the sign of active power flowing from the UC by setting phase shift angle "χ" opposite to motor current vector ($\chi = \phi \pm \pi$), because the vectors are subtracted the maximum output voltage is limited to $V_{N\_IV\_max} = (V_{bat} - V_{uc})/\sqrt{3}$. In Figure 3-14 the graph illustrate modulation boundaries for H-Bride for vector

in phase A (blue vector) and three-phase bridge in SVM, green circle represent V_{ref_max}. For a ratio between the main source and the UC of higher than two, the modulation can be performed through the whole sector. The power control by phase shift "χ" for amplitude of reference voltage $V_{N\_IV\_max}$ can be performed for any angle. If the reference voltage is higher than $V_{N\_IV\_max}$ the maximum phase shift is limited by ratio between amplitude of main DC source and reference vector as presented in equation (3-8) and (3-9)(3-10). For $V_{ref} > V_{N\_IV\_max}$ maximum phase shift angle has been defined as "χ_{max}" to simplify control.

-maximum phase shift for given reference voltage

$$\chi = arcsin\left(\frac{V_{bat}}{\sqrt{3}\,V_{ref}}\right) - \frac{\pi}{6} \tag{3-8}$$

-maximum possible phase shift

$$\chi_{max} = arctg\left(\frac{\sqrt{3}V_{bat}}{2V_{uc} - V_{bat}}\right) - \frac{\pi}{6} \tag{3-9}$$

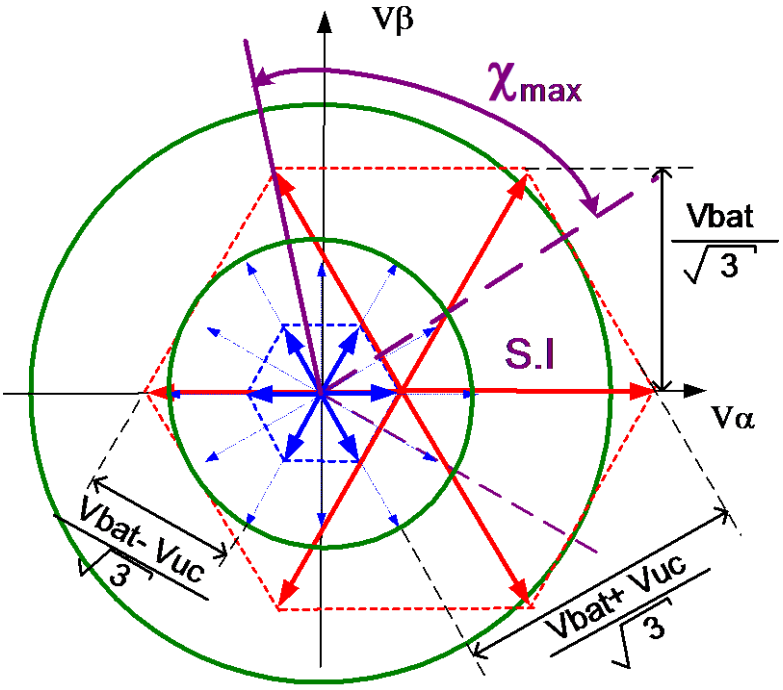


Figure 3-14 Limitation of modulation scheme with H-Bridges switched at fundamental frequency (mode IV). Blue vectors are switching combinations of three H-Bridges; red vectors are switching combinations of three-phase bridge

MODE V: To increase the power delivered from or to the H-Bridges it is possible to extend mode IV by modifying the six-step switching sequence by using two H-Bridges active vectors at the same time. Since two adjacent vectors are switched on together, the operating sector becomes shifted by $\pi/6$. Figure 3-15 shows the vector combinations for this switching strategy and limits for case where H-Bridges in phase A and C are active and three-phase bridge is performing SVM. The maximum modulated voltage is $V_{V\_max} = 2/3(V_{bat} + V_{uc})$ and for six step waveform phase shifted by $+\pi$ or $-\pi$ the output has to be smaller than $V_{N\_V\_max} = (V_{bat} - 2V_{uc})/\sqrt{3}$.

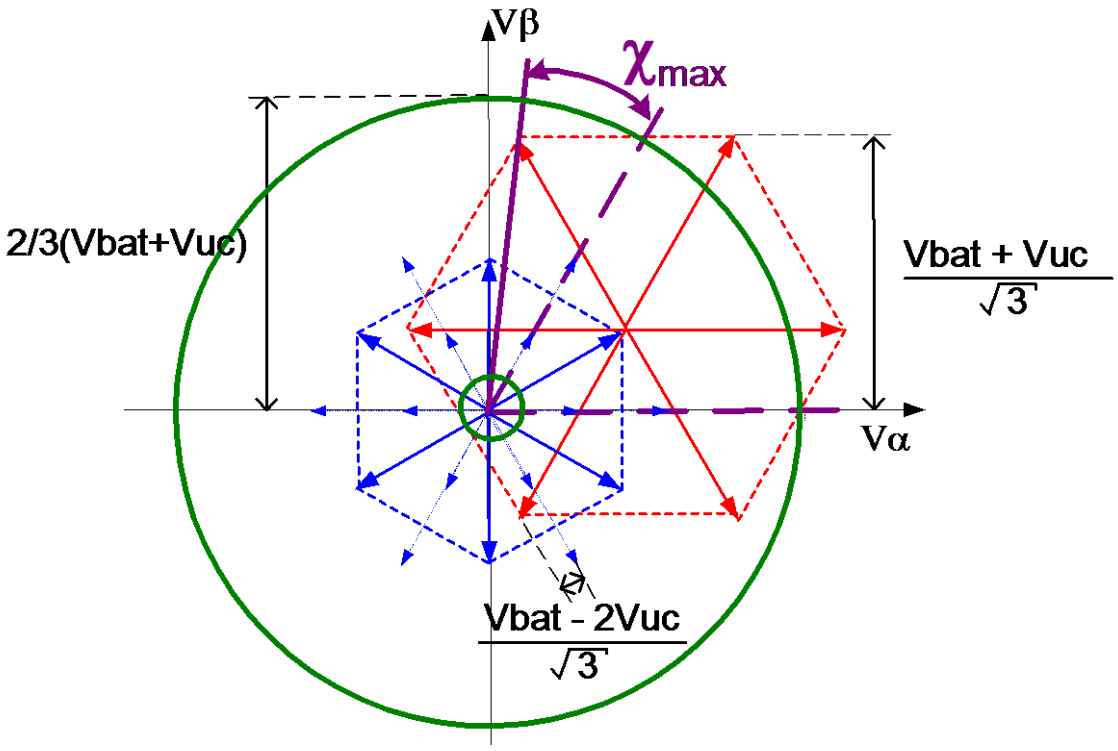


Figure 3-15 Limitation of modulation scheme with H-Bridges switched at fundamental frequency (mode V). Blue vectors are the switching combinations of three H-Bridges; red vectors are the witching combinations of the three-phase bridge and green circles represent limits for reference voltage

The angle where the six-step switching occurs can be phase shifted within limits derived from equation (3-10) and (3-11) where the maximum angle to simplify control is limited to χ_{max}.

$$\chi = arcsin\left(\frac{V_{bat} + V_{uc}}{\sqrt{3}\,V_{ref}}\right) - \frac{\pi}{3} \tag{3-10}$$

$$\chi_{max} = arctg\left(\frac{V_{bat} + V_{uc}}{\sqrt{3}\,\left(V_{uc} - \frac{1}{3}V_{bat}\right)}\right) - \frac{\pi}{3} \tag{3-11}$$

MODE VI: To achieve the maximum output power from the H-Bridges it is proposed to keep all three UC active in six-step mode at fundamental frequency. From Figure 3-16 we can find that the maximum modulated voltage is $V_{VI\_max} = (V_{bat} + 2V_{uc})\sqrt{3}$ and if the six-step waveform is phase shifted by $+\pi$ or $-\pi$ the output has to be smaller than $V_{N\_VI\_max} = (V_{bat} - 2V_{uc})\sqrt{3}$.

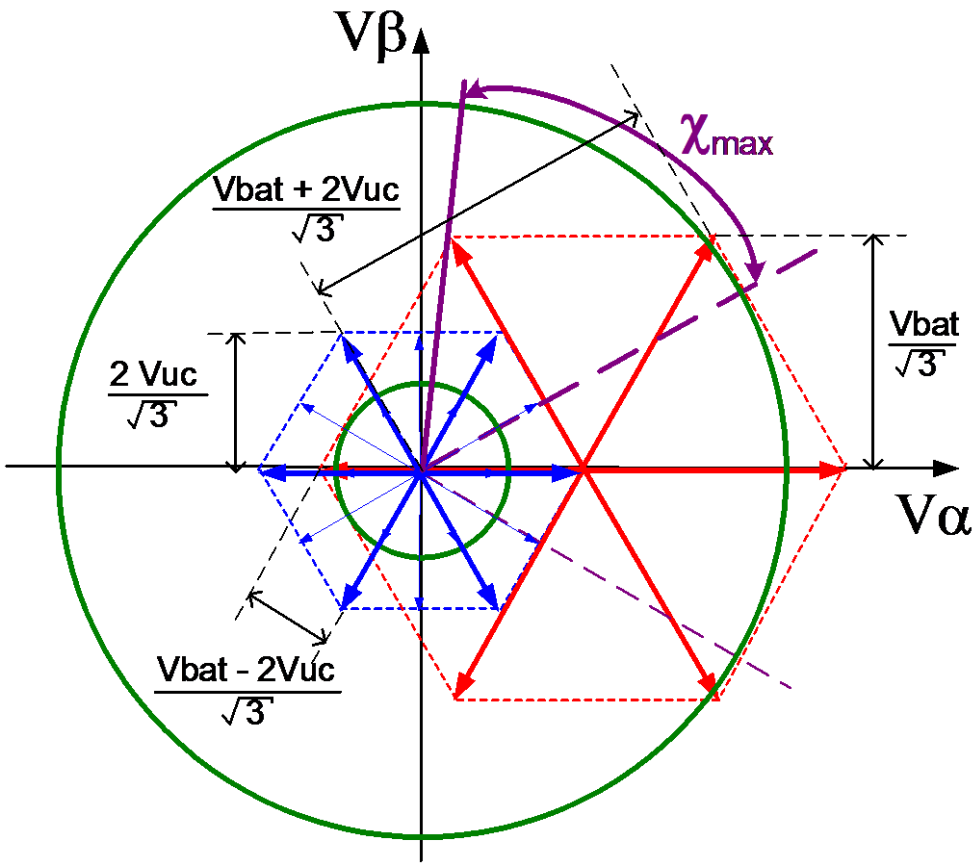


Figure 3-16 Limitation of modulation scheme with H-Bridges switched at fundamental frequency (mode VI). Blue vectors are the switching combinations of three H-Bridges; red vectors are the switching combinations of the three-phase bridge and green circles represent limits for reference voltage

The available phase shift angle for the given reference vector becomes limited by equations (3-12) and (3-13**)**.

$$\chi = arcsin\left(\frac{V_{bat}}{\sqrt{3}\,V_{ref}}\right) - \frac{\pi}{6} \tag{3-12}$$

$$\chi_{max} = arctg\left(\frac{\sqrt{3}\,V_{bat}}{4V_{uc} - V_{bat}}\right) - \frac{\pi}{6} \tag{3-13}$$

Presented analysis demonstrates the voltage limits for identified switching strategies. Figure 3-17 illustrate the positive and negative output voltage limits in relation to the UC's state of charge for each modulation mode (same colour doted and solid lines). By selecting an adequate modulation strategy it is possible to modulate the voltage vector from 0V up to a sum of voltage sources $(V_{bat} + 2V_{uc})/\sqrt{3}$. The negative voltage that is presented by the graph symbolizes modulation with 180˚ phase shift ($\chi = \pm\pi$).

A summary of the available voltage and limiting phase shift angles for strategies with switching at fundamental frequency is presented in Table 3-1. The maximum phase shift χ_{max} has been defined as a limit to simplify calculation and to use phase shift without rapid change of vector amplitude, for a voltage ratio where the battery voltage is at last twice the value of the UC source. An important conclusion from this analysis is that modulation strategies that include H-Bridges in SVM (MODE II and MODE III) have a very limited operating range that is strongly dependent on the UC's state of charge.

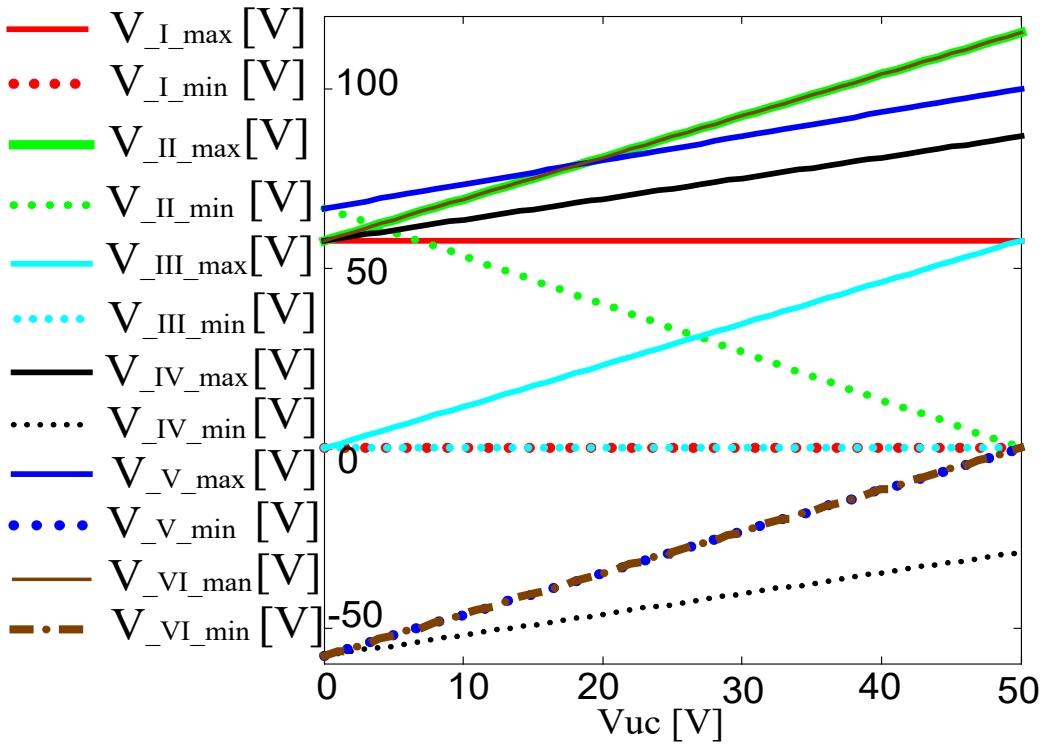


Figure 3-17 Summary of voltage limits for all switching configurations in relation to the voltage of the auxiliary source, solid line – maximum voltage, dotted line – minimum voltage, main source voltage 100V, auxiliary source variable from 0 to 50V

Table 3-1 Equations for voltage limits and phase shift for the six switching strategies identified

Switching mode	Maximum voltage	Minimum voltage	Available phase shift for given reference voltage	Maximum phase shift
MODE I	$\frac{V_{bat}}{\sqrt{3}}$	0	-	-
MODE II	$\frac{V_{bat}+2V_{uc}}{\sqrt{3}}$	$\frac{2(V_{bat}-2V_{uc})}{3}$	$\chi_1 = arcsin\left(\frac{2V_{uc}}{\sqrt{3}\,V_{ref}}\right)-\frac{\pi}{6}$ or $\chi_2 = \frac{\pi}{6}-arcsin\left(\frac{V_{bat}-2V_{uc}}{\sqrt{3}\,V_{ref}}\right)$	$\frac{\pi}{6}$
MODE III	$\frac{2V_{uc}}{\sqrt{3}}$	0	-	-
MODE IV	$\frac{V_{bat}+V_{uc}}{\sqrt{3}}$	0 or $\frac{V_{bat}-V_{uc}}{\sqrt{3}}$	$arcsin\left(\frac{V_{bat}}{\sqrt{3}\,V_{ref}}\right)-\frac{\pi}{6}$,	$arctg\left(\frac{\sqrt{3}V_{bat}}{2V_{uc}-V_{bat}}\right)-\frac{\pi}{6}$
MODE V	$\frac{2(V_{bat}+V_{uc})}{3}$	0 or $\frac{V_{bat}-2V_{uc}}{\sqrt{3}}$	$arcsin\left(\frac{V_{bat}+V_{uc}}{\sqrt{3}\,V_{ref}}\right)-\frac{\pi}{3}$	$arctg\left(\frac{V_{bat}+V_{uc}}{\sqrt{3}\,\left(V_{uc}-\frac{1}{3}V_{bat}\right)}\right)-\frac{\pi}{3}$
MODE VI	$\frac{V_{bat}+2V_{uc}}{\sqrt{3}}$	$\frac{V_{bat}-2V_{uc}}{\sqrt{3}}$	$arcsin\left(\frac{V_{bat}}{\sqrt{3}\,V_{ref}}\right)-\frac{\pi}{6}$	$arctg\left(\frac{\sqrt{3}\,V_{bat}}{4V_{uc}-V_{bat}}\right)-\frac{\pi}{6}$

3.5 Strategy to share power between sources

Simultaneous switching different combinations of the three-phase inverter together with the H-Bridges provides the capability to control the power flow between the batteries, the UCs and the motor, and at the same time to produce precise voltage vectors with reference amplitude. The aim of this power analysis is to define the strategy that will allow the control of the power distribution between the sources of the multilevel inverter within its voltage limits. The system that is described consists of two different voltage sources, of which the second includes three subunits. To allow energy contribution calculations for each source, the algorithm works in a flow tree fashion that can be expanded for a higher number of sources in three stages. At the first stage the three H-Bridges connected to each phases are collectively treated as one section with equal capacitor voltage. The second stage involves sharing of power between the three-phase bridge and H-Bridge section as an entity. The last stage will involve the sharing of power among the individual H-Bridges. This analysis assumes for most cases that the power is split evenly between the UCs since the capacitors are kept at the same state of charge and modulation is symmetrical. The next part of this work includes a strategy to control power sharing between the individual parts of the H-Bridges so that the voltage on each source can be accurately controlled.

3.5.1 Power definition

There is various literature describing power sates but none of them is perfect as there is inadequacy in the physical interpretation or the universal character is used (Hartman and Hashad, 2008a) (Hartman and Hashad, 2008b). For non-sinusoidal voltage the calculation based on instantaneous power provide good results. The active power P is defined as integral of instantaneous power $p(t)$ over an assumed period of time T, where instantaneous power is a product of instantaneous voltage $v(t)$ and current $i(t)$. The active power is sometimes called useful or real power as it is responsible for work at load.

$$P = \frac{1}{T}\int_0^T p(t)dt = \frac{1}{T}\int_0^T v(t)i(t)dt \tag{3-14}$$

$$where \quad v(t) = V \cdot cos(\omega t) \ and \quad i(t) = I \cdot cos(\omega t - \emptyset) \tag{3-15}$$

From the equations above (3-14) and (3-15) one can conclude that for sinusoidal current and voltage, the instantaneous active power oscillates and depends on power factor $cos(\emptyset)$ that represents the phase delay between those waveforms as presented in Figure 3-18.

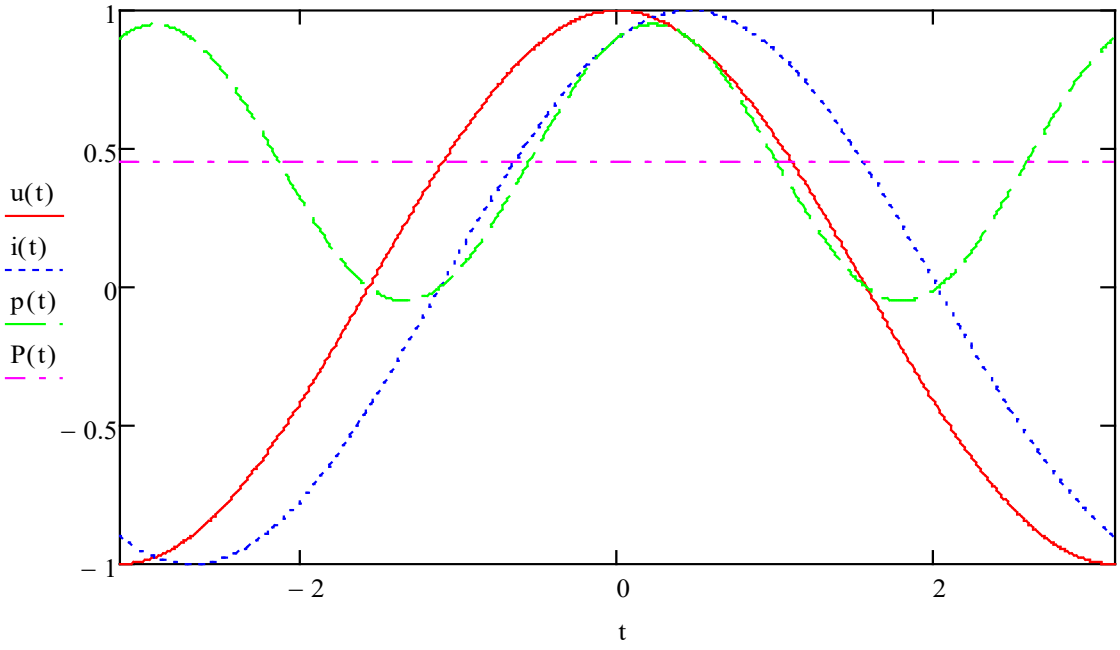


Figure 3-18 Time series of phase voltage *v(t)* and phase current *i(t)*, its instantaneous active power *p(t)* and its average active power *P*

If we ignore the phase relation between the waveforms above, we are able to define apparent power. It is described as the product of current and voltage square roots (3-16):

$$S = \sqrt{\frac{1}{T}\int_0^T v^2(t)dt} \cdot \sqrt{\frac{1}{T}\int_0^T i^2(t)dt} \tag{3-16}$$

The power difference between apparent power and active power is called non-active power N (3-17) and is represented as a square root of the difference between the squares of active power and apparent power (Hartman, 2009):

$$N = \sqrt{S^2 - P^2} \tag{3-17}$$

Additionally, we can distinguish reactive power Q as integral of combinations of the voltage and current derivatives (3-18).

$$Q = \frac{1}{4\pi}\int_0^T \left(v\frac{di}{dt} - i\frac{dv}{dt}\right)dt \tag{3-18}$$

For three-phase systems the total active power is the sum of the instantaneous active powers in individual phases (A, B and C) (3-19).

$$P = P_A + P_B + P_C = \frac{1}{T}\int_0^T p_A(t)dt + \frac{1}{T}\int_0^T p_B(t)dt + \frac{1}{T}\int_0^T p_C(t)dt \tag{3-19}$$

For symmetrical three-phase systems with sinusoidal currents and voltages with the same amplitude in each phase (Figure 3-19), the equation for active power can be simplified to a form where the instantaneous power for the three-phase system is a constant product of the voltage and current amplitudes reduced by a power factor. Similarly, apparent power S is a product of the voltage V and current I amplitude without considering the power factor (3-20),(3-21):

$$P = \frac{3}{2}\cdot V \cdot I \cdot \cos(\emptyset) = p(t) \tag{3-20}$$

$$S = \frac{3}{2}\cdot V \cdot I \tag{3-21}$$

Assuming for the three-phase system that the phase currents and voltages are symmetrical, ideally sinusoidal and with constant amplitude, it is possible to simplify the power calculations to one sixth of the period and to treat instantaneous power as constant. Thanks to this assumption based on calculations for a single sector it become possible to estimate active power required by the sources.

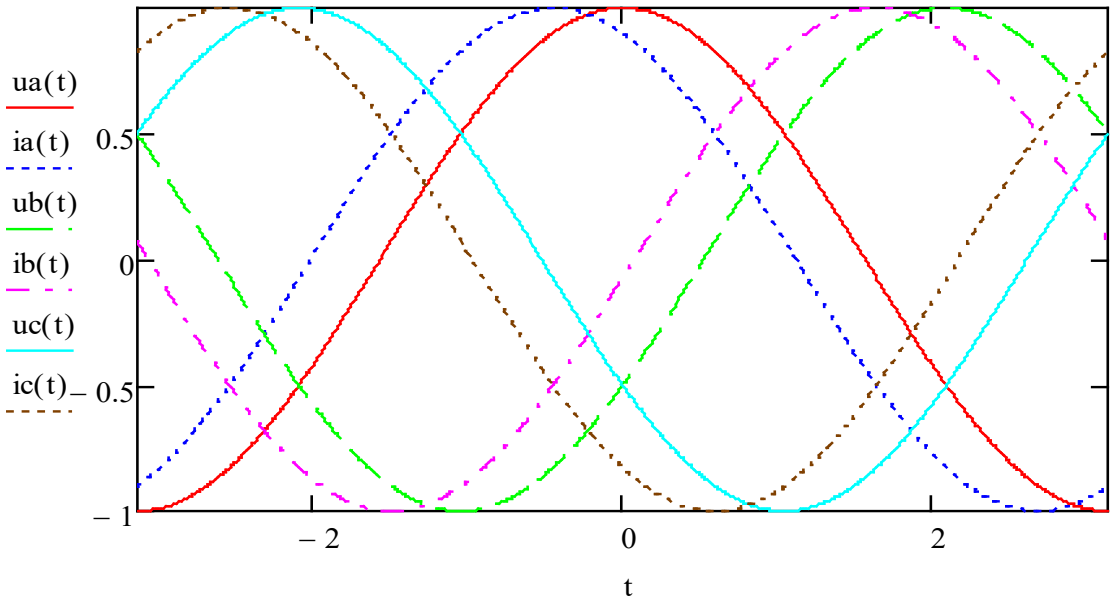


Figure 3-19 Time series of instantaneous three-phase voltages *v(t)* and corresponding phase currents *i(t)* with a $\pi/6$ phase shift between voltage and current in a symmetrical system

For the topology of the multilevel and multisource inverter presented earlier the active power can be taken as a sum of the active power of two source types where in addition the UC power can be distinguished for individual units (3-22):

$$P = P_{bat} + P_{ucap} \tag{3-22}$$

$$where \quad P_{uc} = P_{uc\_A} + P_{uc\_B} + P_{uc\_C} \tag{3-23}$$

P_{bat} - active power delivered by battery, P_{uc} - total active power delivered by three capacitors.

The goal of the control strategy is to deliver the total apparent power S required by the load and at the same time to split the active power between the sources according to set references. The split of the remaining passive power between the sources is not further analysed for control purposes since it should be satisfied by operations within voltage limits; so the algorithm will only aim to minimise current oscillation between the sources in the circuit.

The active power equation for this multilevel inverter can not only be expressed from a load perspective but also from the perspective of DC sources, taking into account the instantaneous power delivered by each source $p_{bat}\ (t)$- battery instantaneous power and p_{uc_A} , p_{uc_B} , p_{uc_C} - UC instantaneous power (3-24),(3-25).

$$P = P_{bat} + P_{uc\_A} + P_{uc\_B} + P_{uc\_C} \tag{3-24}$$

$$P = \frac{1}{T}\int_0^T p_{bat}(t)dt + \frac{1}{T}\int_0^T p_{uc\_A}(t)dt + \frac{1}{T}\int_0^T p_{uc\_B}(t)dt + \frac{1}{T}\int_0^T p_{uc\_C}(t)dt \tag{3-25}$$

Considering only one sixth of the period ($T/6 = 2\pi/6 = \pi/3$), and that the DC sources have constant voltage, produces equations describing the active power for a multisource system (3-26):

$$P = \frac{1}{\frac{\pi}{3}} V_{bat} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} i_{bat}(t)dt + \frac{1}{\frac{\pi}{3}} V_{uc\_A} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} i_{uc\_A}(t)dt + \frac{1}{\frac{\pi}{3}} V_{uc\_B} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} i_{uc\_B}(t)dt + \frac{1}{\frac{\pi}{3}} V_{uc\_C} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} i_{uc\_C}(t)dt \tag{3-26}$$

V_{bat} – amplitude of the battery , V_{uc_A} – amplitude of the UC in phase A, V_{uc_B} – amplitude of the UC in phase B and V_{uc_C} – amplitude of the UC in phase C ; $i_{bat}\ (t)$ – instantaneous battery current ,$i_{uc\_A}\ (t)$, $i_{uc\_B}\ (t)$,$i_{uc\_C}\ (t)$ – instantaneous currents seen by the UC in phases A, B and C

For the average DC currents of each source the above equations can be simplified to form:

$$P = V_{bat} \cdot I_{bat} + V_{uc\_A} \cdot I_{u\_A} + V_{uc\_B} \cdot I_{uc\_B} + V_{uc\_C} \cdot I_{uc\_C} \tag{3-27}$$

I_{bat} - average battery DC current I_{uc_A} - average UC DC current in phase A, I_{uc_B} - average UC DC current in phase B , I_{uc_C} - average UC DC current in phase C.

The equations above (3-27) can be used further for active power calculations of multilevel multisource systems considering the operating modes identified earlier.

3.5.2 Power delivered by Space Vector Operation with only one section of inverter active

MODE I: In this configuration the inverter will operate like a standard three-phase voltage source inverter, where the main source is only outputting power (in this example battery). All H-Bridges in this operating mode will stay in the "00" position, meaning that only the lower switches are constantly on. For inverter operations when only the three-phase bridge is active the power delivered from the DC source (P_{bat}) is equal to the power dissipated at load (P_{out}) if inverter losses are omitted. This can be expressed as a simple product of battery current (I_{bat}) and it's voltage (V_{bat}) or of reference voltage (V_{ref}) vector, motor current in stationary α-β plane (I) and power factor ($cos(\emptyset)$) (3-28).

$$P_{out} = P_{bat} = V_{bat} \cdot I_{bat} = \frac{3}{2} V_{ref} \cdot I \cdot \cos(\emptyset), \quad P_{uc} = 0 \tag{3-28}$$

Since current limits (I_{bat_max} and I_{bat_min}) are placed on the battery used in this system in order to maximize its life, the modulation strategy with a three-phase bridge has to limit its output voltage depending on the output current (I). An example characteristic of the maximum output voltage for a 100V source with maximum battery current I_{bat_max}=1.5A and I_{bat_min}=-0.5A is presented in Figure 3-20 where X axis is battery current, Y axis is UC voltage and Z axis represent maximum inverter voltage to remain within battery power limit. It is expected that when the current reaches its maximum or minimum limits the control strategy will aim to maintain a constant power output by reducing the output voltage in inverse proportion to the current (inverter output voltage remain under 3D plane). Since the UCs are inactive the output voltage is independent of UC state of charge and output voltage is limited when output power is equal battery limits.

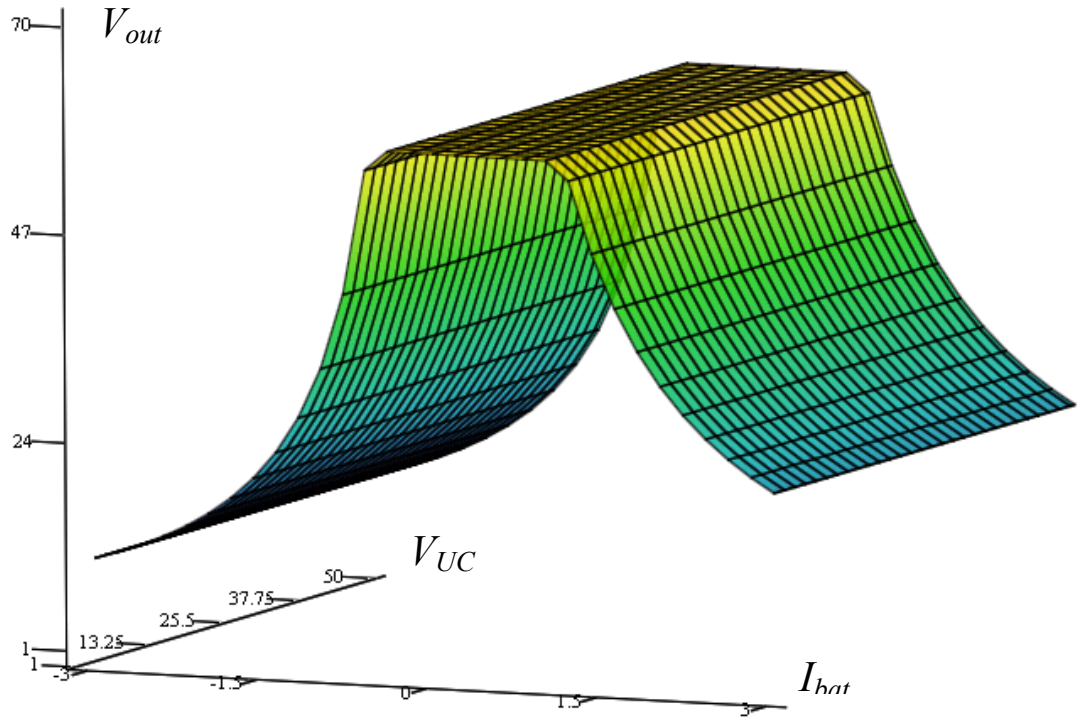


Figure 3-20 Available output voltage (*Vout*) in MODE I in relation with UC's average voltage value (V_{UC}) and maximum output current from main source (I_{bat})

If the DC source has specific current limits, and since the maximum amplitude from the voltage inverter is 1/√3 of supply voltage (in SVM mode without over-modulation), it is possible to find the maximum amplitude of the three-phase current (I_{max}) for a given maximum or minimum battery current (I_{bat_max}) (3-29),(3-30):

$$P_{\max} = \frac{3}{2} V_{ref} \cdot I_{max} \cdot \cos(\emptyset) \tag{3-29}$$

$$= \frac{3}{2} \frac{V_{bat}}{\sqrt{3}} \cdot I_{max} \cdot \cos(\emptyset) = P_{bat\_max} = V_{bat} \cdot I_{bat\_max}$$

$$where \quad I_{max} = \frac{2}{\sqrt{3}} \frac{I_{bat\_max}}{cos(\emptyset)} \tag{3-30}$$

MODE III: In this configuration, the three-phase bridge is left permanently in zero vector state "000", so the total requested output voltage is delivered by the

three-level H-Bridge section. This means that all the active and reactive power required by output is delivered by UC (P_{uc}). If inverter losses are omitted the power equation for the total active power of the system can then be expressed as a sum of the active power delivered by each UC (3-31).

$$P = P_{uc} = V_{uc\_A} \cdot I_{uc\_A} + V_{uc\_B} \cdot I_{uc\_B} + V_{uc\_C} \cdot I_{uc\_C} = \frac{3}{2} V_{ref} \cdot I \cdot \cos(\emptyset), \quad (3\text{-}31)$$

$$P_{bat} = 0$$

The maximum output power is proportional to the UC's state of charge, and since the UC's maximum current in comparison to other elements of the system has much higher limit, the inverter current limit bears greater relation to the maximum motor or switch element current. Figure 3-21 illustrates an example output power characteristic for a UC with voltage varying from 0 to 50V.

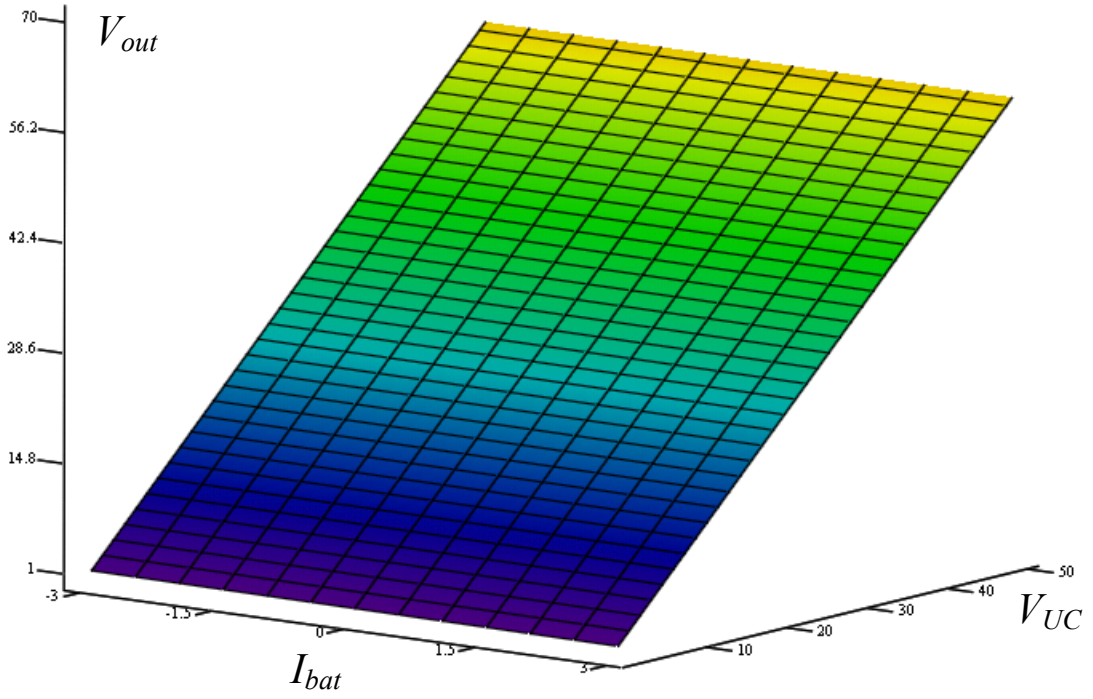
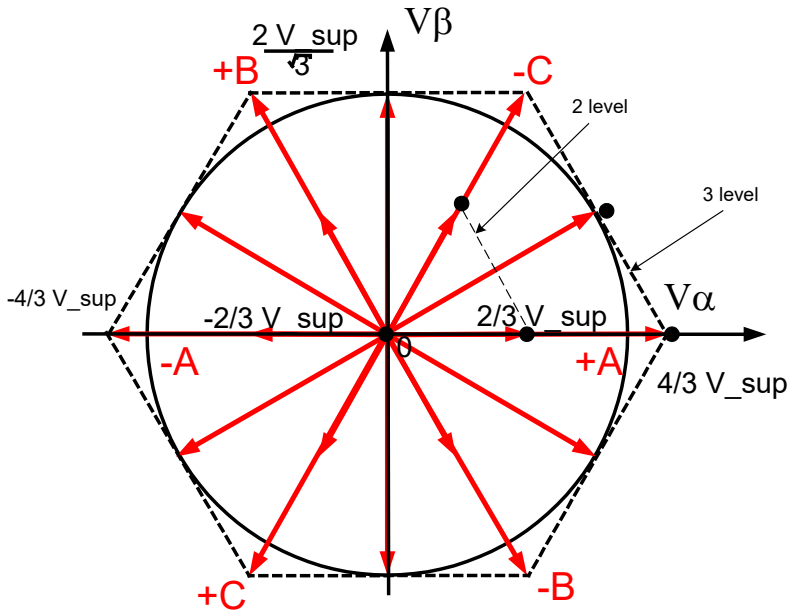


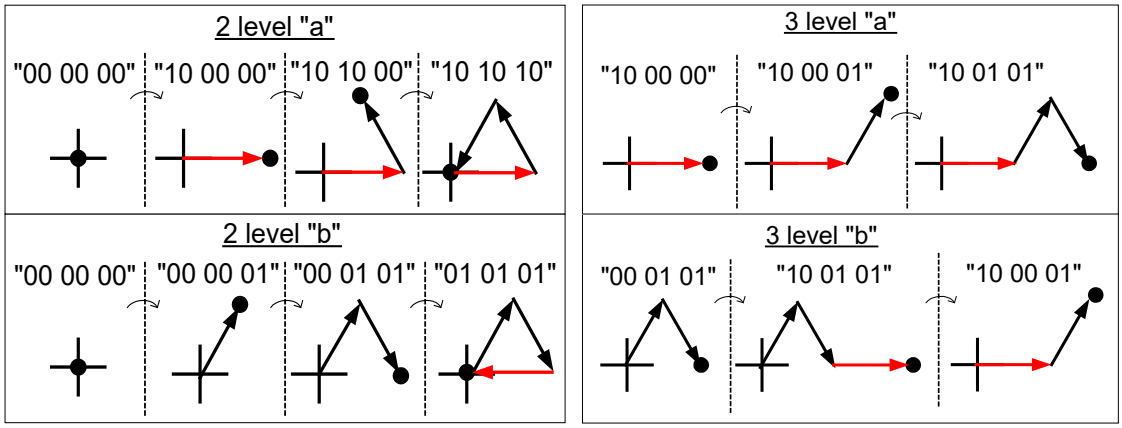
Figure 3-21 Available output voltage (*Vout*) in MODE III in relation with UC's average voltage value (V_{UC}) and maximum output current from main source (I_{bat})

In Figure 3-21 we can see that the voltage limit is a flat plane that doesn't change within current variation but only is in relation to UC voltage amplitude.

The SVM modulation for H-Bridges requires additional control to maintain the voltage of all three UCs at the same level. For normal operations the symmetrical switching of voltage vectors provides good results, but in the case of a variable load, drift may appear. Figure 3-22 shows two possible switching combinations ("a" and "b") that can be used to generate redundant reference voltage vector for two-level and three-level operations.



(a) Available vectors in three-phase H-Bridge



(b) Vector combinations in two level (c) Vector combinations in thee level

Figure 3-22 Alternative voltage vector combinations for a three-phase H-Bridge three level inverter. Redundant voltage vector combinations are used to control capacitor's voltage

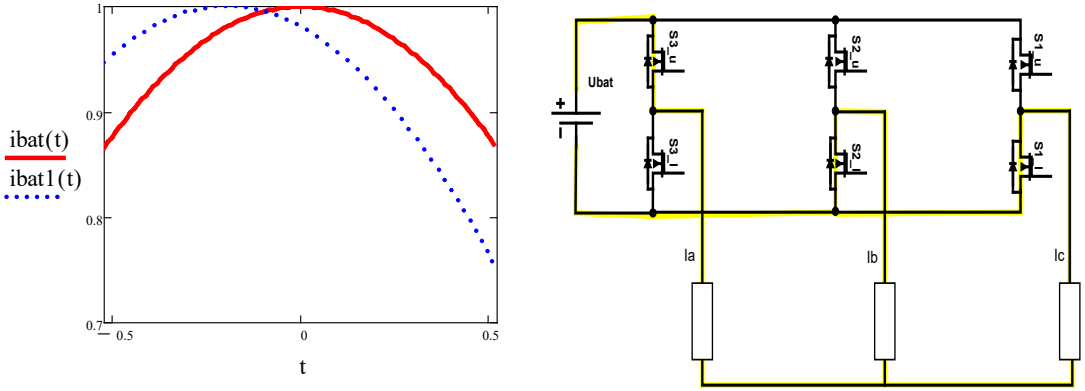
Depending on the direction of the current vector, by selecting an appropriate switching combination it is possible to control the amount of power that is delivered from each source. In the case of two-level voltage modulation, to generate the vector in sector 1 (between vectors +A and -C) it is possible either to select the switching combination with the positive vector "+A" ("a" combination) or to use a second combination where the UC in phase A will see the current in the opposite direction (case "b"). The first combination ("a") for three-level modulation has permanently switched vector +A "100000", allowing the phase current I_{uc_A} to flow through the UC throughout the duty cycle, discharging capacitor in phase A for the case when motor current is positive in phase A. By selecting the second switching scheme "b" for the same current vector the amount of time that UC in phase A sees phase current is reduced by the dwell time of the first vector "000101". In the case of the voltage amplitude at one of capacitors exceeding the average value over a set threshold in adequate sector a switching configuration is selected where the corresponding capacitor is sourcing less current. The control between redundant vector combinations is based on hysteresis control and is correlated with phase current sign in corresponding sector. Example: if current in phase A is positive and reference vector can be achieved by two level modulation in sector one (between vector A+ and C-) then to increase UC voltage in phase B the "b" switching combinations has to be used (2 level "b"). This method of voltage regulation requires the elaboration of separate reference tables for each of the two cases, and, depending on the voltage error and current vector location, to change the switching combination for adequate sector.

3.5.3 Inverter in multilevel operation mode with all sources active simultaneously

As mentioned in the previous section, it is desirable only to switch between selected voltage vectors as there are vector combinations requiring the switching of a high number of transistors as shown in Figure 3-7, which, in proportion to the number of transitions, increase power losses. Additionally there are switching combinations that introduce big voltage and current ripples since the transition states between some vectors can have large differences

between coordinates. For this reason, it is proposed that during multilevel modulation the inverter works with one section operating at fundamental frequency in six- or 12-step mode and the other section provide the remaining voltage by Space Vector Modulation. Distinguishing which part of the inverter is switched at fundamental frequency and which parts are operating in SVM mode helps to calculate how the power share is distributed between them.

For the section of the inverter that is operating in six-step mode it can be assumed that the voltage source will see a sinusoidal phase current, which is repeated every one sixth of the period with a phase shift dependent on the power factor (Figure 3-23).



(a) Current seen by battery during period of $\pi/6$

(b) Inverter section active for vector "100" in three-phase-bridge

Figure 3-23 Current seen by battery during one sixths of period for zero ($i_{bat}(t)$) and $\pi/16$ phase shift ($i_{bat1}(t)$) and current path in three-phase inverter

Based on the assumption above, in order to calculate active power delivered by the sources we can formulate a power equation for six-step switching together with power factor and additional inverter voltage phase shift "χ". The aim of including the phase shift angle parameter "χ" is to allow fine control of the active power that is supplied by the source. Depending witch inverter section is operating at fundamental frequency we can identify following modulation schemes.

MODE II: For operations with a three-phase bridge in a six-step switching, the power delivered by the main battery can be calculated as an integral of the motor phase current seen by the source and battery voltage for one sixth of the period as presented in the equation (3-32).

$$P_{bat} = \frac{3}{\pi}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} V_{bat}\cdot I\cdot\cos(\omega t+\emptyset+\chi)dt\ = \tag{3-32}$$

$$\frac{3}{\pi}V_{bat}\cdot I\cdot\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}}\cos(\omega t+\emptyset+\chi)dt \quad = \quad \frac{3}{\pi}V_{bat}\cdot I\cdot\cos(\emptyset+\chi)$$

The equation above shows that the power can be adjusted by altering the voltage phase of the output six-step waveform where the maximum phase shift is limited by the output voltage, which can be generated by a given phase shift (as presented in section 3.4).

Figure 3-24 illustrates the current from the battery and the influence of the power factor on the output power. The introduction of the phase shift (χ) angle has a similar effect on the main power source while at the same time it is possible to compensate for the power factor by a phase shift. We can find from presented figure relation between phase shift and active power delivered by source.

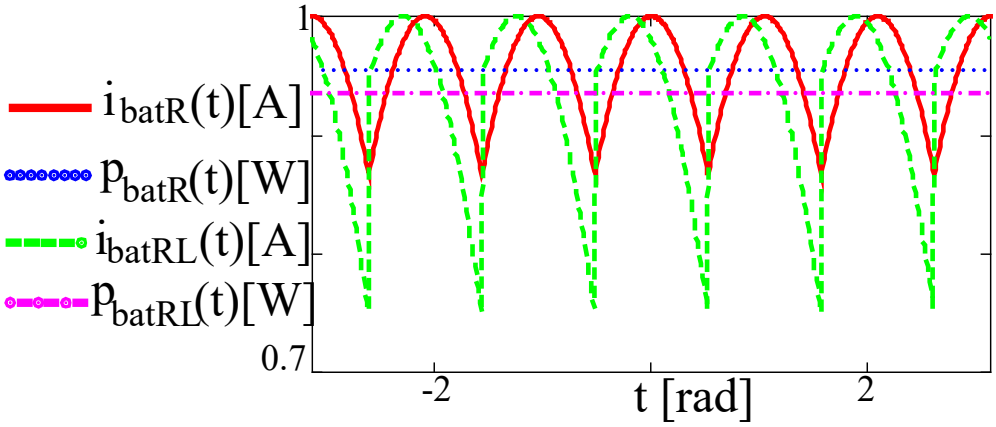


Figure 3-24 Current seen by main source for resistive load $i_{bat\_R}(t)$ (red) (without phase shift) and for RL load $i_{bat\_RL}(t)$ (green) (with phase shift) and corresponding output power

Since the output voltage delivered by the six-step waveform is fixed and depends on the relation between the output power demanded of the inverter and the power that is delivered by the source operating in six-step mode, then it is possible to either sink or source energy from the second source operating in SVM mode. An example is presented in Figure 3-25 where the power delivered by a battery in six-step mode $p_{bat}(t)$ is, in the first case, lower than the total output power $P1(t)$, whereas in the second case the power is higher than the output power $P2(t)$; the corresponding instantaneous power from the UC $p_{uc\_1}(t)$ in the first case is positive and $p_{uc\_2}(t)$ is negative.

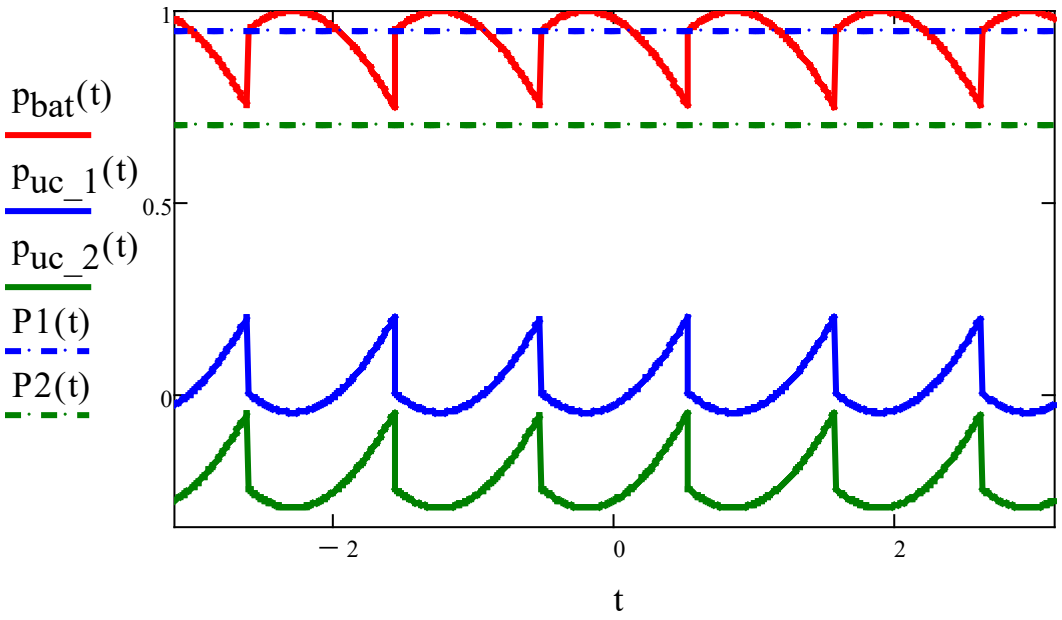


Figure 3-25 Instantaneous power seen by auxiliary source (UC's) in case when power delivered by main source is smaller ($p_{uc\_1}(t)$) or higher ($p_{uc\_2}(t)$) than power sink by load

As discussed earlier for MODE II modulation, the minimum and maximum output voltage is limited by the UC's state of charge. Similarly to SVM, for a three-phase bridge the maximum and minimum output voltage is limited so as not to exceed the battery current limits. Figure 3-26 illustrates the envelope of voltage limits in relation to the battery current and the UC's voltage in MODE II. The maximum and minimum voltage that can be delivered by the inverter depends here proportionally to the UC's state of charge, meaning that this switching mode is very limited in terms of output voltage. We can notice in

presented graph that when UC decrees the boundary of available minimum and maxim voltage linearly decrease. Also the load current has a significant effect on its output voltage envelope, since, as shown by the graph, the phase shift power control is limited, meaning that in case of current increase beyond the battery's limit the modulation scheme has to be changed into one that can provide sufficient current and voltage.

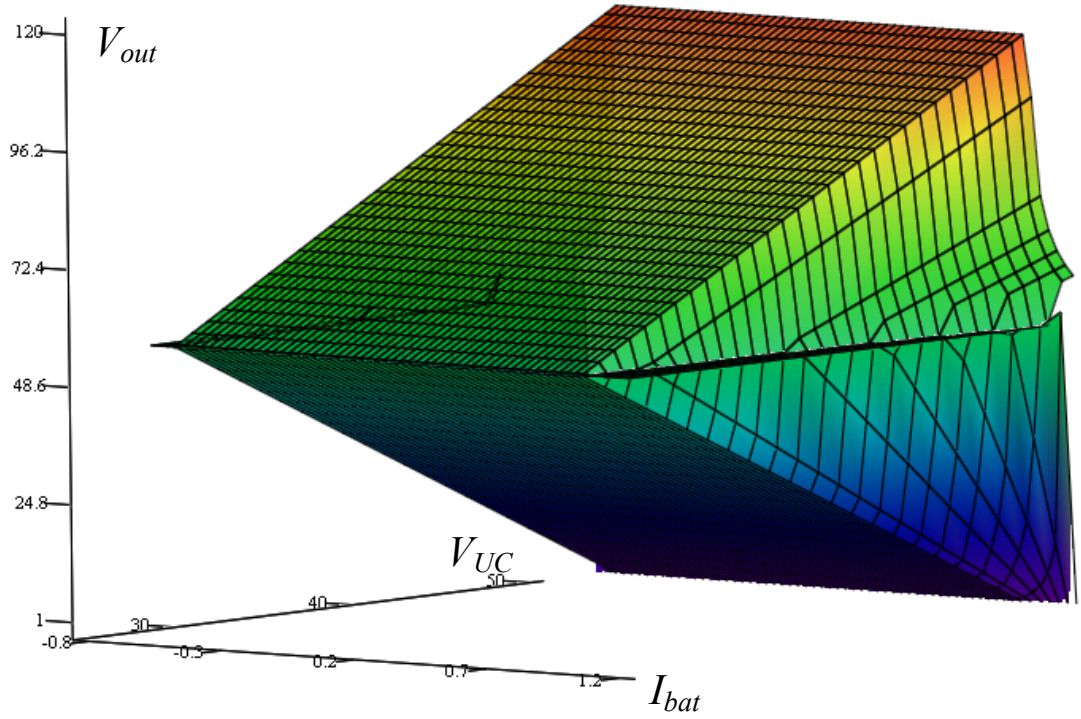
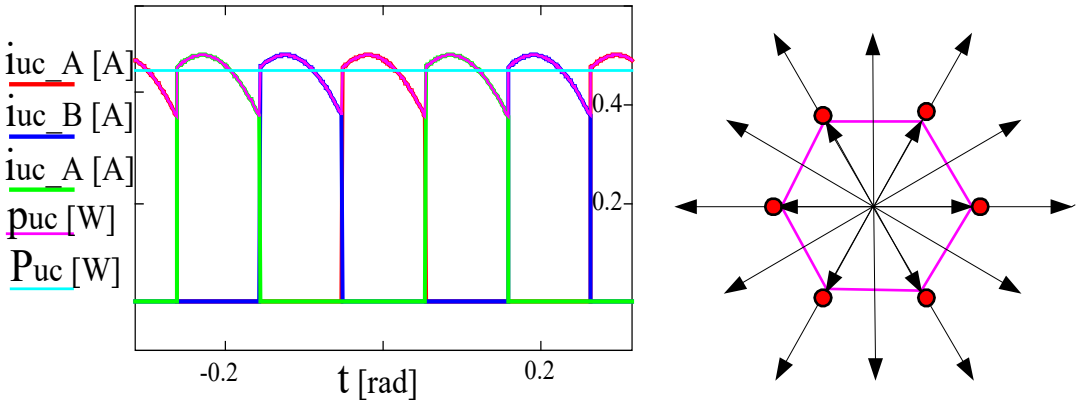


Figure 3-26 Envelope of voltage limits for modulation strategy (MODEII) with three-phase bridge in six-step modulation and H-Bridge compensating error where amplitude of main source V_{bat}=100V is constant and UC's voltage vary from 0 to 50V

MODE IV: The H-Bridge operates in six-step mode at fundamental frequency where only one H-Bridge is active at a time (each H-Bridge is active through a third of the period) and a three-phase bridge is compensating harmonics by SVM. The active power delivered by the UCs is as an integral of the active power seen by the UC's average voltage source V_{uc_avg} which is simplified into the equation (3-33).

$$P_{uc} = \frac{1}{\pi}\left(V_{uc\_A} + V_{uc\_B} + V_{uc\_C}\right) \cdot I \cdot \cos(\emptyset + \chi) = \frac{3}{\pi} V_{uc\_avg} \cdot I \cdot \cos(\emptyset + \chi) \quad (3\text{-}33)$$

The profile of the instantaneous power seen by each H-Bridge source and its average value is illustrated in Figure 3-27.



(a) Current sourced by UCs in mode IV (b) H-Bridge vector trajectory

Figure 3-27 Currents sourced by UC (i_{ucA} , i_{ucB}, i_{ucC}) in mode IV and their total instantaneous (p_{uc}) and average power (P_{uc}) from H-bridges

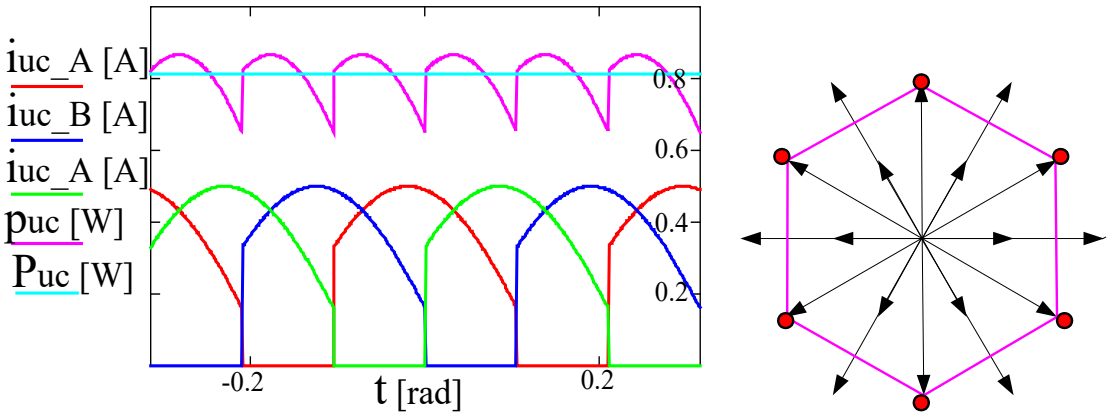
MODE V: If two H-Bridges that produce adjacent vectors are switched on together, the six-step active sector is shifted by $\pi/6$. Solving integral of the instantaneous power within sector I $(0, +\pi/3)$ seen by all three H-Bridges, we receive equation (3-34) and finally (3-35) that allows the calculation of the power sourced from the UCs. The profile of instantaneous power, its sum and average value are shown in Figure 3-28.

$$P_{uc} = \frac{3}{\pi}\left(\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} V_{uc\_A} \cdot I \cdot \cos(\omega t + \emptyset + x)dt + \int_{-\frac{\pi}{6}}^{0} V_{uc\_B} \cdot I \cdot \cos\left(\omega t + \emptyset + x + \right.\right. \quad (3\text{-}34)$$

$$\left.\left. -\frac{\pi}{3}\right) dt + \int_{0}^{\frac{\pi}{6}} V_{uc\_C} \cdot I \cdot \cos\left(\omega t + \emptyset + x - \frac{\pi}{3}\right) dt\right) =$$

$$= \frac{2}{\pi}\left(V_{uc\_A} + V_{uc\_B} + V_{uc\_C}\right) \cdot I \cdot \cos(\emptyset + x) \cdot cos\left(\frac{\pi}{6}\right) dt$$

$$P_{uc} = \frac{\sqrt{3}}{\pi}\left(V_{uc\_A} + V_{uc\_B} + V_{uc\_C}\right) \cdot I \cdot cos(\emptyset + \chi) \quad (3\text{-}35)$$

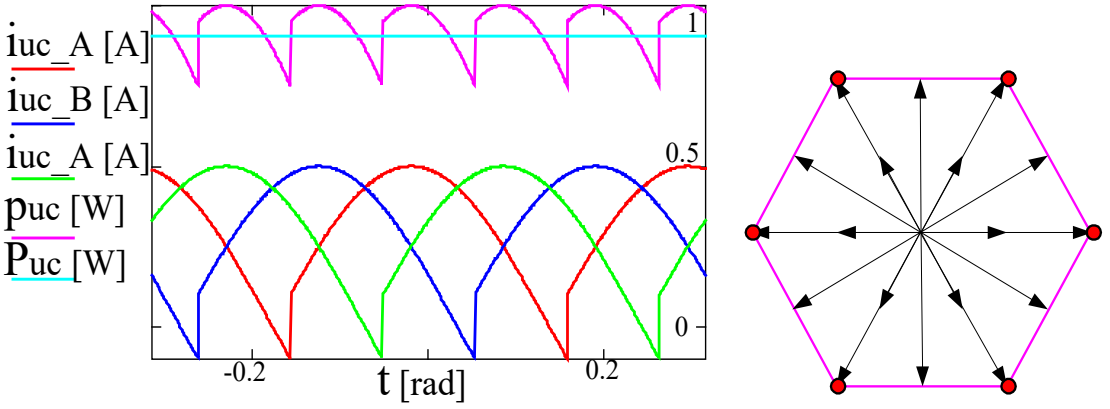


(b) Current sourced by UCs in mode V (b) H-Bridge vector trajectory

Figure 3-28 Current sourced by UC (i_{ucA} , i_{ucB}, i_{ucC}) in mode V and corresponding instantaneous power from three UC (p_{uc}), and average power from H-bridges (P_{uc})

MODE VI: To source or sink the maximum output power from the H-Bridges a switching strategy can be implemented with all three bridges active at the same time. The power sourced from the H-Bridges doubles in comparison with mode IV as it is presented in equation (3-36) and Figure 3-29.

$$P_{UC} = \frac{2}{\pi}(V_{UC\_A} + V_{UC\_B} + V_{UC\_C}) \cdot I \cdot \cos(\emptyset + \chi) \tag{3-36}$$



(a) Current sourced by UCs in mode VI (b) H-Bridge vector trajectory

Figure 3-29 Current sourced by UC (i_{ucA} , i_{ucB}, i_{ucC}) in mode V and corresponding instantaneous power from three UC (p_{uc}), and average power from H-bridges (P_{uc})

For a current-limited source, such as a battery, the maximum output voltage is related to the maximum output current so its output power remains within limits.

For modulation modes where H-Bridges are switched at fundamental frequency (MODE IV, MODE V and MODE VI) the inverter output voltage limit is similar to modulation in MODE I with difference that the whole limiting envelope is offset depending on UC amplitude. The voltage envelope for modulations mode with UC in six-step switching can be described as the sum of the characteristics for Mode I (Figure 3-20) and Mode III (Figure 3-21) as presented in Figure 3-30. The graph shows output voltage limiting boundary for MODE IV and MODE VI where available output voltage is inside the sphere.

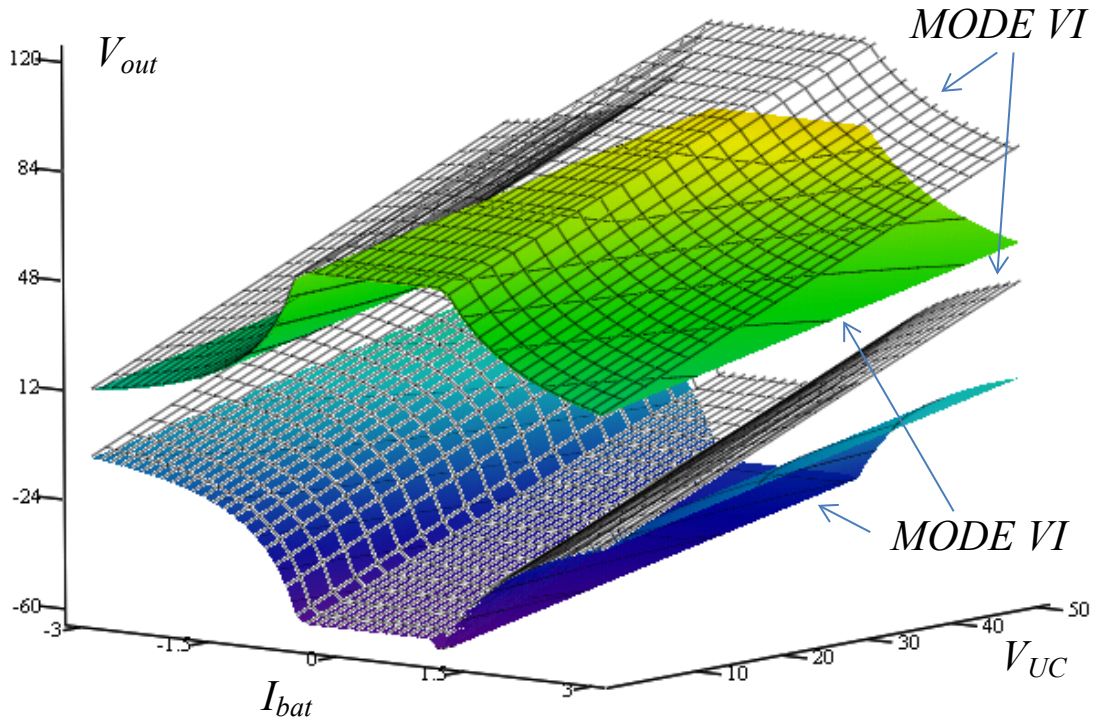


Figure 3-30 Envelope of voltage limits for modulation strategy MODE IV (colour envelope) and MODE VI (transparent envelope) for amplitude of main source V_{bat}=100, UC's voltage variable from 0 to 50V and variable battery current

The characteristic depends here on the UC's state of charge and on whether the vectors from the three-phase bridge and H-Bridges are added to or subtracted from the maximum and minimum voltage limits that were identified. The negative voltage in this case describes the condition where the six-step vectors from H-Bridges are in the opposite direction to the reference vectors so the direct power transfer occurs between sources. It possible to notice that limits of operational voltages become much wider.

In Figure 3-31 the voltage limits for the rest of the switching modes are presented together (MODE I, MODE II and MODE III). The maximum output voltage in this case has a very limited operating range and is related with MODE II. Achieving higher output voltage is strongly narrowed by the battery's current as well as the voltage of the UC.

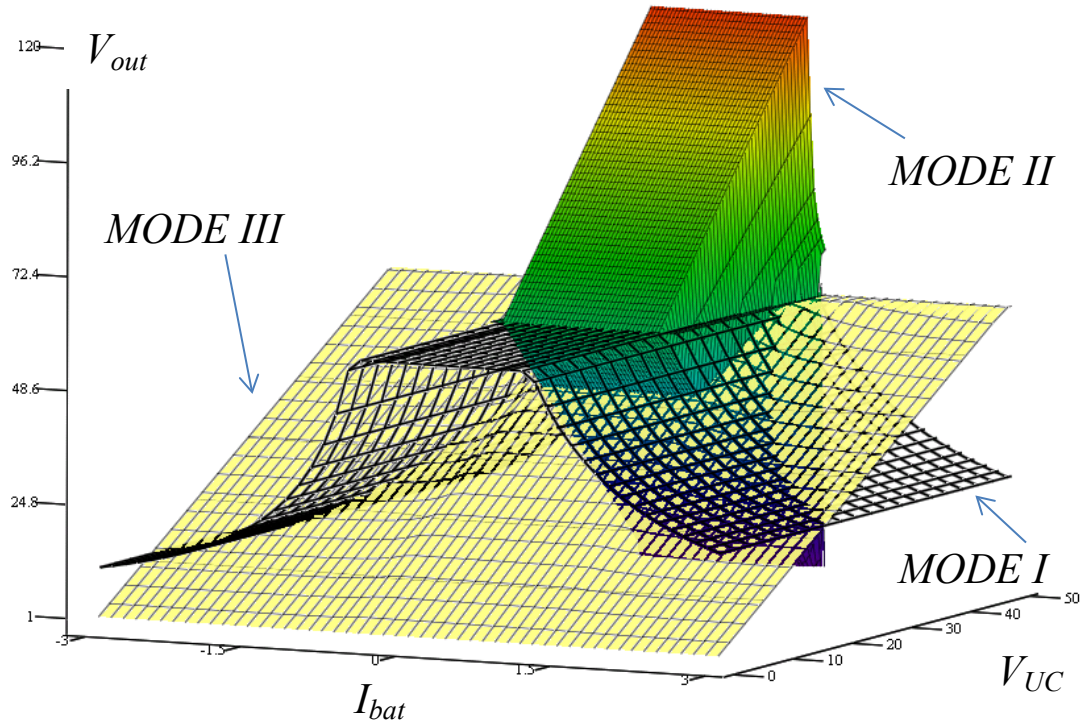


Figure 3-31 Envelope of voltage limits for modulation strategy MODE II (colour envelope), MODE I (transparent envelope) and MODE III (yellow plane) for amplitude of main source V_{bat}=100, UC's voltage variable from 0 to 50V and variable motor current

It can be concluded that to achieve the maximum operating range of a hybrid cascade inverter, the modulation method with six-step switching of three H-Bridges is needed as presented in Figure 3-32, where the limits for all switching strategies are presented. From that graph we can find that if the UC voltage is low or battery current is high then to achieve full available voltage range the other than MODE II modulation scheme has to be used. By utilizing modulations with H-Bridges switching at fundamental frequency the inverter capability is expanded. MODE V is omitted to make illustrations more transparent.

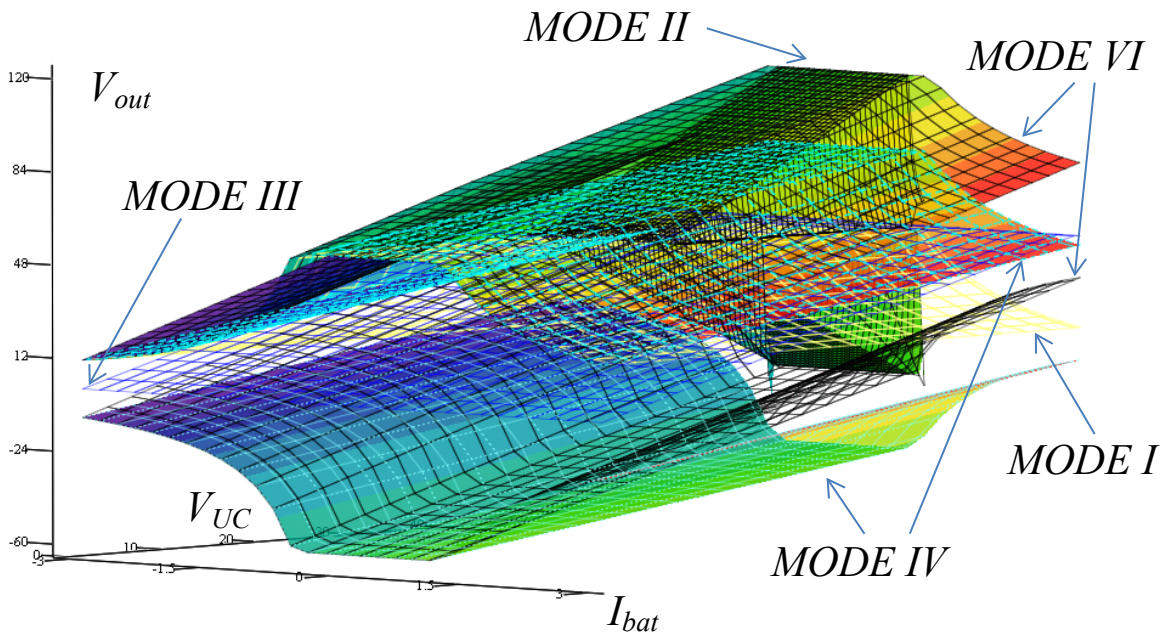
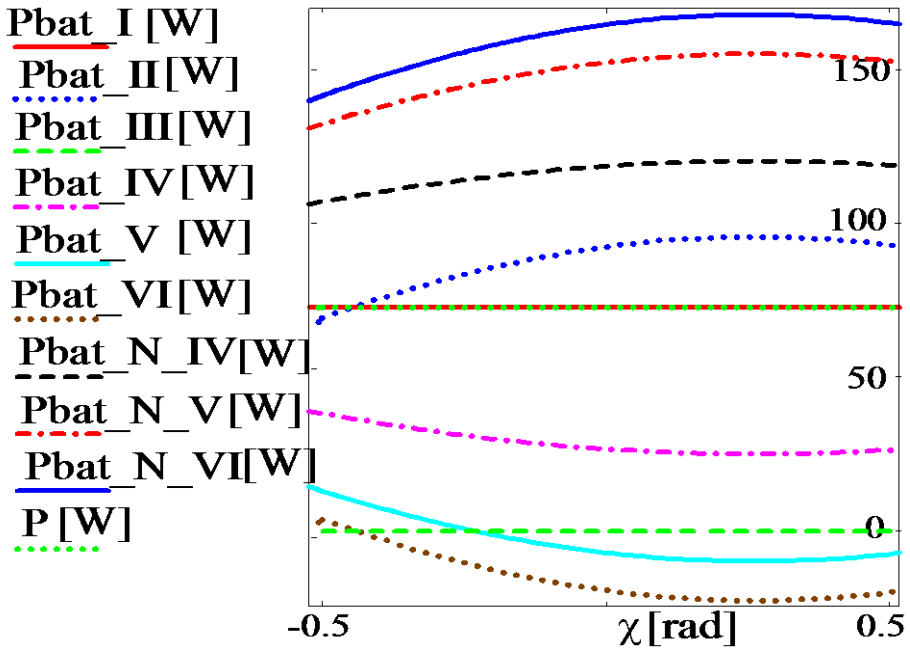
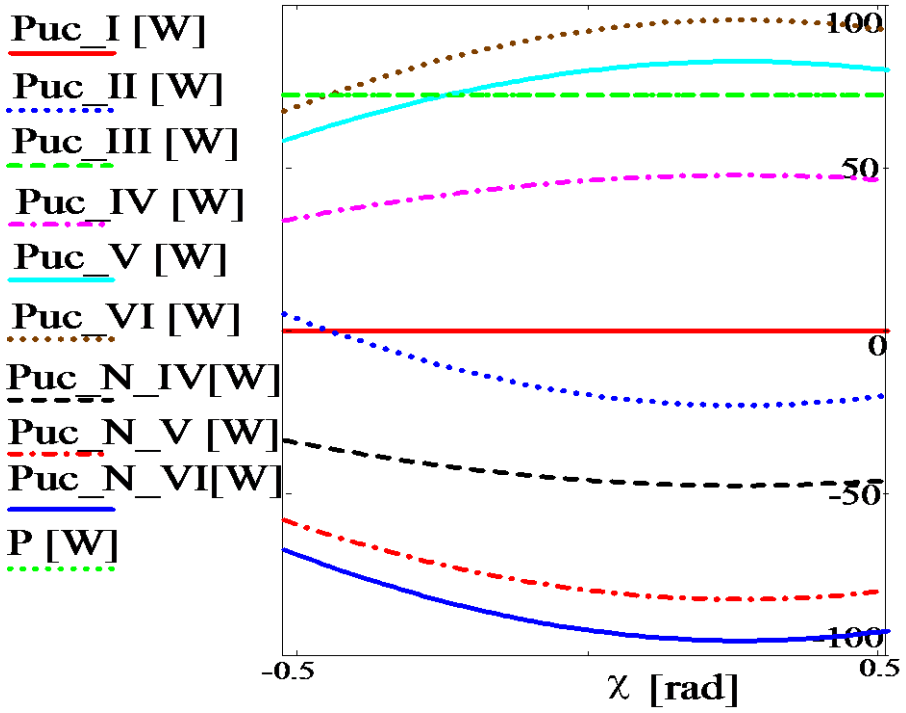


Figure 3-32 Envelope of voltage limits for all modulation strategies (I,II, III,IV and VI) with amplitude of main source V_{bat}=100V, UC's voltage V_{uc} variable from 0V to 50V and variable motor current

To better illustrate the power sharing derived from the power equations above, an example power sharing calculation for variable phase shift angle between (χ<-π/6,+π/6>) and power factor *cos(Ø)*=0.966 are presented in Figure 3-33 (V_{bat}=100V,V_{uc}=50V). It is evident that with implemented a phase shift parameter "χ" it is not always possible to control the output power share from the sources as there are power levels that cannot be achieved by any modulation. Also the power sharing levels that are available in MODE II and MODE III where H-Bridges operate in SVM mode are very limited but with help of modulations where H-Bridges are switched at fundamental frequency the power delivered by battery can be either positive or negative. Few of those modulation strategies (MODE IV, MODE V and MODE VI) allow at the same time to transfer energy between sources and to the load.



(a) Power delivered by battery (P_{bat})



(b) Power delivered by UC (P_{uc}).

Figure 3-33 Power sharing regulation with phase shift angle "χ" for identified switching modes (power factor cos(φ) =0.966)

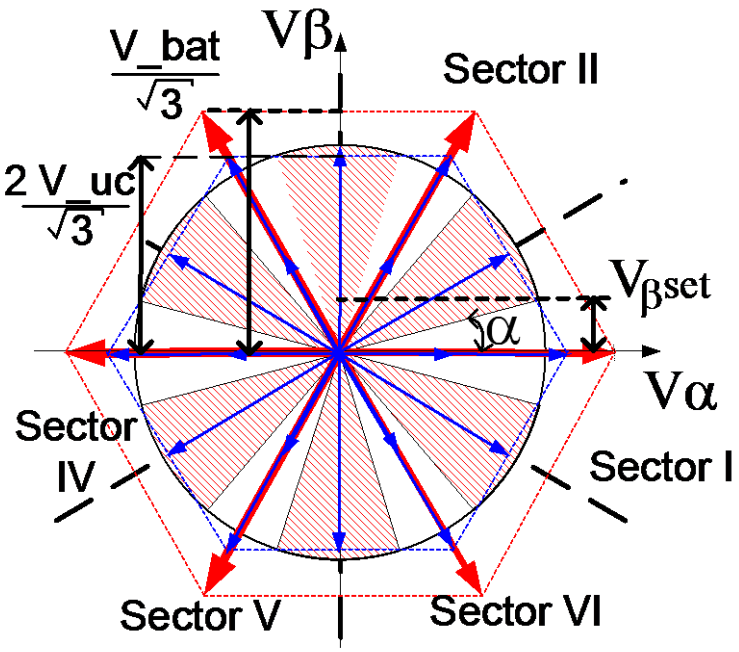
3.5.4 Mixed modulation mode for hybrid multilevel inverter and its power sharing

As presented earlier the phase shift power control is limited by the hexagon boundaries of the voltage vectors specific for each mode. It is also worth emphasising that the operation of the part of the inverter that has the smallest voltage source in SVM mode should be prioritised as this allows the use of the voltage vectors with the smallest error, leading to the lowest current ripples. For MODE II, with a three-phase bridge in six-step switching and H-Bridges in SVM, which is expected to be the nominal switching strategy, the voltage ratio between the UCs and the battery is variable, limiting its operating range. Since the inverter has six symmetrical sectors, it is proposed to alternate between two switching modes twice per every one sixth of the period. To control power the switch angle "$\propto$" has been defined, where the angle can vary from 0 up to $\pi/6$, as presented in Figure 3-34. The illustrations show in this modulation scheme, the output voltage is limited by the maximum output voltage that can be produced by both switching strategies.

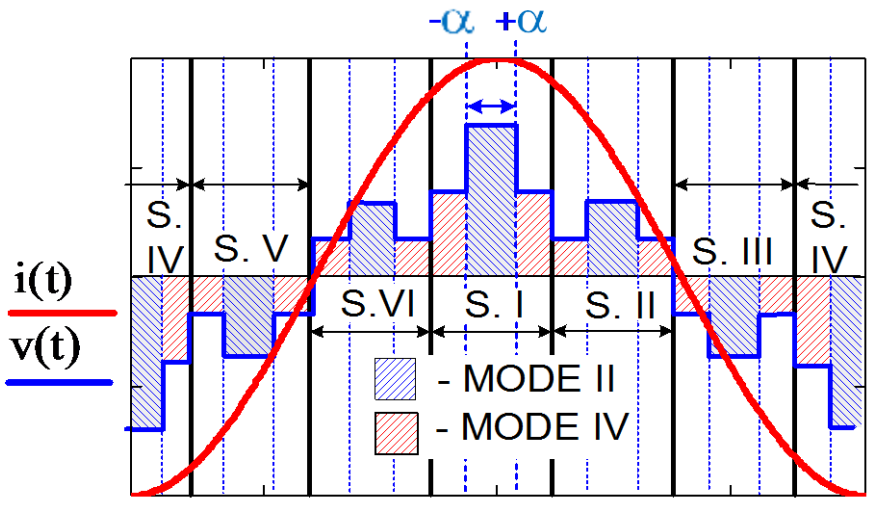
In the case of alternating modulation between two sections of the inverter, the power share between the sources will be proportional to the ratio between the times that each source is active during the period. For alternated SVM with three-phase bridge and H-Bridges only (MODE I and MODE III) it will be possible to share load but not to transfer power between sources. The power delivered by each source can be calculated as integral through one sixth of the period (from $-\pi/6$ to $+\pi/6$) of instantaneous powers seen by sources (3-37), (3-38). It is expected that the use of a three-phase inverter in the region from $-\alpha$ to $+\alpha$ should produce the benefit of lower current ripples, as the three-level inverter with H-Bridges is able to modulate the reference voltage vectors that are close to $\pm\pi/6$ with vectors that have a smaller error.

$$P_{bat} = \frac{1}{\frac{\pi}{3}} \int_{-\propto}^{\propto} p(t)dt \tag{3-37}$$

$$P_{uc} = \frac{1}{\frac{\pi}{3}}\left(\int_{\frac{\pi}{6}}^{-\propto} p(t)dt + \int_{\propto}^{\frac{\pi}{6}} p(t)dt\right) \tag{3-38}$$



(a) Presented in α-β coordinates



(b) Motor current and mixed six step voltage for α axis in time domain

Figure 3-34 Strategy to switch between two modulation modes, blue areas symbolize voltage delivered in MODE II and red areas voltage in MODE IV

By solving the equations (3-37) and (3-38) for constant instantaneous power, the control can be simplified into the following form (3-39) and (3-40):

$$P_{bat} = \frac{1}{\frac{\pi}{3}} \int_{-\infty}^{\infty} p(t)dt \tag{3-39}$$

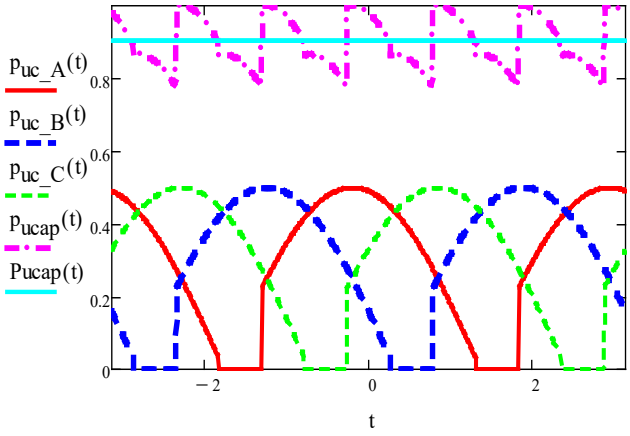
$$P_{uc} = \frac{1}{\frac{\pi}{3}} \left(\int_{\frac{\pi}{6}}^{-\infty} p(t)dt + \int_{\infty}^{\frac{\pi}{6}} p(t)dt \right) \tag{3-40}$$

In this modulation scheme the output voltage is limited by the maximum SVM output voltage for the inverter with the smallest source (inverter with UC's = $(2V_{UC})/\sqrt{3}$). The limit of the output voltage from the inverter can be additionally increased up to $4/3V_{UC}$ depending on the percentage power share between the inverters.

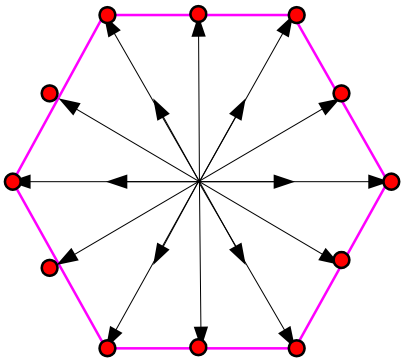
For a mixed operation with a switching strategy using an H-Bridge in six-step switching, it is possible to distinguish a 12-step mode, where instead of every $\pi/3$ the different combinations of two or three UCs are switched every $\pi/6$ ($\alpha=\pi/6$). This switching strategy is a mixed operation consisting either of modes IV and V or modes V and VI. The power that is delivered by the sources can be written as a sum of the integrals for each UC during one sixth of the period. The calculations for the sector between $-\pi/6$ and $\pi/6$ are presented below (3-41):

$$\begin{aligned} P_{uc} = \frac{3}{\pi} \Bigg(& \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} V_{uc\_A} \cdot I \cdot \cos(\omega t + \emptyset + x)dt + \int_{-\frac{\pi}{6}}^{\frac{\pi}{12}} V_{uc\_B} \cdot I \cdot \cos\left(\omega t + \emptyset + x - \frac{\pi}{3}\right) dt \\ & + \int_{-\frac{\pi}{12}}^{\frac{\pi}{6}} V_{uc\_C} \cdot I \cdot \cos\left(\omega t + \emptyset + x + \frac{\pi}{3}\right) dt \Bigg) = \\ = & \frac{2}{\pi} (V_{uc\_A} + V_{ucc\_B} + V_{uc\_C}) \cdot I \cdot \cos(\emptyset + x) * \cos(\frac{\pi}{12}) dt \end{aligned} \tag{3-41}$$

The results of the equation above are presented in Figure 3-35 where instantaneous powers for UCs in phases A, B and C and their sum are presented as $p_{uc\_A}(t), p_{uc\_A}(t), p_{uc\_A}(t)$ and $p_{uc}(t)$ respectively. It is possible to notice that in this operating mode each H-Bridge will be transferring power during 5/6 of the fundamental frequency period.



(a) Current sourced by UCs



(b) H-Bridge vector trajectory

Figure 3-35 Current sourced by UCs (i_{ucA} , i_{ucB}, i_{ucC}) in mixed modes V and VI, and corresponding instantaneous power from three UC (p_{ucap}), and average power from H-bridges (P_{ucap})

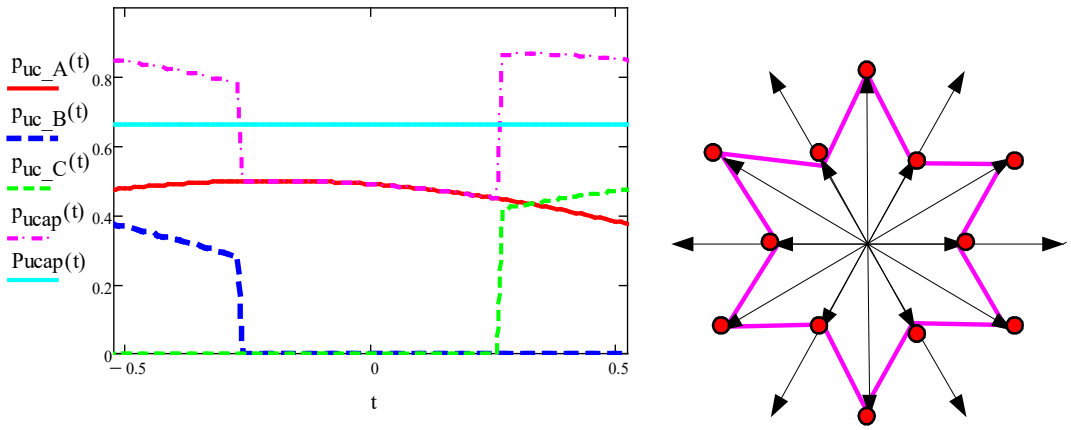
Similarly, equations can be solved for an inverter that operates in 12-step mode with one or two UCs active at a time (3-42) (MODE IV and MODE V):

$$P_{uc} = \frac{3}{\pi}\left(\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} V_{uc\_A}\cdot I\cdot\cos(\omega t+\emptyset+x)dt+\int_{-\frac{\pi}{6}}^{-\frac{\pi}{12}} V_{uc\_B}\cdot I\cdot\cos\left(\omega t+\emptyset+x-\frac{\pi}{3}\right)dt+\int_{\frac{\pi}{12}}^{\frac{\pi}{6}} V_{uc\_C}\cdot I\cdot\cos\left(\omega t+\emptyset+x+\frac{\pi}{3}\right)dt\right)= \quad (3\text{-}42)$$

$$=\frac{2}{\pi}(V_{uc\_A}+V_{uc\_B}+V_{uc\_C})\cdot I\cdot\cos(\emptyset+x)\cdot\cos(\frac{\pi}{4})dt$$

In this mode each H-Bridge will be sourcing or sinking power during only half the period so the output power will be reduced proportionally as shown in Figure 3-36.

To find the expected power distribution between the two sources for all switching modes, the integrals of instantaneous power for mixed modulation strategies alternated at defined variable angle (α) were calculated. It was assumed that for the middle section between $-\alpha$ and α the strategy with a main source that has higher amplitude (battery) is used.



(a) Current sourced by UCs (b) H-Bridge vector trajectory

Figure 3-36 Current sourced by UCs (i_{ucA} , i_{ucB}, i_{ucC}) in mixed modes IV and V and corresponding instantaneous power from three UC (p_{ucap}), and average power from H-bridges (P_{ucap})

The main reason for this modulation order is that the three-phase bridge switched at fundamental frequency has more limitations due to the small amplitude of the voltage vectors from the H-Bridge. The results show a summary of the formulated equations that are expected to be used for the presented modified hybrid cascade inverter.

Modulation with three-phase bridge in SVM alternated with SVM of H-Bridge (MODE I and MODE III). The power share for this scheme is directly proportional to the switch angle α (3-43) (3-44). The power is only transferred by one source at a time and the amplitude is limited by the maximum output from the H-Bridge inverter. It is proposed to use this strategy when the required output vector is small and the H-Bridge voltage is insufficient to use MODE II.

$$P_{bat} = \frac{6}{\pi} \cdot P_{out} \cdot \alpha \tag{3-43}$$

$$P_{uc} = \left(1 - \frac{6}{\pi}\alpha\right) \cdot P_{out} \tag{3-44}$$

Strategy with three-phase bridge in six-step mode alternated with three-phase bridge modulated with SVM (MODE II and MODE I). This strategy can be

useful when a low output vector from the inverter is required but the H-Bridge voltage is too small or it is required to transfer power of the opposite sign to UCs (3-45).

$$P_{bat} = \frac{3}{\pi} V_{bat} I \cos(\emptyset + \chi)\, 2 \sin(\alpha) + \frac{3}{2} V_{ref} I \cos(\emptyset) \left(1 - \frac{6}{\pi}\alpha\right) \tag{3-45}$$

Strategy with three-phase bridge in six-step mode alternated H-Bridges in SVM (MODE II and MODE III). This strategy provides the best performance for small output voltage vectors since H-Bridges with the smallest source are used for SVM, introducing the smallest current ripples. Depending on control angle α it is possible to transfer power to or from UCs (3-46).

$$P_{bat} = \frac{3}{\pi} V_{bat} \cdot I \cdot \cos(\emptyset + \chi) \cdot 2 \sin(\alpha) \tag{3-46}$$

It is also possible to switch the three-phase bridge in SVM alternately with six-step switching from H-Bridge (MODE I and MODE IV). In this case higher voltage than that from the H-Bridge alone can be produced and power can be sourced also from the H-Bridges (3-47).

$$P_{bat} = \frac{3}{2} V_{ref} \mathrm{I} \cos(\emptyset) - \frac{1}{\pi}\left(V_{uc\_A} + V_{uc\_B} + V_{uc\_C}\right) \cdot I \cdot \cos(\emptyset + \chi) \cdot (1 - 2 \sin(\alpha)) \tag{3-47}$$

If the voltage from the UC becomes insufficient it is necessary to alternate six-step modulation from three-phase bridge with six-step switching from H-Bridge (MODE II and MODE IV). This modulation scheme will also increase the power flow from the UC (3-48).

$$P_{bat} = \frac{3}{\pi} V_{bat} \cdot I \cdot \cos(\emptyset + \chi) \cdot 2 \sin(\alpha) + \frac{3}{2} V_{ref} \mathrm{I} \cos(\emptyset) \left(1 - \frac{6}{\pi}\alpha\right) - \frac{1}{\pi}\left(V_{uc\_A} + V_{uc\_B} + V_{uc\_C}\right) \cdot I \cdot \cos(\emptyset + \chi) \cdot (1 - 2 \sin(\alpha)) \tag{3-48}$$

To increase the output power from the UC and for even higher reference output voltage the modulation with the three-phase bridge (MODE II) can be alternated with six-step switching of the H-Bridges in MODE V (3-49).

$$P_{bat}=\frac{3}{\pi}V_{bat}\cdot I\cdot\cos(\emptyset+\chi)\cdot 2\sin(\alpha)+\frac{3}{2}V_{ref}\mathrm{I}\cos(\emptyset)\left(1-\frac{6}{\pi}\alpha\right)- \quad (3\text{-}49)$$

$$\frac{1}{\pi}\left(V_{uc\_A}+V_{uc\_B}+V_{uc\_C}\right)\cdot I\cdot\cos(\emptyset+\chi)\cdot(\sqrt{3}\cos(\alpha)-3\sin(\alpha))$$

For maximum output voltage, and to maximise the output power from the UCs, the six-step switching of the three-phase bridge (MODE II) has to be alternated with six-step of H-Bridges modulation where all UCs are active (MODE VI). In this case the output power from the UCs will be double that of mixed modes, MODE II and MODE IV (3-50).

$$P_{bat}=\frac{3}{\pi}V_{bat}\cdot I\cdot\cos(\emptyset+\chi)\cdot 2\sin(\alpha)+\frac{3}{2}V_{ref}\mathrm{I}\cos(\emptyset)\left(1-\frac{6}{\pi}\alpha\right)- \quad (3\text{-}50)$$

$$\frac{2}{\pi}\left(V_{uc\_A}+V_{uc\_B}+V_{uc\_C}\right)\cdot I\cdot\cos(\emptyset+\chi)\cdot(1-2\sin(\alpha))$$

It is also possible to share power with modulation strategies that use mainly H-Bridges as a power source. In this case we can distinguish conditions where:

The inverter is operating with H-Bridge in six-step mode where only one UC is active at the same time (MODE IV), switched alternately with H-Bridges in SVM mode (MODE III). In this the power delivered by the UCs will be equal to (3-51):

$$P_{uc}=\frac{1}{\pi}\left(V_{uc\_A}+V_{uc\_B}+V_{uc\_C}\right)\cdot I\cdot\cos(\emptyset+\chi)\,2\sin(\alpha)+ \quad (3\text{-}51)$$

$$+\frac{3}{2}V_{ref}\mathrm{I}\cos(\emptyset)\left(1-\frac{6}{\pi}\alpha\right)$$

Modulation with H-Bridges in six-step switching alternated between modulating with one or two UC's active during their section part (3-52) (MODE IV and MODE V).

$$P_{uc}=\frac{1}{\pi}(V_{uc\_A}+V_{uc\_B}+V_{uc\_C})\cdot I\cdot\cos(\emptyset+\chi)\cdot(1+\sqrt{3}+\sin(\alpha)- \quad (3\text{-}52)$$

$$\sqrt{3}\cos(\alpha))$$

Modulation with H-Bridges in six-step switching alternated between modulating with two and three UC's at the same time (3-53) (MODE V and MODE VI).

$$P_{uc}=\frac{1}{\pi}(V_{uc\_A}+V_{uc\_B}+V_{uc\_C})\cdot I\cdot\cos(\emptyset+\chi)\cdot(\sin(\alpha)+\sqrt{3}\cos(\alpha)) \quad (3\text{-}53)$$

The summary of identified modulation schemes for modified cascade inverter is presented in Figure 3-37.

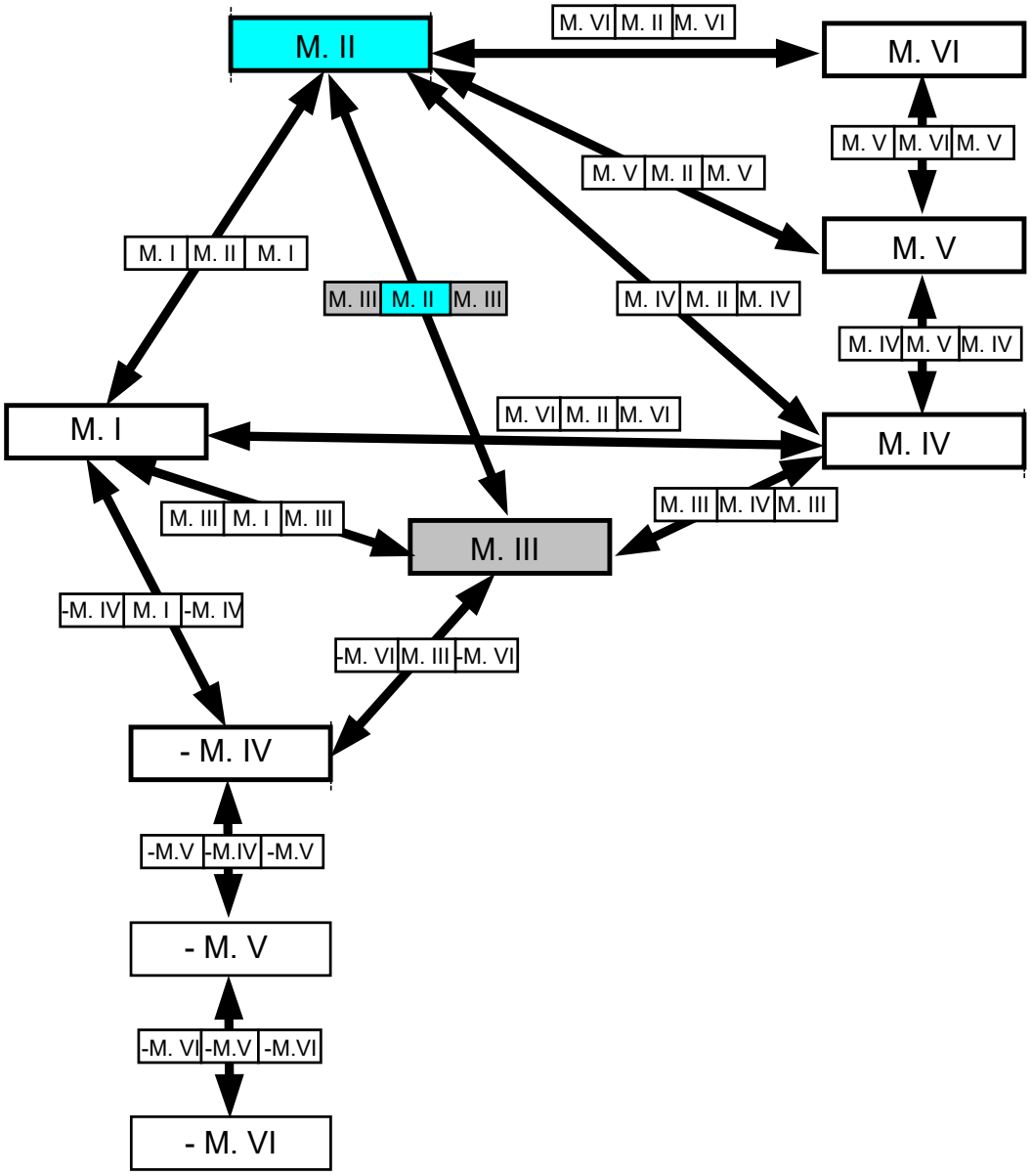
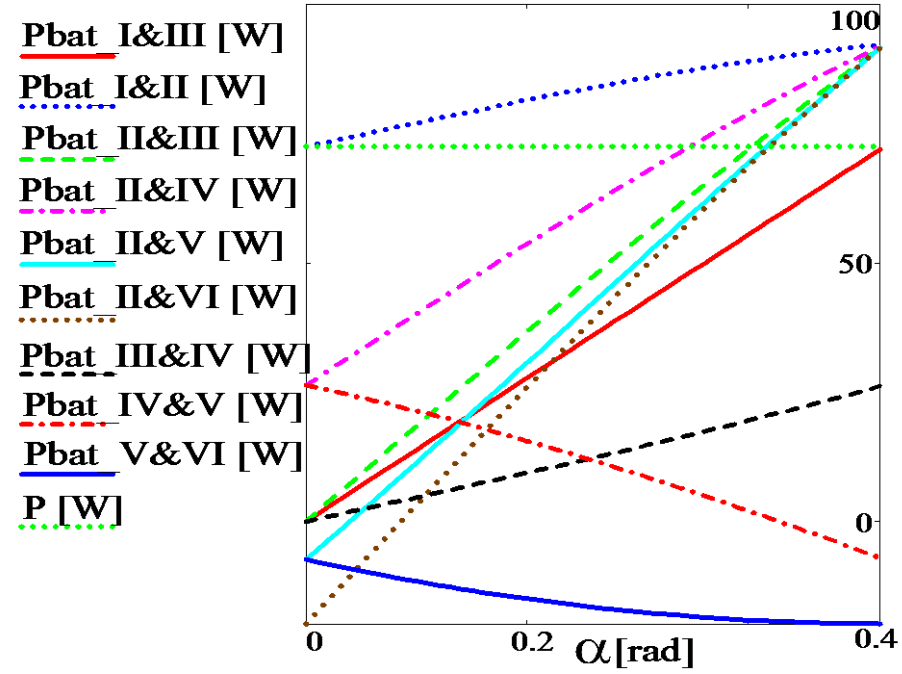


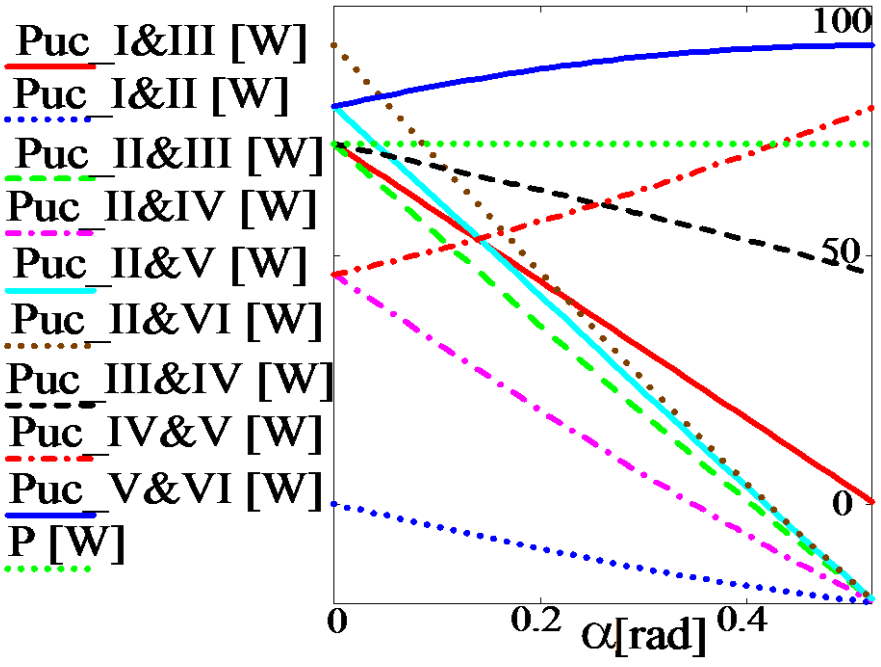
Figure 3-37 Possible modulation schemes and proposed control to switch between them depending on voltage and power share

The MOODE II modulation has been highlighted with blue colour as a starting point in finding the best strategy, since two inverter sections are used and SVM vector is equal to UC voltage. The other important modulation is MODE III with H-Bridges in SVM mode and presented in grey colour (M.III). The transitions between modulation schemes are symbolized with arrows that were identified to allow graduate increase or decrease power, or to increase or decrease voltage with minimum voltage ripple. The voltage ripple criteria are based on relation between voltage reference and vector amplitude. For all cases the transition between modulation schemes can be accomplish by gradually mixing two modulations. For cases when mixed modulation is used, the modulation modes order depends on limiting angles and has been selected to maximize operating range. By implementing those transitions between modulation schemes it become possible to fully utilize inverter capability and gradually change power share between sources. Nevertheless it is allowed to switch instantaneously between all allowed modulation strategies to respond on load step change.

In Figure 3-38 an example of a possible power control for various switching combinations with the following parameters χ=0, *cos(Ø)*=0.966 , V_{bat}=100V, V_{UC}=50V are illustrated. It shows that this strategy allows setting any reference power sharing between maximum and minimum power available by sources. In the case of mixed modulation power control it is possible to set the power share between the sources in a whole range of inverter operations. From presented battery power graph (Figure 3-38 (a)) we can find that maximum battery power is related with MODE II and minimum with MODE VI. By selecting adequate modulation strategies, it is possible to control at what rate power share change, allowing to very precise control power between sources. For mixed modulation in modes V and VI, for defined conditions it becomes possible to deliver power from the UCs to the load and at the same time to the battery. It is also visible that some modulations provide very similar output power what means that not all modulations are necessary in normal inverter operations.



a) Power delivered by battery



b) Power delivered by UC

Figure 3-38 Power-sharing regulation in mixed mode switching for various switching combinations (power factor cos(φ)=0.966)

3.5.5 Harmonics content of mixed operation

The proposed strategy to switch between two modulation schemes was analysed in Mathcad to ensure that this type of switching scheme would not introduce unwanted harmonics. The analysis was performed by numerical calculations of the Fourier series for decomposed waveforms produced by separate source types in single phase (Holmes, 2003),(Mcgrath, Holmes,2002).

The period function can be described as series of functions:

$$f(x) = \frac{1}{2}a_0(x) + \sum_{k=1}^{\infty}[a_k(x)\cos(kx) + b_k(x)\sin(kx)] \tag{3-54}$$

Where parameters can be calculated from equations:

$$a_k(x) = \frac{1}{\pi}\int_0^{2\pi} f(x)\cos(kx)dx \qquad k = 0,1,2... \tag{3-55}$$

$$b_k(x) = \frac{1}{\pi}\int_0^{2\pi} f(x)\sin(kx)dx \qquad k = 0,1,2... \tag{3-56}$$

$$a_0(x) = \frac{1}{\pi}\int_0^{2\pi} f(x)\,dx \qquad k = 0,1,2... \tag{3-57}$$

$$U_{mk} = \sqrt{a_k^2 + b_k^2} \qquad \text{k=1,2,3,4...} \tag{3-58}$$

U_{mk} – magnitude of “k” harmonic

To quantify the results the Total Harmonic Distortion factor was calculated for each type of modulation strategy to describe percentage relation between first harmonic and remaining harmonic content (3-59).

$$THD_u\,(\%) = \sqrt{\left(\frac{U}{U_1} - 1\right)^2}\ 100\% \ = \sqrt{\frac{U_0^2 + \sum_{k=2}^{\infty} U_k^2}{U_1}}\ 100(\%) \tag{3-59}$$

To simplify the calculations the PWM modulation scheme with a symmetrical triangle carrier waveform was used ($F_c(x)$) (Figure 3-39). This type of modulation strategy has many similarities with SVM and is much simpler to solve than the analytical harmonic analysis of SVM.

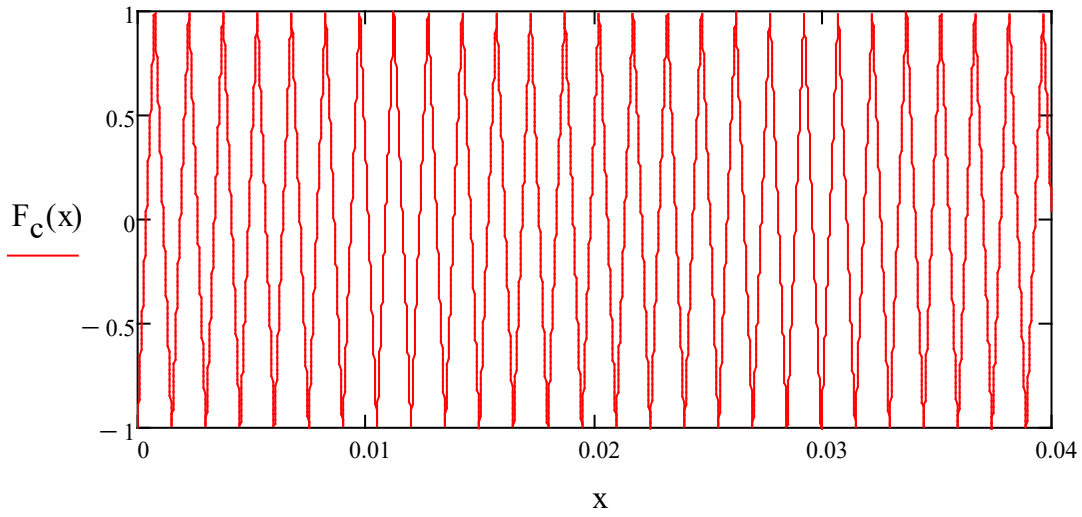


Figure 3-39 Triangle PWM modulation carrier waveform with frequency 21 times higher than carrier frequency

The reference waveform $F_1(t)$ presented in Figure 3-40 is aimed to be synthetized by a modulation strategy with a three-phase bridge in six-step operation and the remaining voltage error $F_3(t)$ modulated by H-Bridges operating in PWM. The inverter output voltage from a battery source in single phase will vary from its positive to negative value twice per period $F_2(t)$.

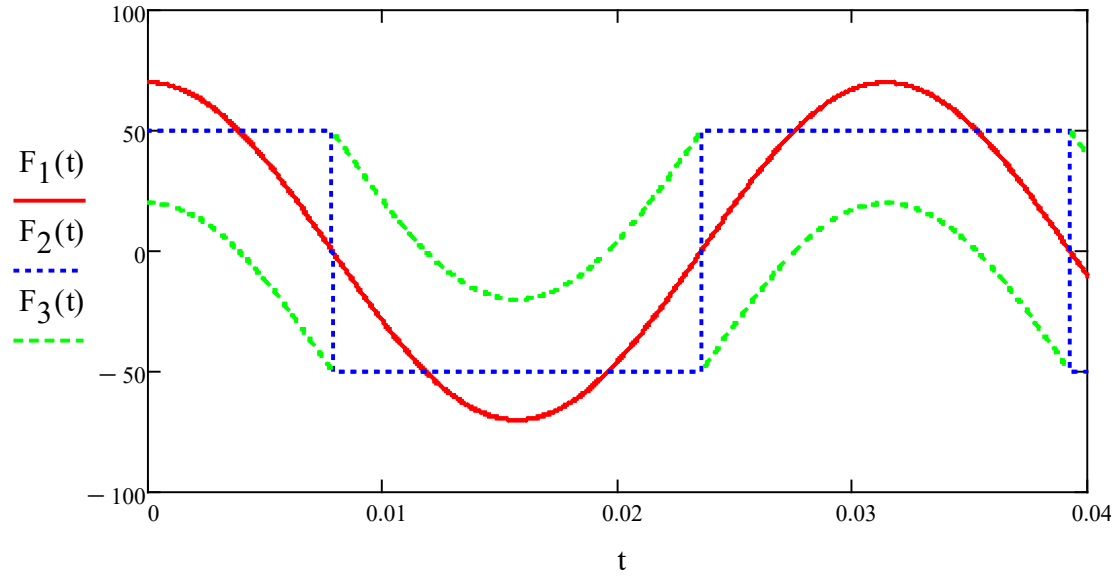


Figure 3-40 Carrier waveform of phase voltage $F_1(t)$, square output voltage from three-phase bridge $F_2(t)$ and remaining voltage for PWM with H-Bridges $F_3(t)$

To analyse the harmonic content in phase voltage for a multilevel inverter with a three-phase bridge switched at fundamental frequency and an H-Bridge in PWM modulation with triangle carrier, first the Fourier series was calculated for a square waveform with first 128 harmonics (Figure 3-41) and later output waveform from the H-Bridge converter (Figure 3-42). The amplitude of the main source supplying the three-phase bridge is equal to 100V and the amplitude of the H-Bridge source is 30V.

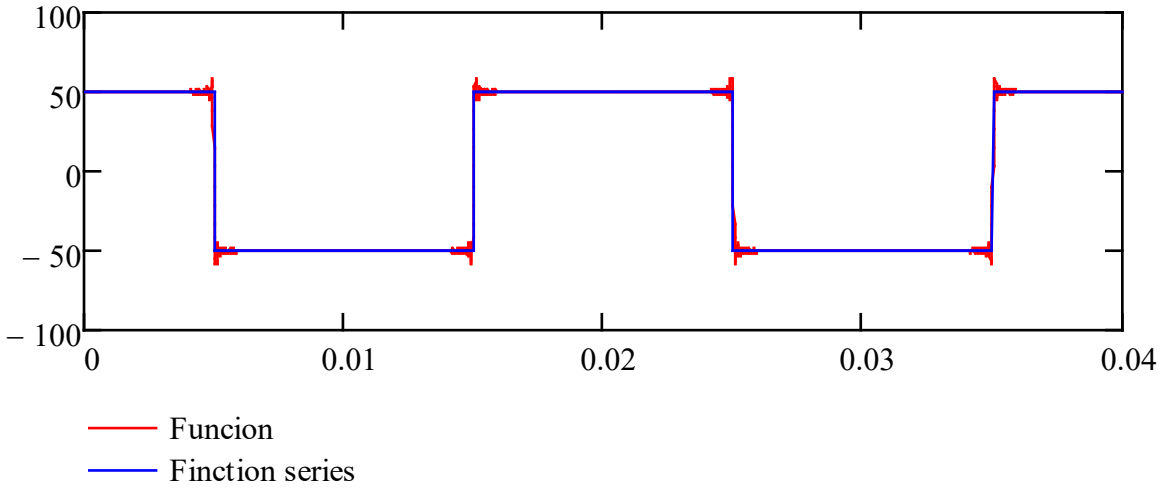


Figure 3-41 Ideal six step waveform (blue) and its series of 128 harmonics (red)

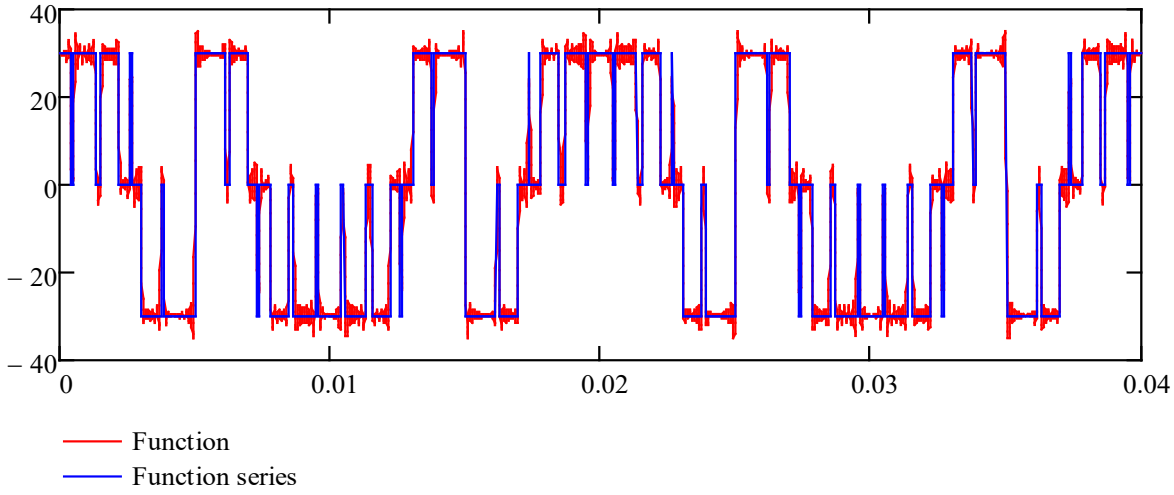


Figure 3-42 The output waveform from H-Bridge section modulated with PWM (blue) and its series of 128 harmonics (red)

The sum of these two waveforms form a synthesized output voltage at single phase what is presented in Figure 3-43 and compared with its time series.

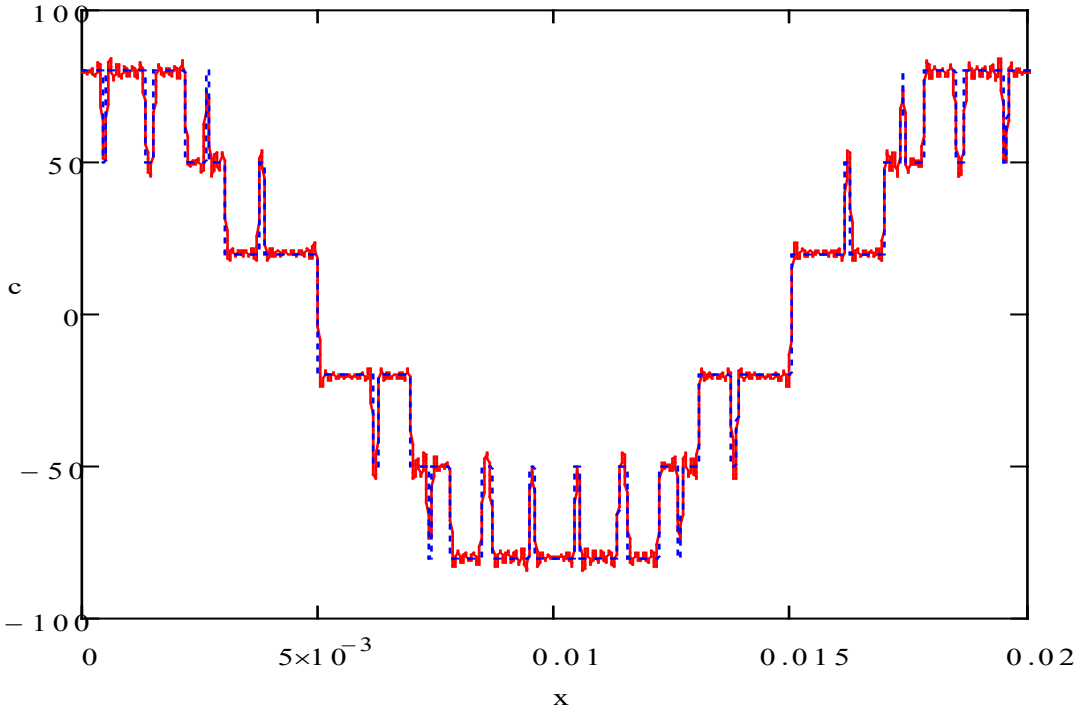


Figure 3-43 The output voltage waveform in single phase from hybrid cascade inverter (blue) and its Fourier series (red)

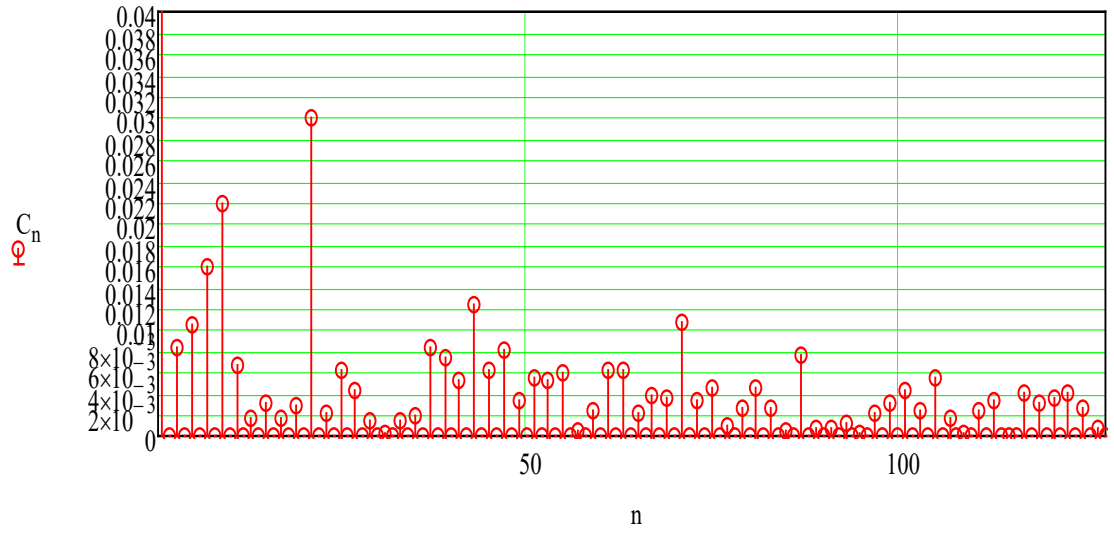


Figure 3-44 Amplitude of 128 harmonics in phase voltage for Mode II modulation scheme

The subsistent harmonic for the waveform under analysis (Figure 3-44) shows the highest harmonic is related with modulation frequency (21 times fundamental frequency), its sidebands and odds harmonics of fundamental frequency (3, 5, 7, 9).

In the case of mixed modulation, the three-phase bridge alternately with the H-Bridge is switched at fundamental frequency with a square waveform. An example of output waveforms and the sum of its harmonic time series are presented in and Figure 3-46, where the switching angle is equal to two periods of carrier frequency. From presented graphs we can find that the sum of those waveform form a square waveform pattern where alternatively voltage change from 50V (half of battery amplitude) to 30V (UC amplitude) six time during period.

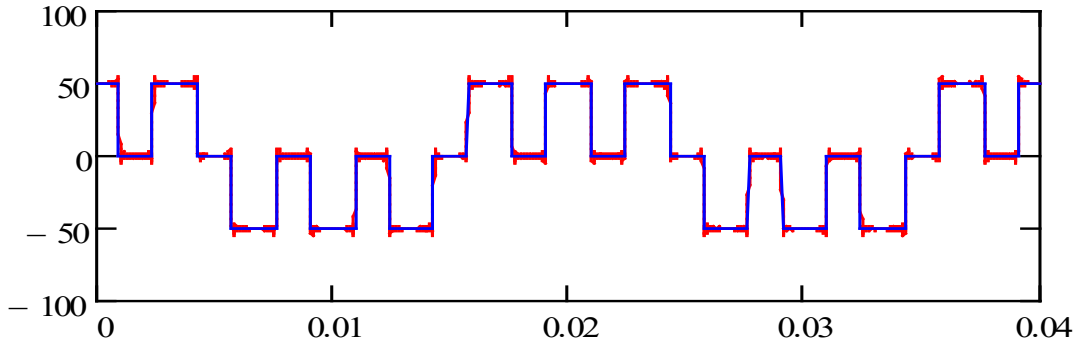


Figure 3-45 Ideal six-step waveform (blue) and its series of 128 harmonics (red) for a three-phase bridge in mixed switching mode

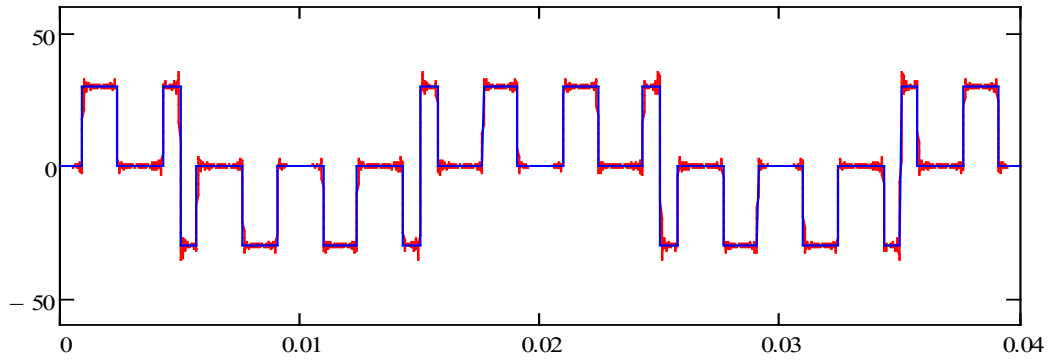


Figure 3-46 Ideal six-step waveform (blue) and its series of 128 harmonics for H-Bridge switched in mixed operation mode

The remaining voltage between square waveform and reference voltage is in the first case generated by the H-Bridge (Figure 3-47) and in the second case by the three-phase bridge (Figure 3-48). The pulses width depends on reference error and amplitude on source used.

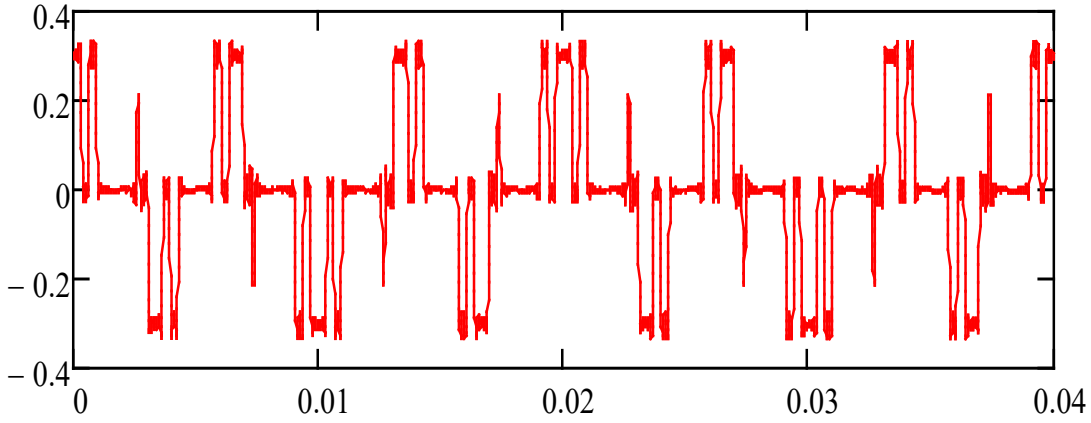


Figure 3-47 Sum of Fourier series modulated in PWM by H-Bridge (amplitude is divided by 100)

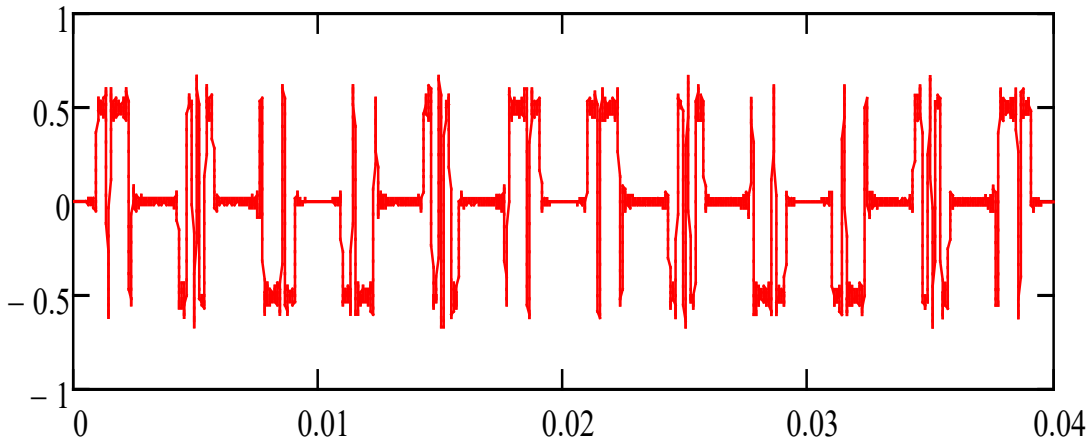


Figure 3-48 Sum of Fourier series modulated in PWM by three-phase bridge (amplitude is divided by 100)

The sum of this Fourier series will give results that represent the output waveform from the inverter when the three-phase bridge, together with the H-Bridge, alternately switch between modulation modes II and IV (Figure 3-49). The sum of the subsequent harmonic in this mode is presented in Figure 3-50.

From harmonics spectrum we can find that only those frequencies related to the carrier frequency increased their amplitude. The analysis results show that 21th harmonic has more than double the amplitude for mixed modulation in comparison to mode II what is related with higher amplitude of switched voltage.

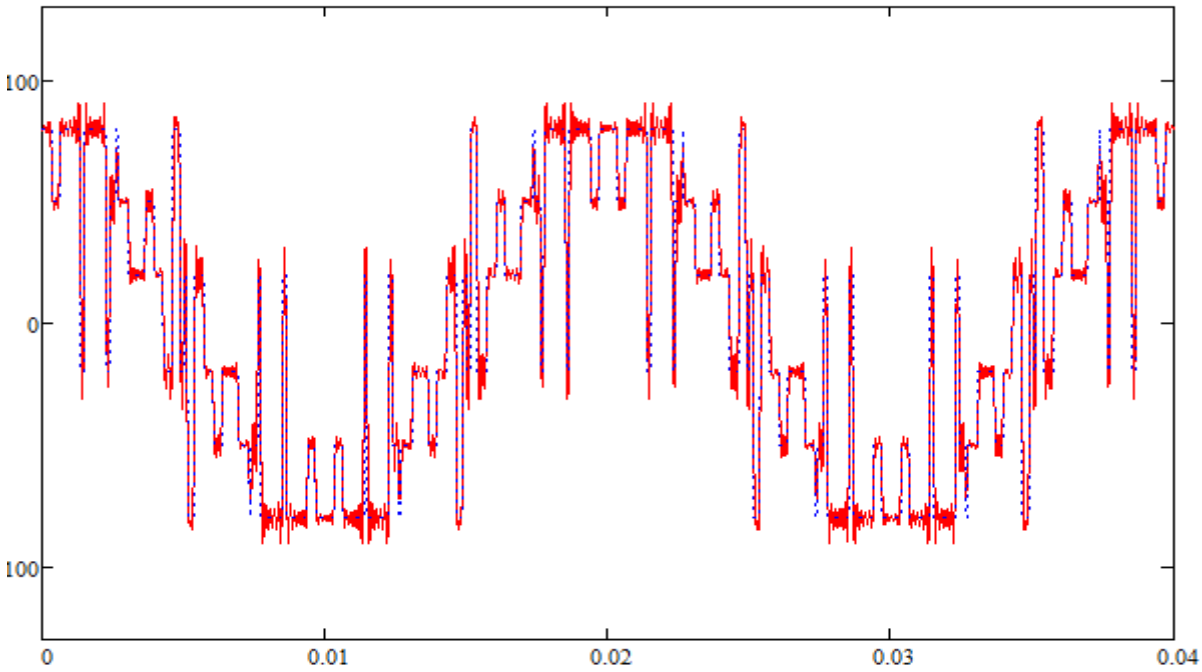


Figure 3-49 Output phase voltage from inverter (blue) and its harmonic series (red) for mixed modulation strategy with mode II and mode IV

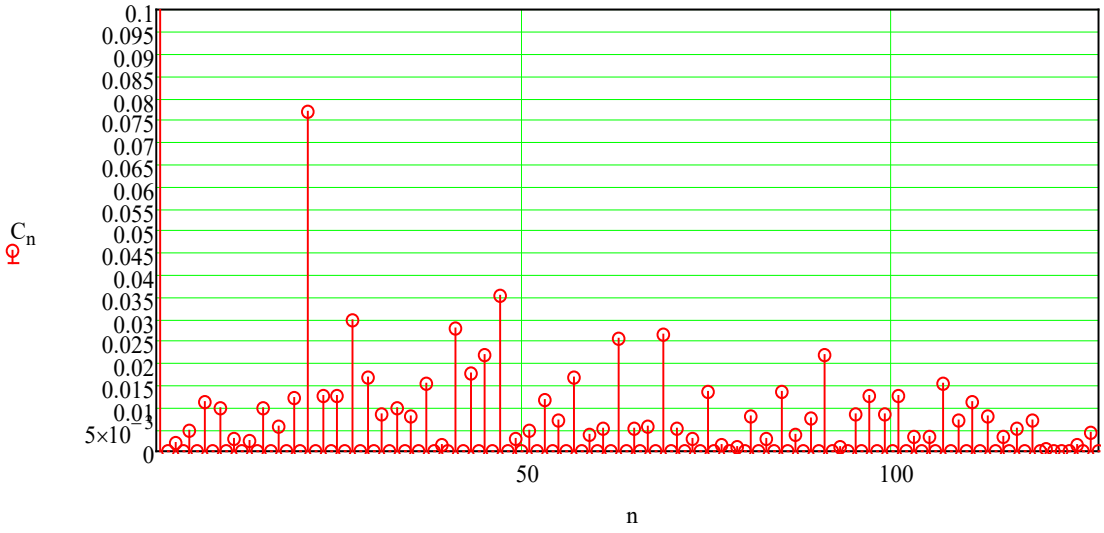


Figure 3-50 Amplitude of harmonics in phase voltage for alternated modulation in modes II and IV

For better comparison, a similar analysis was performed for modulation with the three-phase bridge only where the amplitude of the main source is equal to 200V. The phase voltage in this case will oscillate between positive and negative supply voltage. An example of the waveform for modulation with triangle waveform with 21 time's higher frequency is presented in Figure 3-51.

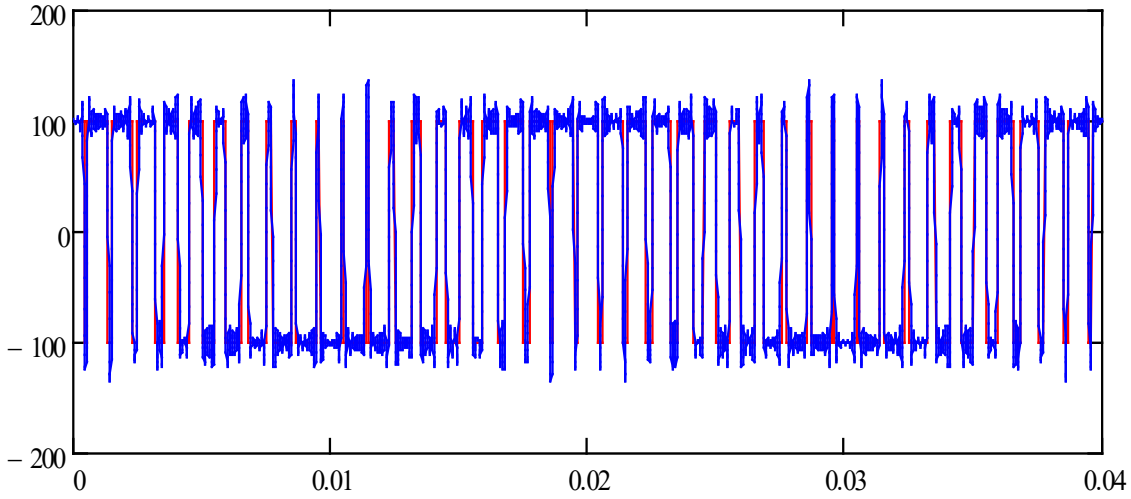


Figure 3-51 Harmonic content for two level inverter with triangle PWM

The spectrum for this type of modulation creates the highest harmonics for frequencies related with the carrier frequency and its harmonics. The side bands for the carrier frequency have also significant amplitude (Figure 3-52).

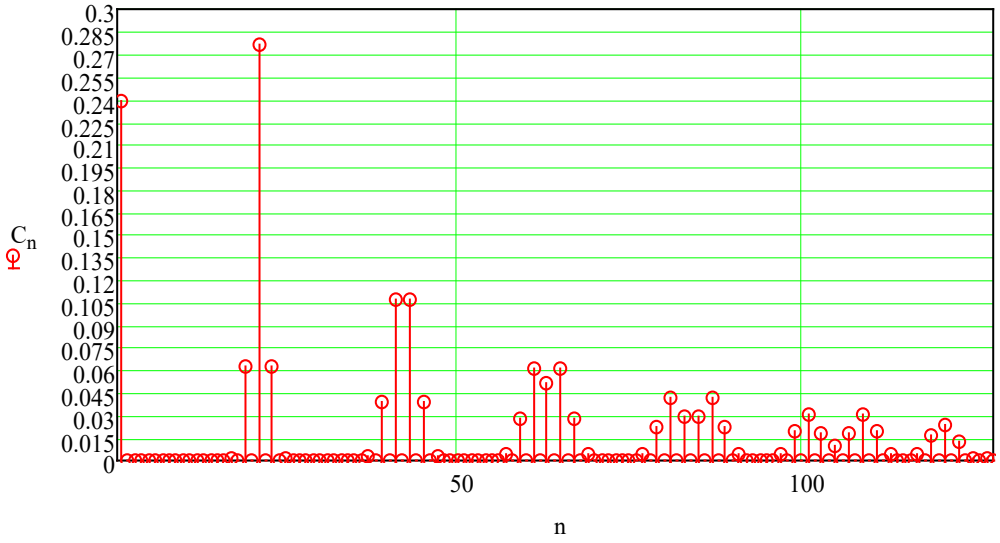
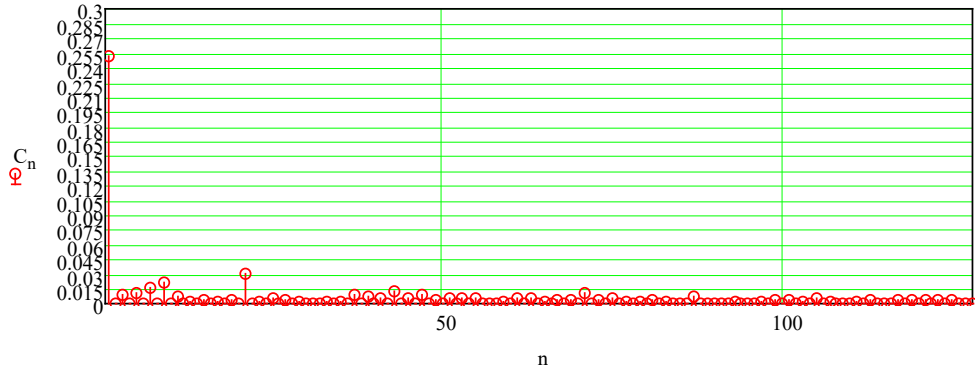


Figure 3-52 Harmonics amplitude in phase voltage for two level PWM modulation

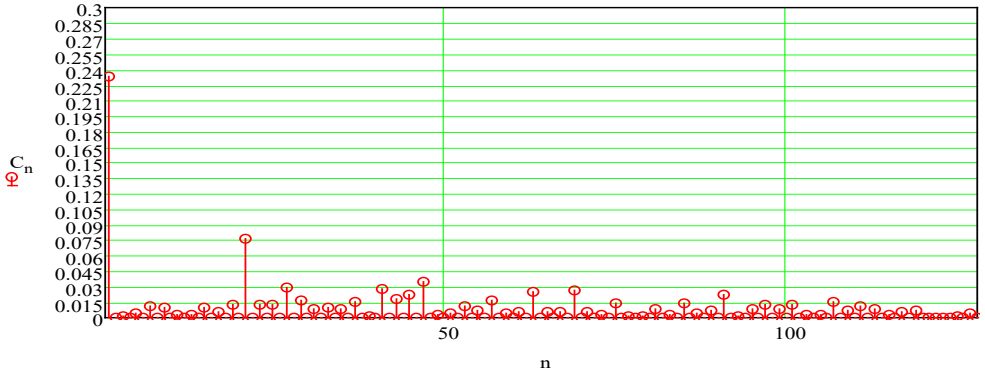
To summarize the results, the harmonic spectrums for all three cases were compared and presented with the same scaling. Also THD factors were calculated for presented three cases Table 3-2. The modulation where smaller voltage source (UC) is switched in PWM and remaining voltage is provided at fundamental frequency from main source has the smallest total harmonics content. The results are almost six times better in comparison to two level modulation with three-phase bridge, this can be explained that the MODE II modulation has a six level output with smaller voltage step (+80V, +50V, +20V, -20V, -50V, -80V) when in MODE I voltage toggle between +50V and -50V. For mixed operations, since the voltage step for PWM is higher for half of the period than in MODE II, the amplitude of unwanted harmonics increase. Nevertheless, the increase in harmonics for a mixed-modulation scheme (modes II and IV) is only double in comparison to MODE II and has similar pattern. It can be also expected that THD will become higher when percentage of period in MODE IV will increase. In comparison with conventional two-level modulations mixed modulation introduce three times lower harmonics as presented in Figure 3-53. From presented results we can conclude that proposed method to switch between two modulation schemes will increase THD of output voltage and this increase is proportional to voltage ratio between sources and percentage of duty cycle that modulation with higher voltage in PWM use. Still mixed modulation method provides much better results that modulation with two level inverter. Since the MODE I modulation is a standard two level modulation that is popular in literature and its performance is well know we can assume that achieved results for MODE II and mixed modulation provide significant improvement in unwanted harmonics elimination.

Table 3-2 Total harmonic distortion in phase voltage for six level modulation (MODE II), mixed modulation (MODE II and MODE IV) and two level modulation (MODE I)

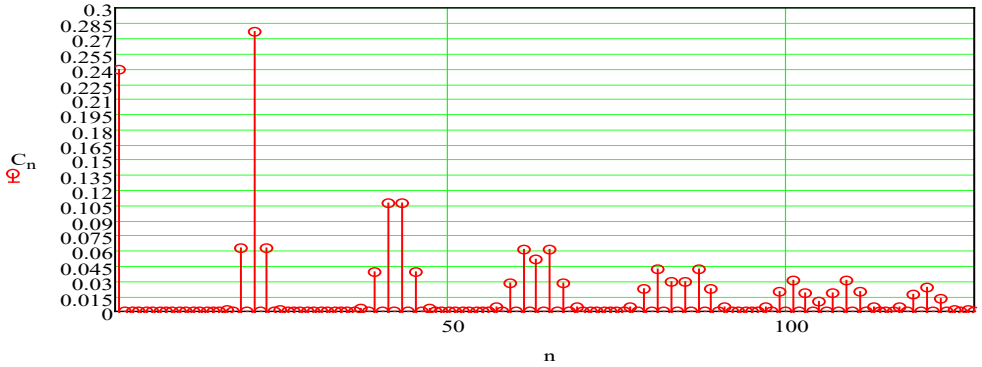
Modulation mode	MODE II	MODE II and IV	MODE I
THD	0.217	0.528	1.524



(a) Six level modulation in MODE II



(b) Mixed modulation between MODE II and MODEIV



(c) Two-level modulation - MODE I

Figure 3-53 Comparison of harmonics amplitude for different modulation strategies

3.6 Calculations of battery and ultracapacitors reference power

3.6.1 Ultracapacitors reference voltage in relation to kinetic energy

In the proposed control method similarly to solutions in literature (Camara et al., 2008), (Carter, Cruden and Hall, 2012) the main constraint is to avoid battery operations over its nominal power limitations. At the same time the UC's state of charge should be kept at a level that will allow the maximum recuperation of kinetic energy. Additionally, to minimise current ripples and switching losses it is proposed to keep UC's at a state of charge in reference to the speed at which the motor will remain for the longest period of time (cruise speed) to fully utilize multilevel structure.

The first battery constraint is related to the maximum current that the battery can source (I_{bat_max}) and the minimum current that the battery can sink to during charging (I_{bat_min}). For this reason the maximum and minimum battery currents should be controlled according to the battery's state of charge and its life. In presented work it is considered that above maximum and minimum battery currents (I_{bat_max} , I_{bat_min}) are average DC current during one sixth of the period. Since the battery voltage due to the state of charge can have only small voltage variations and since at battery output low pass filter is installed, in later discussion it is assumed that battery voltage is constant. Based on these assumptions and omitting source resistance it is possible to calculate maximum and minimum power that the battery can deliver and the power that should not be exceeded under normal drive operations (3-60),(3-61).

$$P_{bat\_max} = V_{bat} \cdot I_{bat\_max} \tag{3-60}$$

$$P_{bat\_min} = V_{bat} \cdot I_{bat\_min} \tag{3-61}$$

The second power reference constraint is related with the UC's aim of providing additional power during acceleration as well as capturing most of the kinetic energy without losing opportunities to recuperate so the battery can operate within its limits. Based on existing publications (Rosario, 2007), it was chosen to use directly kinetic energy recuperation as a reference for the UC voltage. It is

proposed that the high power source (UC) should be able to capture all available kinetic energy during breaking and provide energy during high power demands such as acceleration. The vehicle's kinetic energy available for regeneration can be described as the total vehicle kinetic energy (3-62).

$$E_{\mathrm{Re}\,g,Max} = \frac{1}{2}Mv^2 \tag{3-62}$$

Where

M-vehicle mass, v - velocity

Since the test platform include only rotating bodies the kinetic energy can be replaced by the relation between inertia and angular velocity

$$E_{Reg,Max} = \frac{1}{2}J\omega^2 \tag{3-63}$$

Where

J-body moment of inertia, ω- angular velocity

On the other hand, the amount of energy that can be regenerated into UCs is related to the difference between the voltage square of the maximum energy that the UC can store and the energy that is currently stored and is represented by the following equations:

$$\Delta E_{UC} = \frac{1}{2}C_{UC}\left(V_{UC\_max}{}^2 - V_{UC}{}^2\right) \tag{3-64}$$

Where

C_{UC}- ultracapacitor capacitance, V_{UC_max} -maximum capacitor voltage,

V_{uc}- UC voltage

Since in the proposed system there are three identical H-Bridges with UCs, the total capacitance is the sum of the capacitances for all three H-Bridges:

$$C_{UC} = C_{UC\_A} + C_{UC\_B} + C_{UC\_C} \tag{3-65}$$

Converting equations (3-63) and (3-64) we obtain relation between speed and reference capacitor voltage to regenerate all kinetic energy through UC's ((3-66) and (3-67)), those equations are illustrated in Figure 3-54:

$$V_{UC\_ref}\ (v) \leq \sqrt{V_{UC\_max}^{\ 2} - \frac{M}{C_{UC}} v^2} \tag{3-66}$$

M-vehicle mass, v-speed , C_{UC}-capacitance

Or

$$V_{UC\_ref}\ (\omega) \leq \sqrt{V_{UC\_max}^{\ 2} - \frac{J}{C_{UC}} \omega^2} \tag{3-67}$$

J-body moment of inertia ω- angular velocity,, C_{UC}- ultracapacitor capacitance

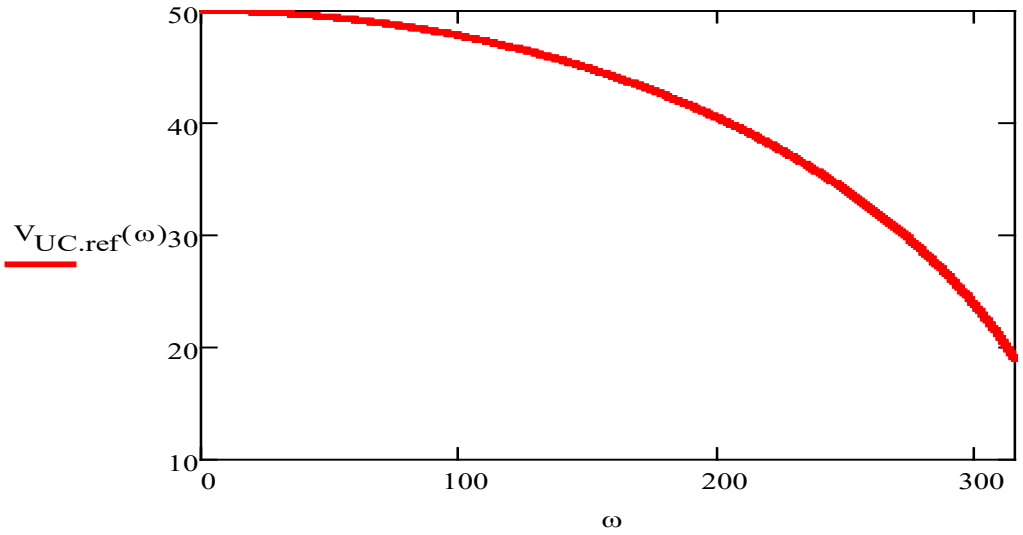


Figure 3-54 Relation between motor angular speed and ultracapacitor reference voltage

Figure 3-54 presents an example relation between the motor angular speed and the UC reference voltage for maximum capacitor voltage V_{UC_max} =50V, Moment of inertia *J*=1.2kg/m2 and UC capacitance C_{UC}=58F.

Based on the capacitor derivative equation $i(t) = C\frac{dv(t)}{dt}$ it is possible to find the current required by the UC to achieve reference voltage in the period of time. The difference between the reference voltage $V_{UC\_ref}\ (v)$ and the UC's actual average value V_{UC_avg} become $dv(t)$, C is capacitance of single H-bridge ($C = C_{UC\_A} = C_{UC\_B} = C_{UC\_C}$) and I_{UC_avg} is average reference UC current. Substituting previous the equations we receive:

$$I_{UC_{avg}} = C\frac{V_{UC\_avg} - V_{UC\_ref}\ (v)}{T} \tag{3-68}$$

$$= C\frac{V_{UC\_avg} - \sqrt{V_{UC\_max}^{\ 2} - \frac{M}{3\cdot C}v^2}}{T}$$

Where T is a sampling time of voltage and speed measurement and can be variable up to one sixth of the fundamental frequency period to prevent control oscillations.

Having the UC's average current the total reference power from or to the H-Bridges can be calculated by multiplying UC average current I_{UC_avg} by the number of sources and their voltage.

$$P_{UC\_ref} = 3\cdot V_{UC\_avg}\ \cdot I_{UC\_avg} \tag{3-69}$$

$$= 3\cdot C\cdot V_{UC\_avg}\cdot\frac{V_{UC\_avg} - \sqrt{V_{UC\_max}^{\ 2} - \frac{M}{3\cdot C}v^2}}{T}$$

It is worth pointing out that the UC's average reference current can have only lower amplitude than motor current I. The relation between these currents can be found from the previous power analysis where the power in six-step mode

with all three H-Bridges active and unity power factor can reach maximum value:

$$P_{UC\_max} = \frac{3}{\pi} \cdot 2 \cdot V_{UC\_avg} \cdot I = \left| -P_{UC\_min} \right| \tag{3-70}$$

Where I is the size of the motor current vector

Comparing this value to the power reference equation we can find:

$$P_{UC\_ref} = P_{UC\_max} = 3 \cdot V_{UC\_avg} \cdot I_{UC\_avg} = \frac{3}{\pi} \cdot 2 \cdot V_{UC\_avg} \cdot I \tag{3-71}$$

This means that the UC's average current has to be proportionally smaller than the motor current:

$$\left| I_{UC\_avg} \right| \leq \frac{2}{\pi} \cdot I \tag{3-72}$$

By having maximum available output voltage from the inverter, maximum active power from the battery, the reference UC active power or its maximum active power, we can find the relation between the available active and apparent power which is presented in Figure 3-55 and Figure 3-56, where the envelope of available voltage vectors in coordinate plane synchronous to motor current is presented for three different motor current values.

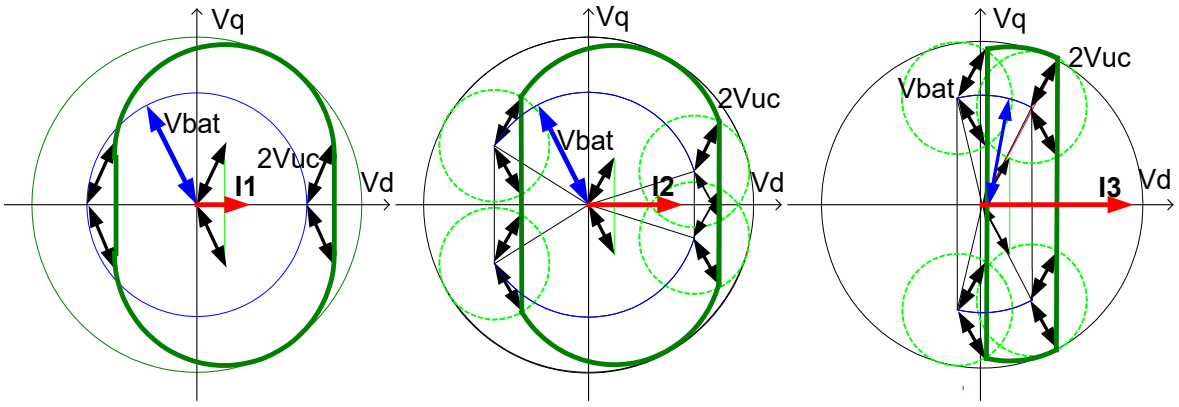


Figure 3-55 The voltage vector limits (dark green) for three different output currents (I1<I2<I3) delivered by battery and for fixed output power delivered by ultracapacitors

When the reference voltage for UCs is used the constant current has to be either sink or source by them. This means that the average value of the voltage vector from the H-Bridges needs a fixed amplitude in “d” axis (in line with the motor current vector) but the remaining amplitude of the UCs can still be used to output passive power (orthogonally to current vector) (Figure 3-55). At the same time the battery’s minimum and maximum current creates limited envelope of available output voltage in the “d” axis (blue line). We can find in the presented graph that the battery voltage limit (blue circle) becomes similar to elliptical since the battery current limit does not allow to output full voltage in “d” axis. At the same time the UCs allow to increase voltage in “d” axis by value that is related to UC reference voltage (green dotted circles).

If the UC’s set voltage is overridden in the case of rapid power demand, its full voltage parallel to current vector can be utilized. Figure 3-56 presents the available output voltage where the only imposed limitation is related to the battery’s minimum and maximum current. We can find in presented figure that the output voltage is defined by battery voltage limit (blue envelope) extended by circle related with UC amplitude. In this case the capability to deliver active power is increased in comparison to case where UC reference voltage is used. In regards to reactive power, the limits for both cases remain same and are related to maximum available voltage from inverter.

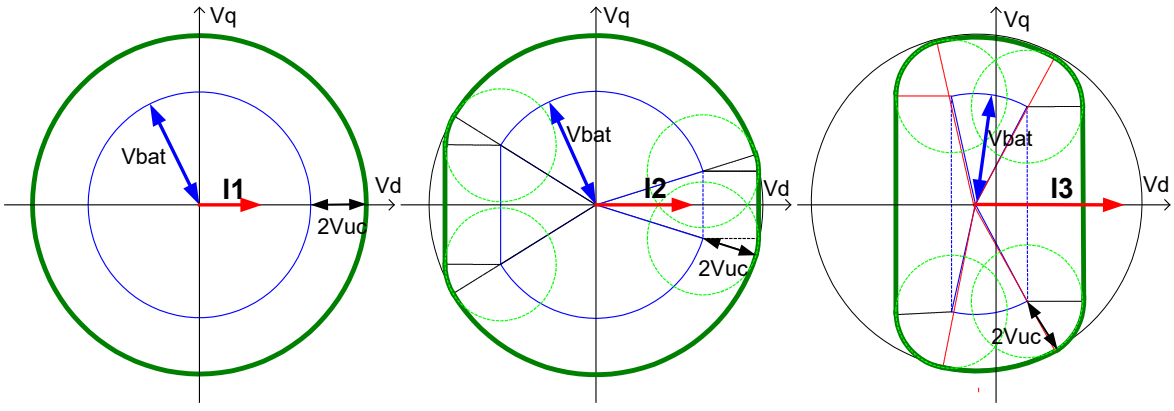


Figure 3-56 The voltage vector limits (dark green) for three different output currents (I1<I2<I3) delivered by battery and ultracapacitors without power setting

3.6.2 Ultracapacitor reference to minimize current ripples

The hybrid cascade multilevel inverter with UCs that have variable voltage can either use a battery or UCs as a source for Space Vector Modulation (SVM). Since the current ripples from SVM are directly related to the coordinates difference of used vectors it is desirable to use switching combinations that will provide the maximum number of levels at which output is modulated. This is the reason why H-Bridges with lower amplitude of DC sources are preferred for SVM. To maintain motor operations at constant speed for longer time it is necessary that the reference H-Bridge active power will be equal to zero so the total power is delivered by the battery and UC stay at constant value. For given output voltage reference it is proposed to find the UC reference voltage that will maximize the number of levels at which the voltage is modulated.

In Figure 3-57 the voltage vectors limiting hexagon from H-Bridges (green and blue arrows) together with three-phase bridge vectors (red arrows) in sector one present range of available reference voltage (purple arches) in MOODE II. From the inverter voltage vector analysis we can find that to allow SVM with H-Bridge inverter together with six-step switching for 3-phase bridge and to provide the maximum number of voltage levels we have to find an adequate UC voltage set point. Base on trigonometry equations for hexagon limiting boundaries as presented in Figure 3-57 it is possible to distinguish the following cases of require UC voltage depending on the amplitude of the reference voltage vector.

- If the reference output voltage vector is smaller than the battery voltage divided by the square root of three $V_{ref} < V_{bat}/\sqrt{3}$ then the relation between the inverter sources and voltage reference V_{ref} has to be smaller than half:

$$(V_{bat} - 2V_{UC})/(\sqrt{3} \cdot V_{ref}) < 1/2 \tag{3-73}$$

- For a reference output voltage greater than $V_{ref} > V_{bat}/\sqrt{3}$ the relationship between the UC voltage and the reference voltage has to be greater than half (3-74):

$$2V_{UC}/(\sqrt{3} \cdot V_{ref}) > 1/2 \tag{3-74}$$

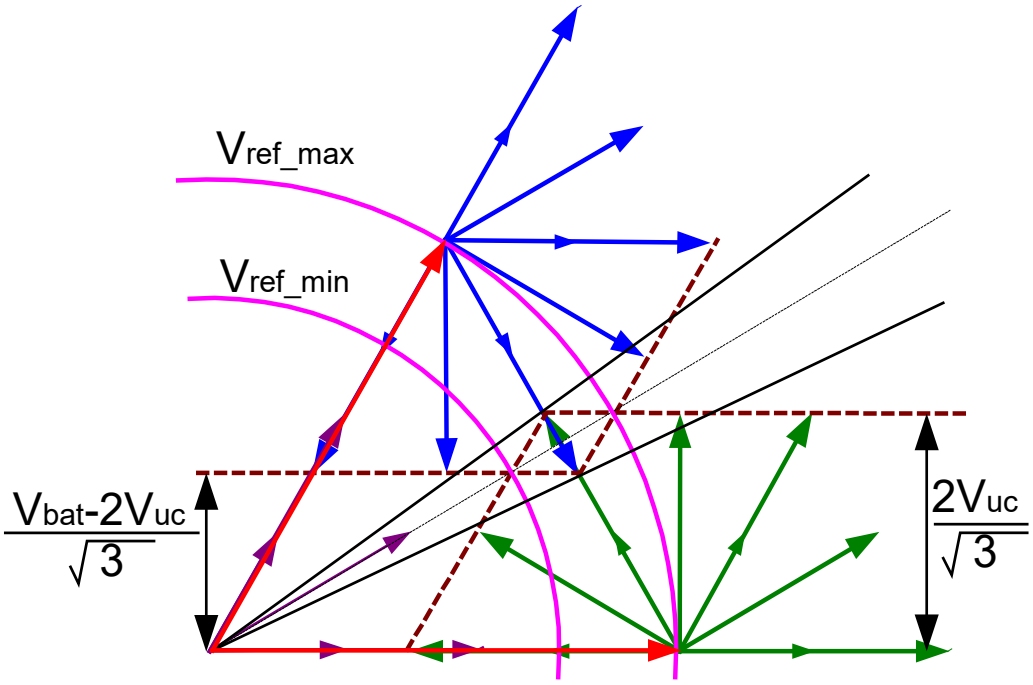


Figure 3-57 Output voltage vectors limits (V_{ref_min}, V_{ref_max}) for a three-phase inverter operations at fundamental frequency with H- Bridge in SVM (MODE II)

As presented in the previous section 3.5.3 it will be possible to have zero active average output power from UCs if the total inverter output power is equal to the active power from the three-phase inverter (3-75).

$$P = P_{bat} = \frac{3}{2} V_{ref} \cdot I \cdot \cos(\varphi) = \frac{3}{\pi} V_{bat} \cdot I \cdot \cos(\varphi) \tag{3-75}$$

This means that by finding specific inverter output voltage reference it is possible to find set point to have zero active power from H-Bridges. If power factor (*cos(φ)*) is equal one then above equation can be simplified (3-76):

$$V_{ref} = \frac{2}{\pi} V_{bat} \tag{3-76}$$

For this reference point we can also find UC voltage that will provide the maximum number of levels in output voltage, what is represented by equation:

$$V_{UC\_avg} = \frac{\sqrt{3}}{2} \cdot \frac{V_{bat}}{\pi} \tag{3-77}$$

This output voltage reference set point is also the maximum voltage that can be generated without outputting active power from the H-Bridge converter for a power factor equal to one. From the equations above (3-76) we can also find that for this modulation strategy it is achievable to generate a maximum output voltage more than 10% higher than the voltage that can be generated by standard SVM using only a battery as a source (3-78):

$$\frac{\frac{2}{\pi}V_{bat}}{\frac{V_{bat}}{\sqrt{3}}} = 1.103 \tag{3-78}$$

Additionally it should be mentioned that the motor current has to be smaller than the battery's maximum current to allow operation in this mode (3-79).

$$I < \frac{\frac{\pi}{3}I_{bat\_max}}{\cos(\varphi)} \tag{3-79}$$

By controlling the phase shift of fundamental frequency it is available to reduce battery output power what allows to use lower reference voltages. Also if the phase shift between the motor current and the output voltage is greater than zero, the passive power from the six-step switching source can be compensated so higher (or lower) output voltage can be generated. The relation between phase shift and power factor is presented in form (3-80):

$$P = P_{bat} = \frac{3}{2}V_{ref} \cdot I \cdot \cos(\varphi) = \frac{3}{\pi}V_{bat} \cdot I \cdot \cos(\varphi + \chi) \tag{3-80}$$

In above equation χ is a control phase shift, for the case where UC voltage is equal half of battery voltage then the phase shift value can be controlled from $-\pi/6$ to $+\pi/6$. This equation allows finding the relation between the phase shift control and the inverter output voltage for continuous operations. Figure 3-58 shows the available output reference voltage for three different power factors (phase shift between reference voltage and current equal to 0, $\pi/12$ and $\pi/6$) and for variable phase shift control χ. We can note that if the phase difference between the output voltage and the current is high, there is a greater possibility

to control the output reference voltage by changing the phase shift and to set zero active power from the UCs (black dotted line vary from 0.74 to 0.38). The relation between output voltage, phase sift control angle and power factor is described by equation (3-81)

$$V_{ref} = \frac{2}{\pi} V_{bat} \cdot \frac{\cos(\varphi + \chi)}{\cos(\varphi)} \tag{3-81}$$

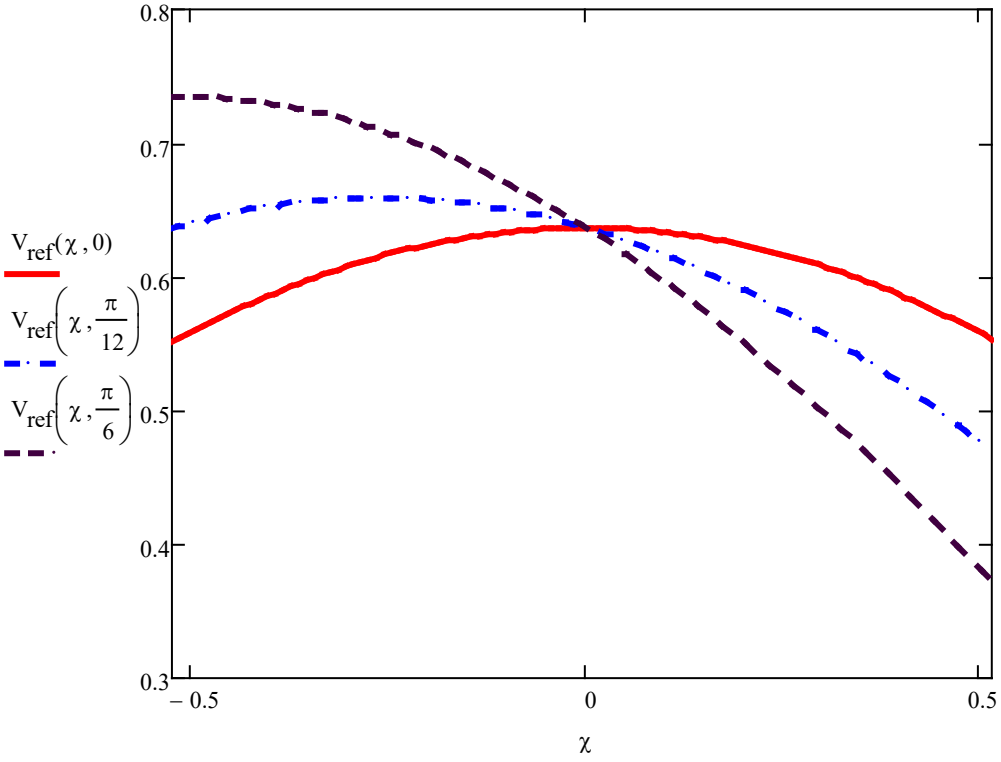


Figure 3-58 Output reference voltages in relation with power factor and phase shift angle, reference voltage presented as ratio to battery voltage

Presented figure shows that by setting phase shift angle opposite to power factor the output voltage can be increased and in opposite case the voltage become reduced. For all cases when the phase shift is introduced it will become necessary to increase the amplitude of the UC adequately to the phase shift angle χ. Figure 3-59 illustrates how, for a set reference inverter output voltage and a set current phase shift, the minimum required UC voltage can be found. The figure presents hexagon boundaries for H-Bridge vectors (blue and green arrows) in combination with three-phase bridge vectors (red arrows). The increase of the UC amplitude also increases hexagon boundaries allowing them

to overlap what gives opportunity to increase phase shift control. The amount of overlapping define available phase shift what indirect define available output voltage.

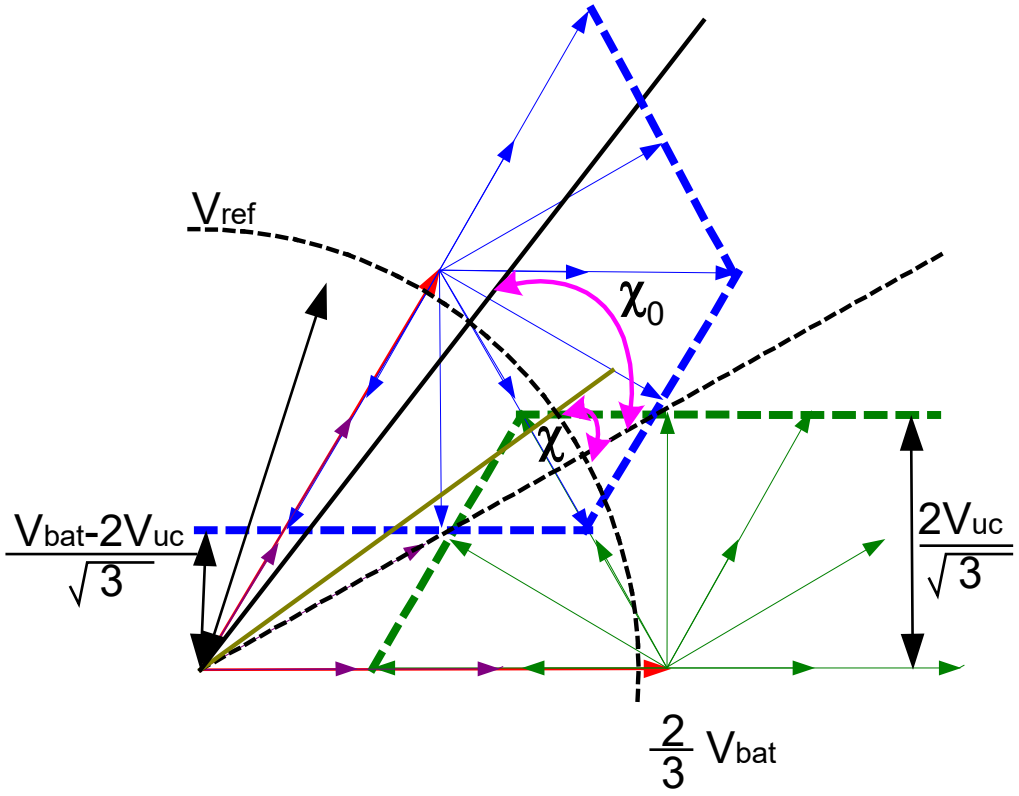


Figure 3-59 Relation between reference inverter output voltage and vectors from H-Bridges

In the graph above for inverter output voltage higher than $V_{ref}>1/\sqrt{3}V_{bat}$, the χ_0 angle is defined as available phase shift angle for given reference voltage V_{ref} limited by horizontal H-Bridge hexagon (3-82).

$$\chi_0 = \operatorname{acos}\left(\frac{V_{bat}}{\sqrt{3}V_{ref}}\right) \quad \text{for} \quad |\chi| < \chi_0 \tag{3-82}$$

In above equation the reference UC voltage is equal to (3-83):

$$V_{UC\_ref} = \frac{\sqrt{3}}{2}V_{ref} \cdot \sin(|\chi| + \frac{\pi}{6}) \tag{3-83}$$

Since for the $|\chi|>\chi_0$ hexagon side is changed then the reference voltage has to be calculated from following equation (3-84):

$$V_{UC\_ref} = -\frac{\sqrt{3}}{2} V_{ref} \cdot \sin\left(-|\chi| + \frac{\pi}{6}\right) + \frac{V_{bat}}{2} \tag{3-84}$$

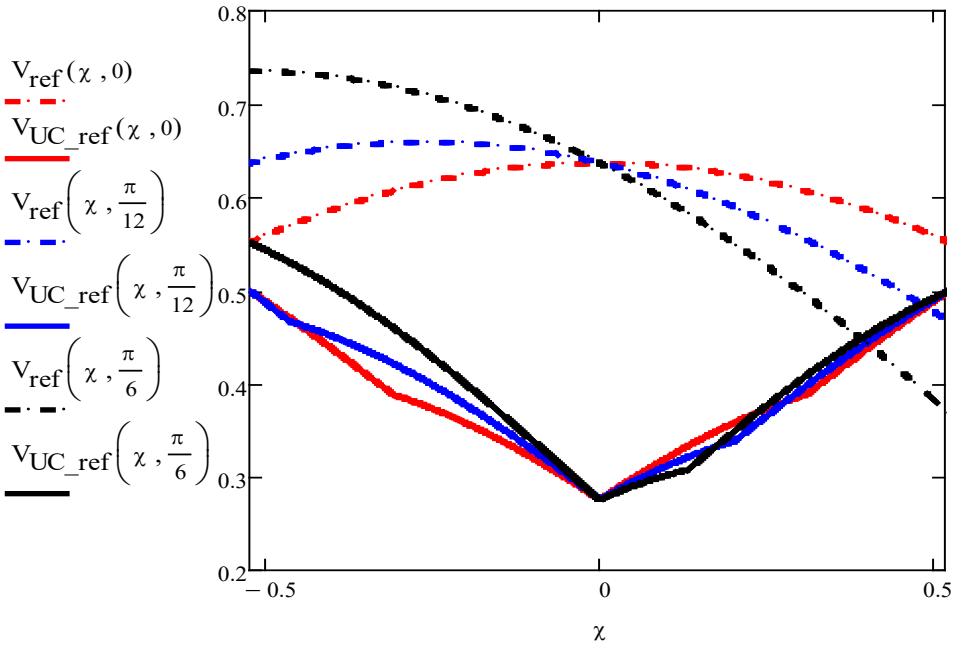


Figure 3-60 Maximum available output voltages in MODE II modulation (dotted lines) together with required reference UC voltage (solid lines) for different phase shift control angle at three different phase delays between current and voltage (0, π/12 and π/6)

In presented Figure 3-60 it is visible that UC voltage should not be lower than 25% of battery voltage and for maximum and minimum phase shift the UC voltage has to be equal half of the battery voltage. The χ_0 angle representing hexagon limiting side change has small influence on UC reference voltage curve especially for power factors close to one. The conservative approach would be to use always higher value out of those two equations.

From the voltage reference curve it can be found that phase shift control is limited by the minimum reference output voltage that can be produced. For presented case the amplitude of output voltage has to be higher than 38% of battery voltage for $\pi/6$ phase angle (Figure 3-60). To overcome this limitation it is proposed to use mixed modulation and switch between a six-step operation of the three-phase inverter and SVM with only H-Bridges. In this case the total

active power through one sixth of period will be delivered only by the battery so the following equation has to be met:

$$P = \frac{3}{2} \cdot I \cdot V_{ref} \cdot \cos(\varphi) = P_{bat} = \frac{3}{\pi} \cdot I \cdot V_{bat} \cdot \cos(\varphi + \chi) \cdot 2\sin(\alpha) \tag{3-85}$$

From above equation the relations between the control angle α and the output voltage from the inverter are formulated (3-86), (3-87).

$$\frac{V_{ref} \cdot \cos(\varphi) \cdot \pi}{4 \cdot V_{bat} \cdot \cos(\varphi + \chi)} = \sin(\alpha) \tag{3-86}$$

$$or \qquad \frac{4 \cdot V_{bat} \cdot cos(\varphi + \chi) \cdot sin(\alpha)}{cos(\varphi) \cdot \pi} = V_{ref} \tag{3-87}$$

For zero phase shift ($\chi=0$) the equation (3-86) can be simplified to the following form (3-88):

$$\sin(\alpha) = \frac{V_{ref} \cdot \pi}{4 \cdot V_{bat}} \tag{3-88}$$

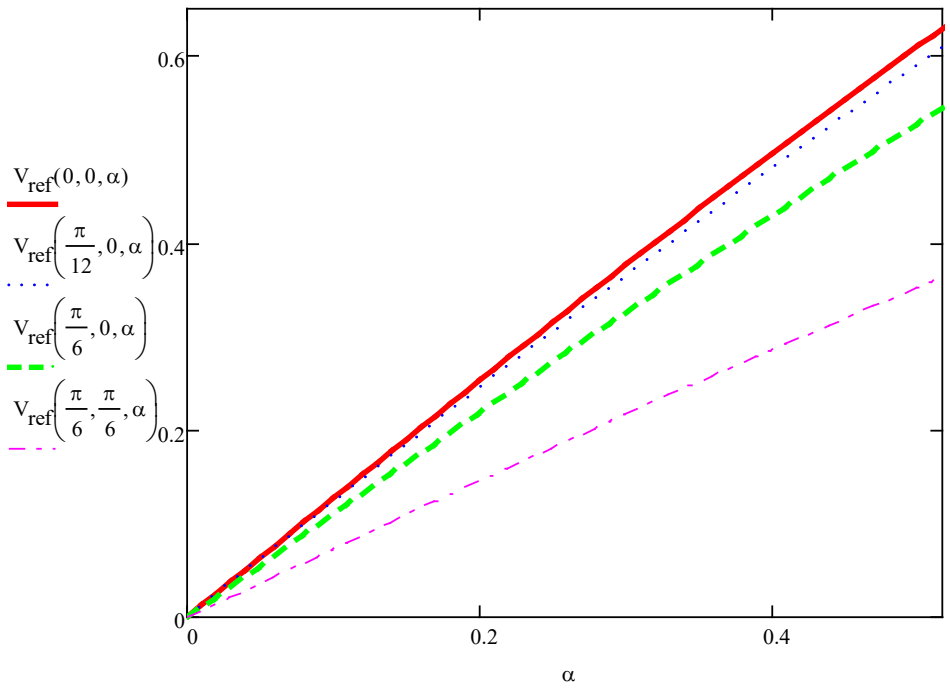


Figure 3-61 The relation between control angle α and output voltage reference in relation to phase shift angle χ and current phase angle φ

The relation between the control angle and the output voltage for various power factors and phase shifts control angles for six step switching is presented in Figure 3-61. For this operation with H-Bridge the UC voltage has to be sufficient to modulate reference voltage vector so the following requirements have to be met (3-89), (3-90):

$$V_{ref} < \frac{2V_{UC}}{\sqrt{3}} \tag{3-89}$$

$$or \qquad V_{UC\_ref} > \frac{\sqrt{3}V_{ref}}{2} \tag{3-90}$$

Also for given switch angle α, the modulation in MODE II require sufficient UC voltage to produce set voltage. Base on hexagon limits this relation can be described by equation (3-91).

$$V_{UC\_ref} = -\frac{\sqrt{3}}{2}V_{ref} \cdot \sin\left(\frac{\pi}{3} - \alpha\right) + \frac{V_{bat}}{2} \tag{3-91}$$

This relation between control angle α, the inverter output voltage and the minimum UC voltage for variable phase shift control and variable phase angle is presented in Figure 3 62.

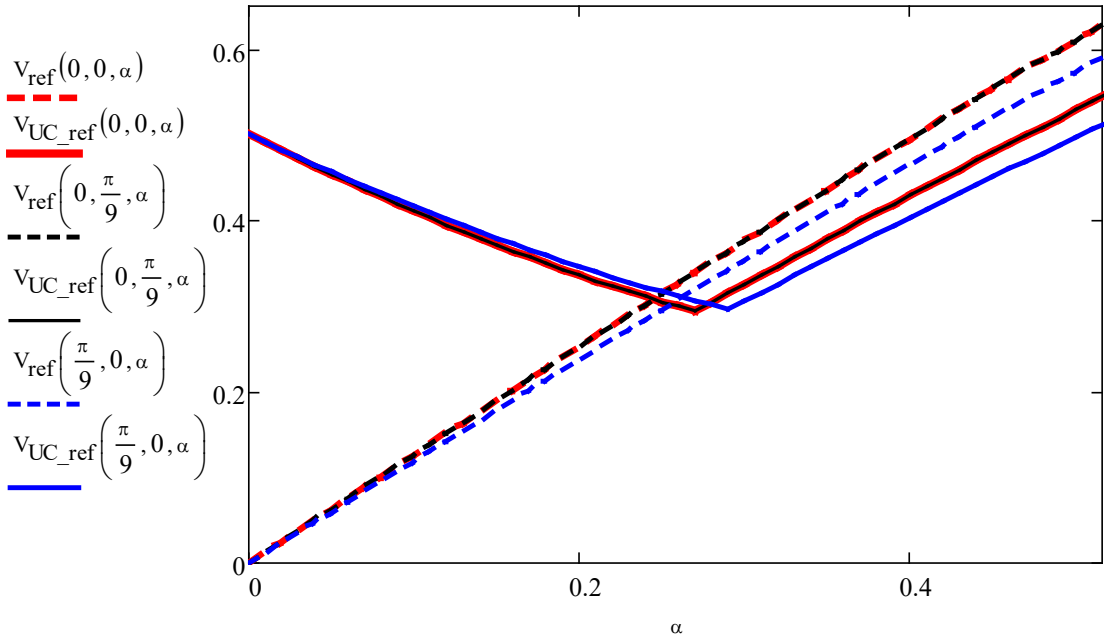


Figure 3-62 Required UC voltage for mixed modulation and corresponding output voltage for different phase angle and phase shift control, solid line represent UC reference voltage and dotted line output voltage

The equations above ((3-90), (3-91)) are valid when the inverter output voltage is lower than $V_{ref} < 1/\sqrt{3}\ V_{bat}$.

In conclusion, if the required output power from the inverter is lower than the maximum battery output power $P < V_{bat} \cdot I_{bat\_max}$ and the reference voltage is smaller than relation (3-92):

$$V_{ref\_max} < \frac{2}{\pi} V_{bat} \cdot \frac{\cos(\varphi \mp \chi)}{\cos(\varphi)} \tag{3-92}$$

Then it is possible to find a control strategy for multilevel operations with an H-Bridges switching in SVM that will not sink or source active power from UCs. For this strategy the UC voltage can be charged or discharged to a defined reference voltage to achieve maximum number of levels in output voltage. It is noticeable that for higher amplitude of reference voltage the required UC voltage for lowest current ripples is contradictory to the UC voltage that depends on motor speed presented in paragraph 3.6.1. This means that in cases where UC voltage is set high, ability to recuperate the kinetic energy become limited.

3.6.3 Algorithm for power sharing

Having the H-Bridge reference power and battery power limits, the aim of the algorithm is to compare these reference values with the total power requested by the load. Additionally, if the motor is operated for longer periods at constant speed the UC voltage can be adjusted for operations with the maximum number of levels. Based on these requirements it is possible to formulate power sharing control strategy.

1. The algorithm requires that the motor torque is limited by its control preventing reference output power from exceeding the total available power, which can be delivered by battery and UC. This is achieved by controlling that the reference output voltage vector is smaller than the maximum voltage that can be produced by the inverter (3-95). At the same time the reference output power (including losses) have to be smaller than the maximum power that can

be delivered by the battery together with the UCs at a given motor current (3-93),(3-94). In the case of the power being exceeded the motor torque is reduced.

$$P < P_{bat\_max} + V_{UC\_avg} \cdot I \cdot \frac{6}{\pi} \tag{3-93}$$

$$and \quad P > P_{bat\_min} - V_{UC\_avg} \cdot I \cdot \frac{6}{\pi} \tag{3-94}$$

$$V_{ref} < \frac{V_{bat} + 2V_{UC\_avg}}{\sqrt{3}} \tag{3-95}$$

The total active reference inverter output power is calculated based on a voltage reference from motor control and actual motor current (or predicted current) in polar or Cartesian coordinates (3-96) (3-97).

$$P = \frac{3}{2} \cdot V_{ref} \cdot I \cdot \cos(\varphi) \tag{3-96}$$

$$or \quad P = \frac{3}{2}\left(V_\alpha I_\alpha + V_\beta I_\beta\right) \tag{3-97}$$

2. From reference output power P the H-Bridge inverter reference power P_{uc_ref} related with motor speed is subtracted and this remaining power is compared with the maximum and minimum power available from the battery. If the remaining power is greater than the battery's maximum power or smaller than its minimum, the algorithm will use the battery's maximum or minimum current as a reference respectively (3-98),(3-99).

$$if \quad P - P_{UC\_ref} > P_{bat\_max} \tag{3-98}$$

$$then \quad P_{bat\_ref} = P_{bat\_max}, \quad P_{UC\_ref} = P - P_{bat\_max}$$

$$or \quad if \qquad P - P_{UC\_ref} \; < P_{bat\_min} \tag{3-99}$$

$$then \quad P_{bat\_ref} \; = P_{bat\_min}, \; P_{UC\_ref} = P - P_{bat\_min}$$

If the requested battery power does not exceed the battery current rating, the remaining power is used as a reference for the three-phase inverter (3-100).

$$P_{bat\_ref} \; = P - P_{UC\_ref} \tag{3-100}$$

It has to be mentioned that the reference active power is limited by motor drive control so it should always be possible to achieve the required power by available sources, battery and UC (3-93). This is achieved by controlling that the reference voltage vector is smaller than the maximum output voltage from the inverter (3-95) and at the same time that the motor output power, together with losses, is smaller than the maximum battery power together with the maximum UC reference power. In the case of power being exceeded the motor torque has to be reduced.

3. The speed-related voltage reference can be overridden by the UC voltage reference to provide maximum number of levels and to minimise harmonic distortions. This can be achieved when the motor speed is constant and the requested active power from the UCs is equal to zero $P_{UC\_ref}=0$ (or close to zero as the switching losses of the H-Bridges have to be compensated) and the motor remains at this speed for a longer time. The aim of this strategy is to provide sufficient voltage in the UCs to allow operation with the maximum number of voltage levels. For this reason the modulation strategies that use H-Bridges in SVM with small voltage source (MODE II and MODE III) have priority as presented in section 3.6.2. Depending on whether the output reference voltage is higher than $V_{ref} \geq V_{bat} / \sqrt{3}$ the phase shift adjustment can be used until the inverter is able to operate fully with the three-phase inverter section in six-step mode. For output reference voltage that is lower ($V_{ref} < V_{bat} / \sqrt{3}$), modulation with MODE II will cause UCs charging. For this reason the

modulation method has to be altered between six-step operations of three-phase bridge (MODE II) and modulation with H-Bridges only (MODE III) (3-101).

$$sin(\alpha) = \frac{V_{ref} \cdot \pi}{4 \cdot V_{bat}} \qquad for\ \chi=0 \tag{3-101}$$

Finally the UC voltage has to be kept at level where until relations are satisfied:

$$V_{UC\_ref} > \frac{\sqrt{3} V_{ref}}{2} \tag{3-102}$$

$$and \qquad V_{UC\_ref} = -\frac{\sqrt{3}}{2} V_{ref} \cdot sin\left(\frac{\pi}{3} - \alpha\right) + V_{bat}/2 \tag{3-103}$$

For those conditions it will become possible to switch to mixed modulation mode with best utilization of multilevel inverter structure.

The proposed power control scheme is presented as a block diagram in Figure 3-63 where particular blocks represent earlier mention equations. In first stage the reference power and reference voltage is limited to available values as well reference UC voltage in relation with kinetic energy is calculated from (3-67). In case the motor is operated at cruise speed the UC voltage can be set to minimize harmonics in output voltage. In next step the reference power for both inverter sections is selected to allow operation within battery current limits.

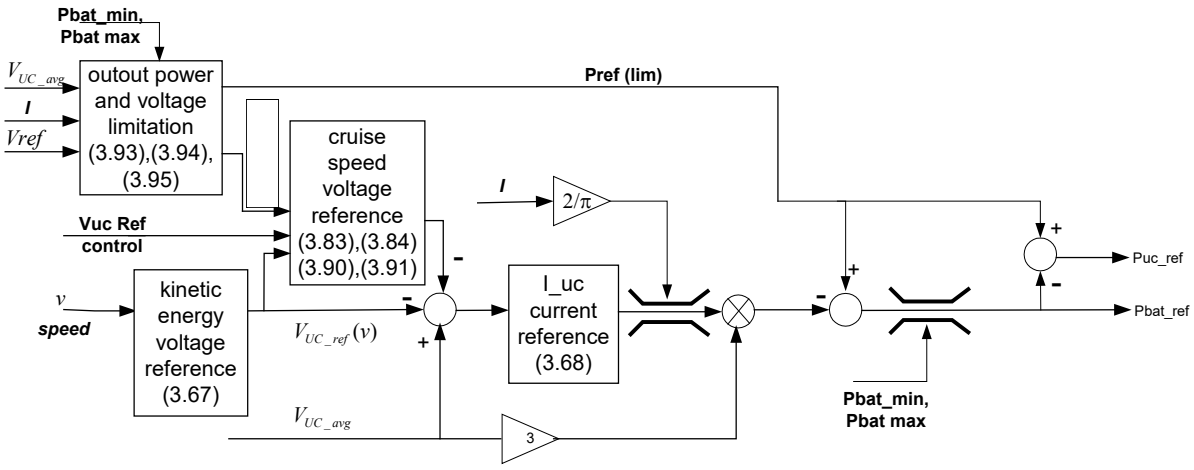


Figure 3-63 Block diagram of proposed power management logic

The power management has been defined, taking into account relation with the vehicle's kinetic energy, UC and battery voltage, battery current limitation and reference UC voltage for minimum voltage vector step. The control strategy is required to constantly monitor the reference voltage from motor control and actual motor current so the requested power would not exceed inverter available power. For presented system with multiple sources it is proposed to control the UCs in relation to the motor speed with an option to override this control at cruise speed to minimize current ripples an harmonics. The strategy allows the maximisation of recuperated energy and at the same time to find a reference voltage for the best quality of output waveform when remain at constant speed. The final stage of power share control is limited by maximum and minimum battery current. This control hierarchy ensures that in the case of rapid power demand the main source will operate within its limits so the transient power would be supported by UCs. It was also found that to achieve the best modulation strategy from voltage ripple perspective, the UC voltage has to be equal at last a quarter of the main source voltage. This requirement in some cases might be contradictory with the UC's state of charge for maximum kinetic energy recuperation.

3.7 Further modification to hybrid cascade inverter to increase its operating range

3.7.1 Overview

To increase the performance and operating range of presented hybrid cascade inverter the additional analysis of possible modifications was performed. The main aim of this analysis was to find possible further modifications to the multilevel inverter structure that could eliminate problems related to increased harmonics of output voltage in conditions when the auxiliary source becomes discharged. In literature it is possible to find number of publications presenting various modifications to the multilevel inverter structures (Perez et al., 2015). Especially in recent years the Modular Multilevel Converters (MMC) get a lot of attention and number of modification to the inverter cells were introduced (Debnath et al., 2015). Nevertheless for the case presented in this thesis the

multisource system has to be adapted to particular needs. The work focused on an analysis of multilevel inverter structures with multiple sources to improve mainly efficiency of the motor drive by minimization of THD by increasing variety of voltage vectors. At the same time the investigation aims to increase maximum amplitude of output voltage by compensation of passive power and elimination of unwanted harmonics. By better utilization of voltage sources and sharing power between them, the transient power capability could be increased. Eliminating dependency between UCs amplitude and voltage waveform quality could better protect main source against overloads during transient state and increase its ability of regenerative breaking.

3.7.2 Cascade inverter consisting three-phase inverter supplied by battery and three H-Bridges supplied by ultracapacitors

This multilevel inverter structure presented in Figure 3-64, analysed earlier, allows the delivery of a high number of output voltage levels with a low number of switches. In the structure analysed the three-phase bridge delivers active power from the battery at a set output current. Three H-Bridges work to minimise harmonic content and additionally compensate for the transient demands of power.

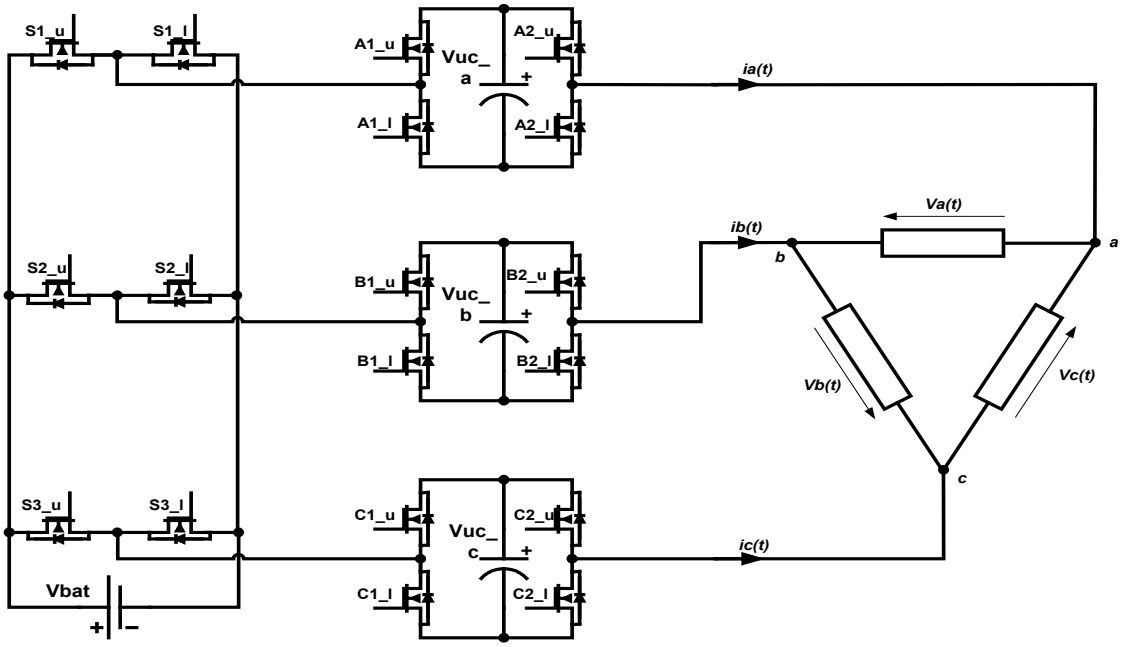


Figure 3-64 Structure of the cascade inverter with three-phase bridge and three H-Bridges , motor windings configuration in delta

The amount of passive power that can be compensated and the distortions of the delivered output voltage are closely related to the amplitude of the UC's voltages. If the UC has transferred most of its stored energy, the inverter's capability becomes very limited. As discussed earlier, if the voltage amplitude that supplies the UC is lower than 25% of the main source voltage, the nominal modulation with the three-phase bridge switched at fundamental frequency (MODEII) cannot be used. Figure 3-65 and Figure 3-66 show the coordinates of the output voltage vectors on α-β plane for two cases: where the main source has three times the amplitude of the UCs and where the battery amplitude is six times higher. In presented graph the vectors coordinates are presented for load in delta configuration what introduced phase shift by $\pi/6$ angle. To better illustrate vector coordinates, the switch combination with different vector from three-phase bridge are represented by a different colour (example: 100 combination in three-phase bridge mean S1=1, S2=0, S3=0, blue cross).

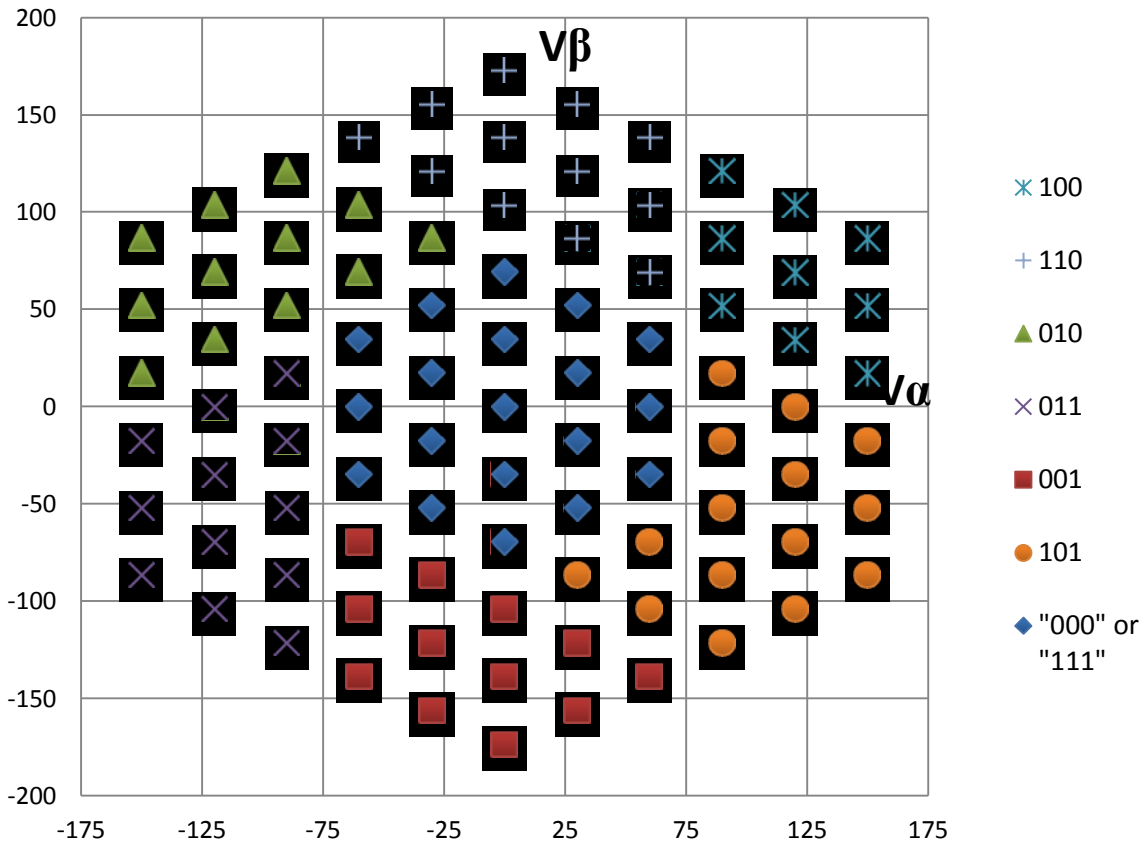


Figure 3-65 Available voltage vectors on α-β plane for V_{bat} = 90V and $V_{UC\_A} = V_{UC\_B} = V_{UC\_C}$=30V

These examples show that discharging UCs to one third of nominal voltage drastically increases the distances between the voltage vectors, which is later translated into higher distortions.

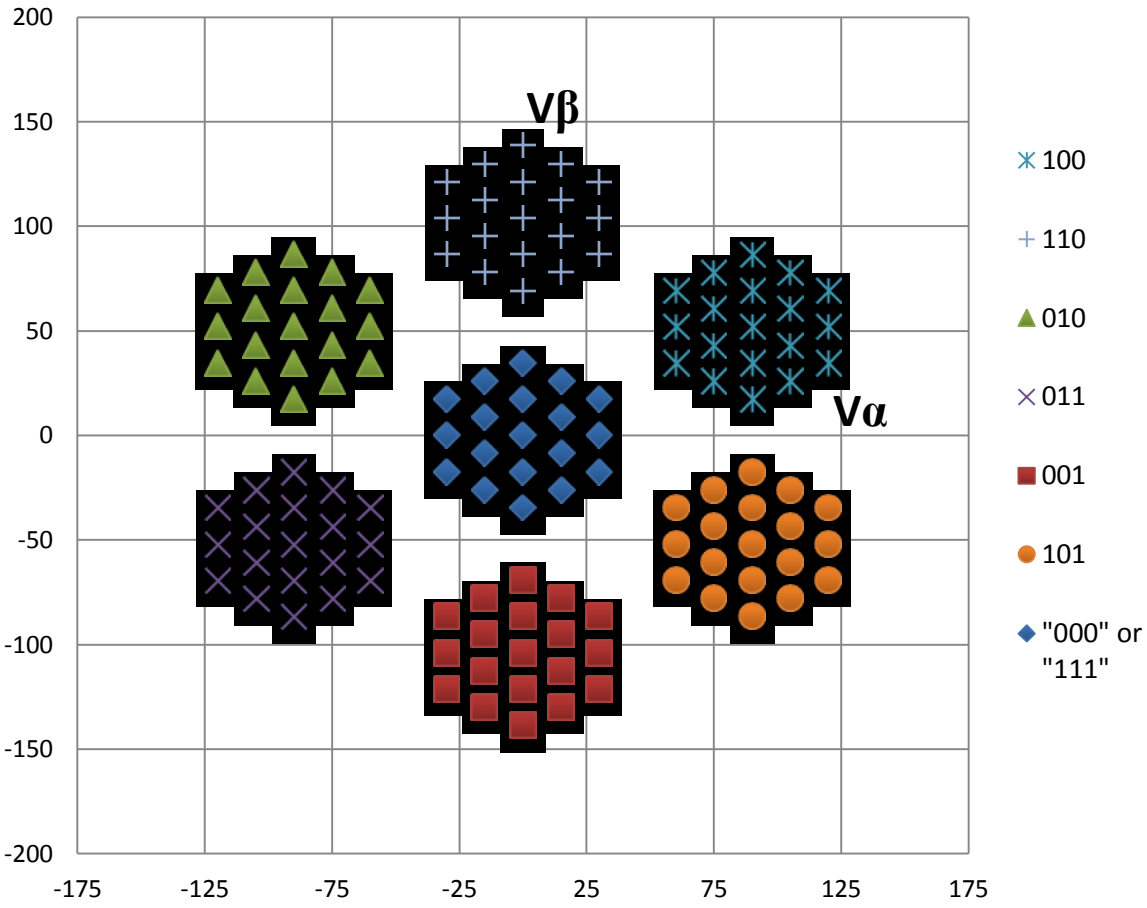


Figure 3-66 Available voltage vectors on α-β plane for V_{bat} = 90v and V_{UC_A} = V_{UC_B} = V_{UC_C} = 15V

3.7.3 Cascade inverter consisting of three-phase inverter supplied by battery and three H-Bridges with modification for two sources

To overcome the limitations of the inverter in Figure 3-64 it is proposed to add two switches and a standard capacitor for each H-Bridge, as presented in Figure 3-67. In this configuration the voltage of V1 (electrolytic capacitor) should be controlled to have amplitude according to reference from section 3.6.2. Since the A3_l switch can block V2 from charging V1 the amplitude of V1 can be greater than the voltage of V2 (ultracapacitor). In this H-Bridge configuration the

additional pair of switches (A3) prevents the source with higher amplitude (V1) from discharging into (V2) and allows the choice of which source is conducting current. Because of the inverter architecture the amplitude of the V1 source can't be lower than V2 source. The complete switching configuration is presented in Table 3-3. Thanks to this modification, the proposed inverter is not affected by the UC's state of charge and can always deliver the same amount of passive power and simultaneously keep the same THD. The main drawback is that it introduces additional components and there are added transistor that increases conduction losses. Nevertheless, the gains by implementing this strategy may be greater since it is possible for small electrolytic capacitors supplying H-Bridges to have voltage amplitude to allow inverter operate with the maximum number of levels in condition when the UCs are completely discharged. The important fact related with efficiency is that the amplitude of the voltage vectors in SVM is smaller than main source and often orthogonal to load current. This benefit that the SVM switching losses are expected to be low, what compensate increase of conduction losses due to additional switches.

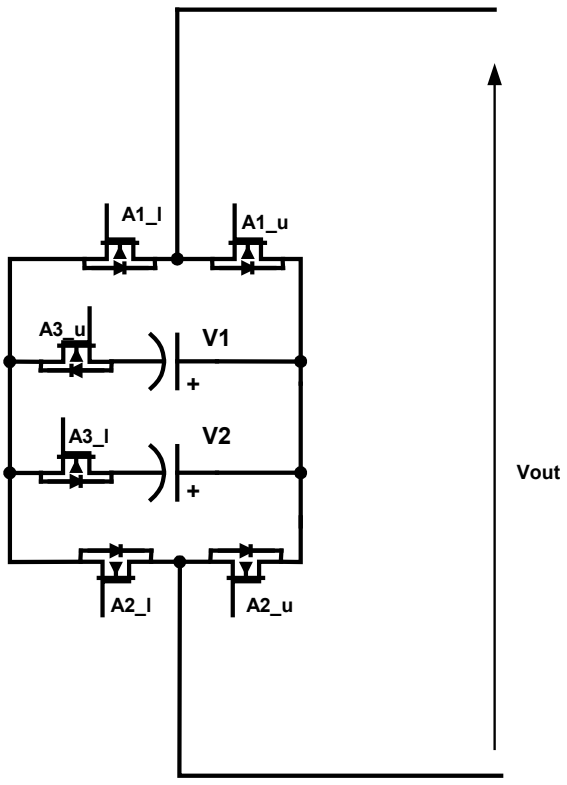


Figure 3-67 Structure of modified H Bridge with additional low energy source

Table 3-3 Switching table for modified H-Bridge with blocking switch A3

Combination number	Switch A1	Switch A2	Switch A3	Output voltage (V_{out})
0	0	0	0	0
1	0	0	1	0
2	0	1	0	-V2
3	0	1	1	-V1
4	1	0	0	V2
5	1	0	1	V1
6	1	1	0	0
7	1	1	1	0

Note: If the switch Ax_u is OFF and Ax_l is ON, the pair is represented as logic 0; if Ax_u is ON and Ax_l is OFF the pair is state 1.

The switching losses related with A3 switch are expected to be low as it is desired to only change its state when both MOSFET's (A1 and A2) are in the same state. This allows using lower grade component for A3 switch without concerns about power dissipation. In Figure 3-68 the complete configuration of the three-phase inverter with modification to the H-Bridges is presented

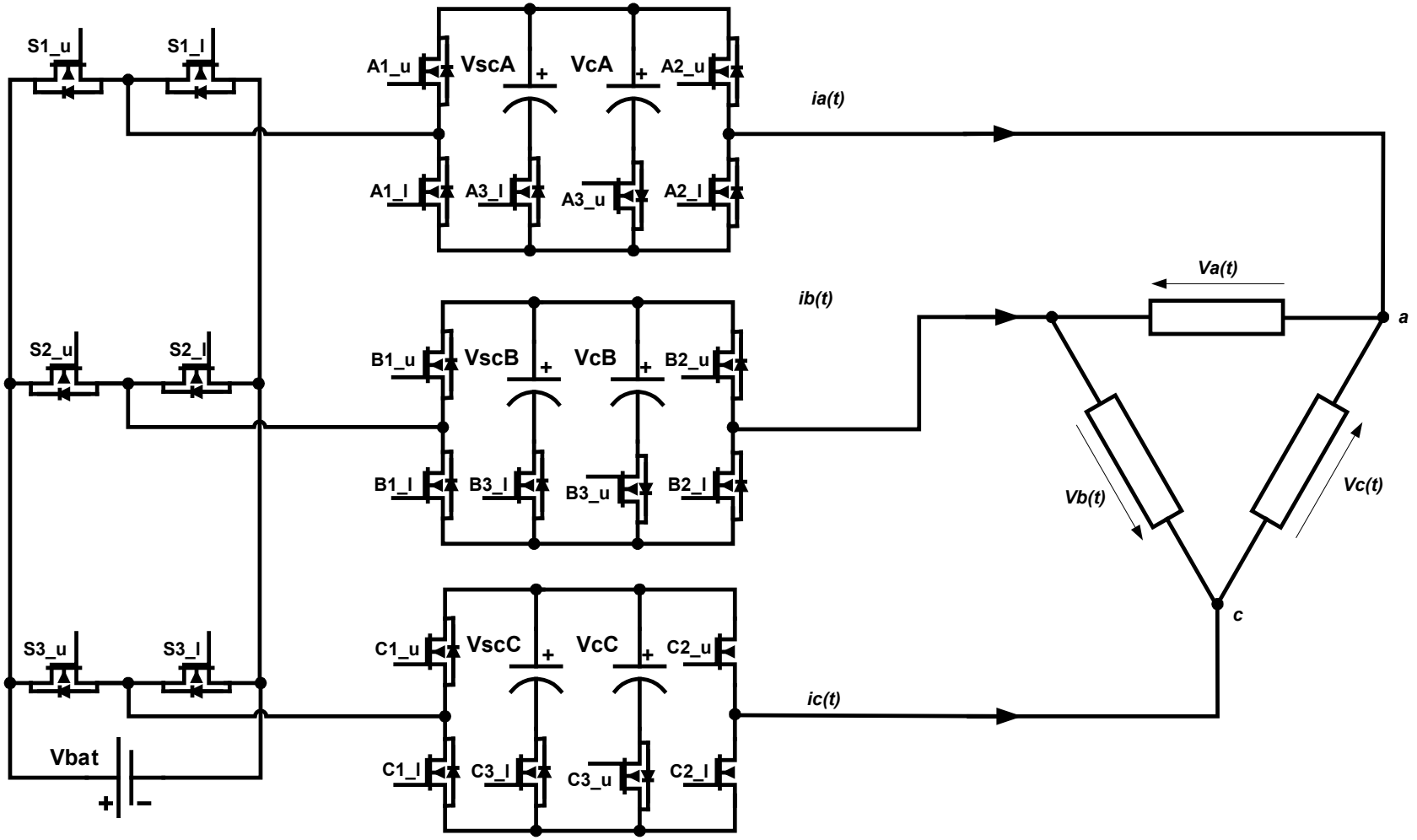


Figure 3-68 Proposed structure of multilevel inverter with modified H-Bridge

For winding configuration in delta all possible vector combinations for voltage ratio between the main source battery and the electrolytic capacitors equal 1:3 and between the battery and UCs equal 1:6 are presented in Figure 3-69.

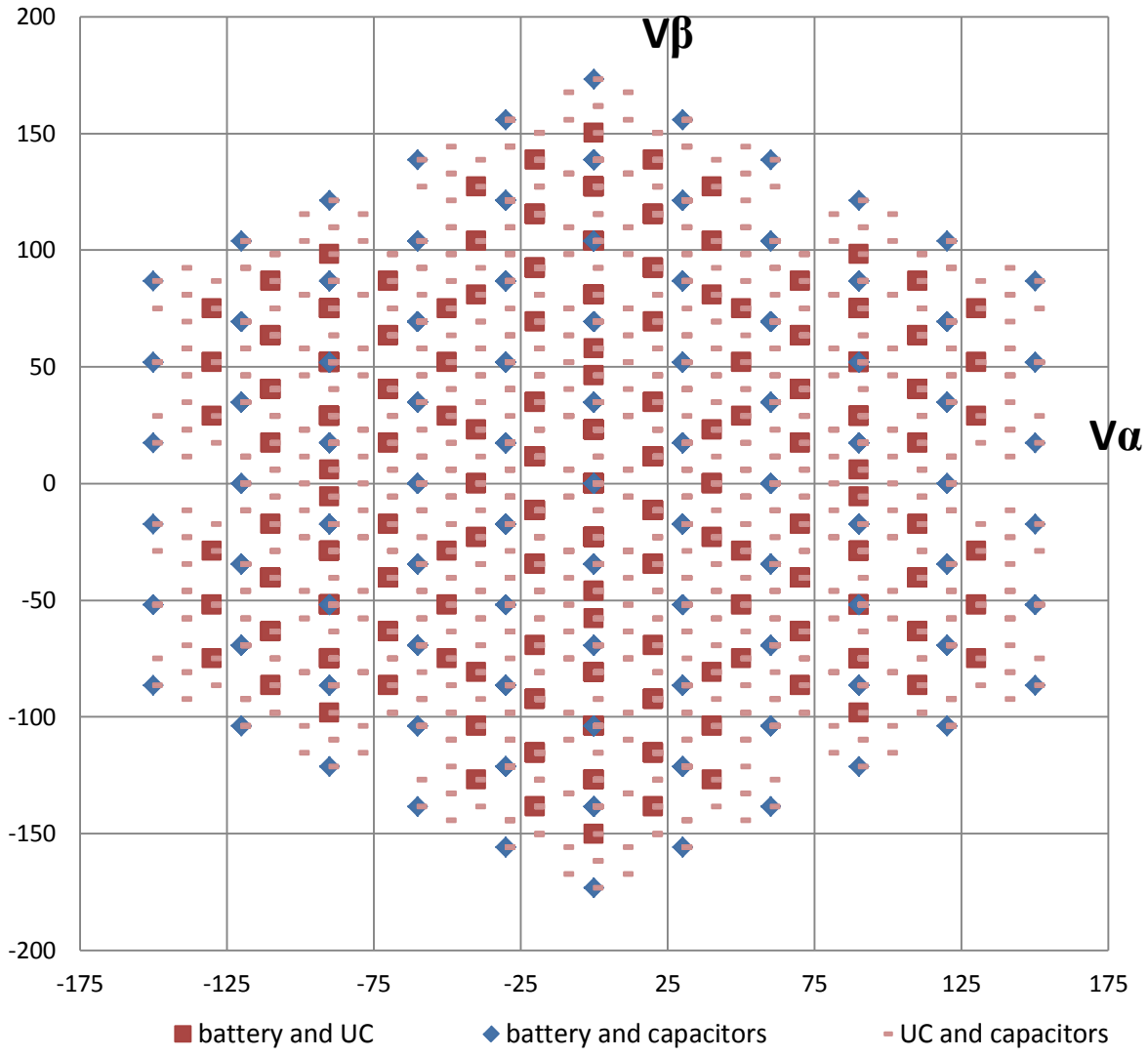


Figure 3-69 Available voltage vectors on α-β plane for V_{bat} = 90v, $V_{ca} = V_{cb} = V_{cc}$ = 30V (standard capacitors) and $V_{sca} = V_{scb} = V_{scc}$ = 20 V (UC)

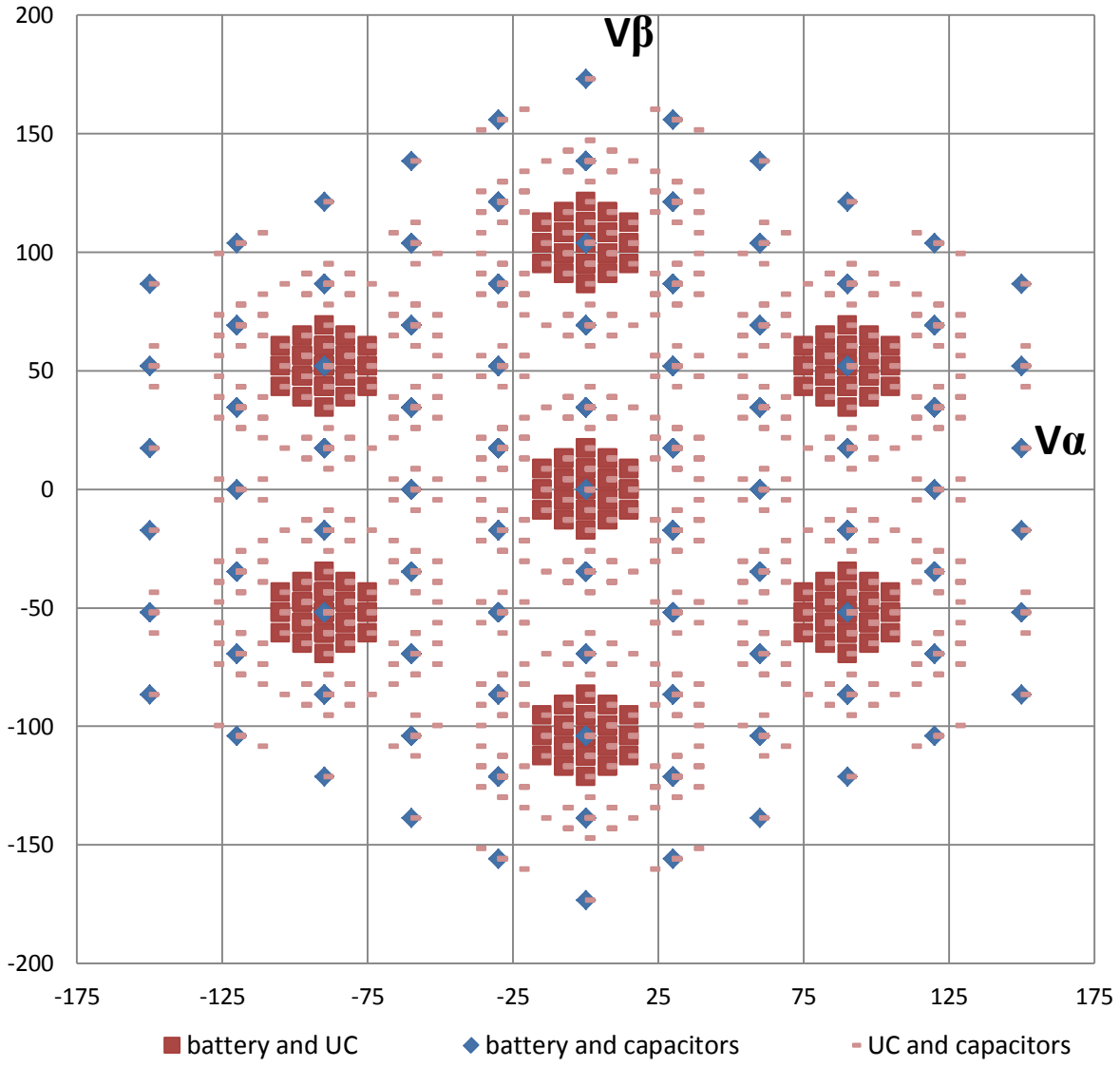


Figure 3-70 Available voltage vectors on α-β plane for V_{bat} = 90V , V_{ca} = V_{cb} = V_{cc} = 50V (standard capacitors) and V_{sca} = V_{scb} = V_{scc} = 7.5V (UC)

The second case where the voltage ratio of the UC has been reduced to 6% of battery voltage is presented in Figure 3-70. The number of available voltage vectors in this configuration significantly increased. It is also possible to keep the same distance between vectors even when the UCs are discharged in case of 90 vectors. This is presented as a blue squares, those coordinates remain constant independently from UC state of charge. The control strategy presented in earlier part of the thesis is still valid with difference that there is option to switch between strategy with UC or electrolytic capacitor.

3.7.4 Cascade inverter consisting of three-phase inverter supplied by battery and three modified H-Bridges with opposite connection of sources.

In the previous configuration each H-Bridge was modified to have two sources but could only deliver voltage from one source at a time. To expand the capability of the inverter the structure of the H-Bridge was modified further to allow the use of two sources simultaneously in each H-Bridge. In this structure two sources are connected in series through additional switches (Figure 3-71).

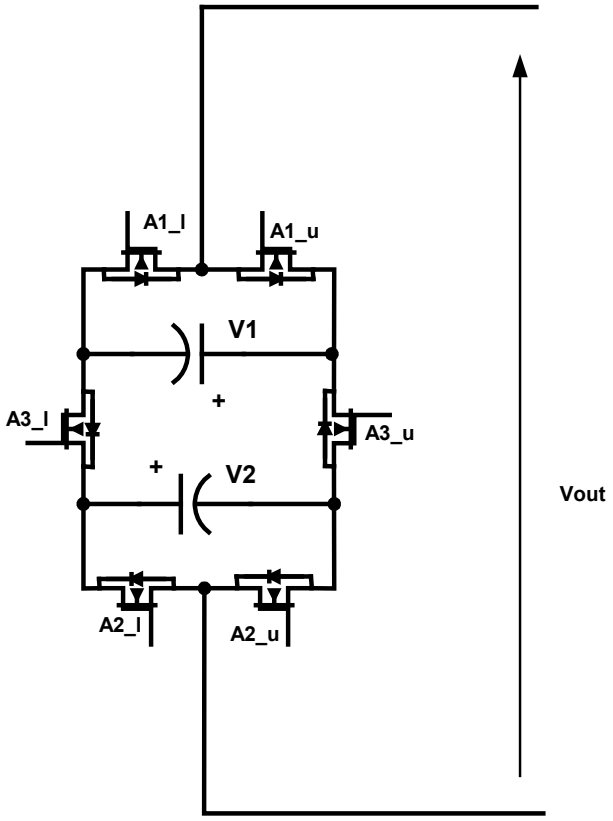


Figure 3-71 Structure of modified H-Bridge and its switching table

The drawback of this configuration is that the switch between the two sources has to be rated to a higher voltage than the sum of the two sources in the bridge. The main advantage is that it requires a very low number of switches to achieve a high number of voltage levels. To avoid undesired states the modulation strategy for this configuration is expected to be complicated and without an efficient algorithm the switching losses can be high. In this H-Bridge

configuration there are only two redundant zero vectors and each active switching states can only be created by unique bridge configurations

Table 3-4 Switching table

Combination number	Switch A1	Switch A2	Switch A3	Output voltage (V_{out})
0	0	0	0	0
1	0	0	1	-V1 – V2
2	0	1	0	V2
3	0	1	1	-V1
4	1	0	0	V1
5	1	0	1	V1 + V2
6	1	1	0	-V2
7	1	1	1	0

The main advantage of this H-Bridge is that it can produce seven different voltage levels at the output (Table 3-4). Unfortunately the A3 switch has to be rated with voltage that is equal to the sum of voltage sources The implementation of this H-Bridge structure into the three-phase inverter with a three-phase bridge (Figure 3-72) allows the generation of a high number of voltage vectors where the effect of discharging UCs can be minimised. Since each H-Bridge is able to deliver seven different voltage vectors the total number of different active states will increase to 2,401 (7^4). The high number of voltage vectors provides good resolution to generate output voltage with small ripples.

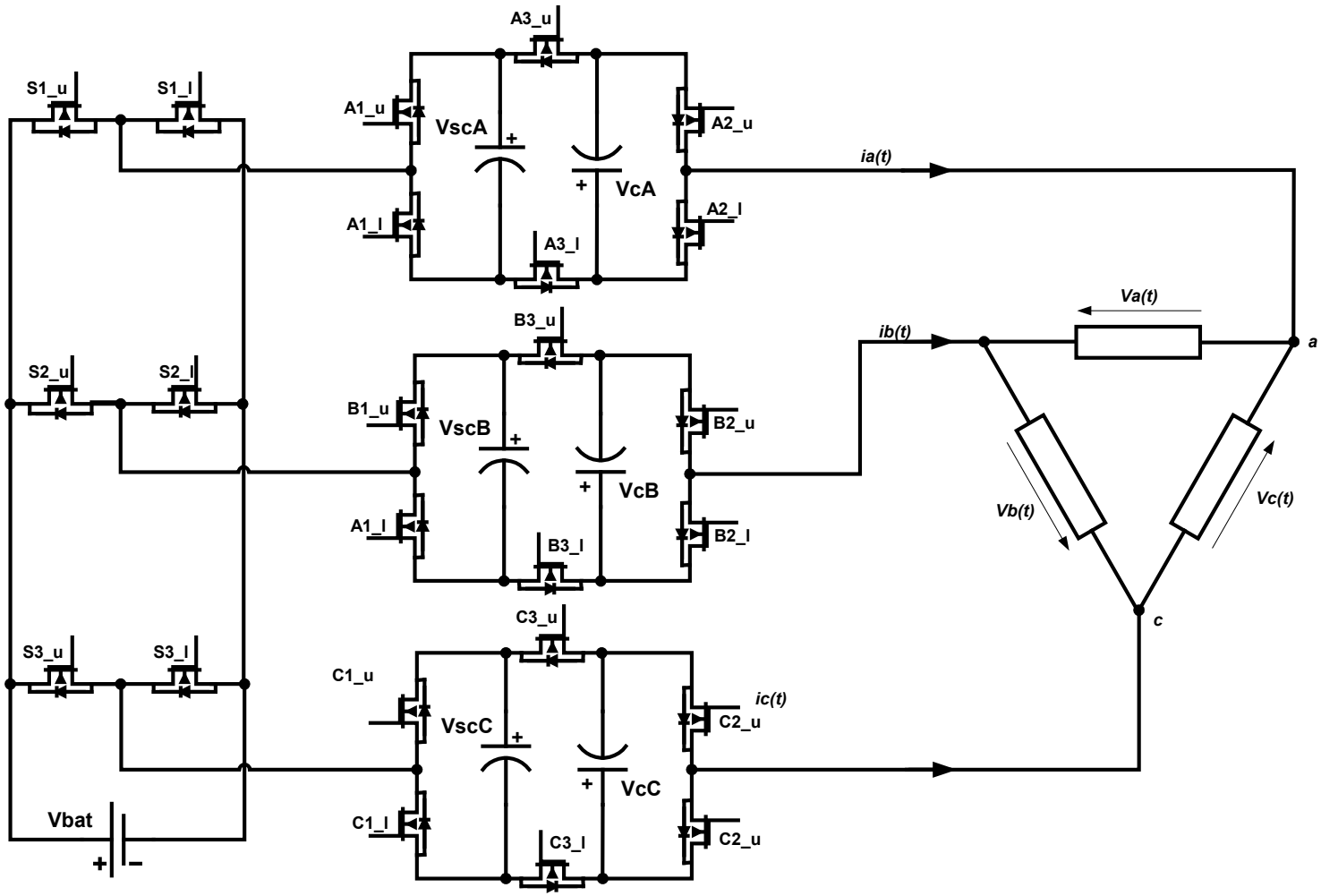


Figure 3-72 Further modified structure of multilevel inverter with seven-levels H-Bridge

In Figure 3-73 and Figure 3-74 the example of voltage vectors patterns are presented for the three-phase inverter implementation.

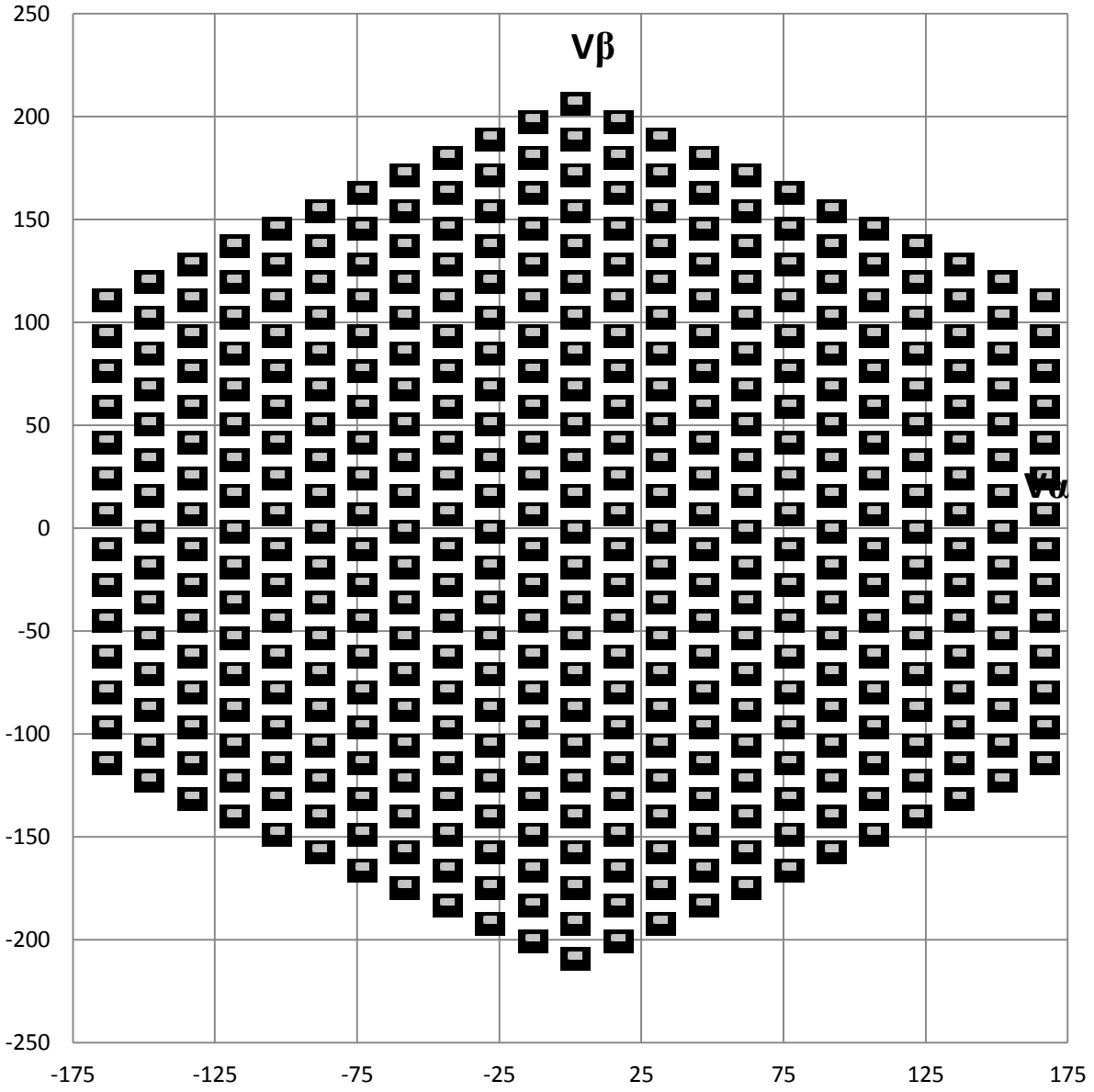


Figure 3-73 Available voltage vectors on α-β plane for V_{bat} = 90V, V_{ca} = V_{cb} = V_{cc} = 30V (standard capacitors) and V_{sca} = V_{scb} = V_{scc} = 15V (UC)

Nevertheless from Figure 3-74 we can find that with low UC voltage the vectors will group next to 90 main voltage vectors similarly to 3.7.3 example.

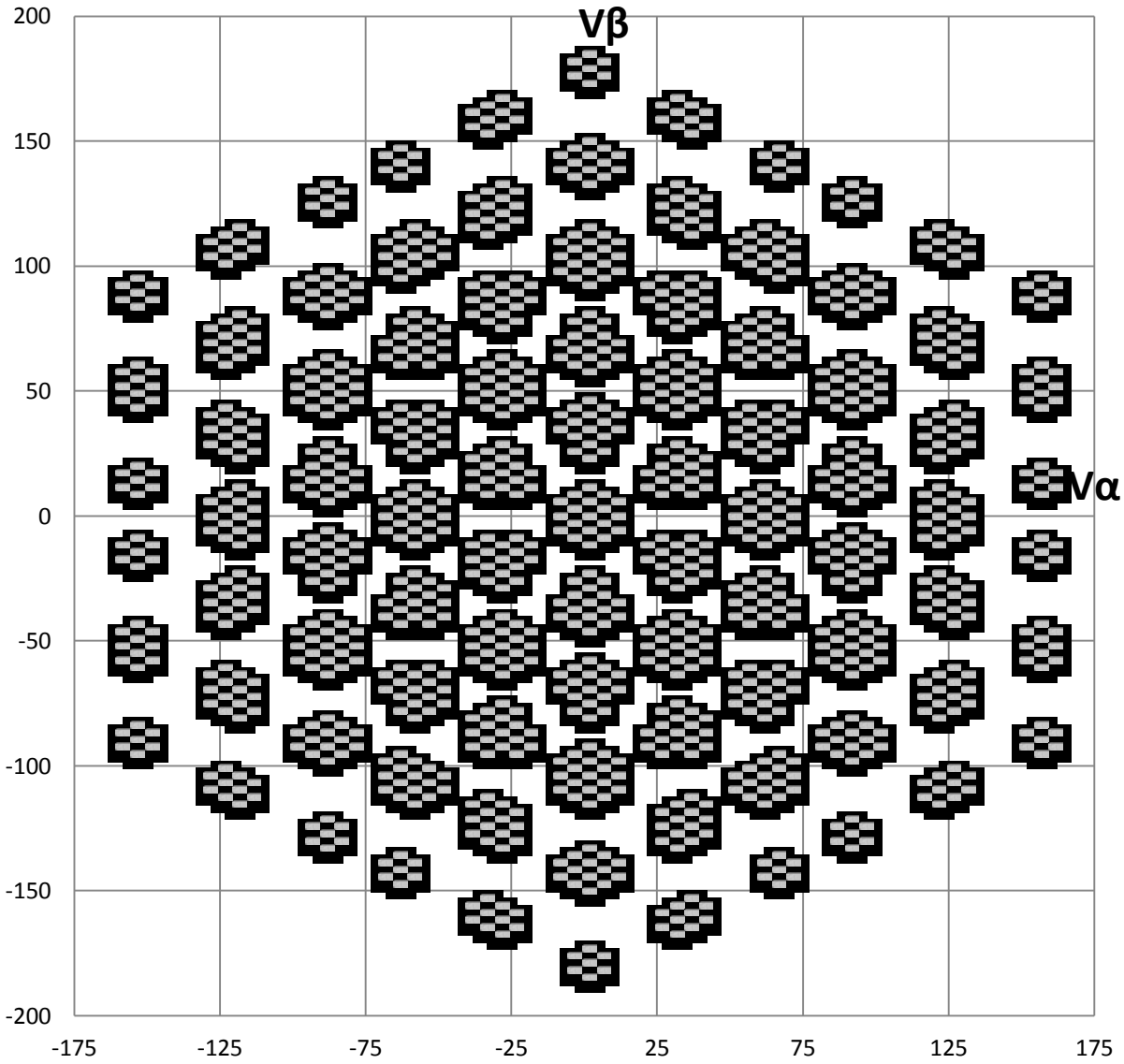


Figure 3-74 Available voltage vectors on α-β plane for V_{bat} = 90V , V_{ca} = V_{cb} = V_{cc} = 30V (standard capacitors) and V_{sca} = V_{scb} = V_{scc} = 6V (UC)

Because of high number of voltage coordinates and big number of redundant voltage vectors the drawings are simplified and redundant coordinated are presented as thicker grey dots. The benefits of high number of voltage vectors become limited for operations with discharged UCs and problem associated with higher switch voltage rating make this solution not attractive for multisource system. Still for applications with stable sources it becomes possible to achieve very low harmonics in output voltage.

3.7.5 Modified cascade inverter

In structure of the cascade multilevel inverter presented in Figure 3-72 the modular structure can be distinguish that consist of a voltage source with two switches connected with source to negative terminal (Figure 3-75). By adding same multiple UC modules it becomes available to expanded inverter architecture for more voltage levels. The structure requires that the voltage rating of the switch between two sources has to be higher than the amplitude of those two voltage sources.

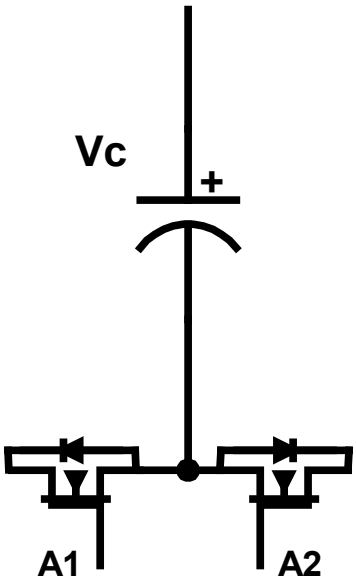


Figure 3-75 Module with single DC sources to expand H-Bridge

The properties of the proposed inverter module allow the expanding inverter to achieve an even higher number of voltage levels (Figure 3-76). By connecting sources with high and low amplitude next to each other it becomes possible to use switches that are rated only for voltages that exceed the sum of the adjacent switches.

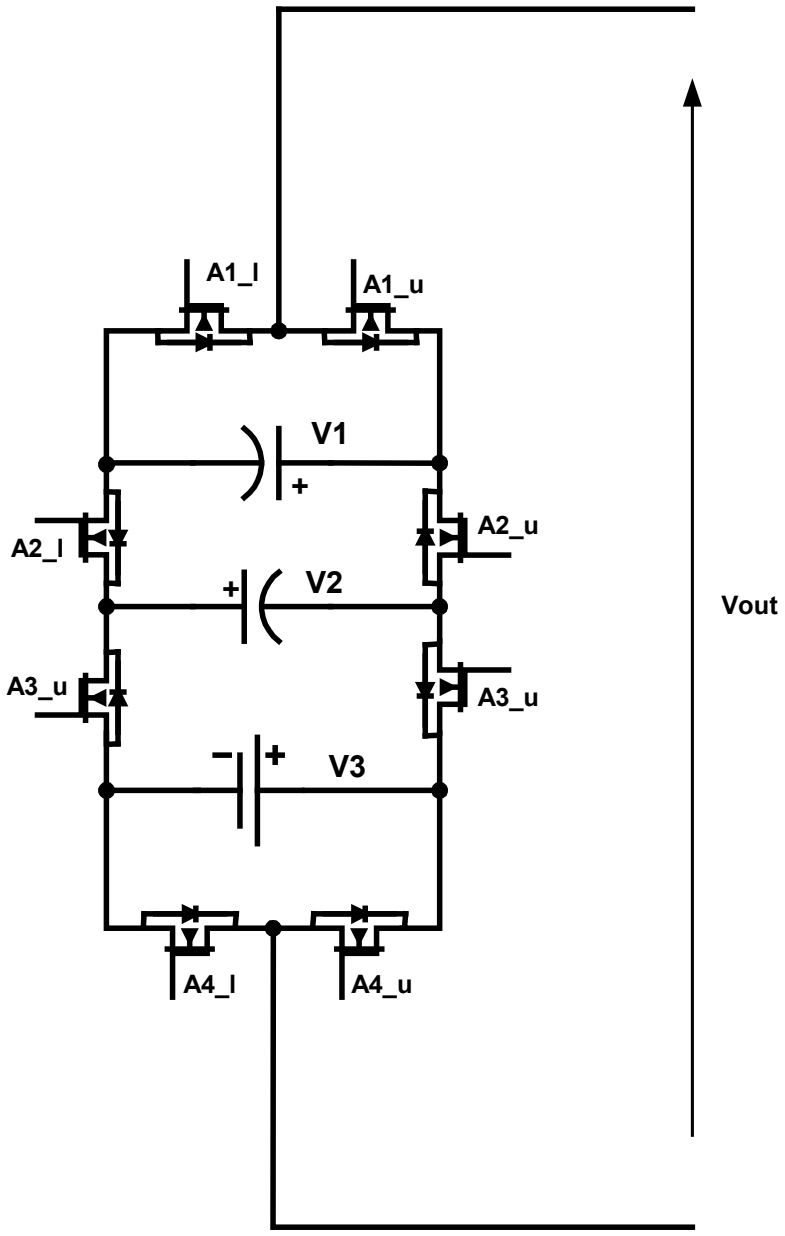


Figure 3-76 Modified H-Bridge inverter with 14 voltage levels

The single phase of the proposed structure with only four MOSFET's pairs and three voltage sources is able to generate 14 active voltage vectors and two zero voltage vectors. The example of possible voltage levels is presented in Table 3-5.

Table 3-5 Switching table for a modified H-bridge section

Combination number	Switch A1	Switch A2	Switch A3	Switch A4	Output Voltage (V_{out})
0	0	0	0	0	0
1	0	0	0	1	-V3
2	0	0	1	0	V2+V3
3	0	0	1	1	V2
4	0	1	0	0	-V1-V2
5	0	1	0	1	-V1-V2-V3
6	0	1	1	0	-V1+V3
7	0	1	1	1	-V1
8	1	0	0	0	V1
9	1	0	0	1	V1-V3
10	1	0	1	0	U1+V2+V3
11	1	0	1	1	V1+V2
12	1	1	0	0	-V2
13	1	1	0	1	-V2-V3
14	1	1	1	0	-V3
15	1	1	1	1	0

The voltage at the output of a single phase section can produce 14 voltage levels but each value can be generated by only unique switch combination. This limits operations of this inverter as to switch between some voltage values a high number of switches has to change its state.

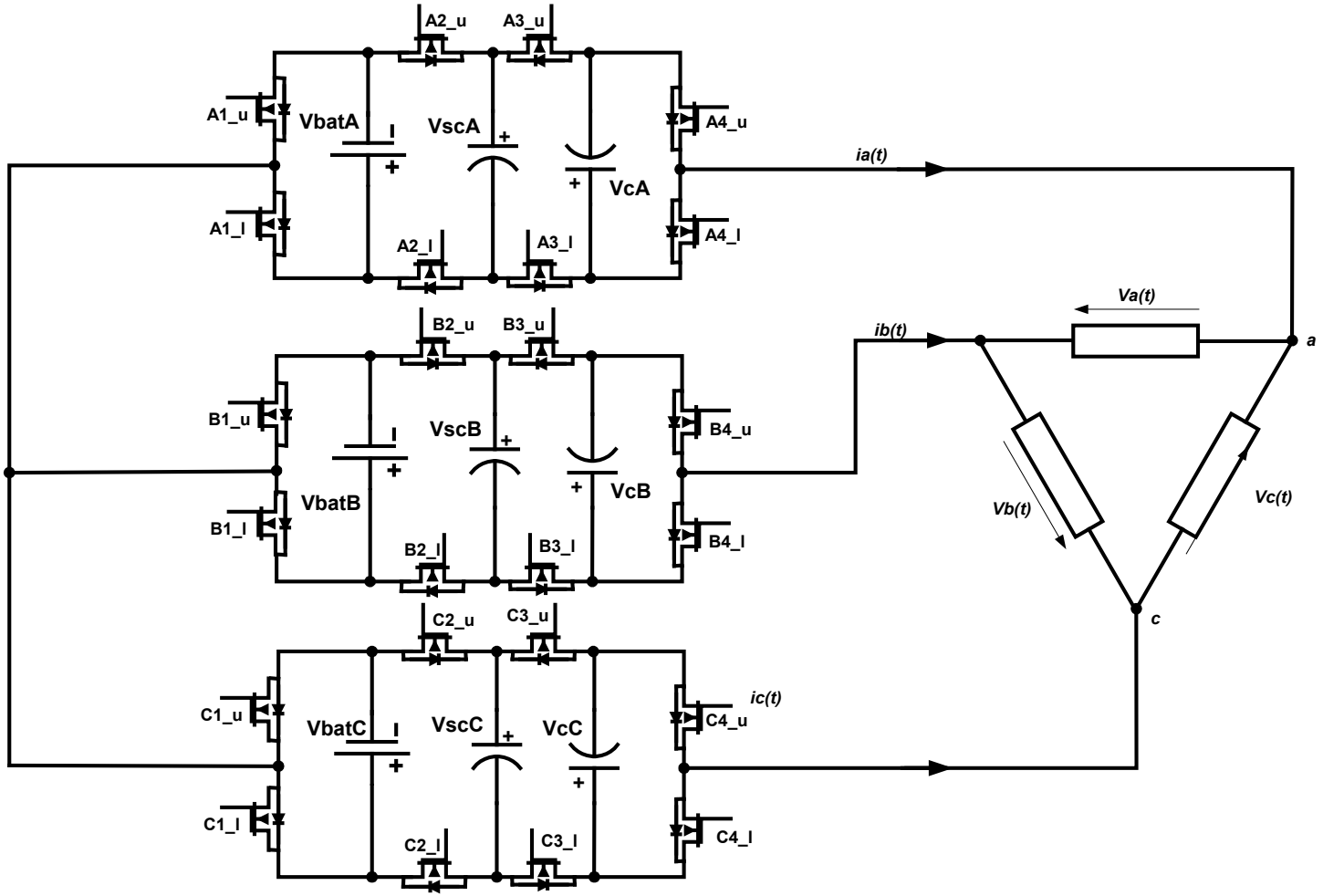


Figure 3-77 Structure of three-phase modified cascade inverter

Implementing the single phase structure as presented into the three-phase inverter (Figure 3-77) creates an inverter that is able to generate a high number of voltage vectors for a relatively low number of switches and voltage sources. As presented in Figure 3-78 and Figure 3-79 for a structure with three sources in each phase the total number of different voltage vectors will increase to 3,375 (15^3).

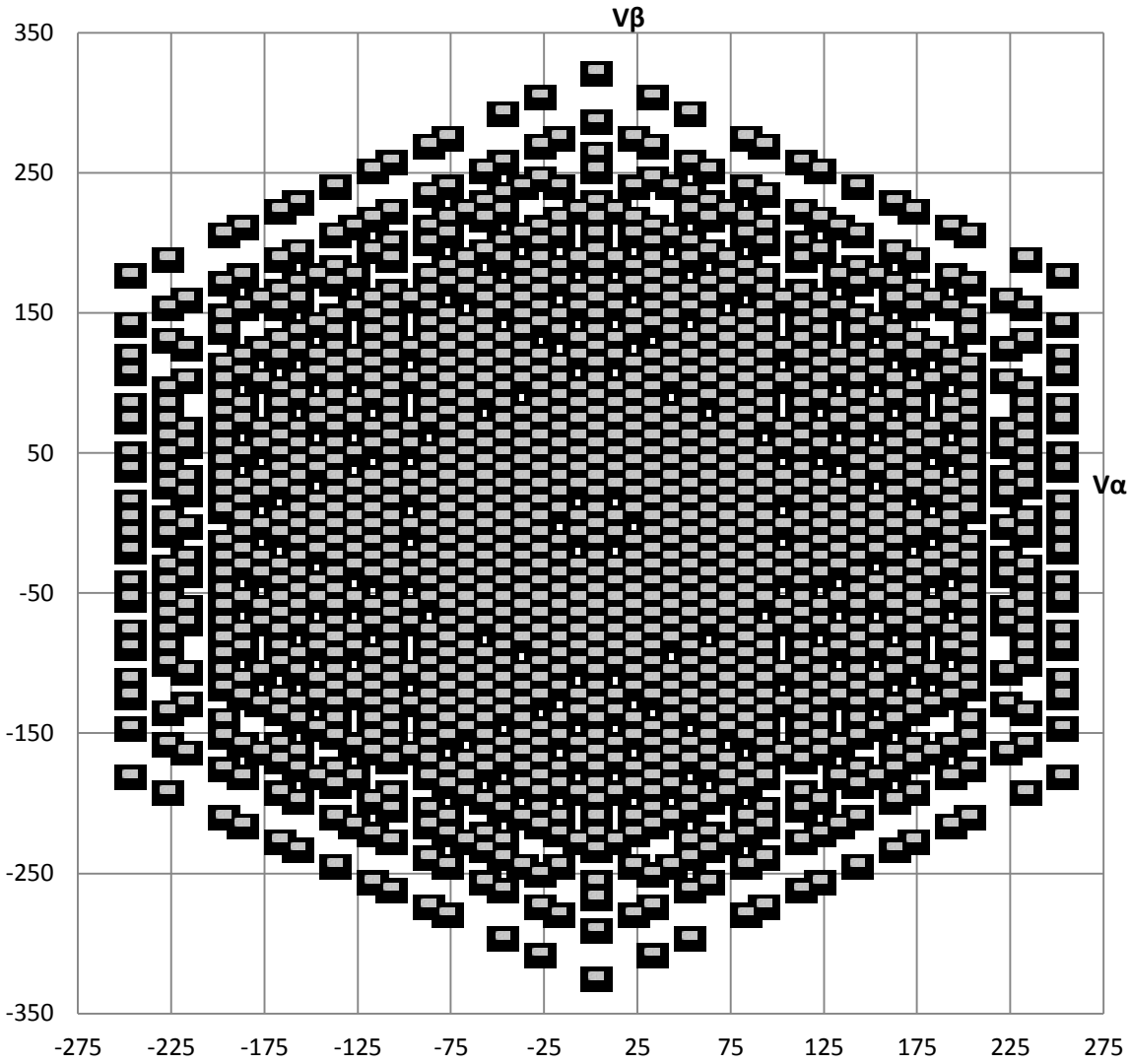


Figure 3-78 Available voltage vectors on α-β plane for $V_{batA} = V_{batB} = V_{batC} = 90V$, $V_{cA} = V_{cB} = V_{cC} = 30V$ and $V_{scA} = V_{scB} = V_{scC} = 20V$

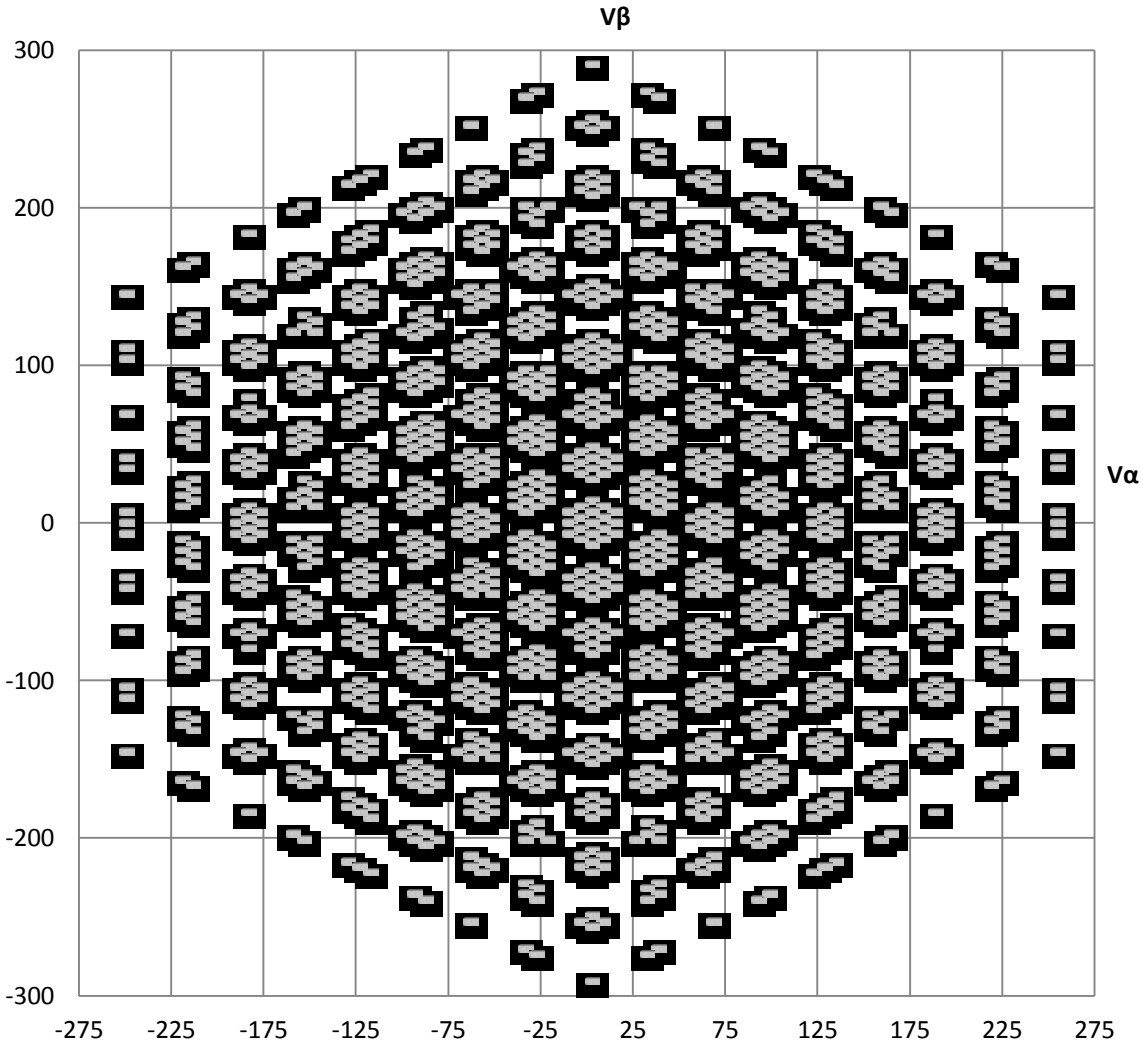


Figure 3-79 Available voltage vectors on α-β plane for $V_{batA} = V_{batB} = V_{batC} = 90V$, $V_{cA} = V_{cB} = V_{cC} = 30V$ and $V_{scA} = V_{scB} = V_{scC} = 6V$

Also In this case a high number of voltage vectors remain with fix coordinates independent from UC variation. This is especially visible in Figure 3-79 where vectors related with UC are grouped next to coordinates produce by battery and capacitors. Due to the control system complexity and increase component number this type of configuration is not attractive for automotive market. There is also no needed to increase number of levels to such a value since the reduction of harmonics in voltage is proportionally insignificant. For those reason the further research work related with modifications to inverter wasn't continue.

3.8 Summary

In this chapter the problem with modulation for multisource hybrid inverters has been identified. Following issues with variable voltage vector configurations, six main modulation schemes were determine to overcome the problems of uneven vector distribution. The analysis of each modulation scheme was performed to find the voltage limitations of each strategy. As presented in Figure 3-17 and in Table 3-1 the availability of modulation schemes will vary depending on the UC's state of charge. To control power for those six main strategies, as well as modulate the vector within the available limits (especially for mode II), the limiting phase shift angle was introduced (χ). The power analyses provided a basis for an estimation of power flow and allowed to find the power control limitations for six main modulation strategies. Since phase shift control does not provide sufficient power regulation between all modulation schemes, it was proposed to alternate between two modulation schemes in each sector with control angle (α). Alternating between modulations can have 36 different strategies. Only nine mixed modulations were identified as useful to help overcome limitations of the six main strategies. As presented in Figure 3-53 it is proposed to switch different modulations only with the pattern given. Through the harmonics analysis it was proven that the strategy of alternated modulation schemes will not introduce additional harmonics, and that based on analytical calculations, it is possible to estimate the power share between sources.

Having described modulation strategy the next step was to define power management approach to maximize kinetic energy capture, to find best amplitude of UC source and to operate battery within set boundaries. Proposed control method monitor motor as well sources parameters and base on results set different power share reference. Thanks to this control the main voltage source is protected against operations with higher than rated current and also It become possible to fully utilize sources voltage. It was also found that in the hybrid cascade inverter there has to be compromise between UC voltage regulated in reference with kinetic energy and UC voltage reference for maximum number of voltage levels at inverter output.

Finally the analysis in this chapter shows that by a simple modification to the H-Bridge it becomes possible to overcome the problem of reduced multilevel inverter performance when UCs becomes discharged. The solution presented in paragraph 3.7.3 appears to be the most attractive since it requires only a minor modification. By including additional low capacity voltage sources and transistors pairs that are only switched at zero current, it is possible to implement a low-cost solution to significantly improve the performance of the inverter. The control algorithm does not have to be heavily modified and it could be possible to use the same analogue input to monitor voltage of two sources depending on which source is used. The additional benefit of this system is that it becomes available to control the amplitude of the third voltage source type according to presented method in paragraph 3.6 to achieve the maximum number of voltage levels and to further reduce the amplitude of unwanted harmonics.

CHAPTER 4 IMPLEMENTATION OF CONTROL STRATEGY

In this chapter the approach to implement control system based on inverter analysis from Chapter 3 is presented. First the concept of the hierarchal control structure for the multisource system is discussed and adopted for the hybrid cascade multilevel inverter. Next, a detail design of the control system elements that provide effective solution to translate mathematical dependencies into simplified commands is presented. Later, the SVM algorithm that allows to modulate given reference voltage vector and to control power usage by each source is discussed in comparison with conventional structures. In further part of this chapter based on existing solutions from literature the implementation of the DTC for induction motor is described. Finally the power management algorithm to supervise proposed SVM modulator is implemented within the control scheme.

4.1 Hierarchical design of control system

In previous chapter, a detailed analysis of the hybrid cascade inverter was presented, and the limitations of the structure with variable amplitude of voltage vectors were found. The relation between the modulation method and the active power shared between sources was defined and a strategy to control power distribution was proposed. To maximize the operation of the inverter and fully utilize its topology it is necessary to design a control system that will constantly monitor the requested power, voltage and the status of the sources to adequately select a modulation strategy and control the power flow between the sources.

Similar to the hierarchical decision system in “A Modular Power and Energy Management Structure for Dual-Energy Source Electric Vehicles” by L. Rosario and P. C. K Luk (Rosario et al., 2006) it is proposed that the control system for the multilevel and multisource drivetrain will adopt a modular structure. This function separation allows also for splitting the algorithm into different types of control platforms, such as FPGA (Field Programmable Gate Array) for

instantaneous calculations and real-time processor for calculations through a longer program cycle.

For this system we can distinguish long-, medium- and short-term layers:

The long-term shell is responsible for energy and power management and is not time critical. The aim of this function is to define power sharing between sources based on motor speed, main source power limits, the sources' actual voltage and actual motor current and voltage. The output from this control provides reference power for sources as well is supervising reference motor flux and torque to assure that drive is within the available power. This allows the main source to operate within limits. Transient energy is handled by UCs and the inverter's output voltage harmonics are minimized for the best performance. The stator flux regulation in the proposed system is limited to a fixed value. Nevertheless, this topology gives the opportunity to find best flux value in relation to the available active and passive power and the UC's voltage that vary as presented in section 3.6.2.

The medium-term shell is time critical and has to be synchronized with motor control and SVM algorithm. Its function is to select the best modulation strategy and to output reference voltage from flux and torque regulators deepening on inverter status, power sharing configuration and requested torque. The control has to ensure that the requested voltage vector can be produced by the inverter and the modulation configuration will provide the requested power sharing between sources. Since the new reference voltage and related modulation setup has to be ready within SVM duty cycle and the algorithm has multiple dependencies it is proposed to implement this control within a real-time processing unit.

The short-term shell is for all elements that interface incoming analogue and digital signals and output lines, where instantaneous signal processing is required. The short-term shell is responsible mainly for a SVM algorithm that generates gating signals for inverter switches. This process is time critical and it is necessary to generate the switching pattern as soon as the reference voltage from the higher-level shell appears. Instantaneous signal processing is also

necessary for the analogue input signals to minimize noise and achieve high accuracy. Additionally it is used for the rotor position sensor where the incoming digital signals are fast. The short-term shell also estimates the electromagnetic torque and flux, and for reference voltage vector, utilizes a set modulation strategy that provide adequate power share between sources.

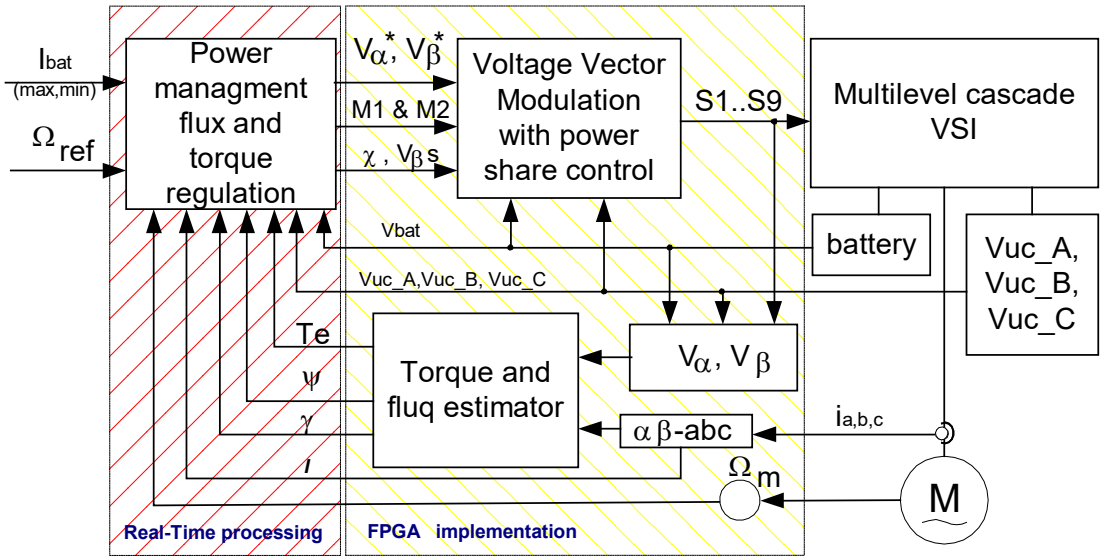


Figure 4-1 Block diagram of cascade multilevel inverter motor drive with power flow management

To meet these requirements the control system for the hybrid cascade inverter with multiple sources was designed as shown in Figure 4-1. The system presented consists of three main functional blocks.

Power management with torque and flux regulation, and a modulation strategy control implemented on real-time processing unit

Voltage Vector Modulator with power share control implemented on FPGA unit

DTC torque and flux estimator implemented on FPGA unit

4.2 Design of SVM algorithm with power transfer functionality

It was concluded from the analysis in Chapter 3 that to control the hybrid cascade inverter in full range it is necessary to use six different modulation strategies. It was proposed for power distribution control to either use phase shift of output six-step waveform at fundamental frequency (χ) or to switch between two modulations strategies twice per one sixth of the period (α). These requirements led to the design of an SVM algorithm that allows the finding of a suitable combination of voltage vectors efficiently, without the need for high computation power from the control system.

The specified system is required to modulate the reference voltage from the input value in α-β plane by producing adequate switching pulses sequence to MOSFET gate derivers. The switching combination produced by the SVM unit should depend on set phase shift angle (χ), selected modulation strategies and switch angle value (α), and be adapted to the amplitude of the voltage sources. To avoid delays that could lead to additional voltage ripples, it is necessary to perform calculations instantaneously when new reference voltage vectors appear.

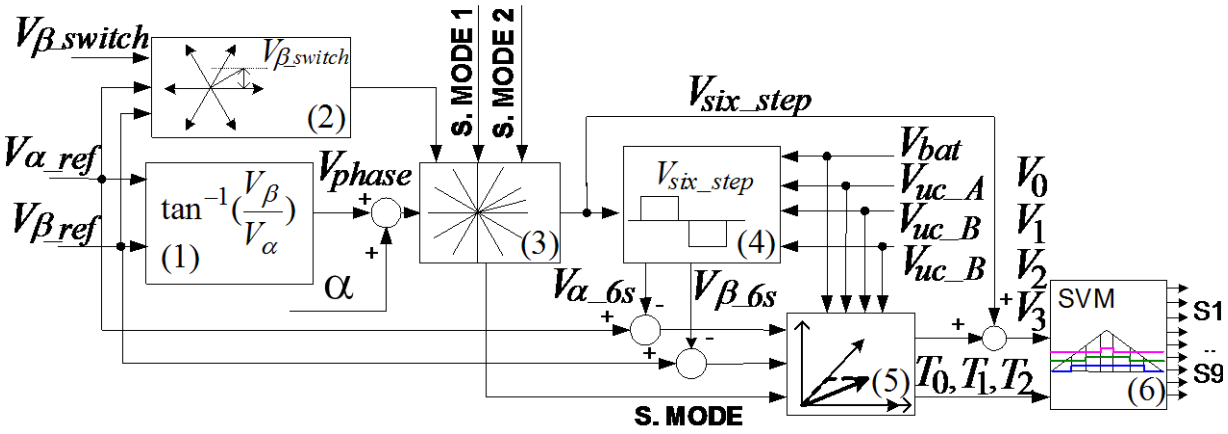


Figure 4-2 Block diagram of modulation algorithm for cascade multilevel inverter with variable sources voltage and power flow control

Figure 4-2 shows a block diagram of the proposed system consisting of the following elements:

1. Cartesian to polar transformation to calculate angular position of reference vector in stationary reference plane (α-β plane) (Figure 4-3).

The angular position of the reference voltage vector is needed for the six-step switching and to allow phase shift control of the generated waveform. This type of calculation is complex and often requires having multiple numbers of iterations. In our case it is expected that the transformation to find the angle will be the main factor delaying the vector pattern calculations. To have adequate resolution the FPGA implementation with Coordinate Rotation Digital Compute (CORDIC) requires 18 FPGA cock cycles for 16-bit value.

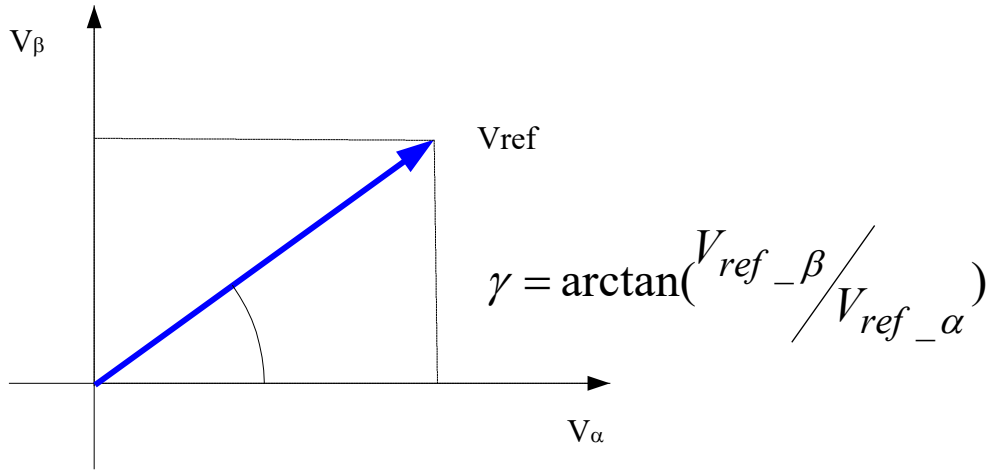


Figure 4-3 Reference voltage vector, its representation in α-β stationary plane and its angular position

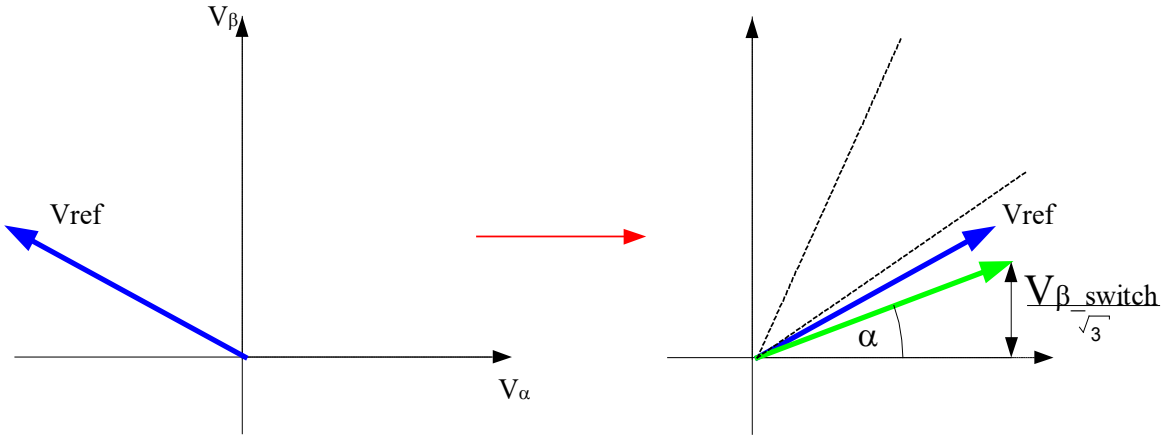
2. Comparator module generating switch signal to change modulation mode when voltage vector is crossing switch angle "α".

In order to find the right angle to switch between modulation methods it is planned to transform the reference voltage vector into a new coordinate system that is positioned in the sector between 0 and $\pi/6$ angle. This operation needs only to convert the reference voltage vector into an absolute value and where its angle is larger than $\pi/6$ to transform its coordinate system by a further $\pi/3$. For the transformed reference voltage it becomes available to find at which point modulation scheme should be changed by comparing voltage value in the

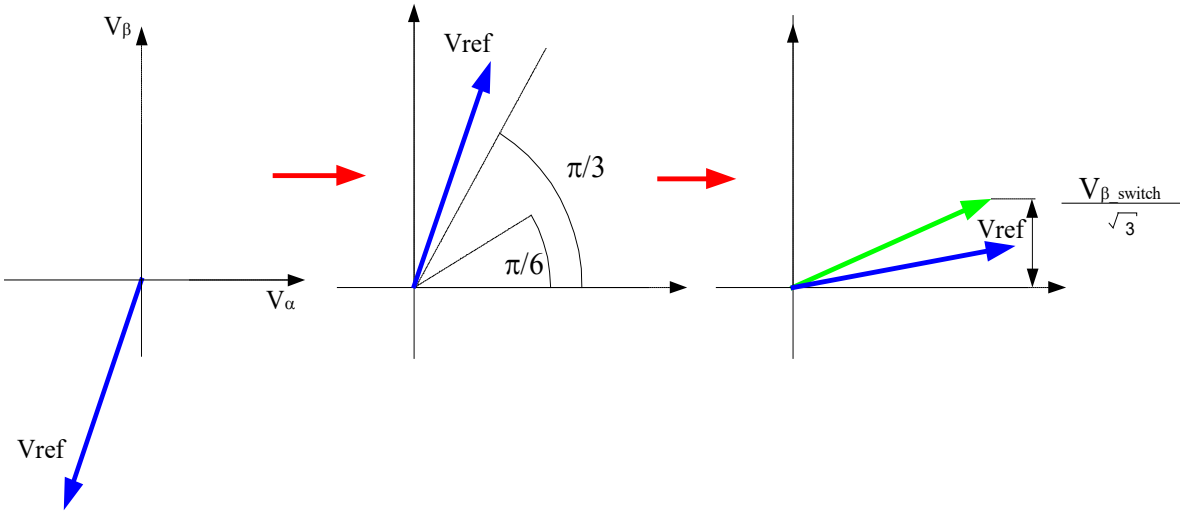
vertical axis with a set value (V_{β_switch}) as presented in Figure 4-4. The relation between the threshold voltage and the set angle is described by equation (**4-1**).

$$V_{\beta\_switch} = \frac{\sin(\alpha)}{V_{ref}} \tag{4-1}$$

The output of the block is a logical signal that provides information about the change of the modulation mode. By setting the threshold voltage (V_{β_switch}) as the amplitude of the source that is used for SVM, it is possible to provide protection against insufficient voltage vectors for given modulation scheme.



(a) Angle lower than $\pi/6$ for absolute value of voltage vector coordinates



(b) Angle higher than $\pi/6$ for absolute value of voltage vector coordinates

Figure 4-4 Transformation of reference vector into 1st sector coordinates between 0 and $\pi/6$ to allow comparison with reference switch voltage

The logic of the block can be described in the following simplified steps:

For reference voltage that meets requirements (4-2),

$$\left|V_{ref\_\propto}\right| \leq \left|V_{ref\_\beta}\right| \cdot \sqrt{3} \tag{4-2}$$

a second modulation scheme is used when equation (4-3) is met,

$$\frac{\left|V_{ref\_\beta}\right| - \sqrt{3} \cdot \left|V_{ref\_\propto}\right|}{2} > \frac{V_{\beta\_switch}}{\sqrt{3}} \tag{4-3}$$

otherwise the first modulation strategy is used.

In the second case when relation (4-4) is valid

$$\left|V_{ref\_\propto}\right| > \left|V_{ref\_\beta}\right| \cdot \sqrt{3} \tag{4-4}$$

the second modulation mode is used for relation (4-5)

$$\left|V_{ref\_\beta}\right| > \frac{V_{\beta\_switch}}{\sqrt{3}} \tag{4-5}$$

otherwise the first switching strategy is selected.

3. Look-up table with six-step switching combination for the six modulation strategies (from MODE I to MODE VI) and voltage vector angle comparator for six sectors.

In the next step the voltage vector angle with added phase shift (χ) is compared to the six sectors reference boundaries ($\pi/6$, $\pi/2$, $5\pi/6$, $-\pi/6$, $-\pi/2$, $-5\pi/2$) (Figure 4-5). The unit consists of six separate look-up tables for each modulation scheme that have different switch configurations for each sector. Based on the position of the phase shifted voltage vector, and information about the selected modulation strategy, the appropriate vector state combination is selected from the look-up table. For strategies that use six-step switching for H-Bridges the look-up tables include multiple configurations for the same sector. This allows the selection of a vector combination that will balance the UC's voltage such that each capacitor has similar voltage.

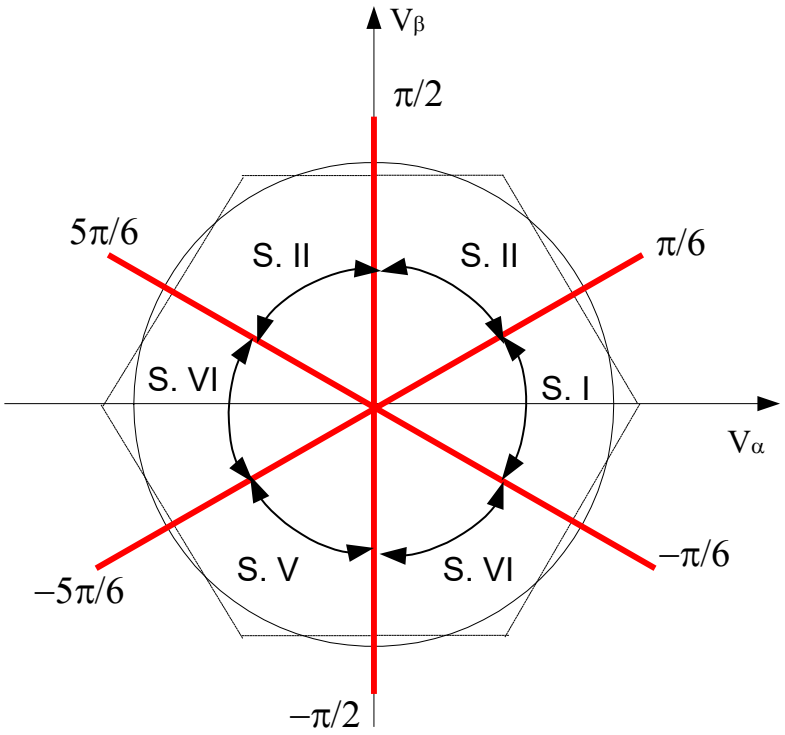


Figure 4-5 Limiting boundaries for six step switching

The control logic for UCs is based on hysteresis comparator, if one source has smaller amplitude than average, the second vector combination is selected as presented in section 3.5.

4. Transformation of six-step waveform into vector in stationary reference plane (α-β).

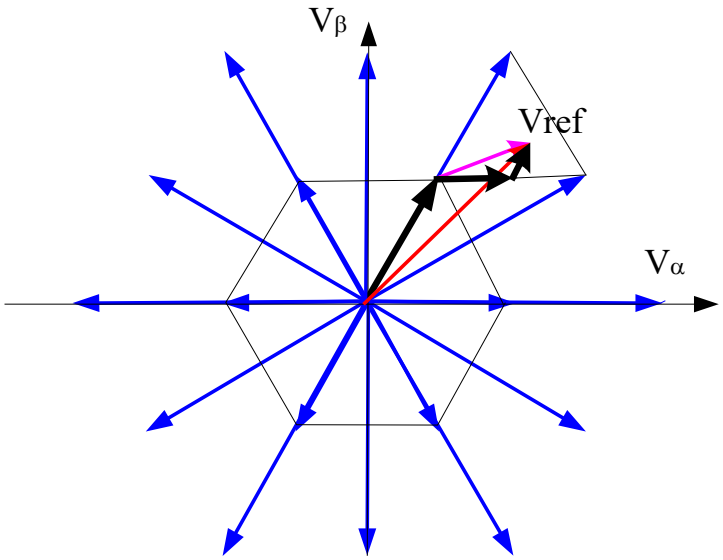
The output switch configuration from a look-up table (block 3) for an inverter section that is switched at fundamental frequency is processed further to calculate its coordinates in stationary reference plane (α – β). To find the size of a voltage vector the equations (4-6) and (4-7) are derived from the formulas in Chapter 3 (3-1)-(3-5). Their implementation consists of a combinations process between switch states and the amplitude of all voltage sources. The output voltage vector is then used to subtract from the reference voltage vector and the remaining voltage is forwarded to the SVM module.

$$V_\alpha = \frac{2}{3}\left(\frac{V_{bat}}{2}(2\cdot S1 - S2 - S3) + \right. \tag{4-6}$$

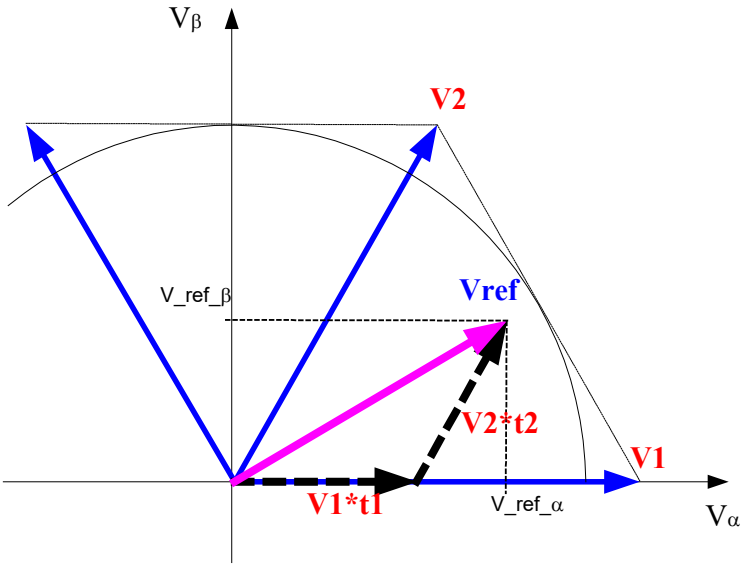
$$\left. + V_{UC\_A}(A2 - A1) - V_{UC\_B}(B2 - B1) - V_{UC\_C}(C2 - C1)\right)$$

$$V_\beta = \frac{\sqrt{3}}{3}\left(\frac{V_{bat}}{2}(2\cdot S2 - 2\cdot S3) + V_{UC\_B}(B2 - B1) - V_{UC\_C}(C2 - C1)\right) \tag{4-7}$$

5. Space Vector Modulation with look up table for voltage vectors selection and its dwell time calculation.



(a) Three level voltage vector modulation represented as a sum of vectors



(b) Modulation for the remaining vector and its dwell times

Figure 4-6 Space vector diagram, three-level to two-level transformation

To calculate dwell times for the given voltage the remaining part of the voltage vector is first located in one of the six sectors by coordinate value sign and the relation between the coordinates similarly to that implemented in block 2. Based on vector position in one of six sectors and depending on the selected modulation method, the closest voltage vectors are chosen from the corresponding look-up table. If the H-Bridge section is selected for SVM, then additionally the amplitude of the modulated voltage is compared with the UC's voltage to distinguish whether two- or three-level modulation is needed. In the case of three-level switching the adequate voltage vector is subtracted so that only the remaining voltage vector has to be synthetized by SVM as presented in Figure 4-6. The dwell times for standard SVM are calculated from geometry relation presented in Figure 4-6 based on volt-second balance equations (4-8) - (4-16) that can be found in literature (Bishuang, Guanzheng and Shaosheng, 2014), (Gholinezhad and Noroozian, 2013), (Li and Li, 2006).

The reference voltage vector in a three-phase system can be presented as a sum of three vectors multiplied by a dwell times.

$$V_{ref} \cdot T = V0 \cdot t_0 + V1 \cdot t_1 + V2 \cdot t_2 \tag{4-8}$$

For a first section from 0 to $\frac{\pi}{3}$ we have two active vectors (V1 and V2) and one zero vector V0.

$$V1_{\propto} = \frac{2}{3} V_{source}, \quad , \quad V1_{\beta} = 0 \tag{4-9}$$

$$V2_{\propto} = \frac{2}{6} V_{source}, \quad , \quad V2_{\beta} = \frac{1}{\sqrt{3}} V_{source} \tag{4-10}$$

The sum of all dwell times is equal to the SVM period.

$$T = t_o + t_1 + t_2 \tag{4-11}$$

Then the reference voltage vector in α and β plane is represented as:

$$V_{ref\_\propto} \cdot T = V1_{\propto} \cdot t_1 + V2_{\propto} \cdot t_2 \tag{4-12}$$

$$V_{ref\_\beta} \cdot T = V2_{\beta} \cdot t_2 \tag{4-13}$$

Where dwell times are calculated from following equations:

$$t_2 = \frac{\sqrt{3} \cdot V_{ref\_\beta} \cdot T}{V_{source}} \tag{4-14}$$

$$t_1 = \frac{3 \cdot V_{ref\_\alpha} \cdot T}{2 \cdot V_{source}} - \frac{1}{2} t_2 \tag{4-15}$$

$$t_o = T - t_1 - t_2 \tag{4-16}$$

Since dwell times are calculated every duty cycle with filtered battery and UCs amplitude then the output voltage error will remain minimum.

6. Three-phase SVM with symmetrical placement of zero vector and 10-bit counter.

For space vector modulation the most popular method with symmetrical zero states has been selected due to its low harmonic spectrum and good common mode voltage performance (Mcgrath, Holmes and Lipo, 2003). The input to the modulator includes switch combinations for four vector states V0, V1, V2 V3 that are formed from a sum of the six-step vectors and the SVM vectors from block 5. Additionally, to ensure that the vector trajectory pattern will include minimum changes of switch states the vector bit numbers are compared and sorted in incrementing order. The whole algorithm is synchronized with a 10-bit counter that is counting up and down. The vector combinations as well as the dwell times are registered at its input one clock cycle before the new period (T) of SVM starts. For the implemented symmetrical zero vector placement the first zero vector is placed at the beginning and end of the cycle for time equal to $T_0/4s$ and the second zero vector is inserted centrally for $T_0/2$. The new vector switching configuration is outputted to the gate drivers on each event when the counter reaches an adequate value for the particular vector as presented in Figure 4-7. The period T was set to 1024μs with 1μs resolution (t1) due to control hardware digital output card limitation.

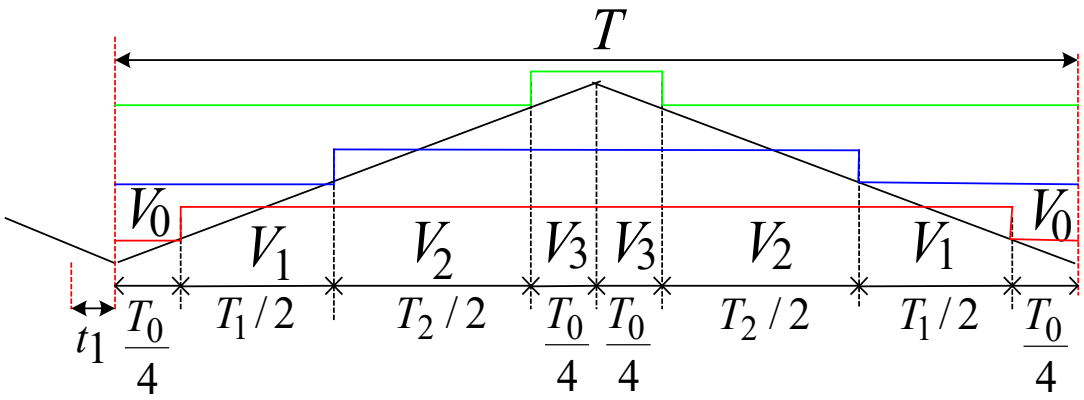


Figure 4-7 Example Space Vector Modulation sequence with symmetrical zero states and corresponding gate signals for switches in a three-phases (A-green, B-blue and C-red)

The whole modulation algorithm takes only less than 40 clock cycles to find adequate voltage vectors and their dwell times which for 40Mhz FPGA clock gives 1μs delay. The 40 cycle's computation time can be considered a good achievement since program requires multiple coordinate system changes. The output voltage vector will be similar to results achieved from conventional SVM with symmetrical zero states as presented in literature (Celanovic et al., 2000), (Malla and Malla, 2010) but with the main difference that there is additional control of modulation method that provide power sharing ability and modulation indecently from voltage ratio between sources.

In case the inverter is modified as described in paragraph 3.7.3 with additional electrolytic capacitors and pairs of switches, the control SVM algorithm has to be modified to have ability to select either the UC's or capacitor voltages values for vector calculations.

4.3 Implementation of DTC for induction motor

The main task of the system is to drive the electric motor during static and dynamic operations. To allow correct and stable performance and to control power transfer to and from the motor, the reference voltage has to be generated according to the feedback signals. One of the most popular controls of induction motor is Direct Torque Control due to its simplicity and good dynamic response. The idea of DTC is based on stator voltage vector equations of AC motor as

presented in below formulas from literature (Grabowski et al., 2000),(Kazmierkowski et al., 2011), (Malinowski and Kazmierkowski, 2002).

The stator voltage in α-β plane is equal to resistive voltage drop in motor winding and to stator flux derivative

$$V_{\propto} = R_s I_{s\_\propto} + \frac{d\Psi_{s\_\alpha}}{dt} \tag{4-17}$$

$$V_{\beta} = R_s I_{s\_\beta} + \frac{d\Psi_{s\_\beta}}{dt} \tag{4-18}$$

By transforming the equation into integral of the motor back electromagnetic force (EMF) the stator flux can be estimated

$$\Psi_{s\_\alpha} = \int (V_{\propto} - R_s I_{s\_\propto}) dt \tag{4-19}$$

$$\Psi_{s\_\beta} = \int (V_{\beta} - R_s I_{s\_\beta}) dt \tag{4-20}$$

To avoid DC drift and initial value issues related with pure integrator, the flux estimator was implemented with common method to include Low Pass Filter (LPF) (4-21),(4-22).

$$\frac{d\Psi_{s\_\alpha}}{dt} = (V_{\propto} - R_s I_{s\_\propto}) - \frac{1}{T_{LPF}} \Psi_{s\_\alpha} , \tag{4-21}$$

$$\frac{d\Psi_{s\_\beta}}{dt} = (V_{\beta} - R_s I_{s\_\beta}) - \frac{1}{T_{LPF}} \Psi_{s\_\beta} \tag{4-22}$$

Estimated flux with Cartesian coordinates is also transformed into polar coordinates with CORDIC calculations so the flux amplitude and its angular position are found for its further motor regulation.

In the system presented the motor voltage vector is calculated from the switching combination applied to the inverter and the instantaneous amplitude of voltage sources as presented earlier in equations (4-6) and (4-7).

The stator current vector is computed from sampled phase current that later is transformed by Clark transformation into stator fixed coordinates system (4-23).

$$I_{s\_\propto} = \frac{2}{3}(i_a - \frac{1}{2}i_b - \frac{1}{2}i_c) \quad , \quad I_{s\_\beta} = \frac{1}{\sqrt{3}}(i_b - i_c) \tag{4-23}$$

Finally the electromagnetic torque is estimated from the product of stator flux and stator current which is given by equation (4-24).

$$T_e = \frac{3}{2}p_b(\Psi_{s_\alpha} I_{s_\propto} - \Psi_{s\_\beta} I_{s\_\beta}) \tag{4-24}$$

Since the SVM control algorithm operates with a fixed period of time (T) the DTC control has to be synchronized with its operations. To have accurate flux estimation the instantaneous stator voltage is integrated with SVM counter resolution (1μs) and from its accumulated value the average is used as a new flux value. Similarly, the instantaneous current value is averaged over the period of the SVM algorithm. The implementation of the torque and flux estimator in the FPGA program allows the synchronisation of its operations with the SVM and at the same time the removal of the load from real-time processor.

In the proposed system the rotor speed is not intended to be estimated but calculated from A, B, Z incremental encoder by FPGA with frequency of SVM (1kHz). The sole purpose of the rotor speed is to find the reference voltage for the UCs and to find the reference induction motor stator flux.

4.4 Power management with torque and flux regulation, and modulation strategy control

The power management control was implemented together with torque and flux regulation to provide limited output depending on the UC's state of charge and the maximum and minimum battery current. At the same time the supervisor estimates the available power and expected power share between sources; the latter is sent into the controller, which finds the best modulation strategy. Finally, the reference voltage vector from PI regulators together with selected switching method is outputted to the SVM controller so that the generated output voltage will provide the required torque and flux, and, at the same time, will meet the power distribution objectives. The block diagram of the control system is presented in Figure 4-8.

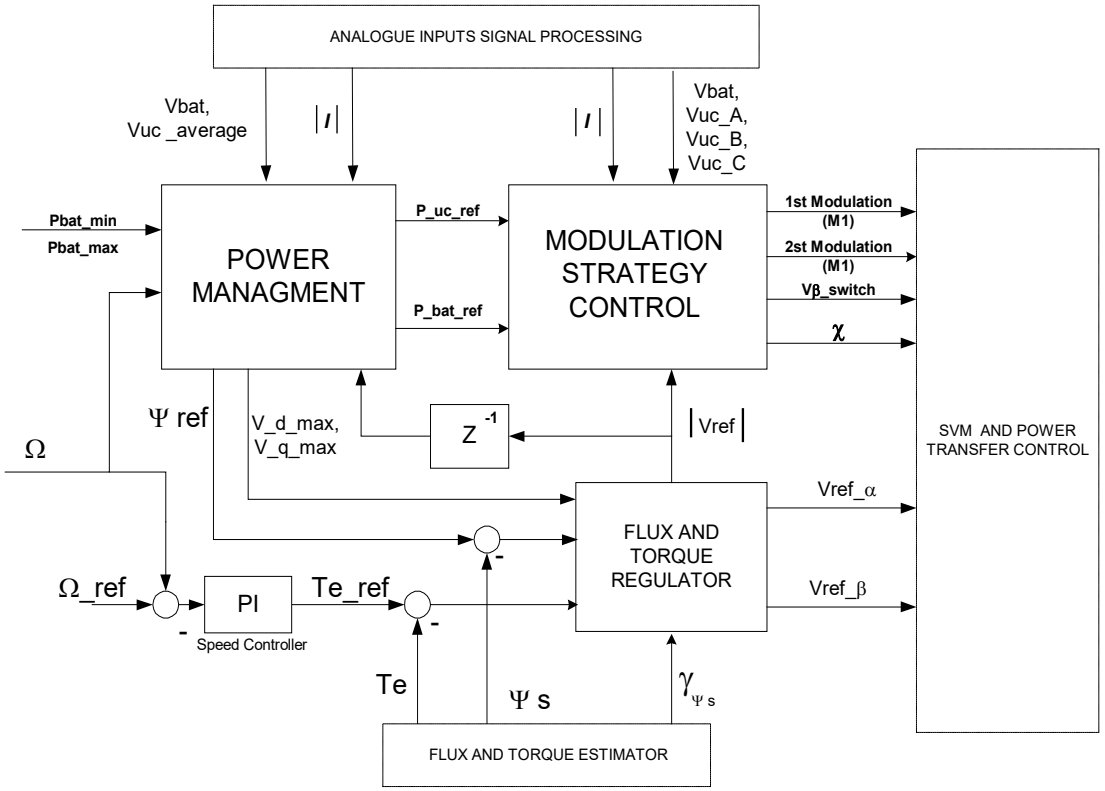


Figure 4-8 Block diagrams of interconnections between power management, flux and torque regulator and modulation controller

Since the processes related to power management, such us the amplitude of the voltage sources, the motor speed and the current, change relatively slowly their control can be implemented with lower priority and at lower frequency. It is also desirable for the new reference for the UC's voltage and power sharing to be calculated only once per 1/6 of fundamental frequency to minimise the effect of voltage variation during switching. For modulation control and flux-torque regulator it is necessary to schedule the program to operate with duty cycle equal to the SVM period.

The aim of the flux and torque regulator is to find the error between their actual and set values and to produce the voltage vector necessary to minimise the difference between them. In the proposed flux and torque regulation scheme the reference values are compared with the estimated values as described in DTC control. The torque and flux are further regulated by PI controllers, and their output is limited by the power management block according to the available voltage as presented in paragraph 993.4. Finally, the reference

voltage is converted from d-q coordinate system synchronous with stator flux into stationary coordinate's α-β (Figure 4-9). The Park transformation takes into account reference in rotary reference frame (V_{ref_d} and V_{ref_q}) and flux angular position (γ_Ψ) (4-25), (4-26). For the purposes of other control the amplitude reference voltage vector is also calculated.

$$V_{ref\_\propto} = V_{ref\_d} \cdot \cos(\gamma_\Psi) - V_{ref\_q} \cdot \sin(\gamma_\Psi) \quad (4\text{-}25)$$

$$V_{ref\_\beta} = V_{ref\_d} \cdot \sin(\gamma_\Psi) + V_{ref\_q} \cdot \cos(\gamma_\Psi) \quad (4\text{-}26)$$

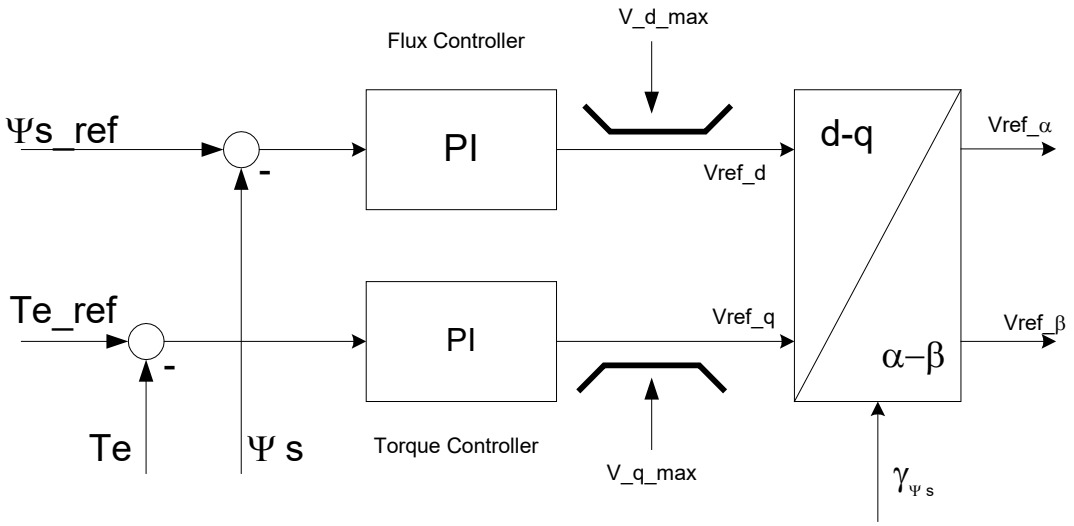


Figure 4-9 Torque and flux regulation to generate reference voltage in stationary coordinates

Power management is achieved through the control algorithm presented in paragraph 3.6.3. (Figure 3-63). The calculation of the reference power for the UCs and battery are set as a low-priority task, which it is not necessary to control with the calculation frequency of the motor drive. Since the reference voltage vector is limited by the power-management block, the value generated in the previous cycle is used. The stator flux reference is set at a constant value. Nevertheless, as presented in section 2.4 , this could be controlled in relation with the available voltage and power. Flux control and weakening were not implemented due to the limitations of the work and the limited processing power of the selected platform.

The reference power sharing between the sources and the reference voltage vector are outputted into the modulation strategy control block, which selects the appropriate switching configuration. The output from the power management module to the vector modulator includes the voltage reference in the α-β plane (V_{ref_α}, V_{ref_β}), two selected switching modes (S. MODE1 and S. MODE2), the phase shift angle (χ) and switch angle (V_{β_switch}) for modulation mode change. Since it is desirable to use the smallest vectors to minimise switching losses and distortions in the output voltage, the modulation that uses H-Bridges in SVM is always prioritized (MODE II and/or MODE III).

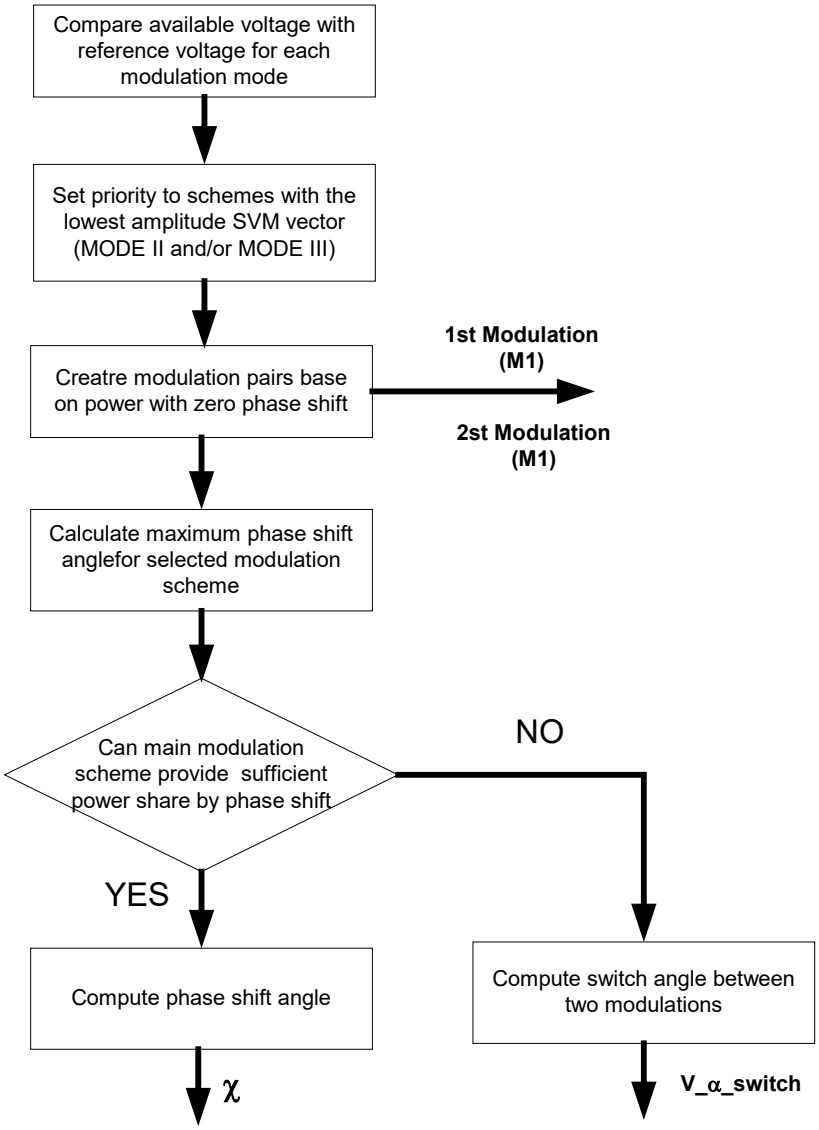


Figure 4-10 Structure of algorithm to find best modulation strategy and its control angles

The logic to find the appropriate modulation strategy within the inverter limits is based on the following steps summarized in Figure 4-10:

As a first step in selecting the correct modulation strategy the new reference voltage vector is compared with the maximum voltages that can be generated by each modulation scheme. Based on Table 3-1 five maximum voltage levels can be distinguished: one minimum for the six-step modulation of the three-phase bridge and two minimum for H-Bridges in six-step mode with 180˚ phase shift (Figure 4-11). Those switching modes that are not able to provide sufficient output voltage become inhibited and are not used for further calculations. The modulation schemes are also sorted into an order that first uses those where the voltage source with the smallest amplitude is used for SVM (MODE II and MODE III). The complete method to identify available modulation combinations was presented in Chapter 3 (Figure 3-37)

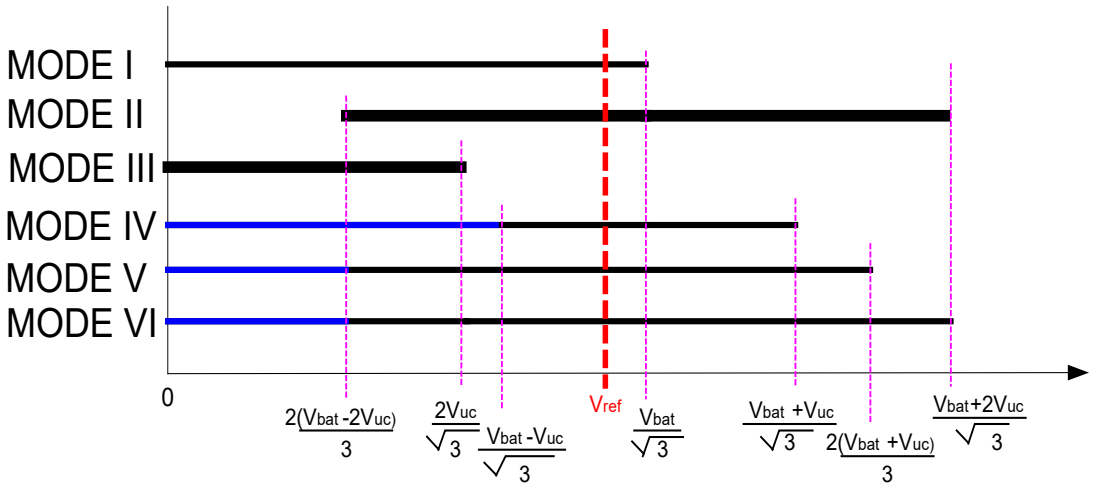


Figure 4-11 Modulation method selection based on available voltages

2. In the second step for the modulation strategies that meet earlier voltage requirement the active power delivered by the sources is calculated for the actual power factor and the zero phase shift according to Table 4-1. The calculations allow the identification of modulation schemes that could deliver reference power share between sources by phase shift control or by mixed modulation in combination with second modulation scheme.

Table 4-1 Estimation of active power delivered for six main modulation modes

Modulation strategy	Power distribution between sources
MODE I	$P = P_{bat}$
MODE II	$P_{bat} = \frac{3}{\pi} V_{bat} \cdot I \cdot \cos(\emptyset)$
MODE III	$P = P_{UC}$
MODE IV	$P_{UC} = \frac{3}{\pi} V_{UC\_avg} \cdot I \cdot \cos(\emptyset)$
MODE V	$P_{UC} = \frac{2\sqrt{3}}{\pi} V_{UC\_avg} \cdot I \cdot \cos(\emptyset)$
MODE VI	$P_{UC} = \frac{6}{\pi} V_{UC\_avg} \cdot I \cdot \cos(\emptyset)$

Next, if the second modulation strategy (MODE II) is selected, it is verified if the modulation strategy can be used through whole sectors without mixing with additional modulation methods. In section 3.6 it was presented that for a reference voltage higher than the battery voltage divided by the square root of three ($V_{ref} > 1/\sqrt{3}\ V_{bat}$) the UC's voltage has to be higher than: $2/\sqrt{3}\ V_{UC} > V_{ref}/2$. Where the reference voltage is lower the following relation has to be met $(V_{bat} 2V_{UC})/\sqrt{3} < V_{ref}/2$.

The limiting phase shift angles for the selected modulation schemes with priority for MODEII are calculated. This also allows verification of whether the modulation scheme can be used by itself or must be combined with a second type of modulation. It also allows the finding of limits for phase shift control. The calculations are simplified to use only trigonometric relations between the reference voltage vector and the amplitude of the voltage source from the equations presented in Table 3-1.

The control limits are used further to select only those two modulation schemes that are able to provide the requested reference power. When the phase shift power control is selected the second modulation mode is still chosen to

generate sufficient output voltage in case the first one is not able to provide a set voltage when the source's amplitude has large variations.

3. Based on reference power for main or auxiliary inverter the control angles are calculated from the equations presented in paragraph 3.5. To limit the number of computations required only the control angle for phase shift regulation or mixed modulation is calculated depending on which power-sharing control method has been selected.

The structure of the modulation control block is presented in Figure 4-12.

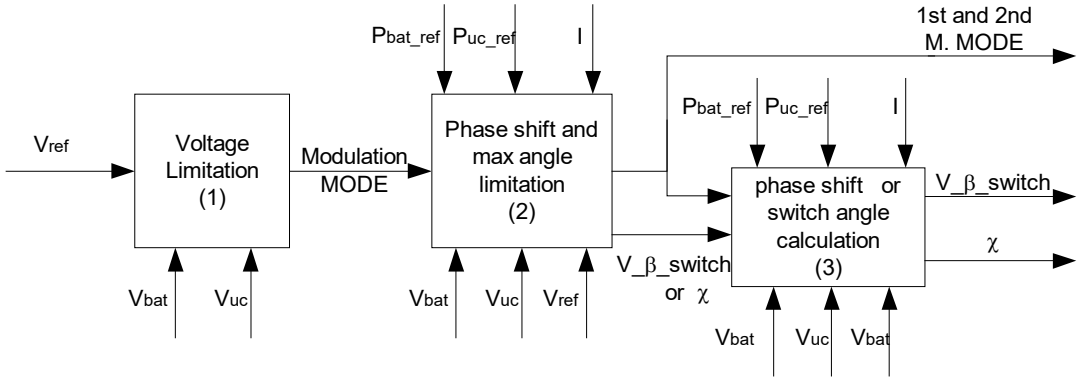


Figure 4-12 Selection of modulation method based on available voltage and reference voltage and power

4.5 Summary

This chapter has shown that based on the inverter analysis in Chapter 3 it is possible to formulate a control strategy to meet the objectives of the proposed system. Presented control is combining a new modulation method that allows delivering requested torque to motor and at the same time to adjust power sharing ratio between the sources. The voltage modulating unit provides ability to select one of the six modulation modes and to switch between them at set voltage vector angle. Also the modulation module has a function to introduce phase delay or advance for inverter section that is switched at the fundamental frequency. The modulation mode is supervised by a control block that identify modulation strategy base on demanded voltage with parameters that meet power requirements and at the same time provide lowest ripples in output

voltage. Due to the algorithm complexity, the developed method has been placed in a hierarchical arrangement depending on the required processing speed. The power management supervision was set as a long term process to identify strategy for power distribution and to assure that drive operate within limits. By implementing the following structure of control algorithm it has been shown to be possible to simplify the amount of calculations required to meet the system targets. The control algorithm has been designed with the intention of using real-time platform with FPGA. Based on this specification National instrument platform cRIO-9112 with FPGA (Virtex-5 LX30) operating at 40MHz and real-time processing unit with 500MHz clock has been selected. The examples of implemented Labview program are placed in Appendix A. Splitting algorithm into tasks depending on their time domain allowed processing complicated calculations and at the same time achieving high speed control of inverter output. Based on system architecture it becomes possible to have system response within a single SVM dusty cycle what for selected platform is equal to 1ms.

CHAPTER 5 NUMERICAL SIMULATION OF MULTILEVEL AND MULTISOURCE SYSTEM

In this chapter a Matlab/Simulink simulation model of the proposed multilevel multisource system with power distribution control is presented with brief overview of designed structure. The aim of the simulations is to validate control algorithm that was given in Chapter 4 and to find performance of the system before its physical implementation. Later in this chapter the simulations results for modulation strategies are given and discussed.

5.1 Design of simulation model

The control method that was derived in previous chapters presents a new solution for a multisource multilevel motor drive with high level of complexity. Since the system requires a hardware and software development it was proposed to validate the concept of motor drive first by the numerical computations in Matlab\Simulink software. It was decided to focus on control algorithm to help define software structure and assure that the proposed solution provide expected results. Implemented system consists of a full model of introduced structure including multilevel inverter with multiple sources, induction motor and complete control that was presented in Chapter 4. The main focus of performed analysis was to validate behaviour of defined earlier logic as well to quantify performance of introduced modulation modes in term of its harmonic content. The overview of build model is presented in Figure 5-1 where we can distinguish the main elements such as a three-phase induction motor, modular multilevel inverter (blue block), DTC control to estimate motor reference voltage (purple block), space vector modulation module for vector selection (yellow block) and power share control (grey block).

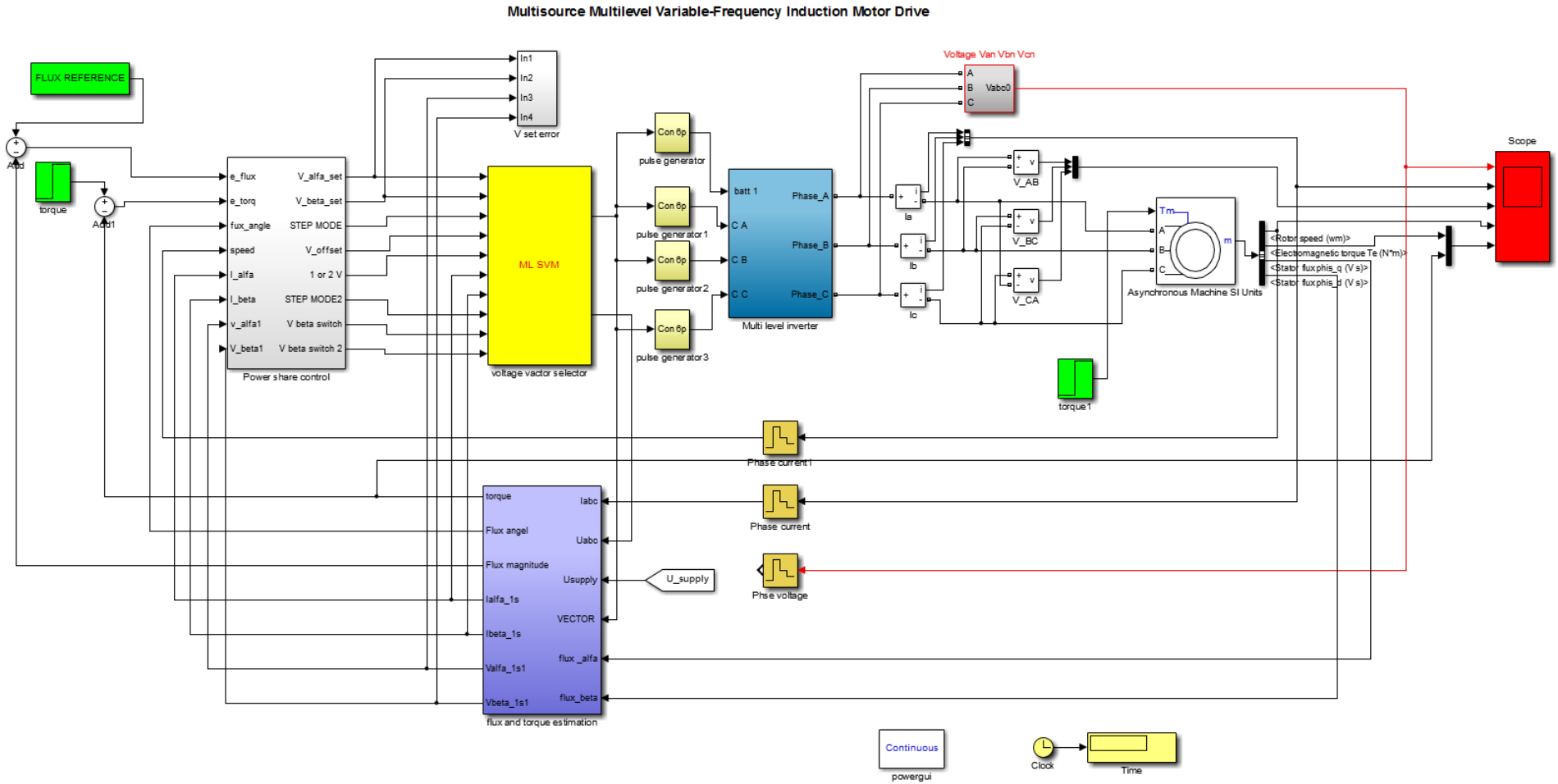


Figure 5-1 Matlab/Simulink model of proposed system

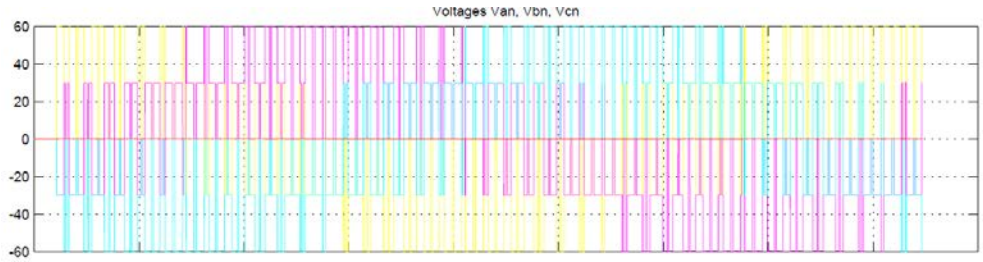
The induction motor used in simulation is based on asynchronous machine model from Matlab\Simulink SimPowerSystems machine library. The motor mode of operation is dictated by the sign of the mechanical torque (positive for motoring, negative for generating). The electrical part of the machine is represented by a fourth-order state-space model and the mechanical part by a second-order system. All electrical variables and parameters are referred to the stator. All stator and rotor quantities are in the arbitrary two-axis reference frame (dq frame). In this model saturation and core losses effects are neglected (MATLAB , 2012). The physical machine has been set as a squirrel cage motor with 5kW of output power, 400V nominal voltage and single pole pair. The inverter used in simulations is the modified cascade with three-phase bridge and three H-Bridges as presented in Chapter 3. The model of VSI is based on universal bridge with MOSFET power electronic elements close to ideal power electronic devices. The main source for multilevel inverter is modelled as an ideal DC voltage sources and UCs are modelled as ideal capacitors with series resistance. The remaining elements of the control system were designed according to the strategy presented in Chapter 4 with the same hierarchical structure. The schematics of mention block diagrams are presented in Appendix B. The long term and medium shell is clocked at 1 kHz and the resolution of Space Vector Modulator is 1us, similarly as a clock available in hardware platform. The simulations are run in most cases with variable step and relative tolerance of 1e^-3. The main aim of performed simulations was to verify the control system under various modulation strategies.

5.2 Simulation results

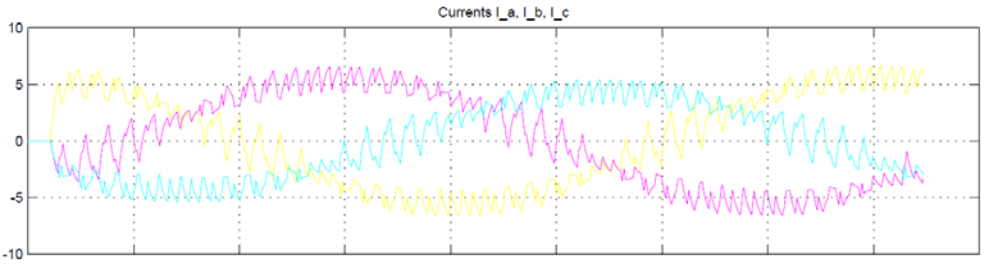
5.2.1 Modulation with three- phase bridge only (MODE I)

In the first stage of model validation the inverter operations with configuration where the inverter operates as a standard three-phase bridge supplied by a constant voltage source were simulated. The supply voltage was set as 90V and the reference output voltage vector was set at a fixed frequency of 25Hz with fixed voltage at 45V. The aim of this test was to validate that the model is

configured properly and to have starting point for future performance comparison.



(a) Phase voltage at inverter output



(b) Phase current at inverter output

(c) Phase to phase voltage at inverter output

Figure 5-2 Inverter output voltages and currents in MODE I where only three-phase bridge operates (yellow - phase A, purple – phase B and blue – phase C)

Figure 5-2 shows the output voltages and currents delivered to the load by structure with multilevel inverter where only three-phase bridge is operating. From presented curves it can be learned that current from inverter is sinusoidal but it include a high ripples especially when voltage change its polarity and a small amplitude of voltage is needed. From voltage waveforms it is noticeable that the voltage vector is correctly modulated with symmetrical zero voltage placement (two pulses with same duty next to each other). In Figure 5-3 the voltage vector trajectory is presented in complex plane for one period. It can be

found that there are all six active and one zero vector used and that switching transition occurs only for the adjacent vectors.

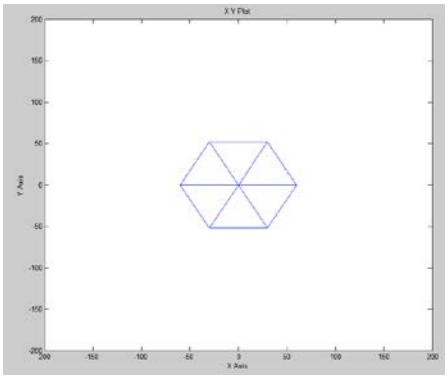
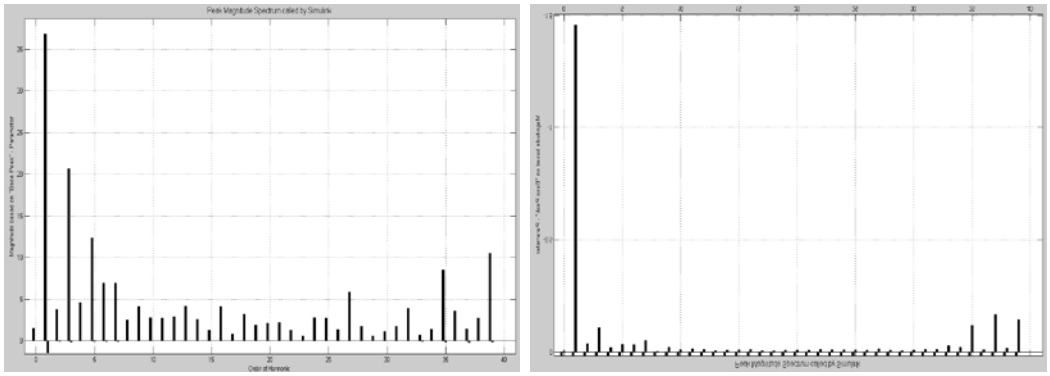


Figure 5-3 Voltage vector trajectory on complex plane for MODE I modulation

The THD for above presented phase voltage was calculated as 68.5% and for the phase current the factor was equal to 14.3% what is very similar to expected results for two level SVM as found in literature (Gupta and Kumar, 2012), (Holmes, 2003). As presented in Figure 5-4 the harmonics in voltage as well in current contain 3rd and 5th order frequency but in current the majority of peaks is related with modulation frequency around 35th and 39th harmonics.



(a) Harmonic content in voltage (b) Harmonic content in current

Figure 5-4 Harmonic content in voltage and current for MODE I modulation

The whole output power in this operating mode is delivered by main voltage source (battery) as shown in Figure 5-5. Since the inverter section is switching constantly between zero and full current the supply current include high ripples but thanks to implemented LC filter the source supply current become averaged and remain almost constant with smaller peak values.

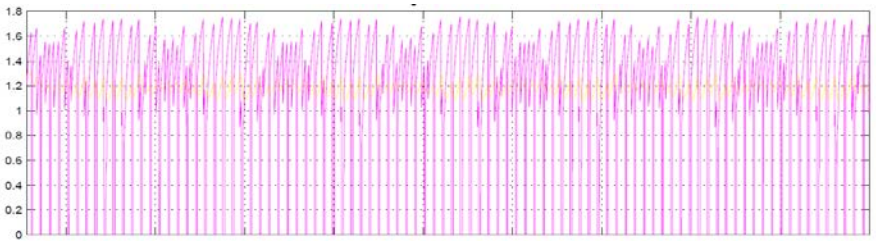
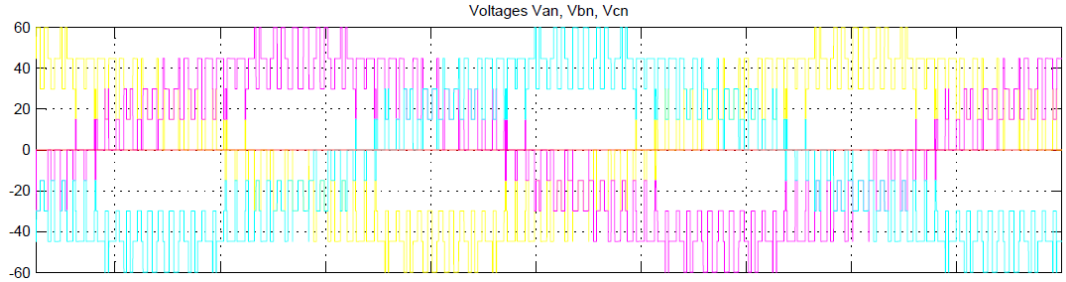


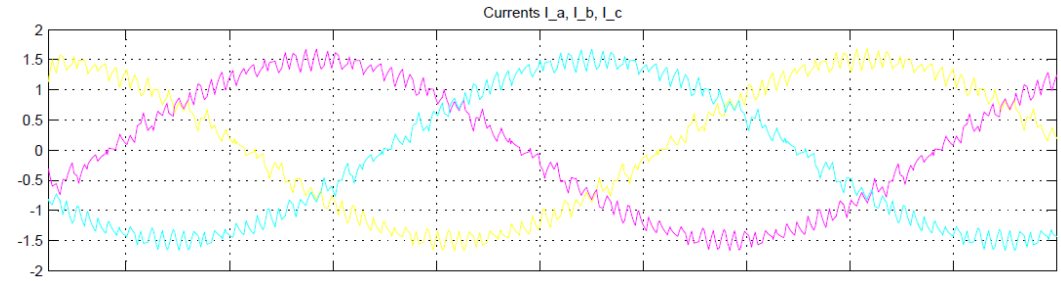
Figure 5-5 Current sourced by main source, purple current before LC filter, yellow at source output after LC filter

5.2.2 Modulation with three H-Bridges only (MODE III)

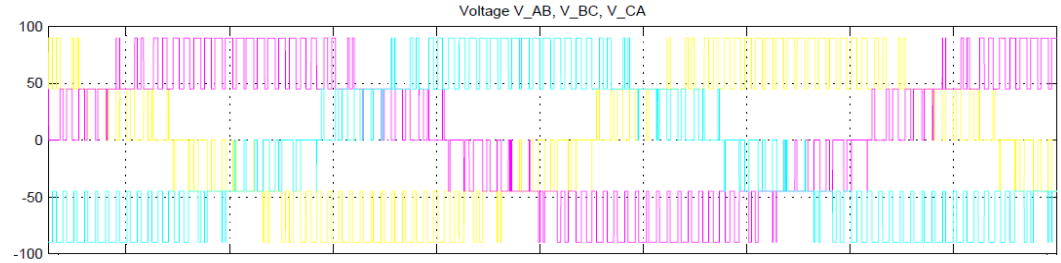
In the next step the modulation mode where only H-Bridge section operates was tested to verify three level modulation with UCs as a voltage source.



(a) Phase voltage at inverter output



(b) Phase current at inverter output



(c) Phase to phase voltage at inverter output

Figure 5-6 Inverter output voltages and currents in MODE II where only three H-Bridge operates (yellow - phase A, purple – phase B and blue – phase C)

In this configuration each UC was charged at initial 45V and the reference output voltage vector was modulated to 45V set point and at 25Hz frequency, same value as in previous case. In Figure 5-6 we can notice that by using multiple sources with amplitude equal half of the voltage than in previous case the current ripples can be significantly reduced. The output voltage includes now additional levels making output voltage looking more similar to sinusoid.

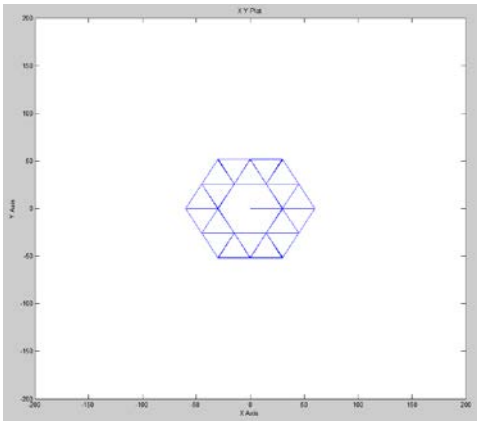
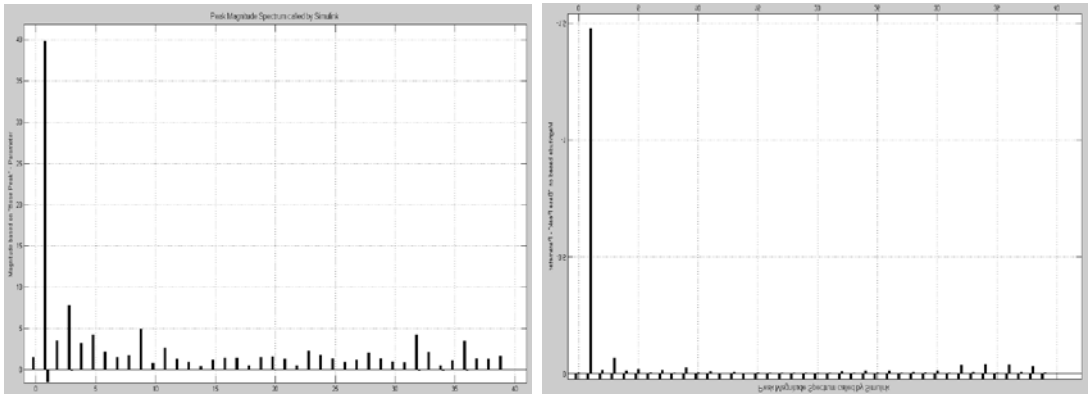


Figure 5-7 Voltage vector trajectory on complex plane in MODE III

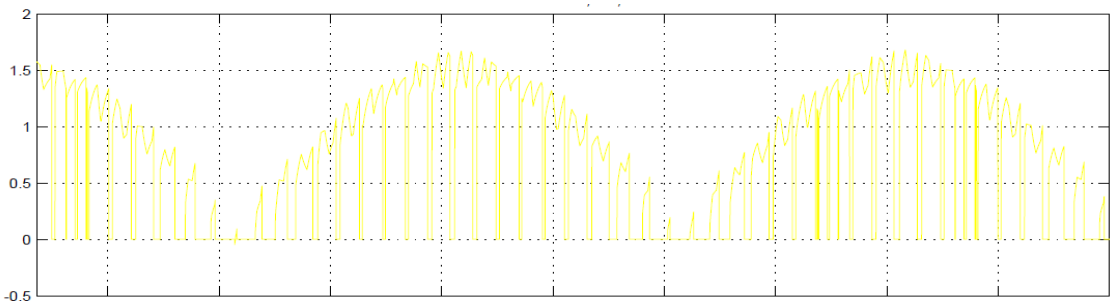
The Figure 5-7 shows that implemented algorithm for the cascade H-Bridge SVM minimise switching transitions and modulate output voltage only by the closest vectors. Correct switching with voltage vectors that have amplitude equal to the half of the main source amplitude allowed to reduce THD almost by 50%. The harmonic content in case of phase voltage was reduced down to 35.5% and current THD was reduced to 7.9% what is expected when number of levels increase from two to three (Qashqai, Sheikholeslami and Vahedi, 2016).



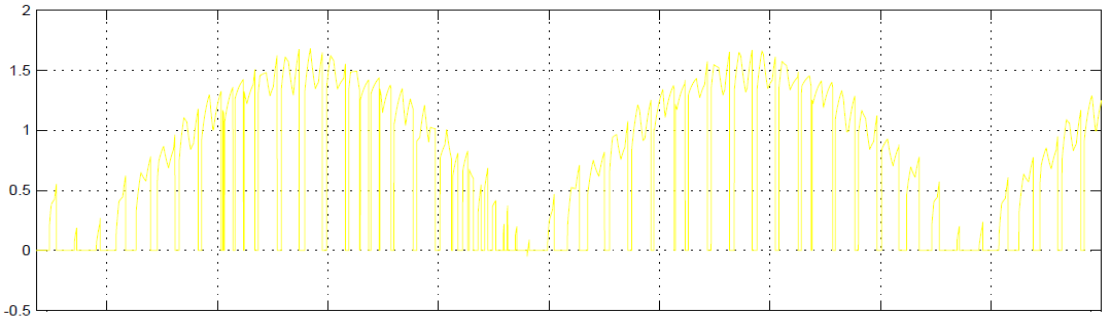
(a) Harmonic content in voltage (b) Harmonic content in current

Figure 5-8 Harmonic content in voltage and current for MODE III modulation

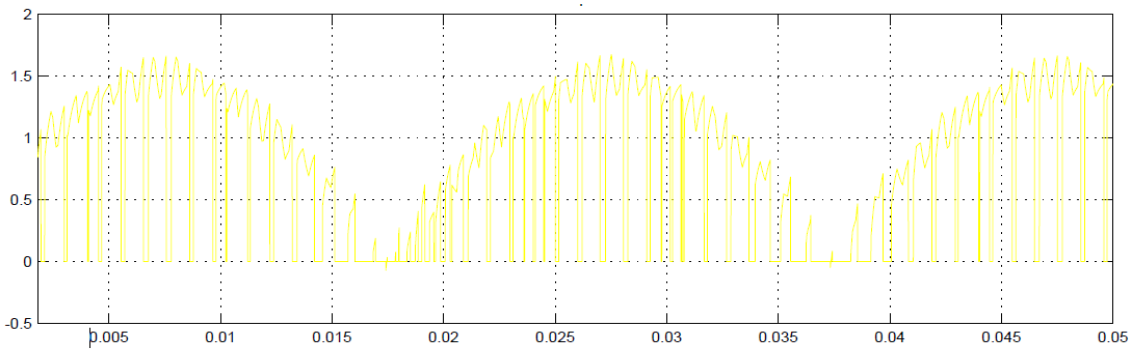
Presented harmonics spectrum (Figure 5-8) shows that all frequencies other than the fundamental frequency have much smaller amplitude especially 3rd and 5th harmonic become reduced. In MODE III modulation the whole output power is delivered by the UCs. From presented UCs current graphs in Figure 5-9 it is noticeable that the current delivered by each UC is almost same but phase shifted by $2/3\pi$ what allows to provide an equal power distribution between sources.



(a) Current sourced by UC in phase A



(b) Current sourced by UC in phase B

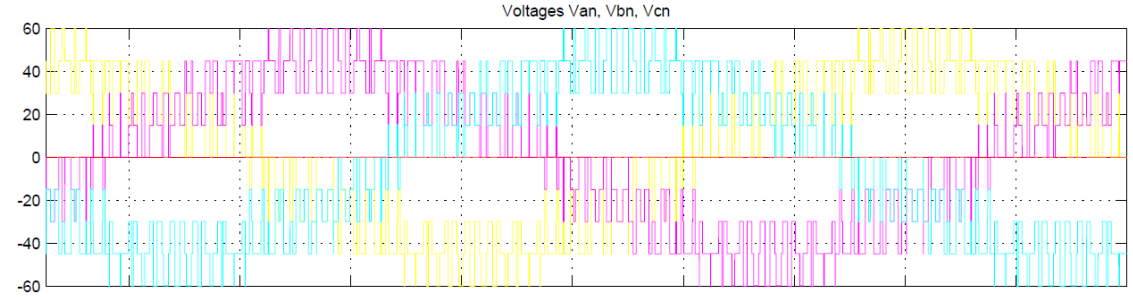


(c) Current sourced by UC in phase C

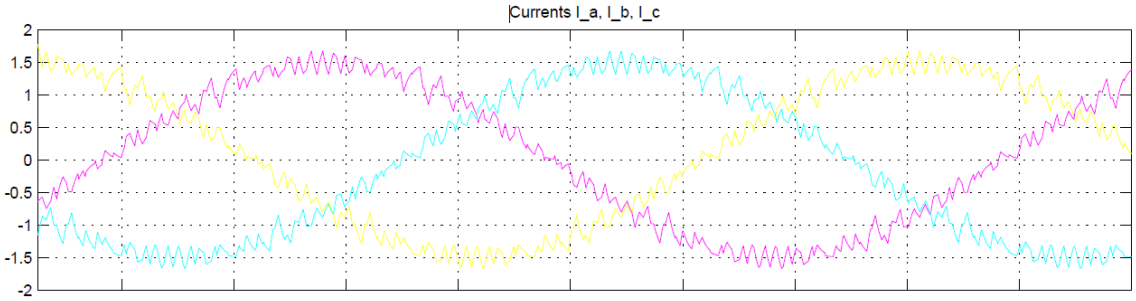
Figure 5-9 Current sourced by H-Bridges supplied from UCs

5.2.3 Modulation with three-phase bridge switched at fundamental frequency and three H-Bridges in SVM (MODE II)

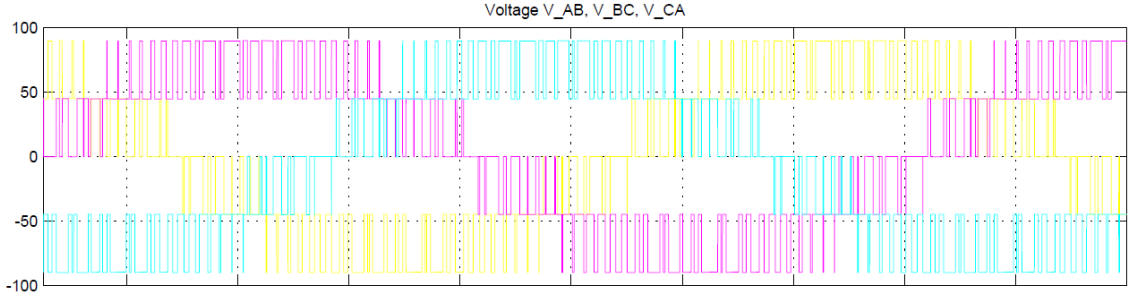
By combining operation of the three-phase bridge together with the H-Bridges it is possible to distribute power between inverter sources and also to achieve higher output voltage. In previous chapter it was mentioned that the modulation with a three-phase bridge switched at fundamental frequency is able to provide low harmonic content and at the same time allows a good power distribution between the sources. To allow comparison of this modulation method the simulations for the same reference output voltage vector were performed. In Figure 5-10 an example voltage and current waveforms are presented.



(a) Phase voltage at inverter output



(b) Phase current at inverter output



(c) Phase to phase voltage at inverter output

Figure 5-10 Inverter output voltages and currents for MODE II modulation (yellow - phase A, purple – phase B and blue – phase C)

In presented case the voltage ratio between the voltage sources was set as 2:, where the UCs voltage is equal to 45V and the battery voltage is equal to 90V. The results that were achieved are very similar to discussed earlier modulation in MODE III. Nevertheless it is possible to notice that the phase current include slightly more ripples. As presented in Figure 5-11 the voltage vector step is same as for the case where modulation with H-Bridge only was used. Also during vector transitions only the closest vectors are selected but since in this modulation mode there is transition between large voltage vectors then on those events the higher voltage ripples appear.

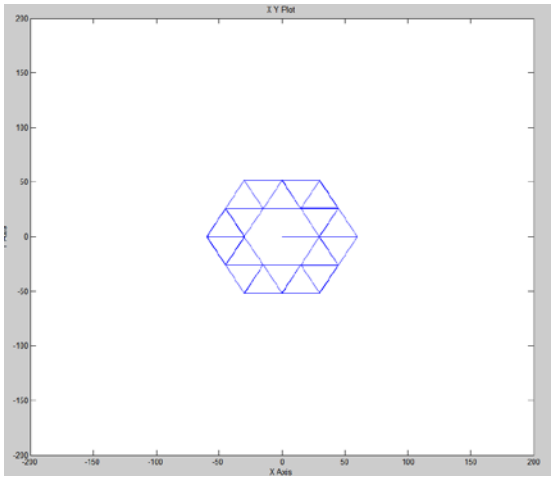
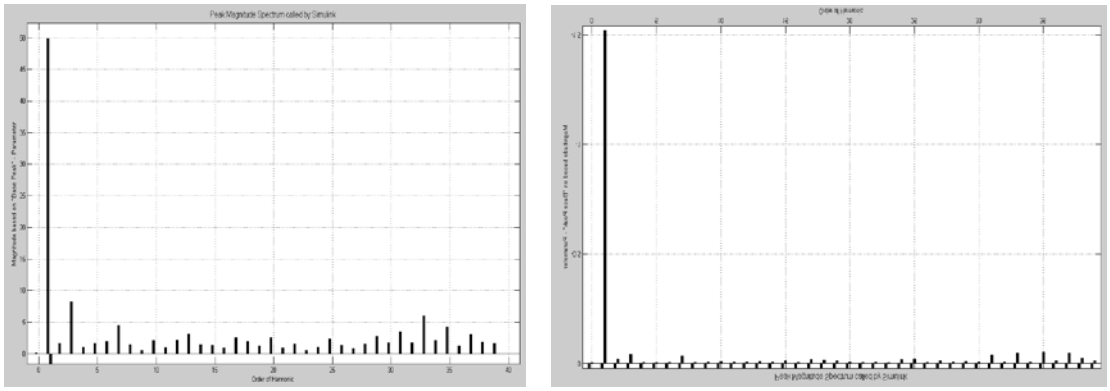


Figure 5-11 Voltage vector trajectory on complex plane in MODE II

Calculated THD for presented waveforms proved that the total distortion in either voltage or current have a very low value and is only marginally higher in comparison to MODE III modulation. In case of the phase voltage the THD value increased only by 0.2% to 35.7% and in the phase current the THD become higher by 0.5% reaching 8.3%. The harmonic spectrum also remains almost unchanged with only marginal increase of harmonics related with the modulation frequency as presented in Figure 5-12.



(a) Harmonic content in voltage (b) Harmonic content in current

Figure 5-12 Harmonic content in voltage and current for MODE II modulation

The main advantage of this modulation mode is that the power is shared between all voltage sources and power ratio depends on reference voltage and control angles. For presented case where the voltage amplitude from a three-phase bridge switched in six step mode is higher than the reference output voltage then the active power will flow from the main source to the load and also to the UCs. Figure 5-13 presents instantaneous power delivered by each voltage source where it is noticeable that maximum power (yellow trace) is provided by the main source and within the UCs power is oscillating and the total UCs power is negative (green trace).

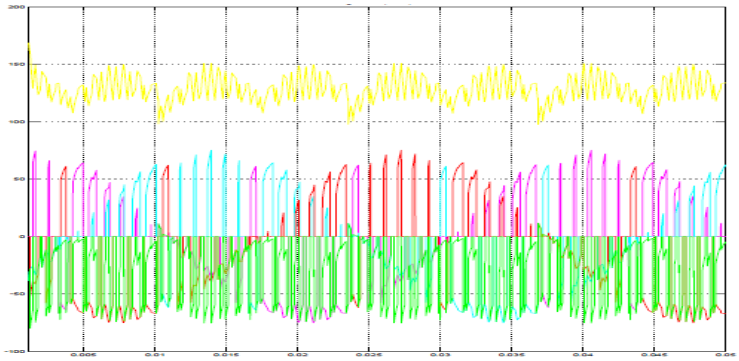
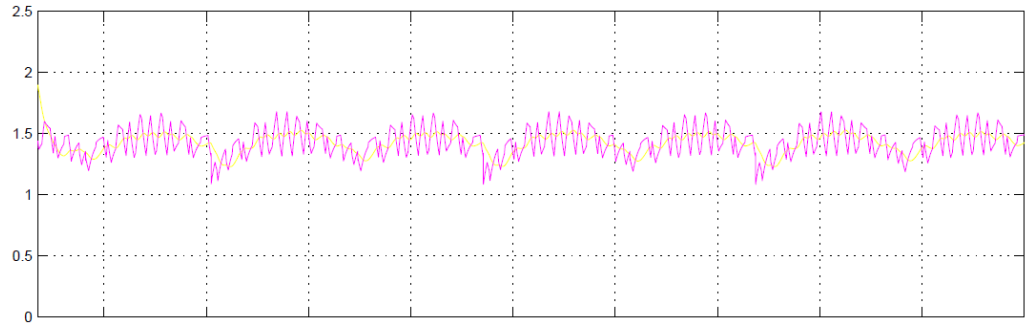


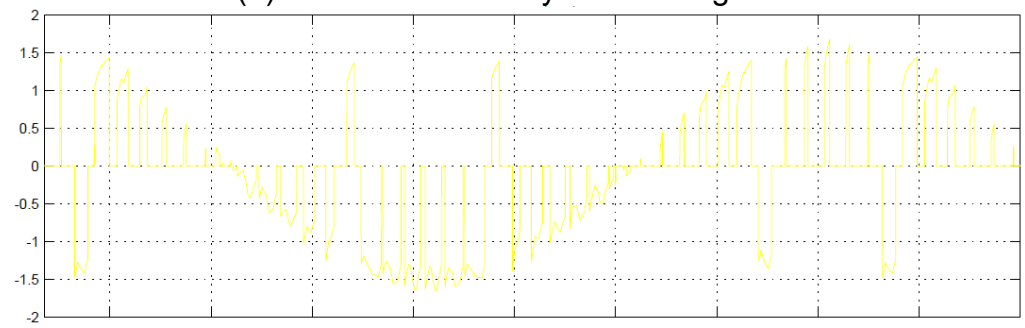
Figure 5-13 Instantaneous power delivered by sources, yellow – main voltage source, blue – UC in phase A, red – UC in phase B, purple – UC in phase C and green – total power delivered by H-Bridges

To better illustrate power flow between the sources, in Figure 5-14 the currents that flow to and from sources are illustrated. It is visible that the main source delivers almost constant current when all three phase UCs sink and source

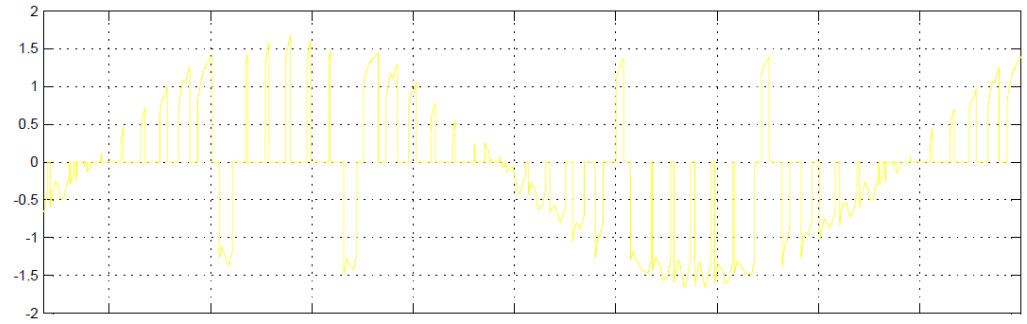
current. Since the duty of the current pulses that are flowing from UCs (positive current) are shorter than the ones with the negative sign the total active power delivered by UCs will remain negative.



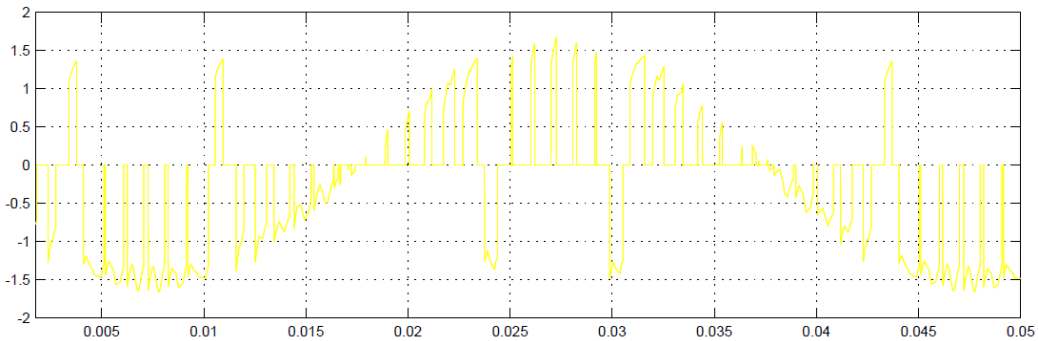
(a) Current sourced by main voltage source



(b) Current sourced by UC in phase A



(c) Current sourced by UC in phase B

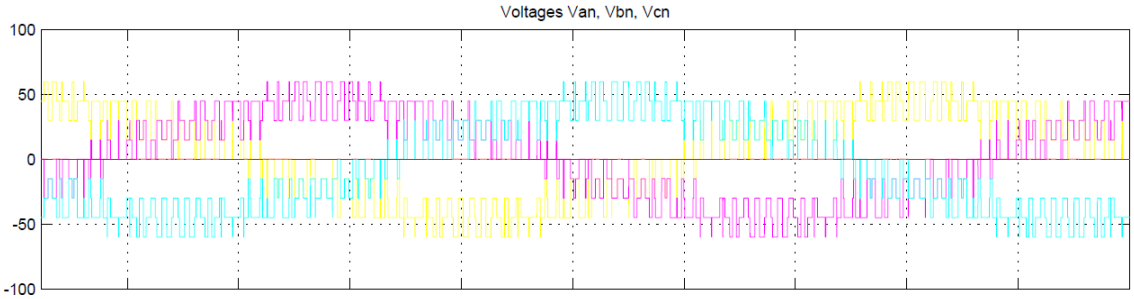


(d) Current sourced by UC in phase C

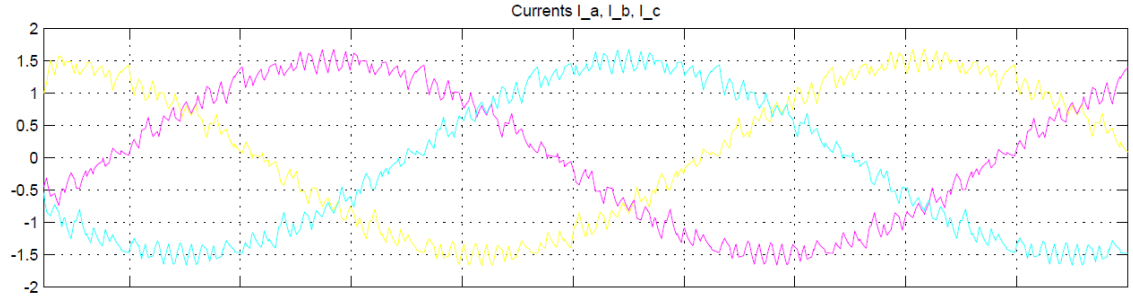
Figure 5-14 Currents delivered by each voltage source in MODE II modulation

5.2.4 Mixed Modulation method with switching between MODE II and MODE III

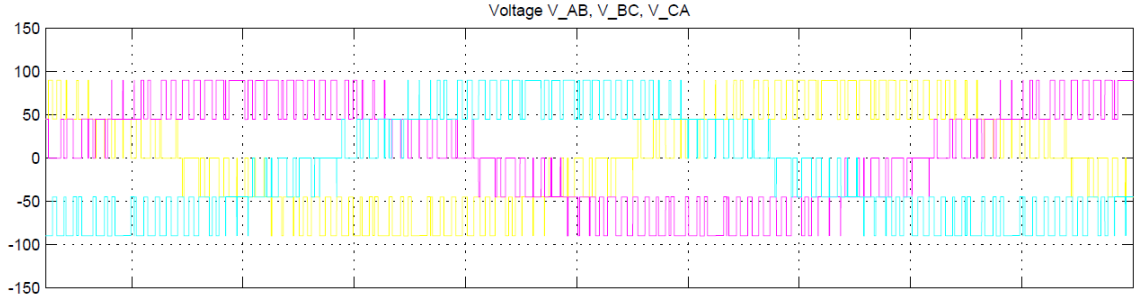
For presented earlier modulation methods where the sources were supplied with 2:1 voltage ratio and the reference output voltage from inverter was lower than the main voltage source, then the power sharing between sources was not well distributed and either whole power was delivered by the UCs or by the main voltage source. The solution to this problem can be accomplished by alternating between those two modulation methods so the power between the sources will be distributed according to control angle. In Figure 5-15 an example voltage and current waveforms are presented for the method where modulation is changed between MODE II and MODE III.



(a) Phase voltage at inverter output



(b) Phase current at inverter output



(c) Phase to phase voltage at inverter output

Figure 5-15 Inverter output voltages and currents for mixed modulation between MODE II and MODE III (yellow- phase A, purple – phase B and blue – phase C)

The voltage and current appear to be not affected by the alternating between modulations and the waveform shape is almost identical to previous cases where individual modes were used. Also transitions between the vectors coordinates appear to be similar and always the closest voltage vectors are used.

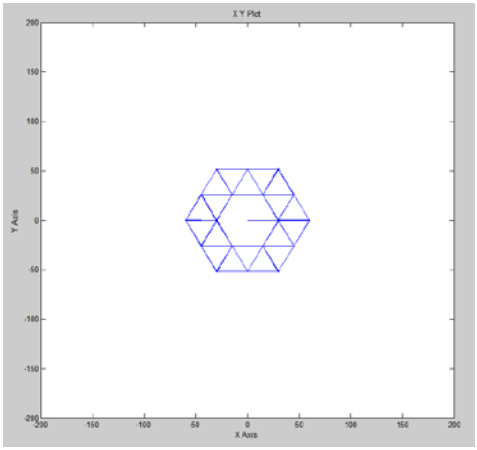
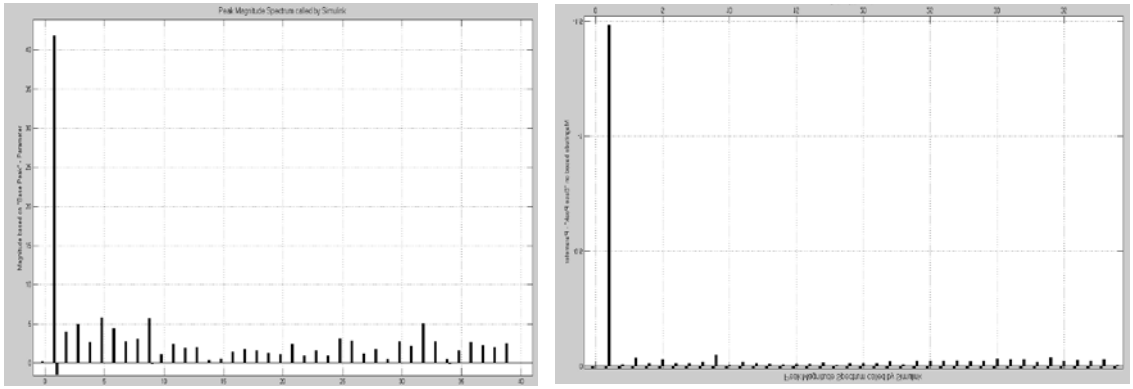


Figure 5-16 Voltage vector trajectory on complex plane for mixed MODE II and MODE III modulation

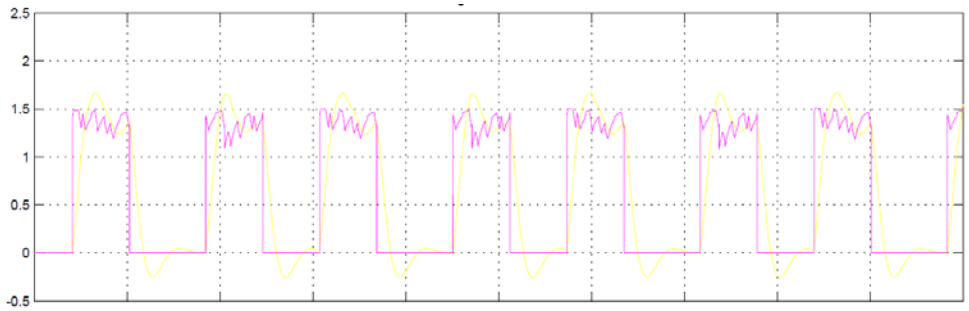
The percentages of unwanted harmonics become the average value of two cases achieving 35.7% THD for phase voltage and 7.9% for phase current. Presented in Figure 5-17 harmonic spectrums prove that introduced method to switch between the modulations will not create increase in the amplitude for any of unwanted harmonics.



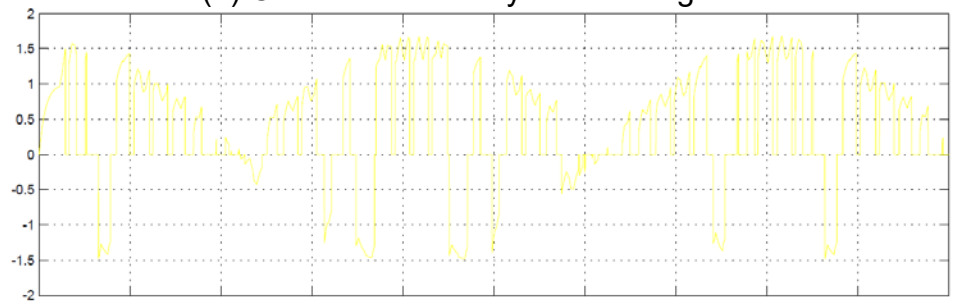
(a) Harmonic content in voltage (b) Harmonic content in current

Figure 5-17 Harmonic content in voltage and current for mixed modulation mode (MODE II and MODE III)

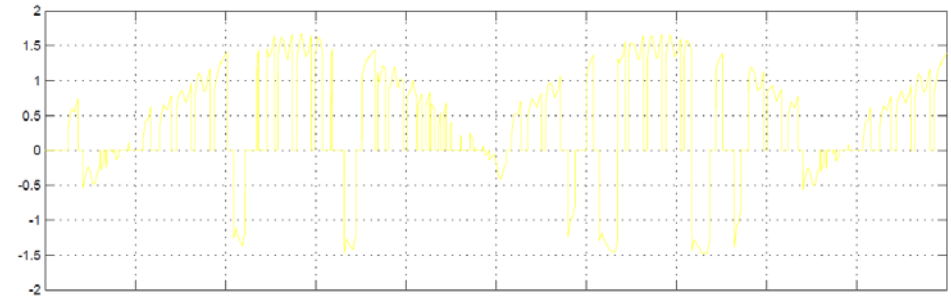
The main difference in the proposed strategy to alternate between modulation modes is that the amount of current delivered by each source can be controlled by the angle where modulation mode is switched, so the active power distribution between sources can be changed.



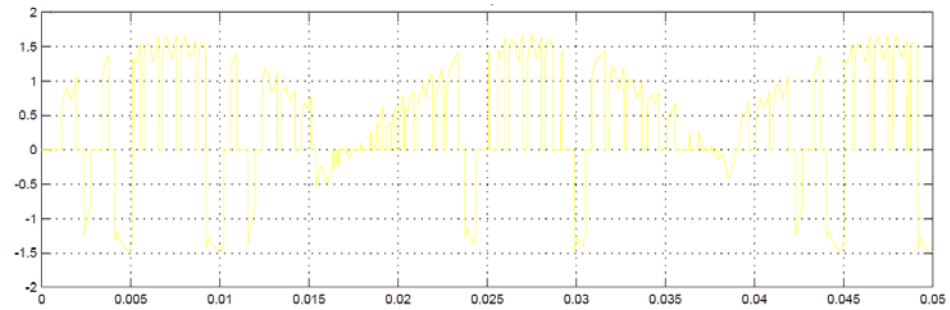
(a) Current sourced by main voltage source



(b) Current sourced by UC in phase A



(c) Current sourced by UC in phase B



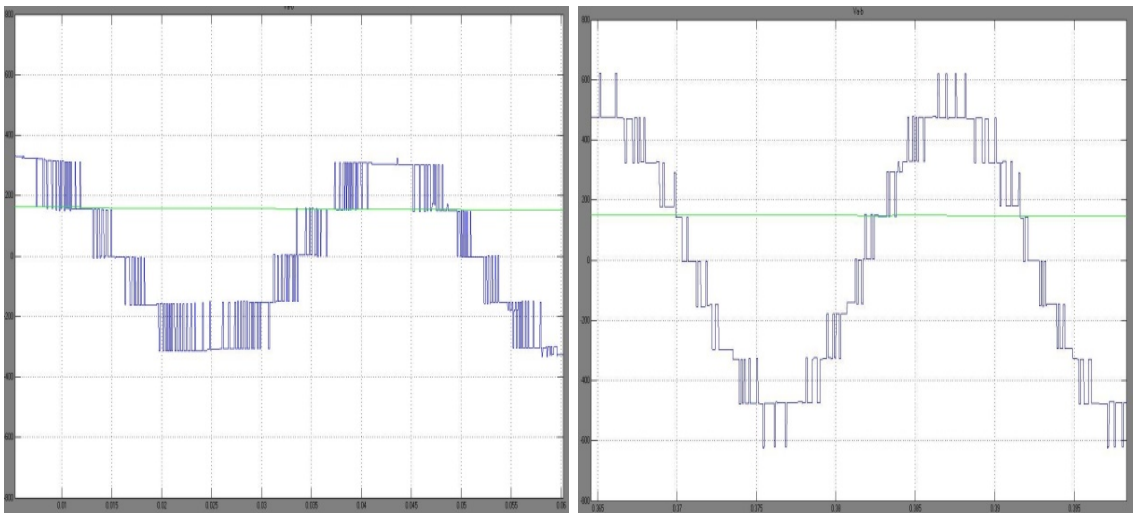
(d) Current sourced by UC in phase C

Figure 5-18 Currents delivered by each voltage source

Presented example in Figure 5-18 shows that for the same reference voltage vector and load power as in earlier examples the average current delivered by main source become smaller when UCs current became almost entirely positive. This means that the active power that is provided to the load is shared almost equally between the sources.

5.2.5 Motor drive acceleration

The final test that was performed aimed to validate how presented simulation model behave during transients. For this reason the system was set to accelerate from zero speed up to the motor nominal frequency (50Hz). In tested case the UCs were charged to the maximum value and during motor operation their voltage and current was closely monitored The results show that the proposed configuration adapts to the changing battery/UC voltage ratio and is able to modulate the required current and voltage in the entire speed range by using modulation strategies described earlier. It was also proven that the multilevel inverter provides much lower ripples and total harmonic distortions in comparison to the conventional two level inverter. Additionally available inverter maximum output voltage without using additional passive components was increased when both inverter sections operate together what is especially visible at motor maximum speed.



(a) At low speed (b) At high speed

Figure 5-19 Voltage between phases “A” and “B” during acceleration

In Figure 5-19 the voltage between two phases at two different speeds has been recorded. From graphs we can find that the control algorithm at the lower-speed to construct required voltage waveform needed four voltage levels, when at higher speed the output voltage has eight different voltage levels.

The next Figure 5-20 shows the voltage waveform during complete motor acceleration. It is noted that with increasing of motor speed the number of voltage levels also increases. Despite the UC's falling voltage, the control algorithm is able to provide stable output.

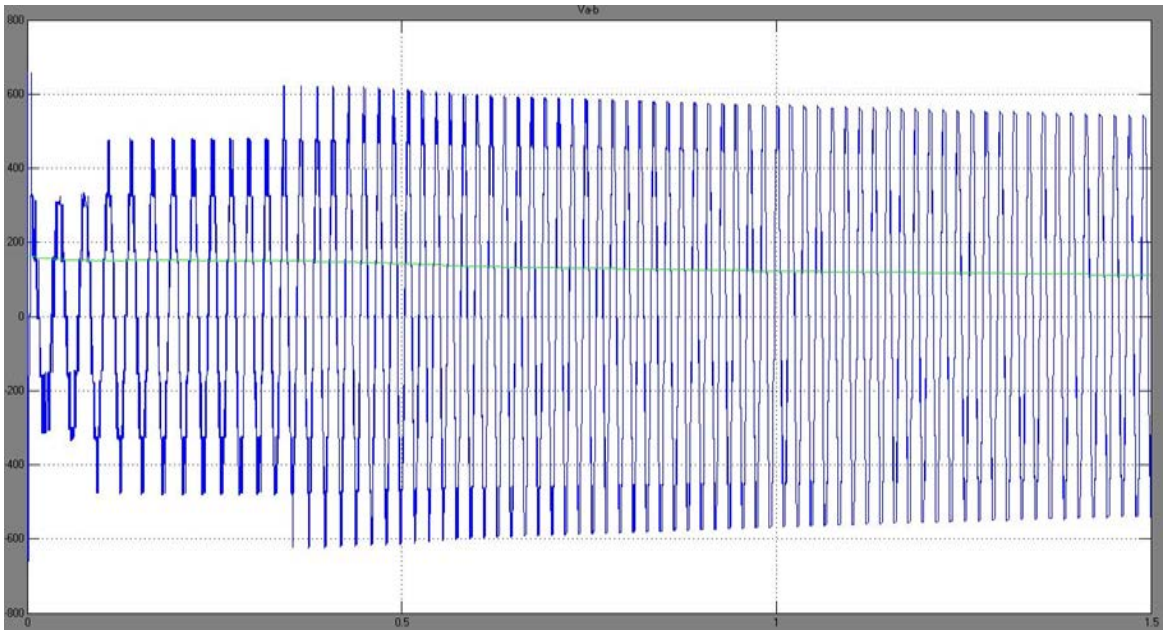
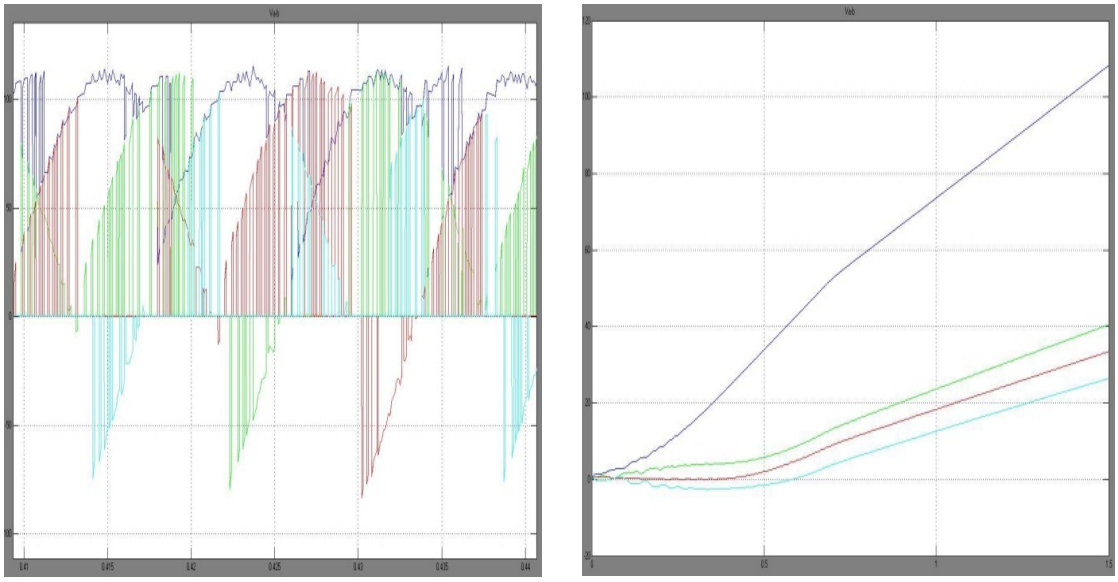


Figure 5-20 Voltage waveform during acceleration

The final Figure 5-21 (a) illustrates the load-sharing between the UCs and the batteries. It is shown that the UC's currents (red, green and light blue traces) circulate and this source is also used to compensate harmonics when the battery current (blue) remains positive and provides only active power. The energy consumption for each source during acceleration is presented in Figure 5-21 (b) where power delivered by each source is integrated. It is noted that for this control setting the battery will supply most of the energy, and the supercapacitors are used mainly to reduce harmonics and to accelerate to high speed.



(a) Currents delivered by sources for one period

(b) Cumulative energy delivered by sources during acceleration

Figure 5-21 Current and energy delivered by multisource system during motor acceleration, dark blue colour symbolize battery current, green, red and blue represent UCs currents in three-phases

5.3 Summary

Presented system simulations in this chapter aimed to validate that the proposed structure of the multilevel multisource inverter can be controlled to modulate output voltage with low distortions and at the same time the active power distribution between the sources can be achieved. Computed results demonstrated that distinguished modulation modes deliver output waveforms with harmonic content that is typical for standard SVM modulation. The amount of harmonics that were present in output voltage and in current depended directly on inverter operating levels and with the increase of invert levels the total harmonic distortions were reduced proportionally. The main advantage of analysed system is that introduced modulation modes give possibility to control average current delivered by sources so the amount of power each source is delivering can be controlled. It was proven that by using two modulation methods at the same time and alternating them it is possible to control power seen by voltage sources without introduction of unwanted harmonics content.

Presented model allowed also to test the complete system during motor acceleration and to prove that the variable UCs amplitude do not affect system performance. The Simulink model allowed verifying the effectiveness of the proposed modulation strategy and enhancing control logic for further hardware implementation.

CHAPTER 6 EXPERIMENTAL VALIDATION

In this chapter the developed hardware platform that was used during experimental testing is presented with review of all the main elements that proposed system of multilevel multisource inverter consist off. The further part of this chapter includes selected experimental results that were captured during various operating conditions.

6.1 Hardware description

The experimental setup is a motor drive consisting of a 0.37kW induction motor, a cascade multilevel inverter and the National Instruments Real-Time system with FPGA. The architecture of the system is presented in Figure 6-1 where the main elements include a three-phase induction motor together with hardware implemented decoder and connected to the cascade multilevel inverter. The inverter is supplied by the battery bank as a main voltage source and three sets of H-Bridges are supplied by 45V UC's. Since the system include multiple floating voltage sources the gate drivers circuits as well current and voltage sensing electronic had to be optoisolated. The whole system is controlled and supervised by National Instruments Compact RIO Real-Time platform.

6.1.1 Induction Motor

The motor that is used in the system is a "KAPAK" three-phase induction motor built by English Electric Machines AEI (Figure 6-2). The motor power is 0.37kW when the supply voltage is 220/250V in Delta configuration or 380/440 in Star configuration. The corresponding phase current is 1.5A in Delta and 0.9A in Star configuration. For nominal supply voltage at 50Hz the motor is able to reach speed of 2,840 rev/min. Measured winding resistance in Delta configuration have 21Ω and 30Ω in Star configuration. The motor in the system as described is used with windings connected in a Delta configuration only since the maximum peak voltage that is available from the inverter is only 210V (120V battery and 45V UCs in each phase).

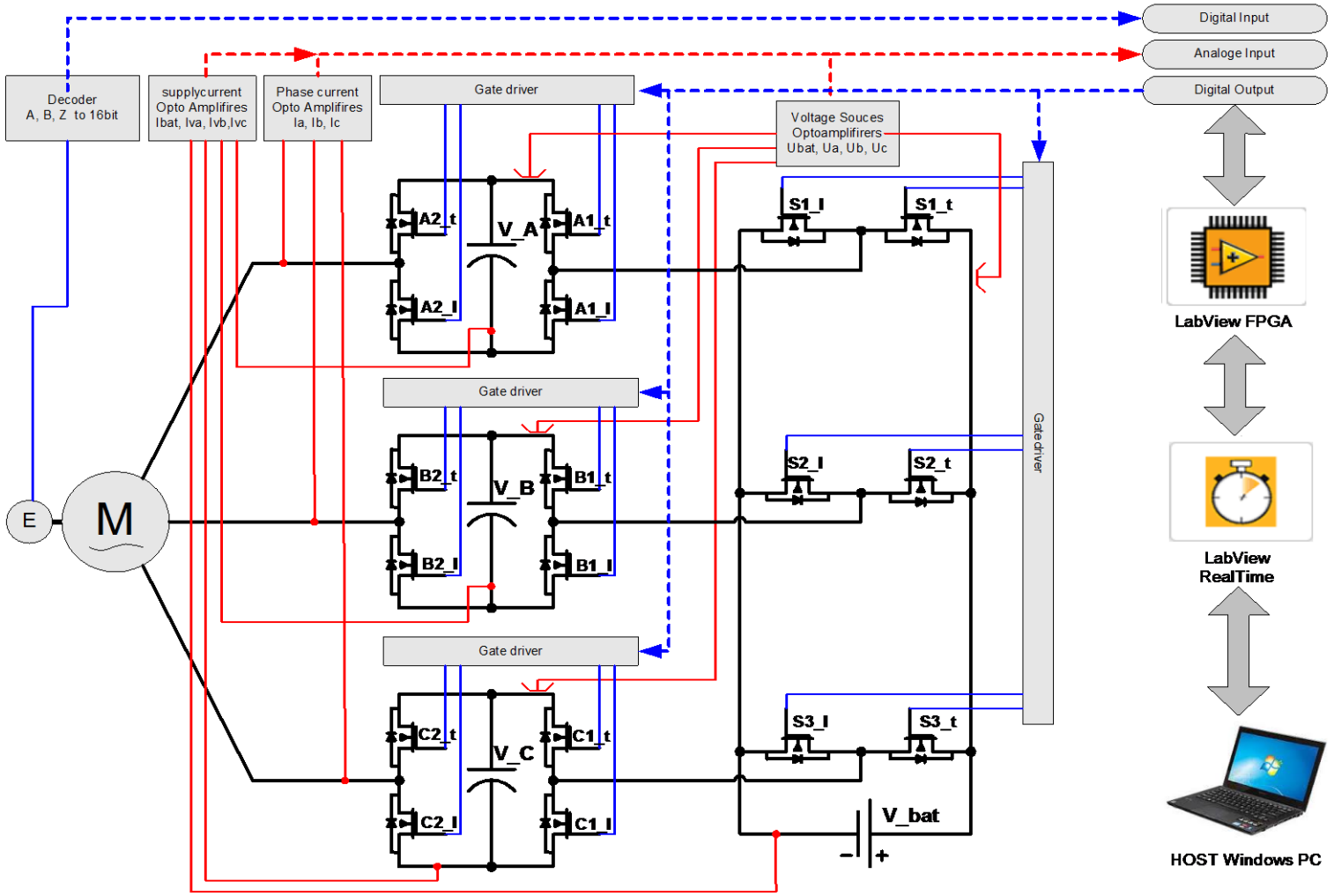


Figure 6-1 Overall scheme of developed system

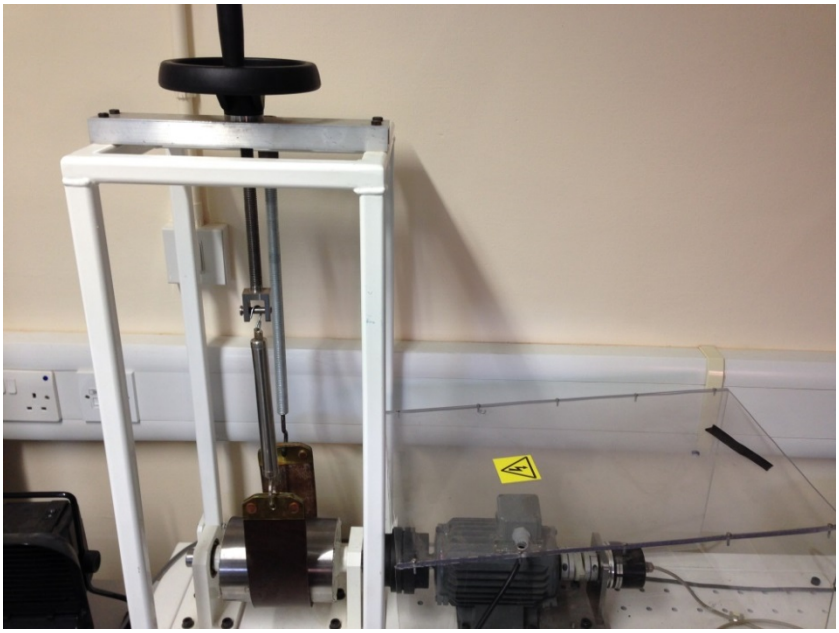


Figure 6-2 induction motor used as the load for created platform

The motor is connected to the inverter through the simple LC filter that is placed between the inverter legs (A, B and C) and motor phases to minimise switching noise as presented in Figure 6-3.

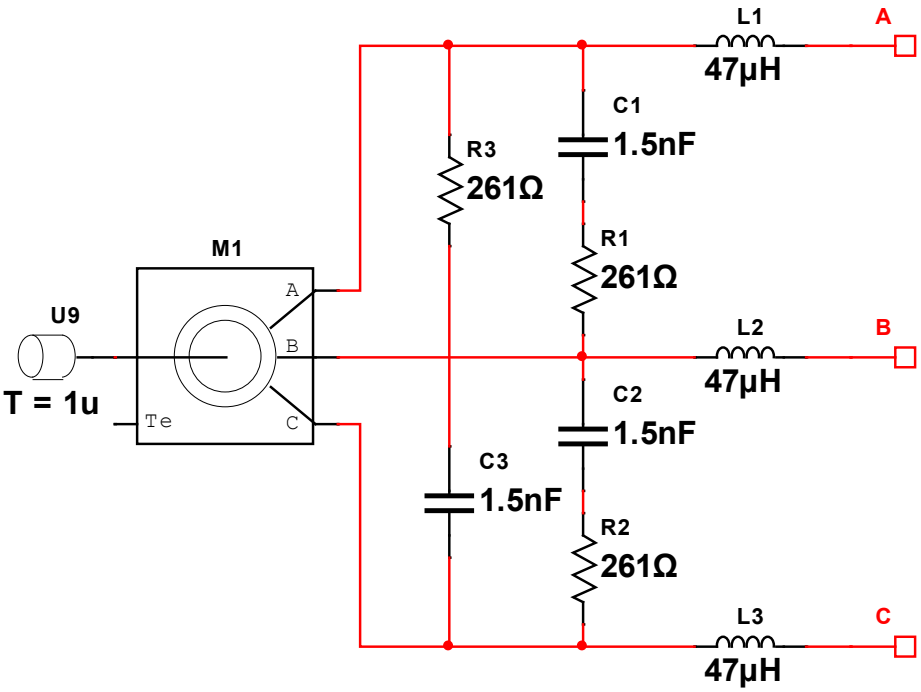


Figure 6-3 LC filter on the input to the induction motor

6.1.2 Encoder with a hardware decoder

To measure the motor's speed the ABZ optical shaft encoder is installed with 2,000 pulses per revolution. Because the motor's maximum rotation speed is high (2,840 rev/min), it was necessary to shift the intensive pulse counting from the control system into additional hardware. The 16-bit HCTL-2017-A00 component that was selected is an Integrated Circuit (IC) that performs the function of a quadrature decoder and an up-and-down counter, and has an 8-bit bus interface. The decoder was configured to operate with a 14MHz clock and with a synchronised toggle signal that changes the output between high and low byte. Since the decoder outputs a count signal for every state transition from encoder channel A and B the count signal is multiplied by a factor of four, which gives a resolution of 8,000 pulses per revolution.

6.1.3 Cascade Multilevel inverter

The structure of the multilevel inverter consists of one three-phase bridge supplied from the main source (battery) and three H-Bridges supplied by UCs and connected in series to each phase (Figure 6-4).

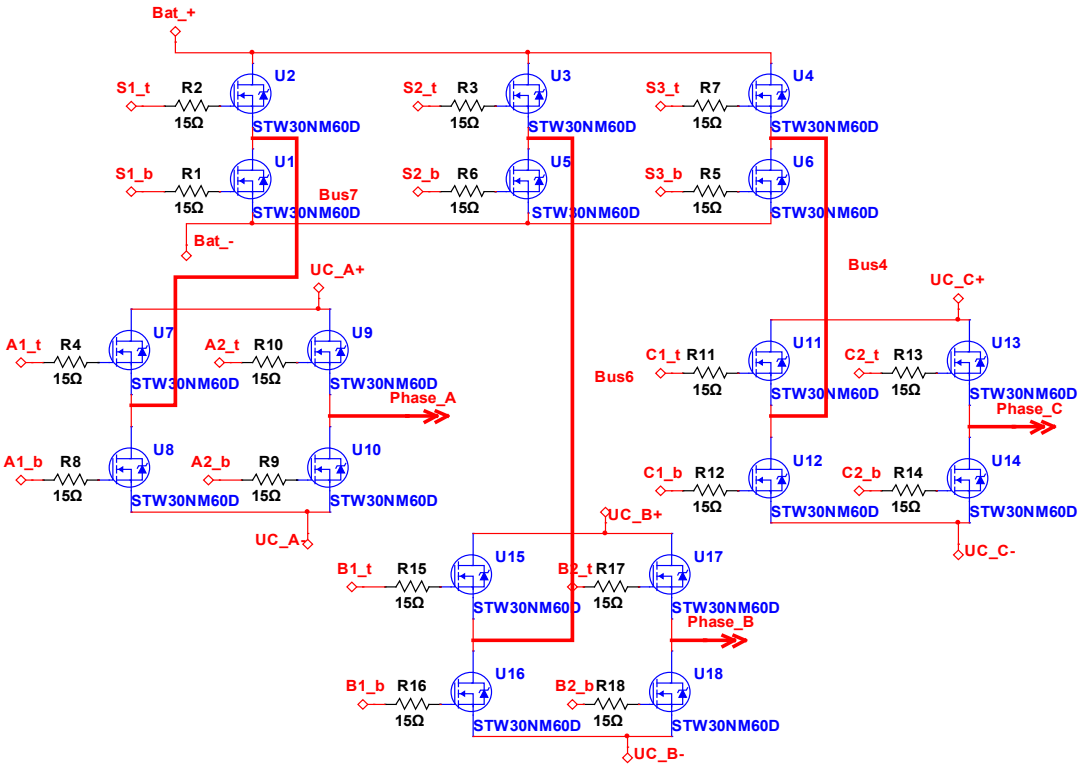


Figure 6-4 Cascade multilevel inverter

The power MOSFET that is used in the circuit is the N-Channel power MOSFET STW30NM60D from ST (FDmesh). The switch was chosen because it can operate with a maximum voltage (drain-source voltage) of up to 600V, much higher than expected in the system, and at the same time it has relatively low resistance $R_{\_on}$=0.125Ω. The maximum drain current for this part is 30A, which should provide a large margin of error in the control algorithm (up to 3A expected under normal operation). The other features of this MOSFET are: high dv/dt and avalanche capabilities, low input capacitance and gate charge, fast internal recovery diode.

Since the conducted current in MOSFET (I) is only around 2A and never exceeds values higher than 3A, the effective switching frequency is low and only about 2kHz. The power dissipation from MOSFET should not exceed 1.2W in the worst case base on calculated conduction losses (**6-1**).

$$P_{cond} = I^2 \cdot R_{on} = 3^2 \cdot 0.125 = 1.125\ W \quad (6\text{-}1)$$

The estimated switching losses should be low as calculated below, where t_{on} is switch on time and t_{off} is switch off time, and f_{sw} is switching frequency:

$$P_{sw} = (t_{on} \cdot U \cdot I \cdot f_{sw})/2 + (t_{off} \cdot U \cdot I \cdot f_{sw})/2 = \quad (6\text{-}2)$$

$$(119\text{ns} \cdot 150V \cdot 3A \cdot 1kHz)/2 + (43.4\text{ns} \cdot 150V \cdot 3A \cdot 1kHz)/2 = 0.06\ W$$

Although the maximum dissipated power is low for TO-247package (only 1.2W), all MOSFET are equipped with heatsinks (FK243-MI-247) that have thermal resistance to ambient of 18.4K/W and the surface between the MOSFET case and the heatsink is filled with SIL-PAD 2000 for better heat transfer (heatpad thermal resistance is 0.2C/in2/W). It is expected that in the worst case the MOSFET temperature will not rise further than 20Deg above ambient. The hardware implementation next to the UCs is presented in Figure 6-5.

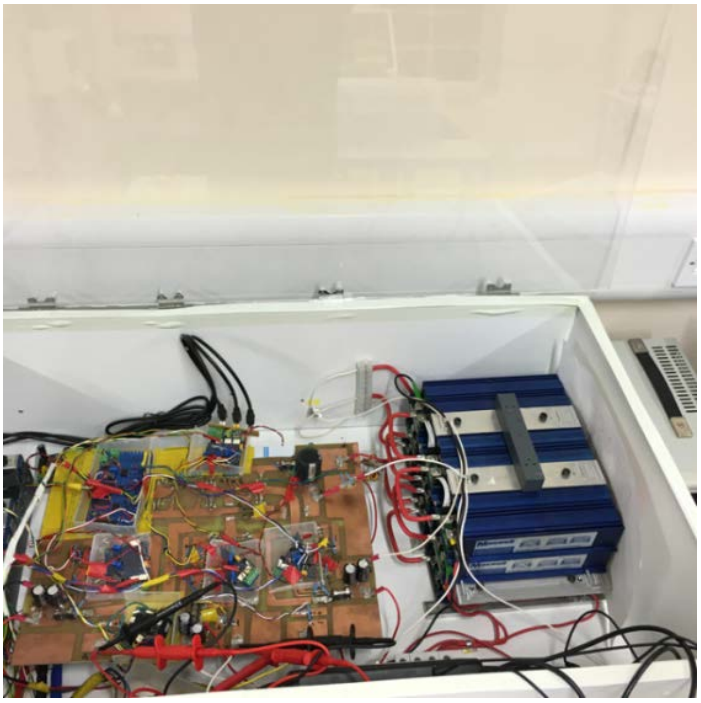


Figure 6-5 Implementation of cascade multilevel inverter together with Maxwell ultracapacitors

6.1.4 MOSFET gate drive circuit

One of the most difficult parts of this inverter design was to provide galvanic isolation between each of the floating energy sources (the battery and UCs) and the control system. To deliver a stable 15V supply for the gate drivers in each bridge isolated DC/DC converters are used, and all analogue and digital inputs/outputs to the NI CRIO control platform are optoisolated.

A block diagram of the cascade multilevel inverter with gate drive circuits is presented in Figure 6-6. The diagram also includes 15V power supply units that deliver stable and isolated auxiliary voltage from each bridge. The PSU1, PSU2, PSU3, PSU4 are galvanic isolated 3W and 6W universal DC/DC converters. The power supplies input voltage range is from 18V to 75V and the outputs voltage is provided at 15V.

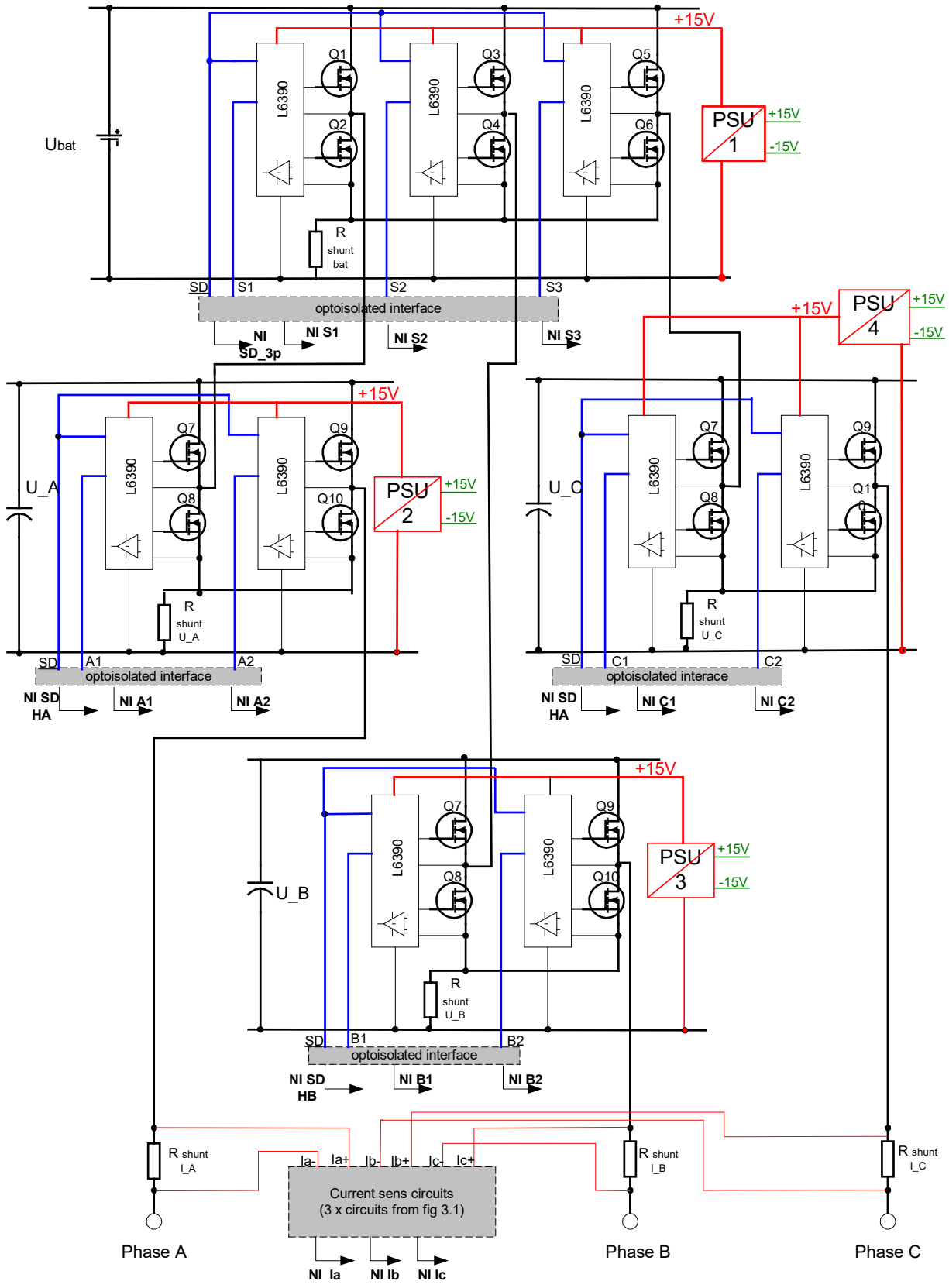


Figure 6-6 Block diagram of cascade multilevel inverter with gate drive circuit

For this application the L6390 gate driver from ST has been chosen. The selection of this IC is justified by its functionality that include adjustable dead-time, smart shutdown function and high voltage rail up to 600V with good immunity on voltage spikes (dV/dt +/- 50v/nsec). The circuit include integrated bootstrap diode, operational amplifier for current sensing and comparator for fault protection. A detailed schematic of the gate driver circuit for the pair of upper and lower MOSFET is shown in Figure 6-7, a total of nine circuits in the whole inverter are used.

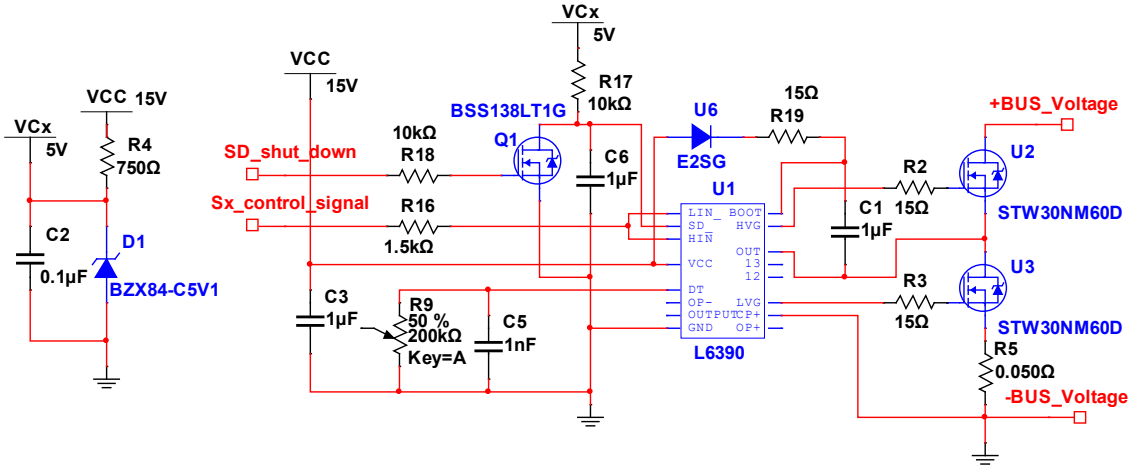


Figure 6-7 Detailed schematic of gate drive circuit

One of the biggest advantages of the L6390 part is hardware implemented dead time control that can be adjusted by the R9 resistor. Also, thanks to the internal interlock it was possible to use just one control signal (Sx control signal) to drive the upper and lower switches without worry of causing a short in the converter branch. Additionally, the circuit includes a smart shutdown functionality which, by monitoring the voltage drop on the shunt resistor, is able to immediately shut down the power converter in the case of an overcurrent. Another very useful feature is the integrated operational amplifier that can be used to amplify the measured voltage signal from the shunt resistor.

The 15Ω gate resistor was selected based on simulation and experimental validation as for this value the compromise between switching speed and gate signal ringing was achieved.

6.1.5 Optoisolated digital signal interface

To realize galvanic isolation between control signals from NI system and converter gate drivers, the High Speed Logic Optocouplers are used. The HCPL2601 component presented in Figure 6-8 is selected because of its common mode rejection (10kV/us) and high speed (10Mbit/s) when required resolution for gate signal is at last 1μs.

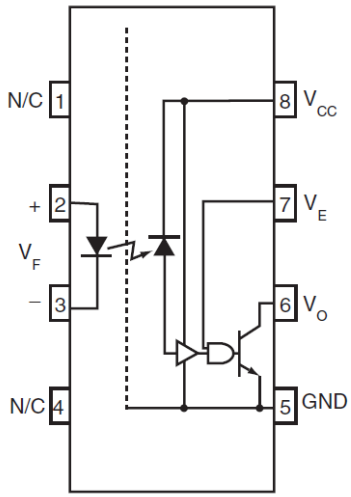


Figure 6-8 Simplified diagram of the HCPL2601 optocoupler

A schematic of the digital signal interface for a single control signal (13 circuits in total used, nine for gating signals and four shutdown signals) is presented in Figure 6-9.

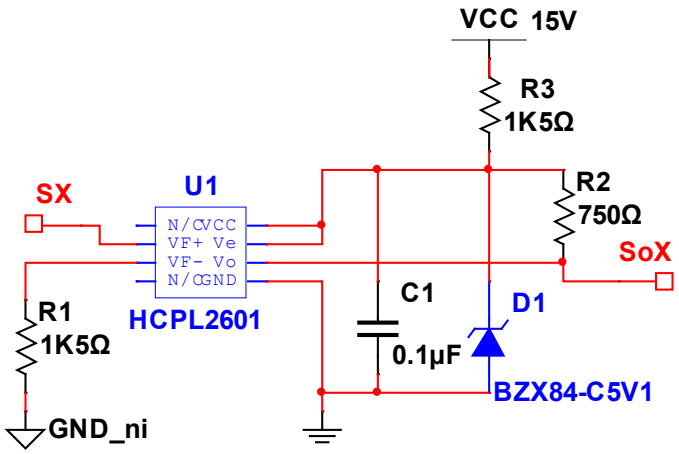


Figure 6-9 Circuit diagram for digital optoisolator

6.1.6 Optoisolated current sensing circuit

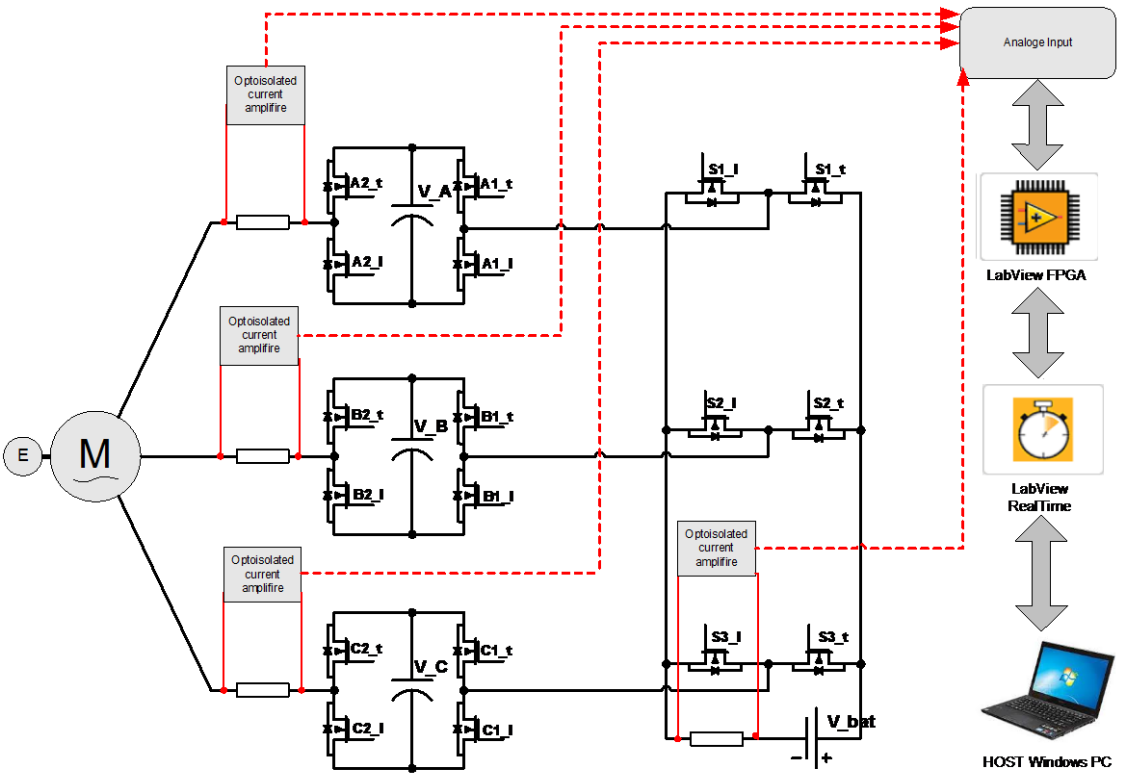


Figure 6-10 Block diagram of implemented current sensing

For accurate phase currents and main source supply current measurements the 0.05Ω shunt resistors are used on the outputs from the inverter and on the output from the main source (Figure 6-10). Because all the voltage drops on the resistors have different references and the amplitude of the signals is low, a separate circuit with isolation amplifiers HCPL-7840 was built for each sense line. An example schematic for one current-sensing signal is presented in Figure 6-11. The HCPL-7840 component features 100kHz bandwidth with 0,004% nonlinearity and at the same time provides galvanic isolation. The primary and secondary sides of the amplifier require separate +5V supply, so to achieve this the secondary side is supplied by an isolated 1W DC/DC converter (15V to -15V) that is supplied from +15V bench power supply. Stable +5V for the primary side is provided by a Zener diode. Since the gain of the isolation amplifier is only eight, the next stage includes a standard operational amplifier to increase the amplitude of the measured signal by five. These two stages of

the signal processing convert the measured current on the shunt resistor that is in the range +/-6A into voltage between -10V and +10V.

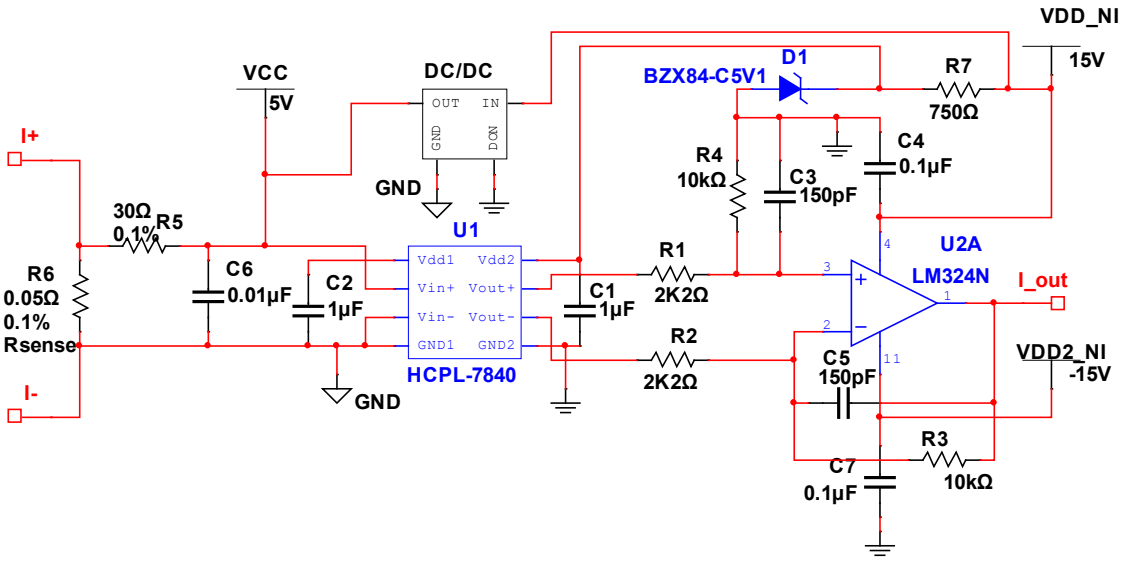


Figure 6-11 Circuit diagram for analogue optoisolator

6.1.7 Optoisolated Voltage Measurements

Accurate voltage feedback from three UCs as well as the battery (Figure 6-12) is required in order to allow estimation of maximum available energy that can be delivered to the motor as well as the amount of energy that can be recuperated. Additionally sources supply voltage is needed to stabilize capacitors voltage balance between phases, for Space Vector Modulation and for motor flux estimation. As all four energy sources are floating, an additional requirement for the voltage-measurement system is to provide isolation between each voltage source and control system. This goal was accomplished by a High-Linear Analogue Optocoupler HCNR201 with LED that illuminates two closely matched photodiodes (Figure 6-13). The output photodiode produces a photo current that is linearly related to the light output of the LED. Thanks to their close matching, these photo-diodes are able to provide very high bandwidth (up to >1MHz) with low nonlinearity (under 0.01%) and 5kV RMS isolation.

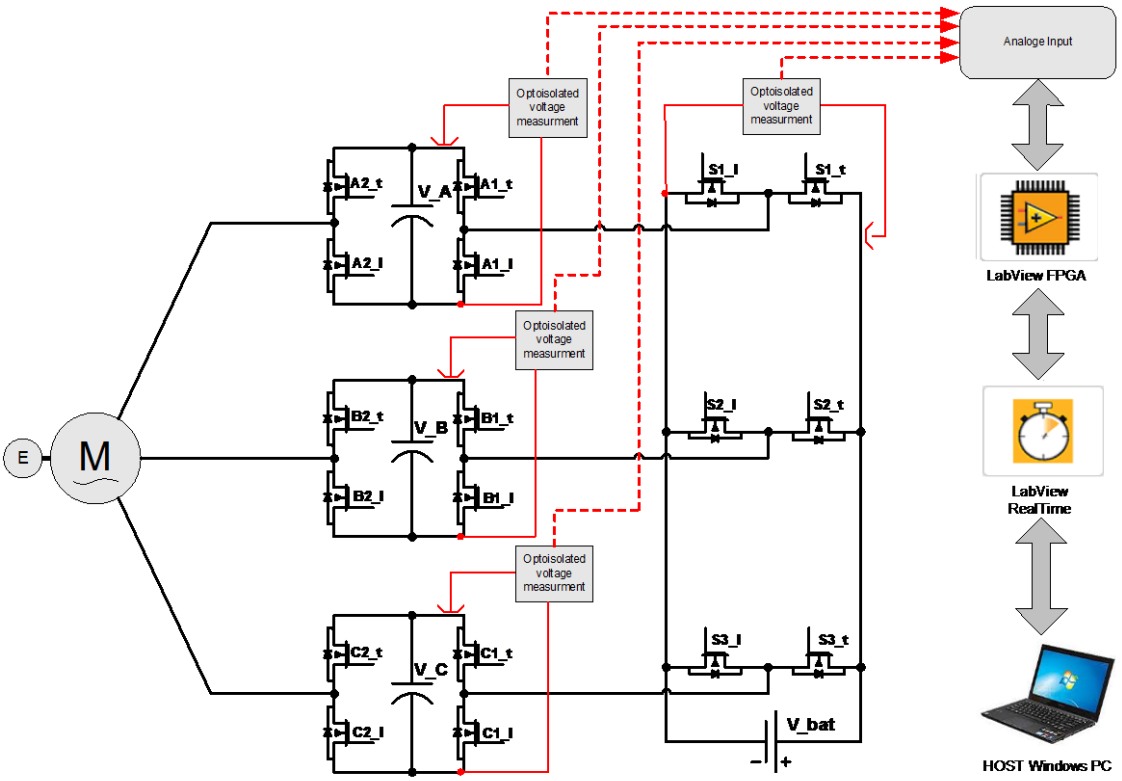


Figure 6-12 Block diagram of implemented current sensing

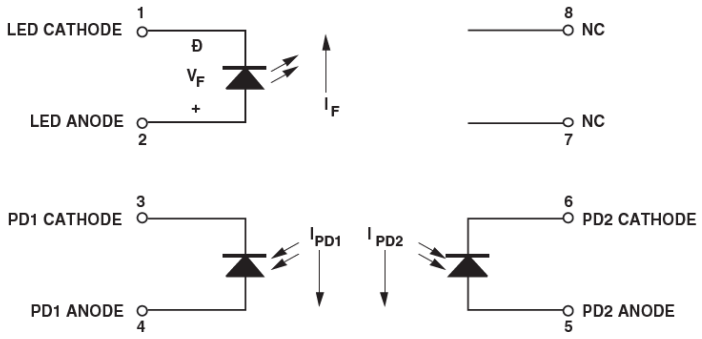


Figure 6-13 Schematic of linear analogue optocoupler

A schematic of the voltage-sensing circuit that was built for each voltage source can be seen in Figure 6-14. The voltage of the energy source between U_sense+ and U_sense- is first scaled by voltage divider R5, R1 and then converted by optocoupler into galvanic separated signal on output pins 5 and 6 of HCNR201. At the next stage the measured signal is compared with a 5V reference LT1027 and amplified by operational amplifier LM324 so the measured signal that arrives to the control system is isolated and the scaled

voltage between 0 and 10V. The secondary side of the system is supplied by a 15V bench power supply.

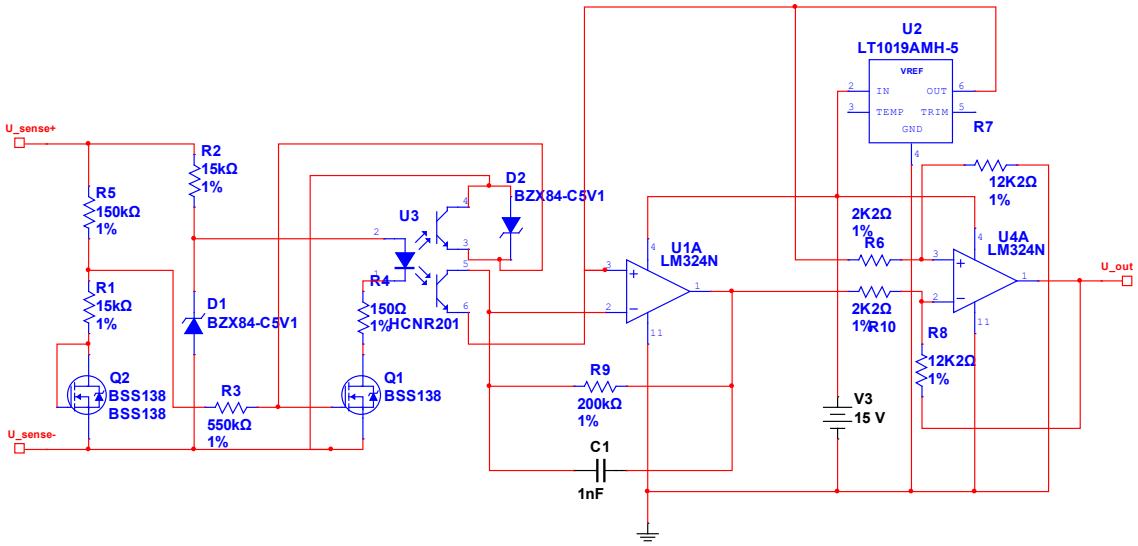


Figure 6-14 Schematic of voltage measurement interface

6.1.8 Ultracapacitor Storage System

An electric double-layer boostcap UC from Maxwell Technologies (BMOD0350-15) (Figure 6-15) with individually balanced cells was selected. The pack working voltage is 15V, so to achieve the 45V required, three cells had to be connected in series. Since the capacitance of the single module is 58F the total capacitance of the series of connected modules in one phase is 19.33F at 45Volts. This gives the maximum energy that can be stored in each phase of 19.6kJ, so in three-phases the total energy of 58.7kJ can be stored.

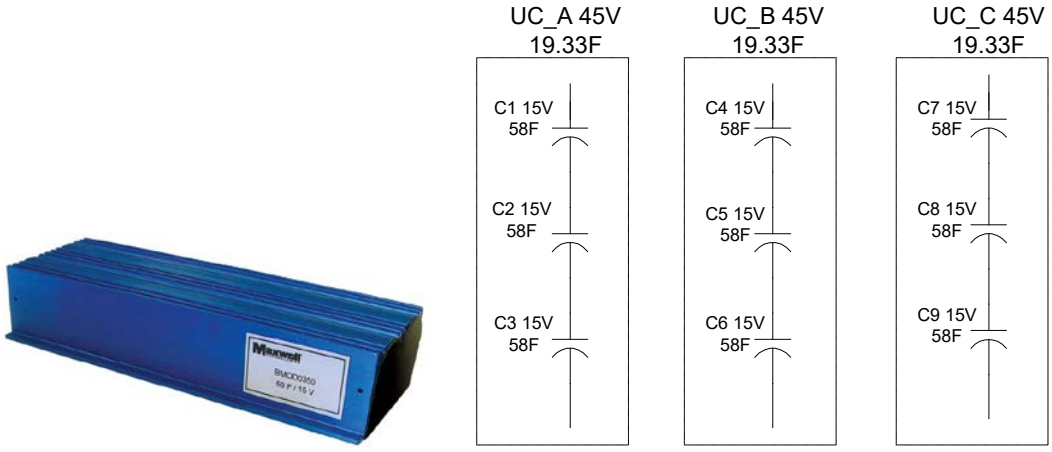


Figure 6-15 Selected capacitor and module-wiring diagram

6.1.9 Main Voltage Source: – Battery Bank

The main voltage source supplying the three-phase bridge in the multilevel inverter consists of 10 Leoch LP12-4.0 Sealed Lead Acid batteries (SLA 12V 4.0Ah) with 40mΩ internal resistance per single battery having a total of 400mΩ internal resistance (ten connected in series).

To minimise current ripples that would stress the batteries, the connection to the inverter is through an LC filter that consists of an 80μH inductor in series with the batteries and a set of two 1mF electrolytic capacitors (the capacitors' maximum voltage is 200V) connected in parallel (Figure 6-16). Additionally, the 50mΩ shunt resistor is included to allow a current measurement that is necessary to precisely control the charging and discharging of the battery within limits.

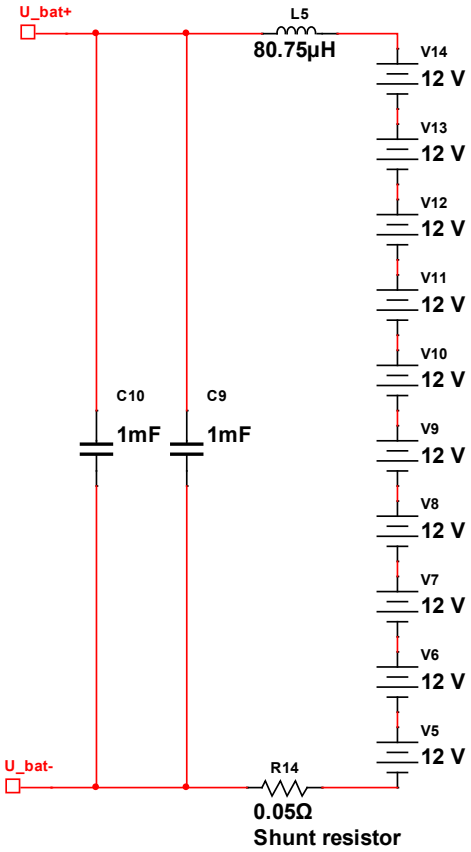


Figure 6-16 Voltage source with input filter for a three-phase bridge

6.1.10 Control System Design

The National Instruments CompactRIO system was chosen since it combines an open embedded architecture together with a straightforward NI LabVIEW graphic interface. The embedded FPGA is a good-performance, reconfigurable chip that can be programed with LabVIEW FPGA tools, eliminating the need to use complex FPGA programing languages such as VHDL. The FPGA hardware embedded in CompactRIO allow the implementation of custom timing, triggering, synchronization, control, and signal processing for analogue and digital I/O with its internal clock at 40 MHz. Additionally, the CompactRIO system has an integrated real-time 400 MHz Freescale processor to execute Real-Time routine. The FPGA is connected to the embedded real-time processor via a high-speed PCI bus. The whole system is supplied by a 15V bench power supply. The architecture of the typical NI CompactRIO system is presented in Figure 6-17.

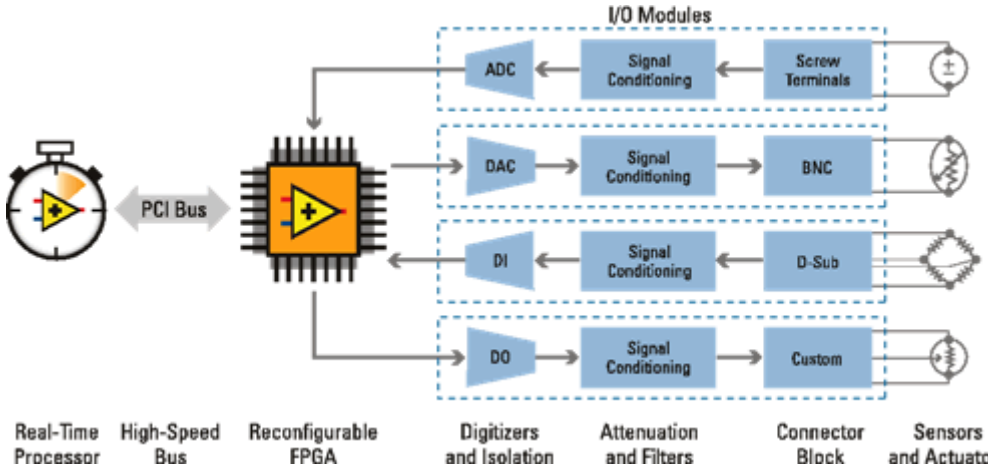


Figure 6-17 Architecture of the CompactRIO system (Architectures, Practices and Applications, n.d.)

The complete configuration of the control system is presented in Appendix C and its physical implementation is shown in Figure 6-18.

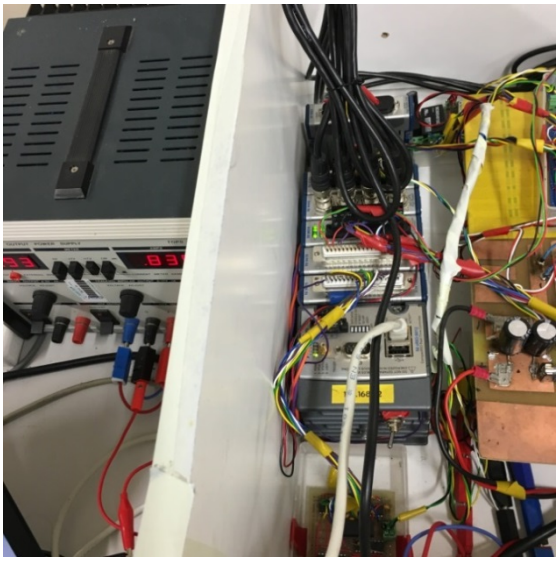


Figure 6-18 Implementation of Compact RIO control platform together with input / output allocation

In Figure 6-19 the complete experimental platform is presented that include developed inverter together with control system.

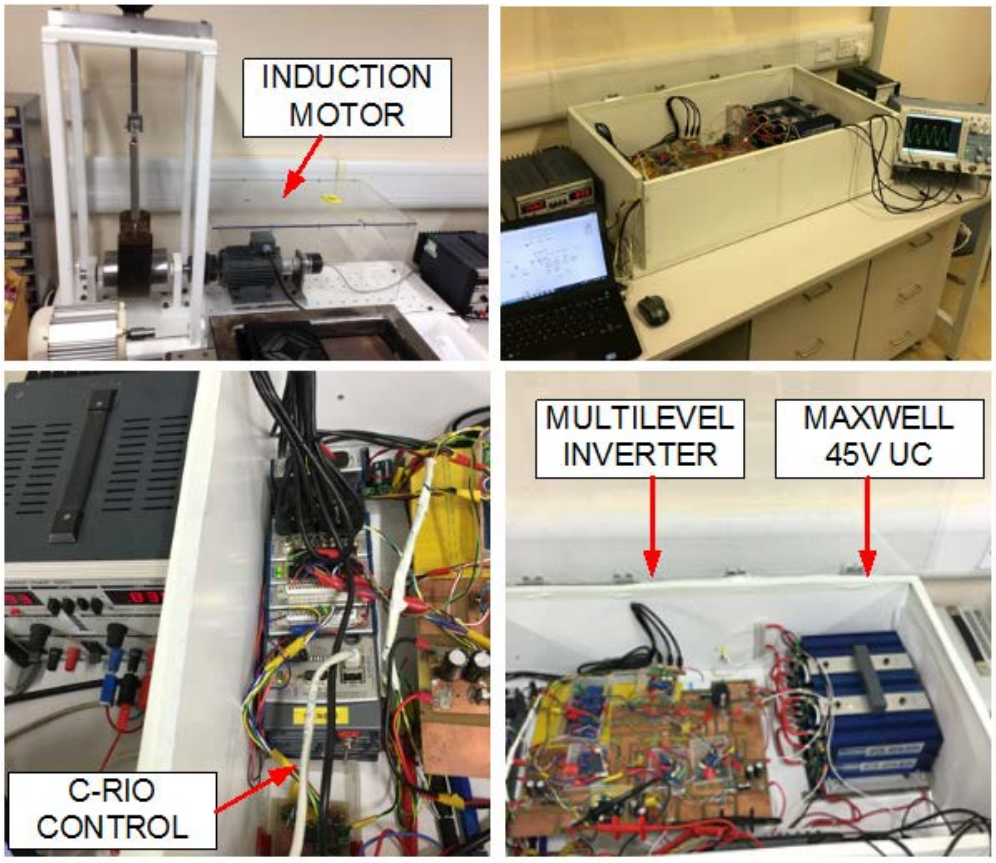


Figure 6-19 Overview of developed system

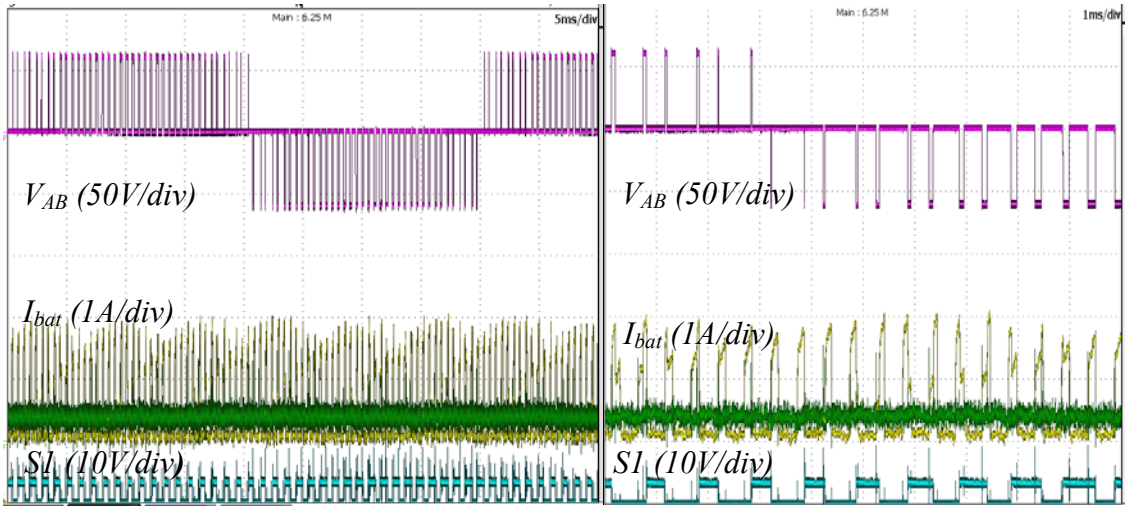
6.2 Experimental validation

Developed experimental platform with the multilevel multisource inverter was put under various operating constraints to assure that the proposed concept is valid. Firstly the unit was verified in terms of its performance under steady conditions mainly to test performance of its modulation method. Secondly unit was set under different transient conditions to find its operational limits. The final platform test included motor acceleration profiles to validate complete control method that was presented in Chapter 4. The final results are compared with the previous simulations to better understand limitation of discussed system. Under all tests the same hardware and control platform was used with the same modulation frequency.

6.2.1 Two level modulation with three-phase bridge

The first test on the inverter platform was to find its performance during standard two level modulation with only battery as a source. The aim of the test was to simulate performance of the conventional voltage converter and to generate data that could be later used to compare system behaviour under introduced novel operating modes. In this test the three-phase bridge has been supplied by the voltage source with 60V amplitude. The output frequency was set as 25Hz and motor was running with 25% load and 0.3 modulation index.

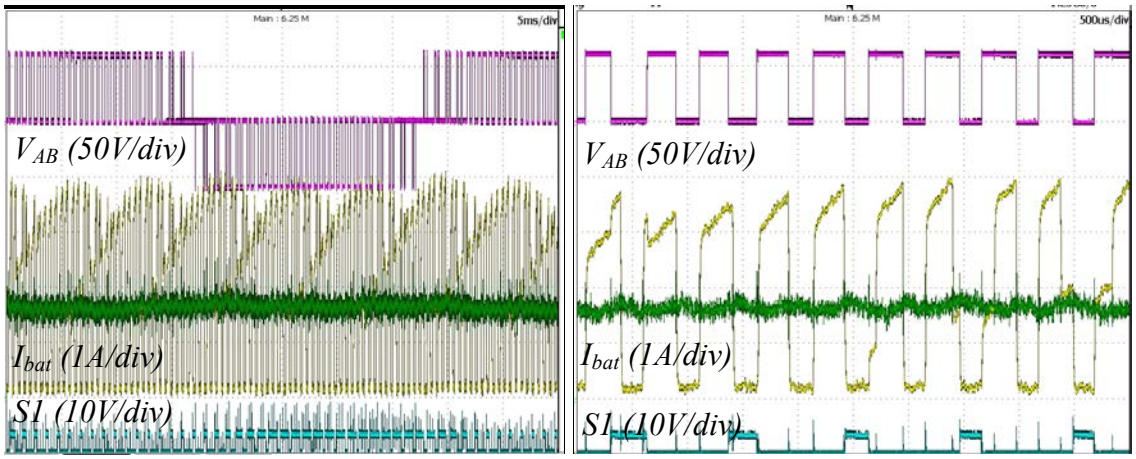
The waveforms presented in Figure 6-20 shows the phase to phase voltage (V_{AB}) that is delivered to the motor. It is possible to find from graph that the SVM with symmetrical zero voltage vector placement is used since in the modulation period of 1ms we can find two same size voltage pulses. Also inverter gate control signal (S1) has one rising and falling edge in 1ms period what means that the switching frequency is limited to 1 kHz. Since the LC filter is used between main voltage source output and inverter the supply current ripples are limited. In presented graph (Figure 6-20) the supply current that is sink by the inverter (yellow trace) has four times larger amplitude in comparison to the constant current that battery output (green trace).



(a) Waveforms for full period (b) Zoomed waveform

Figure 6-20 Phase to phase voltage (V_{AB}) and battery current profile (I_{bat}) before and after LC filter for SVM with three-phase bridge only and 0.3 modulation index, ($S1$) phase A gate signal

In the next test the modulation index has been increased to 60% as well the motor load has been doubled. In Figure 6-21 it is noticeable that in comparison with previous graphs the duty cycles of modulated voltage increased. Also the supply battery current doubles its amplitude.



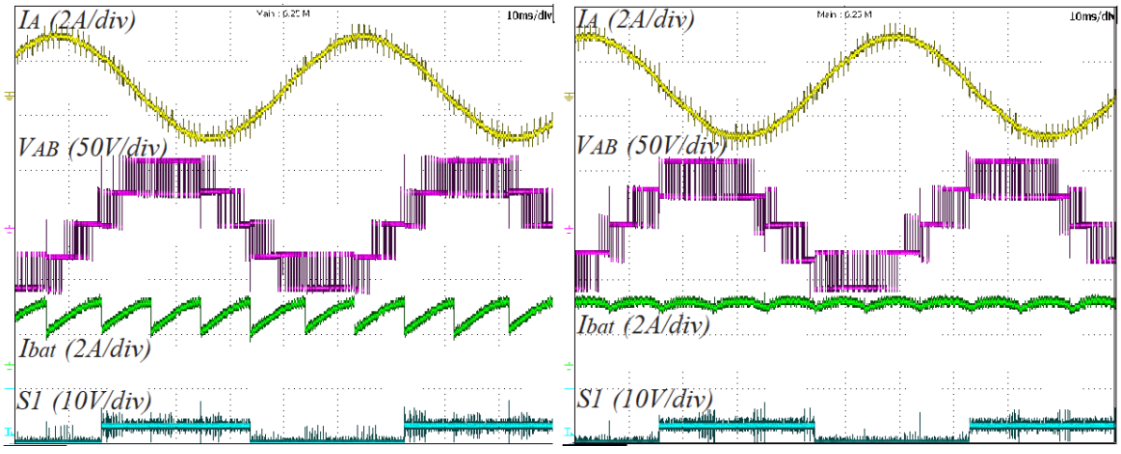
(a) Waveforms for full period (b) Zoomed waveform

Figure 6-21 Phase to phase voltage (V_{AB}) and battery current profile (I_{bat}) before and after LC filter for SVM with three-phase bridge only and 0.6 modulation index, ($S1$) phase A gate signal

The achieved results appear to be as expected and the output voltage has typical waveform shape for SVM. It was also found that introduced LC filter allows to significantly reduce battery peak current what should improve battery lifetime. It is possible to find analogy between the simulation results in section 5.2.1 where battery current and phase voltage had identical shapes.

6.2.2 Phase shift control

It is desirable to use the modulation where the three-phase bridge is switched at fundamental frequency for most of the drive activity but to keep UCs voltage at constant value. In this case the active power delivered by three-phase bridge has to be controlled by phase shift angle. The aim of this test is to find influence of the phase shift control on the sources current and to verify if motor current is affected. Figure 6-22 presents an example of the waveform captured in MODE II for two different phase shifts "χ". For the first maximum phase shift (Figure 6-22 (a)) the current seen by the main source has sawtooth shape and its average value is low, whereas in the second case the phase shift is adjusted for maximum battery current (six-step switching synchronized with the phase of the motor current). The change in the phase shift allowed to change the main source current by almost 25% without any impact on the load phase current (I_A).

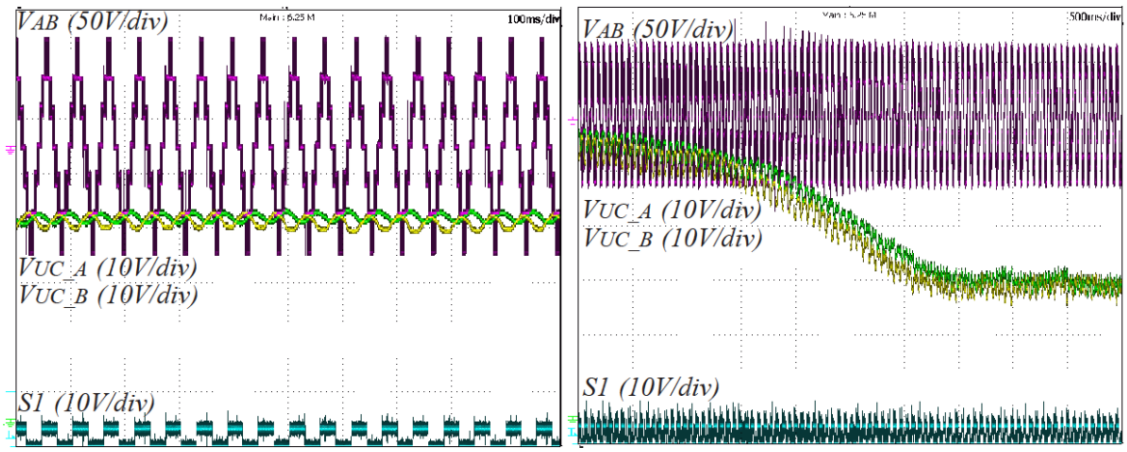


(a) Phase shift χ + ϕ > 0 (b) Phase shift χ + ϕ = 0

Figure 6-22 Motor phase current (I_A), phase to phase voltage (V_{AB}), battery current (I_{bat}) and three-phase bridge phase A gate signal ($S1$) in switching MODE II for two different values of phase shift

From detail observation of the phase voltage we can discover that the spikes in voltage appear when the three-phase bridge changes its voltage vector. These types of spikes were not present during simulations in Chapter 5 since used switches were ideal. Those spikes in the voltage are unavoidable when multiple vectors are switched but since developed modulation strategy minimize those events the three-phase bridge and H-Bridge change their states simultaneously only six times during the fundamental frequency period.

For higher amplitude of the output voltage the phase shift regulation of the capacitor's voltage becomes more appropriate. The effectiveness of the phase shift control was tested to validate the voltage regulations of the capacitors that supply H-Bridges. For this test the UCs were disconnected from H-Bridges and replaced by the electrolytic capacitors with 2mF capacitance. Reducing H-Bridge sources capacitance allows much quicker voltage regulation. In Figure 6-23 the output voltage from the inverter in six-step operation is presented. It can be noted that the capacitor's voltage is kept at a constant value and the capacitors in phases A and B have the same amplitude (V_{UC_A} and V_{UC_B}). The second image presents the case where the capacitors were charged to 50V and a new UC reference voltage of 25V was set.

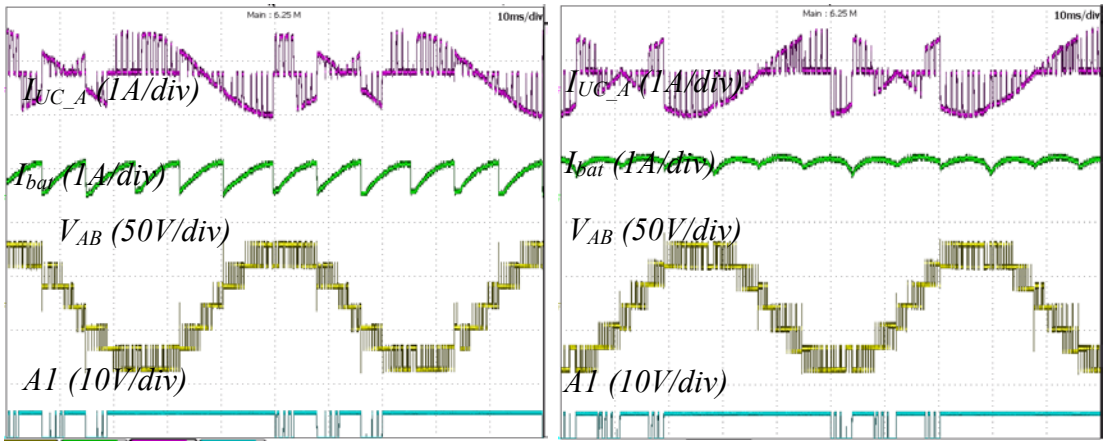


(a) Zoomed steady state (b) Transient respond on V_{UCref} change

Figure 6-23 Motor phase to phase voltage (V_{AB}), capacitor voltages (V_{UC_A} and V_{UC_B}) and three-phase bridge phase A gate signal (S1) for capacitors voltage level control in MODE II modulation with phase shift and its response to capacitors reference voltage change

The energy transfer was accomplished by the phase shift in MODE II regulation and all capacitors reached the same set point.

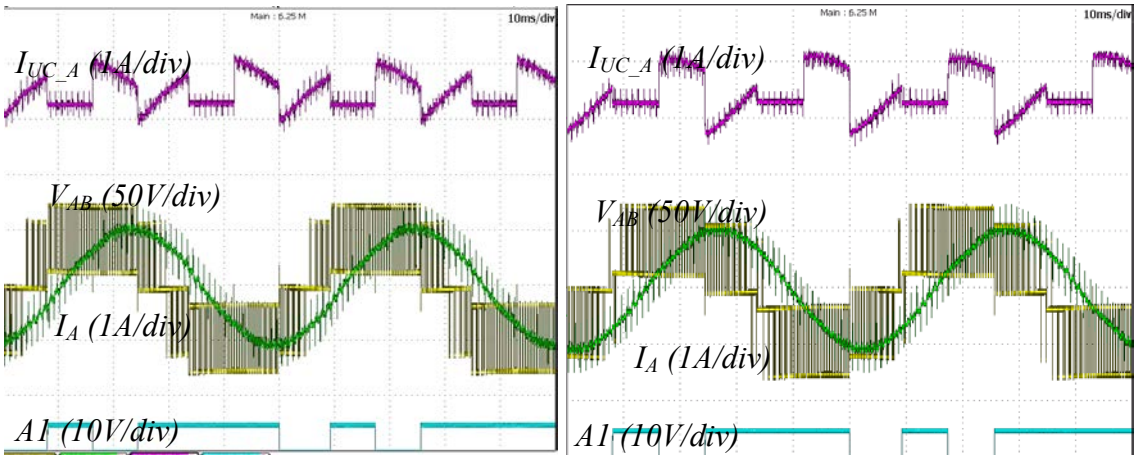
To explain phase shift control and its influence on capacitors current in next test the UC current has been captured. In Figure 6-24 it is visible that UC current (I_{UC_A}) is oscillating between the positive and negative values and depending on the phase shift angle the current average value change. In first case when phase shift is large the duty cycle of positive UC current pulses is larger and reaches higher amplitude. For case when the voltage from three-phase bridge is synchronised with motor current the positive current pulses become reduced and negative side increase. The results from this test appear to be same to the ones that were achieve during simulations in section 5.2.3.



(a) Phase shift χ + ϕ > 0 (b) Phase shift χ + ϕ = 0

Figure 6-24 Motor phase to phase voltage (V_{AB}), capacitor current (I_{UC_A}), battery current (I_{bat}), and H-Bridge phase A gate signal (A1) for capacitors voltage level control in MODE II modulation with phase shift

In Chapter 4 it was defined that the phase shift control is still valid in MODE IV, MODE V and MODE VI. This type of strategy can be used when UCs have to be discharged or charged at maximum rate since their switching can be synchronise with the motor fundamental frequency giving maximum current.



(a) Phase shift χ = 0 (b) Phase shift χ <0

Figure 6-25 Motor phase to phase voltage (V_{AB}), capacitor current (I_{UC_A}), motor phase current (I_A), and H-Bridge phase A gate signal (A1) for phase shift control in MODE IV modulation mode

In Figure 6-25 the results for phase shift control in MODE IV are presented. The UCs voltage amplitude is set at 15V when the main voltage source amplitude is equal to 60V. In presented case the UCs are switched at fundamental frequency and are not fully in phase with motor current what cause that UCs deliver limited current. By introducing negative phase shift the amplitude of the UC current (I_{UC_A}) increase improving voltage discharge rate. To increase discharge rate further it is possible to switch into MODE VI modulation where all capacitors are constantly switched on. In Figure 6-31 and example waveform in MODE VI modulation is shown where for the same operating conditions the UC current (I_{UC_A}) increase and is sourcing power during a whole period. It is also visible that the six-step voltage waveform has now higher amplitude and the modulation by three-phase bridge has smaller duty cycle. By controlling phase shift angle in this mode it is possible to maximize output power that is delivered by UCs. The change of modulation mode from MODE IV to MODE VI did not cause any negative effect on the phase current, the switching ripples remain at similar level what is mainly related with the amplitude of voltage that supply the three-phase bridge that operates in SVM.

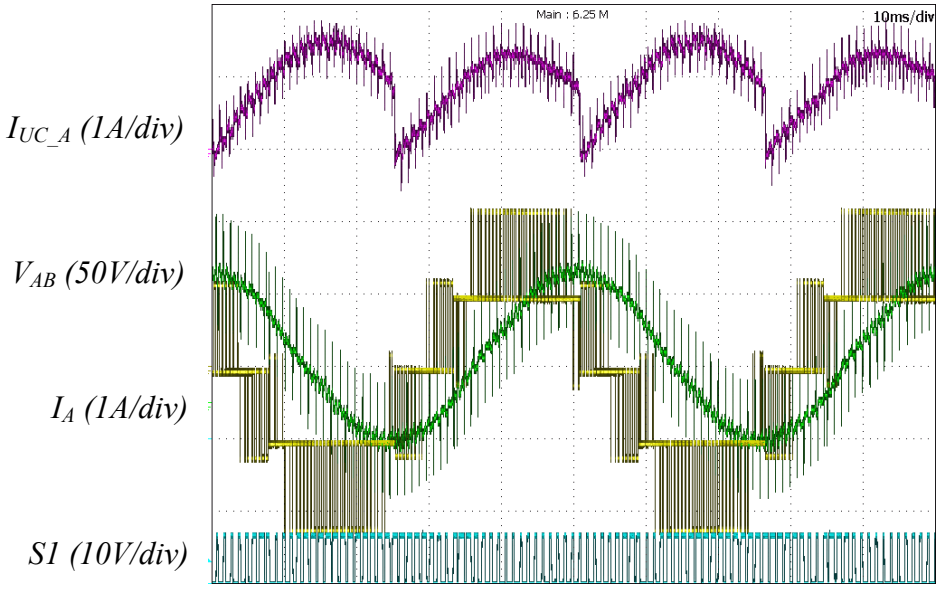
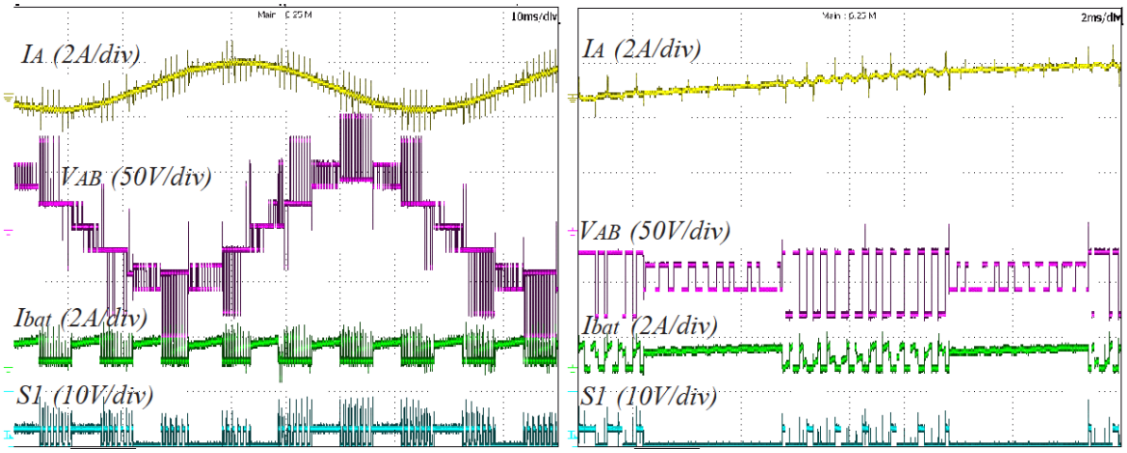


Figure 6-26 Motor phase to phase voltage (V_{AB}), capacitor current (I_{UC_A}), motor phase current (I_A), and three-phase bridge phase A gate signal (S1) for phase shift control in MODE VI modulation mode

6.2.3 Mixed modulation

In cases where the UC's voltage is not sufficient for the continuous six-step switching in MODE II or the required power split cannot be met, then a mixed switching operation has to be used. From earlier mathematical analysis in section 3.5.5 it is known that alternating between two modulation modes will impact output voltage waveform where the harmonic content depends on averaged value between those two modulations. By further simulations in section 5.2.4 it was confirmed that if both modulations modes have low THD the product of those two alternated modulations would have similar harmonic content. The aim of this experiment is to verify empirically the influence of the mixed modulation mode on output voltage and current.

The first waveforms example for mixed operations, including MODE II and MODE IV with $\alpha=\pi/12$, are presented in Figure 6-27.



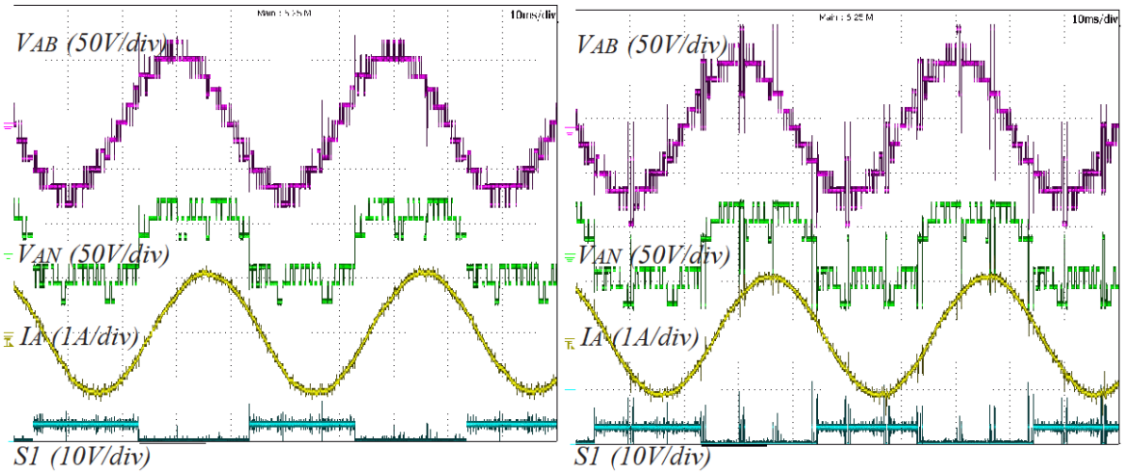
(a) Full waveform (b) Zoomed trace

Figure 6-27 Motor phase current (I_A), phase to phase voltage (V_{AB}), battery current (I_{bat}) and three-phase bridge phase A gate signal (S1) alternated switching between modulation in MODE II and IV for $\alpha = \pi/12$

The mode change does not introduce any additional switching ripples other than the ripples specific to the modulation mode since switching is synchronized with the SVM duty cycle. The presented modulation allowed a reduction in current that is sinking by the battery. In the presented example the amplitude of the main source is around three times greater than the amplitude of the UCs what is related with current ripples around three times higher when the main source is used in SVM. In presented graph it is visible that as soon the modulation MODE IV is used the current ripples in phase current (I_A) increase proportionally but general waveform shape is unchanged. In case of battery current (I_{bat}) the average value is now reduced but the UCs energy contribution is increased.

The next example presents a case where the maximum output from the inverter is generated and the ratio between the voltage of the sources is close to four (Figure 6-28). This allows the maximum number of levels (six voltage levels in phase-to-phase voltage) to be produced, which helps to minimize the ripples in the motor current. The phase current in presented case is almost ideally sinusoidal without any ripples. Since as presented in section 3.4, between the vectors in MODE II empty spaces may start to appear as the UC's discharge and power sharing is limited, then to allow motor operations the modulation in MODE VI has to be added (Figure 6-28 (b)). Introduction of modulation mode

with higher amplitude of switched vector cause increase of the current spikes that are typical for MODE VI. Because the percentage of MODE VI in the modulation is small, the increase in motor current ripples is insignificant.



(a) MODE II only (b) MODE II with added mode VI

Figure 6-28 Motor phase current (I_A), phase to phase voltage (V_{AB}), phase voltage (V_{AN}) and three-phase bridge phase A gate signal (S1) for modulation in mode II and mixed MODE II with MODE VI when capacitor voltage drops

To better quantify relations between the harmonic content and modulation mode the motor phase current data capture was used to calculate harmonic spectrum. The harmonic analysis presented in Figure 6-29 proves that the mixed modulation scheme has a harmonic content that is proportional to the average level between the two modulation schemes. It is also possible to notice that MODEII modulations provides the best results since unwanted harmonics do not reach even amplitude of 1%. In case of MODE IV modulation the amplitude of harmonics related with modulation at 1 kHz reach almost 4% for many harmonics related with modulation frequency. For mixed modulation the peak harmonics remain only at 1.5% but the side bands are slightly wider. The sidebands that can be found around the modulation frequency harmonics have similar spectrum as expected for multilevel inverter as found in the literature (Holmes, 2003).

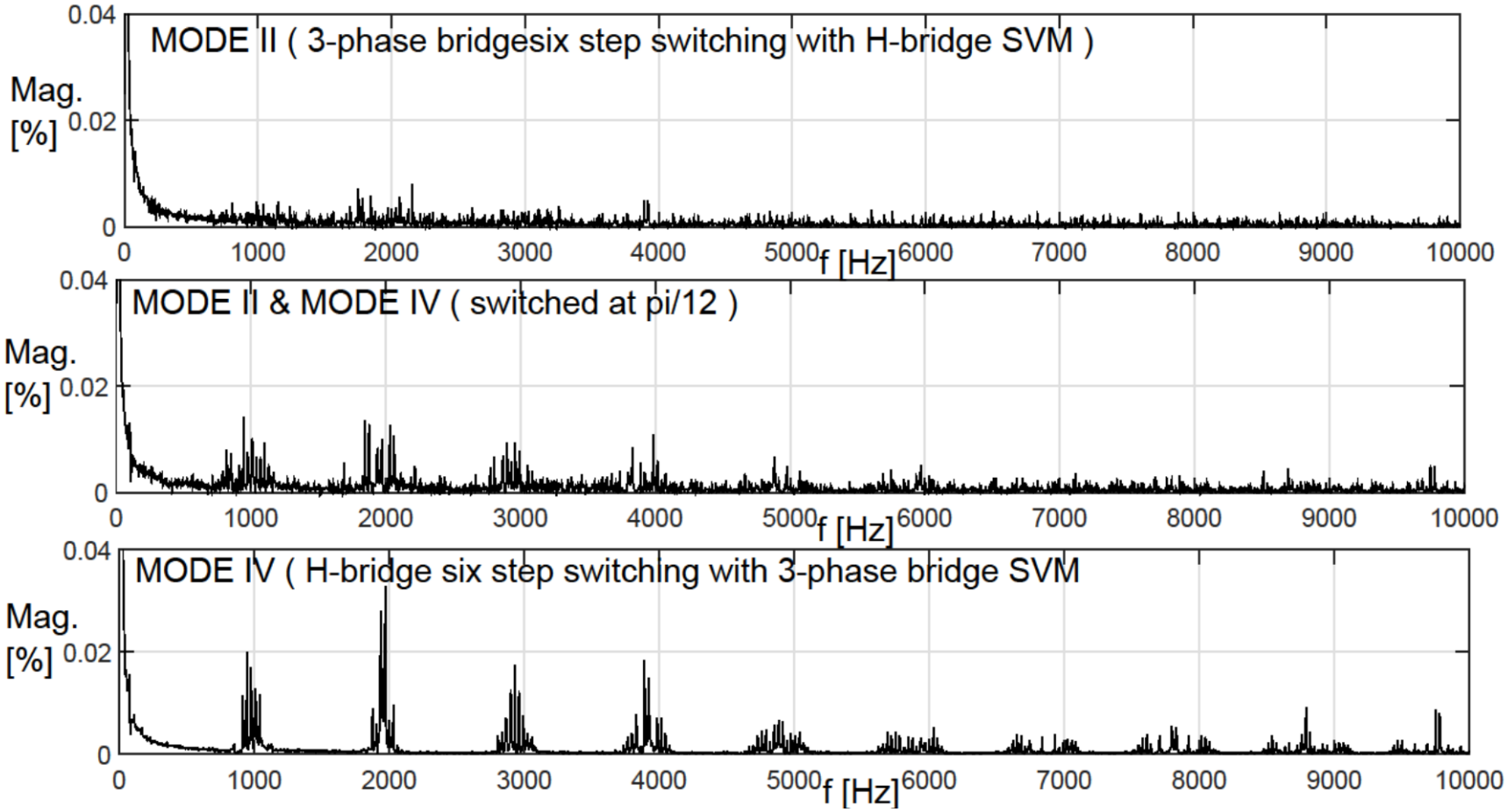
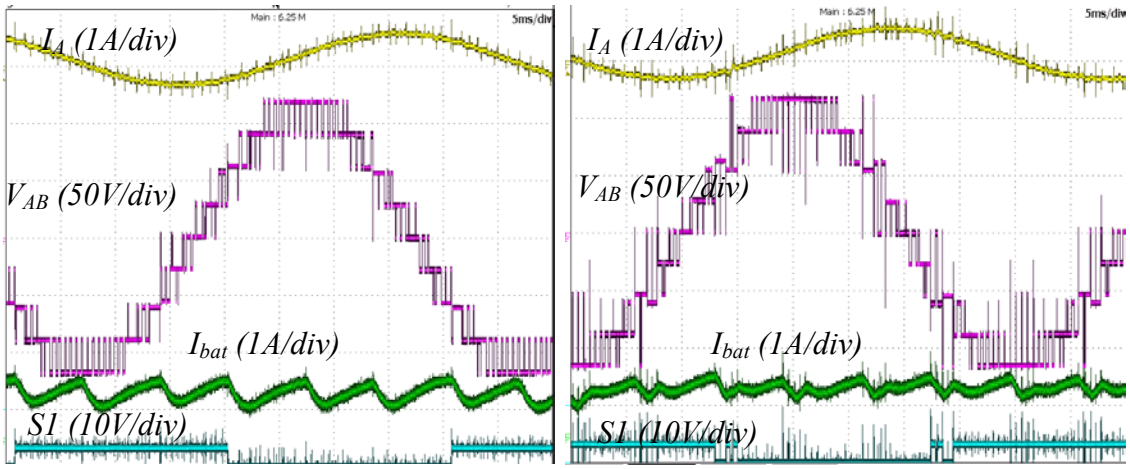


Figure 6-29 Harmonic content (in % 100) in phase current for modulation in MODE II, mixed mode including switching MODE II and MODE IV for $\alpha = \pi/12$ and MODE IV (carrier frequency 977Hz)

Presented earlier case was for MODE II modulation where the output voltage consists of 11 voltage steps. In Figure 6-30 the current waveform was captured for the output phase to phase voltage with nine different voltage levels. With reduced number of output voltage levels the current ripples in the phase current caused by added MODE VI become even harder to distinguish especially for the operations with lower motor load.



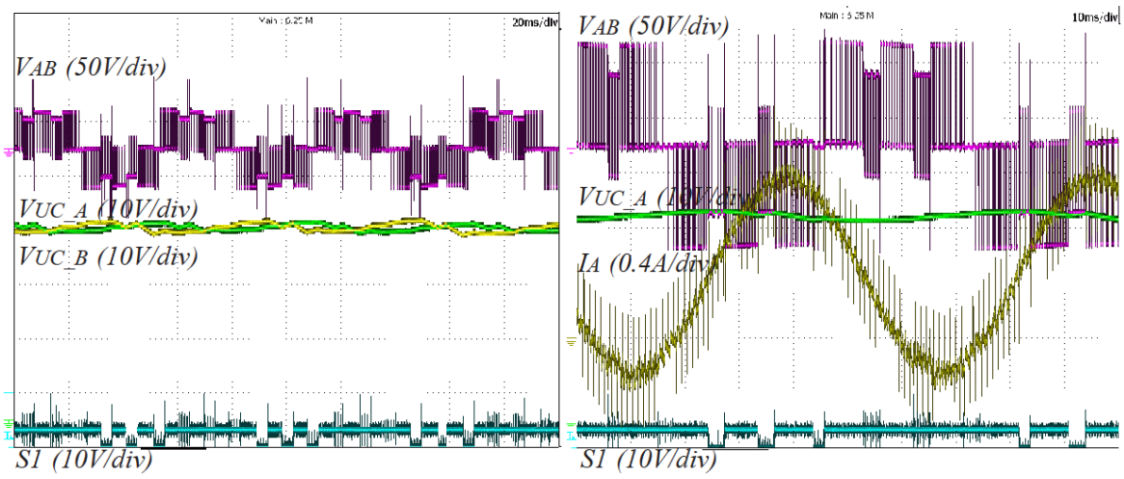
(a) MODE II only (b) MODE II with added MODE VI

Figure 6-30 Motor phase current (I_A), phase to phase voltage (V_{AB}), phase voltage (V_{AN}) and three-phase bridge phase A gate signal (S1) for modulation in MODE II and mixed MODE II with MODE VI

6.2.4 Capacitors voltage regulation

In presented multisource multilevel platform one of the key functions of the modulation algorithm is to keep the same amplitude of each ultracapacitor what is archived by selecting adequate vectors combination (section 3.5.2). Additionally the power management shell is responsible for finding UCs reference voltage so the output voltage has the maximum number of voltage levels, the capability to capture energy from breaking is available and the main voltage source is protected against current transients. To validate stability of regulated capacitor voltage an experiment with 2mF capacitance as a source for the H-Bridge instead of UCs was performed. Lower capacitances allow quicker charge/discharge cycles so more demanding requirements on voltage regulator are put.

In Figure 6-31 the captured waveforms present the variation of the capacitor's voltage but their average value remains stable (UC set voltage around 35V, main source voltage is 62V) and only variations related to H-Bridges switching (around 2V) are present.



(a) Variation during three periods (b) Zoomed view

Figure 6-31 Motor phase to phase voltage (V_{AB}), capacitors voltages (V_{UC_A} and V_{UC_B}) and three-phase bridge phase A gate signal (S1) for capacitors voltage level control for mixed MODE II and III and low reference output voltage

The amplitude of the modulated output voltage is 20V and MODE II alternated with MODE III is used. Because each cycle the capacitor have to compensate passive power its current needs to constantly change direction what cause voltage ripples. Nevertheless even almost 10% voltage oscillations do not lead to capacitors voltage drift from set value. Also the variation in the voltage of the capacitors does not disturb the SVM, what means that the harmonic content in the phase current is unaffected. The mixed modulation mode was also tested for higher output voltage and found that it is still possible to keep capacitors voltage at constant value. As presented in Figure 6-32 the inverter output voltage is set to 40V and the developed control algorithm by switching between MODE II and three level H-Bridge modulations is able to stabilize 2mF capacitors when the motor current has 1A amplitude.

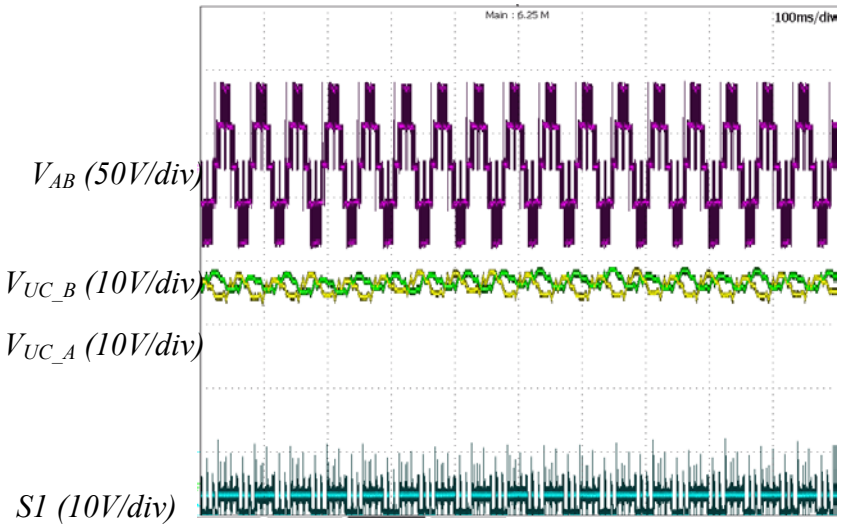
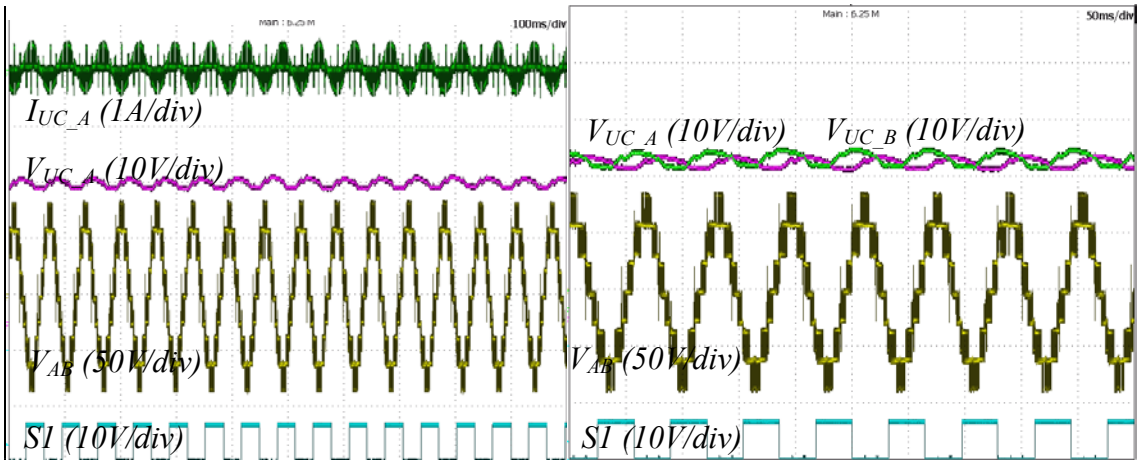


Figure 6-32 Motor phase to phase voltage (V_{AB}), capacitors voltages (V_{UC_A} and V_{UC_B}) and three-phase bridge phase A gate signal (S1) for capacitors voltage level control for mixed MODE II and III, and for high reference output voltage

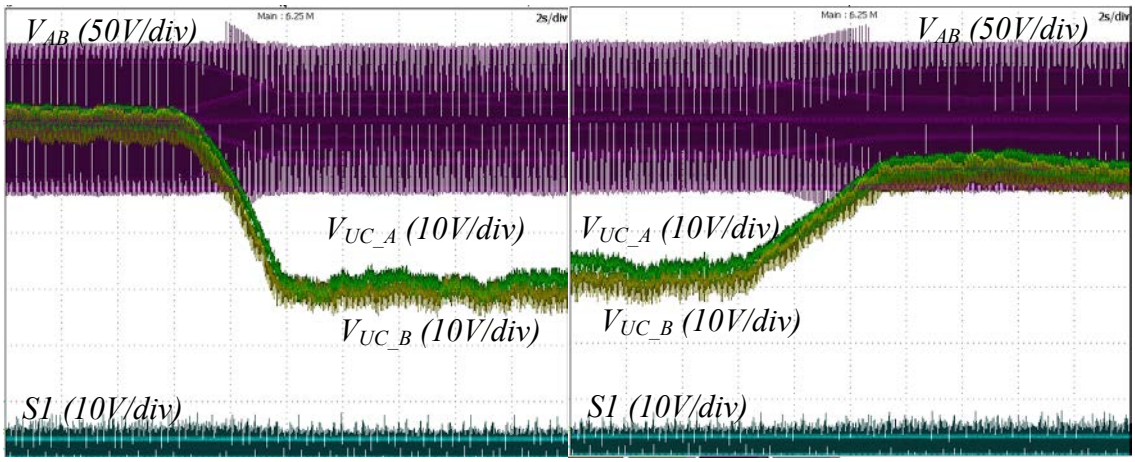
It was proven that for the whole range of output voltage it is possible to maintain the capacitor's voltage with constant amplitude. The mixed modulation strategy was found to be efficient for the capacitor's voltage control.

For higher output voltage the UCs reference voltage can be adjusted by the phase shift control. In Figure 6-33 an example of capacitors voltage regulation with phase shift power control is presented for modulation in MODE II. In presented graphs it is shown that the capacitors voltage oscillation (V_{UC_A}) are related directly with their non-active current (I_{UC_A}) and their average value is remaining zero, meaning that the active power is delivered only by the main voltage source. Since the SVM algorithm use latest capacitors voltage value with resolution of 16μs, the modulated output voltage is not affected by the capacitors voltage oscillations. Implemented voltage vector selection for H-Bridge SVM is also able to keep all three capacitors at same reference level what is visible in Figure 6-33(b).



(a) Capacitor current variation (b) Voltage variation between two capacitors

Figure 6-33 Motor phase to phase voltage (V_{AB}), capacitor current (I_{UC_A}), capacitors voltages (V_{UC_A} and V_{UC_B}) and three-phase bridge phase A gate signal (S1) for capacitors voltage level control for MODE II and high reference output voltage



(a) New reference point 20V (b) New reference point 40V

Figure 6-34 Motor phase to phase voltage (V_{AB}), capacitor voltages (V_{UC_A} and V_{UC_B}) and three-phase bridge phase A gate signal (S1) for capacitors voltage regulation on step change for MODE II modulation

The capacitors voltage regulation was also tested on step response when a new capacitor reference is set. As presented in Figure 6-34 the voltage regulation is stable and it is possible to change capacitors voltage without any overshoot. During transitions both capacitors keep the same voltage value and in around 3 to 4 seconds are able to reach set point by adjusting phase shift

angle in MODE II modulation. This shows that introduced theory (section 3.6.2) to adjust capacitors voltage for minimum current ripples can be implemented also for system with three voltage sources types that was presented in section 3.7.3.

In the next test the capacitor voltage regulation is validated under dynamically changing motor load condition. Performed experiment aim to find system stability when the load current is rapidly changing. Presented results in Figure 6-35 shows data capture for inverter operating in MODE II modulation when the phase current for six periods was increased by almost 50%. In response to changing conditions the control logic was able to keep capacitors voltage at same value. It can be also noticed that with load current increase the oscillations in capacitors voltage get higher but this doesn't have influence on average regulated UCs voltage.

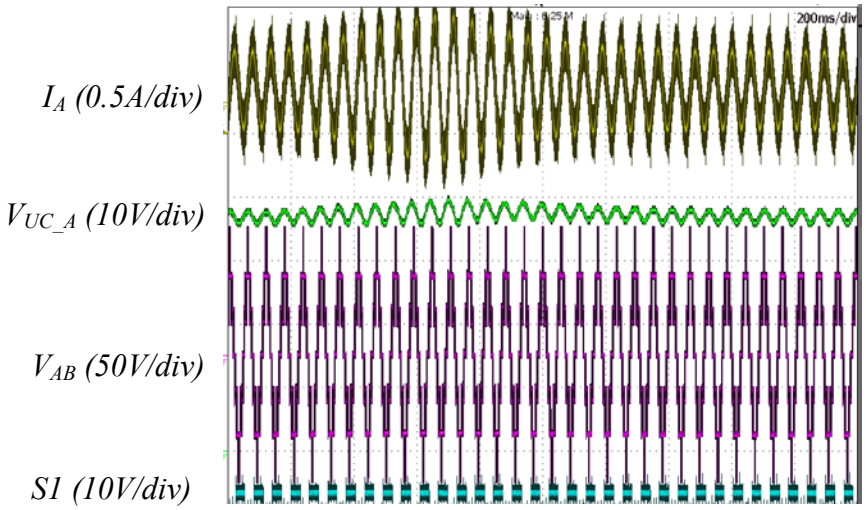


Figure 6-35 Motor phase to phase voltage (V_{AB}), phase current (I_A), capacitor voltage (V_{UC_A}) and three-phase bridge phase A gate signal (S1) for capacitors voltage regulation on dynamic current change for MODE II modulation

The final experiment with capacitor voltage included a test with modified cascade inverter that has H-Bridge section switched from low energy capacitor to UCs. This test aim to verify SVM modulator response when the inverter is switched to use voltage sources with different amplitude. The test supposed to examine how inverter with three sources types from section 3.7.3 could operate.

Figure 6-36 shows that dynamic H-Bridge source change from 2mF electrolytic capacitors charged at 45V and replaced by 19F UCs at 35V will not cause any system instability and inverter is able to continue generate same reference output voltage.

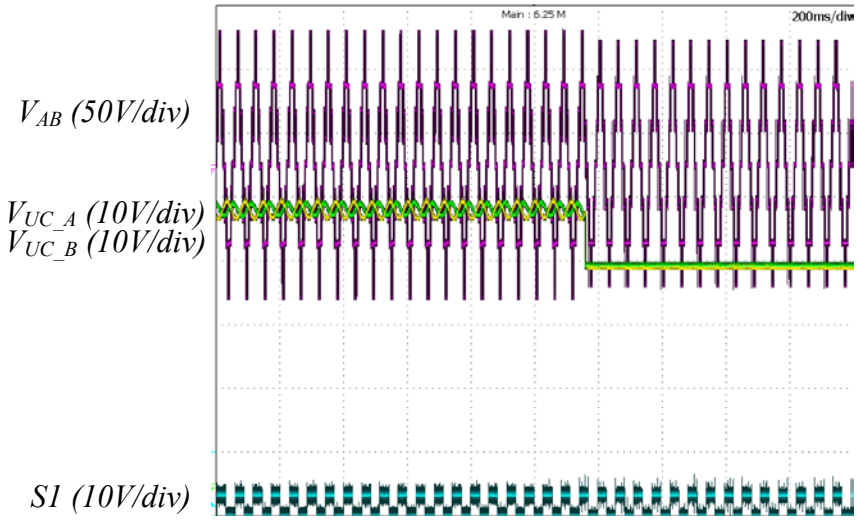
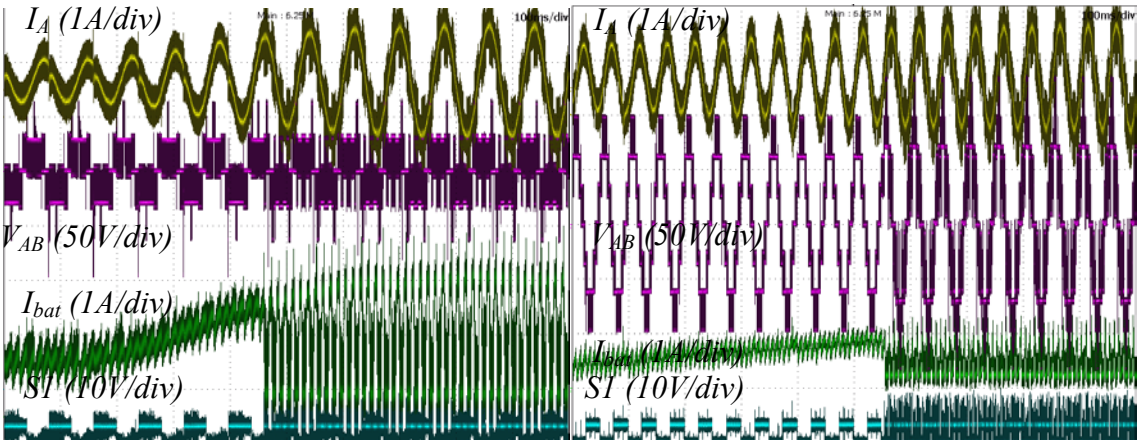


Figure 6-36 Motor phase to phase voltage (V_{AB}), capacitor voltages (V_{UC_A} and V_{UC_B}) and three-phase bridge phase A gate signal (S1) during H-Bridge source change from electrolytic capacitors to UCs for MODE II modulation

6.2.5 Main voltage source current control

The main purpose of the multisource system is to protect the main voltage source against rapid overloads. For this purpose in case when current is higher than the maximum set value, the system control should distribute power to second source. The aim of performed test is to verify if control is able to detect source current increase and change modulation mode so the battery current remains within its limit and inverter output voltage is unchanged. In Figure 6-37 a transient response on phase current increase is presented starting from default modulation in MODE II. In first case the modulated output voltage is equal to 20V and in second case 75V. In moment when the battery current is reaching its maximum set value the modulation mode is changed. In first case the MODE II modulation become alternated with MODE III modulation. In second case the modulation mode is switched directly to MODE VI since high output voltage from H-Bridge inverter is required. The change in modulation

strategy does not impact phase current and output voltage (only slightly higher ripples in phase current) but the battery current is instantaneously reduced.



(a) MODE II to mixed modulation (b) MODE II to MODE VI modulation

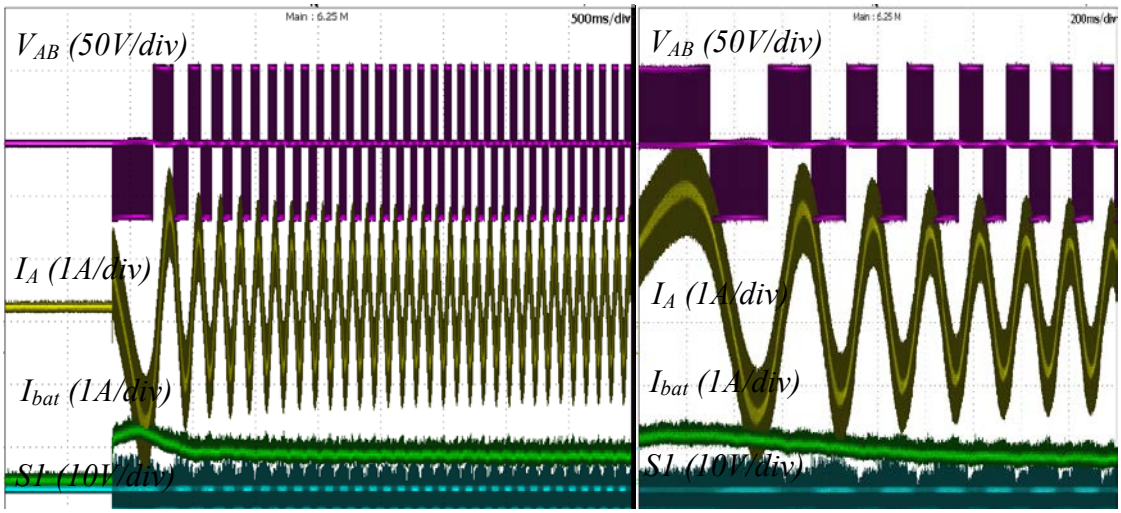
Figure 6-37 Motor phase to phase voltage (V_{AB}), phase current (I_A), battery current (I_B), and three-phase bridge phase A gate signal (S1) during transition when battery current increase above set threshold

6.2.6 Motor acceleration profiles

A power-management algorithm was also validated during motor acceleration with the aim of providing a smooth battery current rise and avoid an increase in its average value over a set threshold. The modulation controller should also select correct modulation strategy that is able to generate output voltage with the lowest number of unwanted distortions and to control UCs reference voltage. To have comparison with traditional two level inverter supplied by the single voltage source the initial test was performed with platform configured to operate with three-phase bridge only and with power management disabled. During all tests the battery current as well phase to phase voltage and phase current was monitored. The motor for all cases was starting from zero speed up to set speed of 2000rpm with same initial load.

The results in Figure 6-38 from the first test with only three-phase bridge shows that initial motor phase current on the motor start is around 50% higher than nominal. In this case, since battery is the only voltage source, its current increases proportionally. The current ripples for this case remains constant

since the same modulation strategy is used during whole motor acceleration. This type of current profile could put additional stress on the voltage source, since big current value appears instantaneously and excides it nominal value what could have impact on batteries lifetime.

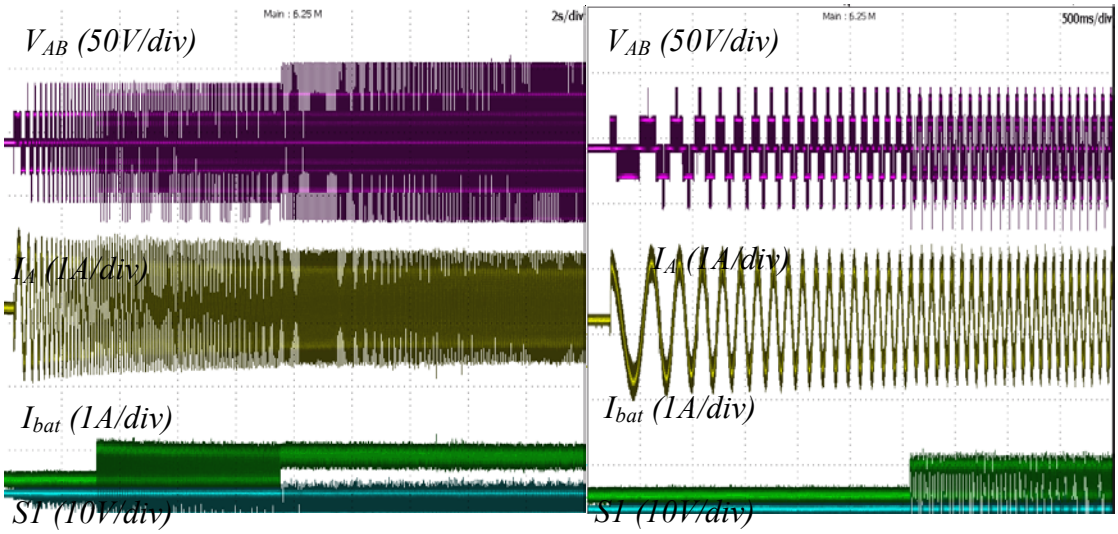


(a) Full acceleration profile (b) Zoomed profile

Figure 6-38 Motor phase to phase voltage (V_{AB}), phase current (I_A), battery current (I_{bat}) and three-phase bridge phase A gate signal (S1) during motor acceleration form 0rpm to 2000rpm for two level operation without power sharing control

In the next experiment the UCs were charged first to around 30V and power management was set to reduce stored energy in them. The motor was started with same load and speed set point. As presented in Figure 6-39 the power management control selected initially only modulation with H-Bridge section (MODE III) to use solely energy stored in capacitors. With further speed increase the modulation strategy started to introduce mixed modulation and to alternate MODE II with MODE III what allowed to modulate higher amplitude of inverter output voltage. At the end when motor current starts to stabilize and motor reaches its speed set point the modulation mode is switched to MODE II only. The energy excess that was stored in capacitors at start-up was transferred to the load during acceleration and system is remaining in steady defined conditions. Presented power management during acceleration allowed not only to regulate capacitors to a new reference value but provided graduate

battery current (I_{bat}) increase. Thanks to this control the main voltage source was protected against high motor inrush current.



(a) Full acceleration profile (b) Zoomed profile

Figure 6-39 Motor phase to phase voltage (V_{AB}), phase current (I_A), battery current (I_{bat}) and three-phase bridge phase A gate signal (S1) during motor acceleration form 0rpm to 2000rpm for motor stating profile starting with H-Bridges only then mixed operation with MODE II and MODE III and finally MODE II

In the final experiment a power management algorithm was validated during motor acceleration with the aim of providing a smooth battery current rise and avoiding an increase in its average value over a set threshold. In this case a UCs voltage reference was not used. In Figure 6-40 an example profile is presented where the motor is accelerating from zero speed up to 2,000rpm with fully charged UCs ($V_{bat}=2V_{uc}$). During acceleration first MODE III is used to cope with the initial inrush current and then gradually the three-phase bridge starts to be added (MODE II with MODE III). When the reference voltage is high enough the inverter changes into operation with the three-phase bridge in six-step switching (MODE II). To limit the current that is seen by the main source initially the inverter operates with the maximum phase shift angle "χ" and as the motor current decreases the phase shift is reduced which can be observed as reduced ripples in the main source current (green).

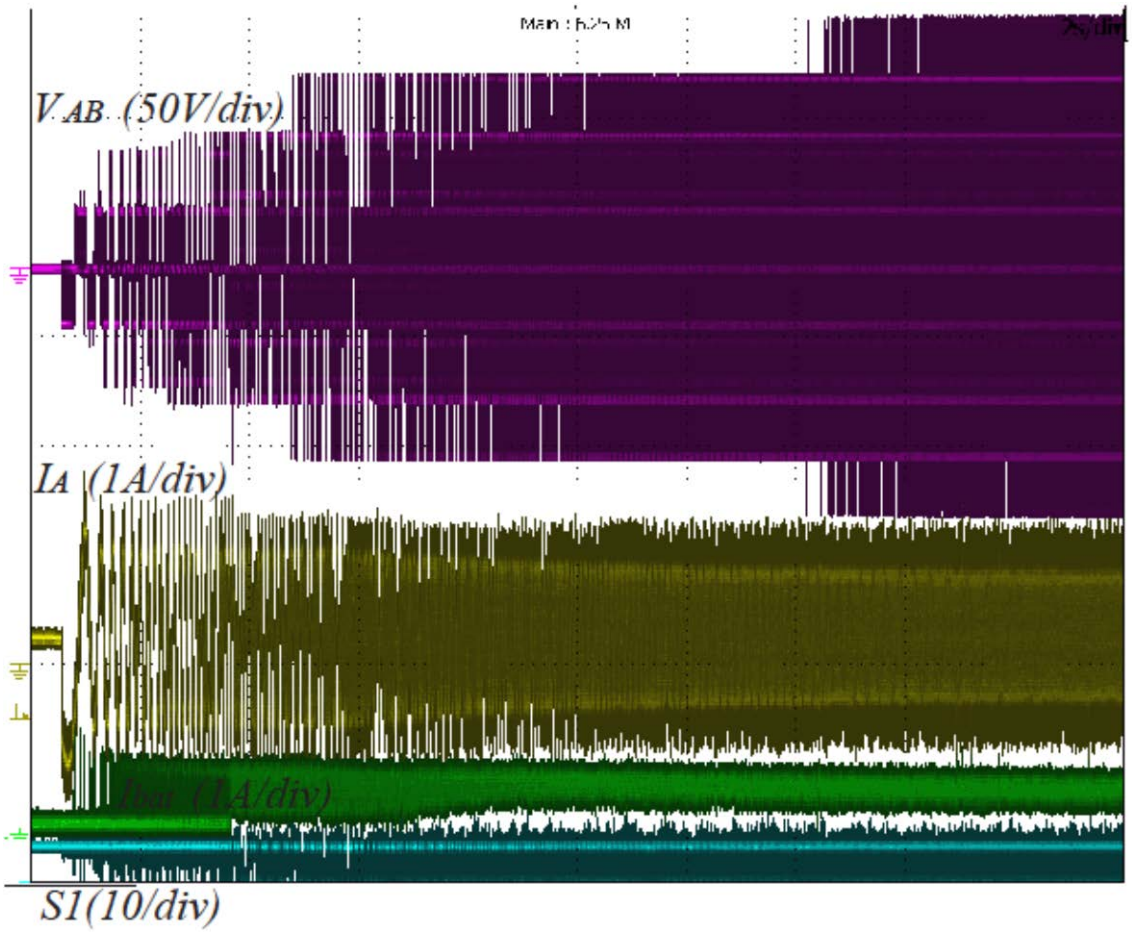


Figure 6-40 Motor phase to phase voltage (V_{AB}), phase current (I_A), battery current (I_{bat}) and three-phase bridge phase A gate signal (S1) during motor acceleration form 0rpm to 2000rpm with battery current control

From capture waveforms we can conclude that the battery current control work effectively under dynamically changing conditions and linearly adapt to variable battery current. At the same time the modulation strategies that are selected provide lowest switching ripples since for the majority of motor acceleration the power distribution is achieve by MODE II phase shift control.

6.3 Summary

In this chapter the physical implementation of proposed system is first presented to provide good understanding of the system architecture. It was shown that developed platform do not require sophisticated electronic components but can be developed with existing technology on the market. Particularly the presented control platform consisted of FPGA and processor

that are available on the market for more than a decade. This means that with existing technology the control method could be easily expanded.

In further part of this chapter the experimental validation of developed platform was accomplish. In first tests it was proven that the SVM modulator is operating as expected and waveforms are similar to the ones from the simulations. In further part of validation the strategy to control power sharing by phase shift and mixed modulation is reviewed. From results it was found that the developed novel modulation strategy is able to distribute power between sources, regulate capacitors voltage and do not introduce additional harmonics inside voltage and current spectrum. Most of the electrical standards define harmonic limits for nonlinear loads but do not define limits for internal characteristics of motor drives since the configuration motor and converter is treated often as a single system. Nevertheless it can be assumed that a well performing system should not generate distortions above the limits defined in the most popular IEEE 519-2014 standard (Committee, Power and Society, 2014). It is recommended for low voltage and low current loads to limit the total current distortion at level lower than 5%, for individual harmonics from 3^{rd} to 11^{th} distortions should be lower than 4%, for harmonics 11^{th} to 17^{th} lower than 2% and for harmonics 17^{th} to 23^{rd} lower than 1.5%. As presented in Figure 6-29 for tested modulation modes the total current distortions were always lower than 5% and in case of individual harmonics only in MODE IV modulation one harmonic was above threshold. Yet as soon MODE IV was mixed with MODE II modulation the harmonics spectrum was meeting IEEE 519-2014 standard. The SVM modulator as well as power management shell was also validated for its ability to regulate capacitors voltage. In completed tests the UCs were replaced with 10000 time's smaller capacitors and developed control method was capable to keep all three capacitors at set reference voltage even under dynamically changing motor operating conditions. The battery current limiting strategy was additionally examined and proved that the main voltage source can be protected against load current variations. In the final tests the system was examined under motor accelerations to find how power management and modulation control is adapting to the variable conditions. The results proved that

the control is stable and is capable to adapt when rapidly changing conditions occur. The power management shell during whole acceleration profile linearly controlled battery current avoiding its overloading with instantaneous response since developed control is operating with 1ms cycle. The results show that the system not only allows distributing power between sources instantaneously but also improve voltage and current harmonic content and reduces current ripples.

CHAPTER 7 CONCLUSIONS

7.1 Discussions

This thesis presents the problems related with multisource systems and their direct implementation into multilevel converters for motor drive applications. The work aimed to find a solution for systems with two sources, where one has a variable limited current and the other is used to compensate instantaneous power variations. To achieve the research objective existing topologies were first analysed to find their limitations and identify solutions that could increase the efficiency, extend the battery life, reduce current ripples and THD, reduce switching losses and switching stress, improve transient response and extend performance at high speed. The direct integration of a second source type into the multilevel inverter was identified as a valuable option to reduce passive components such as inductors and at the same time reduce voltage ripples. It was also identified that the biggest challenge with the direct integration of UCs into a multilevel structure is their constantly changing amplitude during charge/discharge cycles, also causing the voltage vectors coordinates to vary. The modulation strategies become even more difficult if it is necessary to select voltage vectors to provide set power share between sources.

The analysis of voltage vectors that was carried out allowed the identification of possible modulation schemes (of which there were six main ones), the analysis of their voltage limitations and the formulation of their active power equations. The control algorithm has been designed to minimise influence of variable amplitude of voltage sources on output voltage. To control power flow between the sources it was established that two control methods are necessary, either by phase shift or by switching between modulation methods depending on inverter status and reference voltage vector. The thesis has also analysed the use of the UC's voltage to minimise switching losses and the harmonic content of the output voltage. It was proposed to control the UC's voltage by power management to maximize the recuperated energy or to achieve the maximum number of levels. Since these requirements are contradictory, a hardware modification to the H-Bridge structure was proposed to introduce an additional

low-energy and high-power source. Ideas were presented for the further modification of the structure for additional improvements to the performance of the system. It is also worth mentioning that when the UCs and battery are sourcing current at the same time it is possible to achieve even higher voltage output. The sum of the battery and UCs is the maximum amplitude in that case. This allows for the production of high voltage high current for short durations, for example during motor acceleration when back EMF is high.

To validate the proposed method the multisource system was first simulated in Matlab/Simulink and then an experimental platform was developed from discrete components with control algorithm implemented on the C-Rio platform with FPGA. The developed hardware together with its control algorithm presents a platform for further research in the field of multilevel inverters with multiple source types.

The solutions to use multilevel inverter structure for multisource systems existed in literature but never become popular since proposed control methods are very complex and do not provide solutions for all operating conditions. This thesis proved that it is possible to implement multiple voltage sources with variable amplitude into multilevel inverter structure by utilizing introduced novel method. Also the error between reference and output voltage has been minimized by including constant voltage monitoring for each SVM duty cycle. The proposed system has been shown to fully utilize the UCs and increase output voltage in comparison to conventional three-phase bridges while at the same time maintaining constant voltage at the UCs. These results demonstrate that the proposed configuration provides an effective method of power flow management between the battery and the UC and is able to maintain a stable output during transient states while enhancing the performance of the drivetrain. The change in power sharing between sources is only limited by the duty cycle of SVM modulation (1ms) what allows to almost instantaneously increase decrease output power from sources. The concept of modulation strategy and power control was found to be robust and it does not require significant resources in terms of FPGA size and processor performance. The scheme

proved to be a feasible solution for hardware implementation, allowing the opportunity for further use of this type of system for commercial applications.

The main aspect that limits novel solutions their market penetration is mainly product cost. The multisource systems were introduced more than decade ago but this type of topologies never become mainstream products mainly because of their higher cost against benefits they provide. In this thesis it was proposed to use the multilevel inverter structure for multisource system to improve motor drive capability and reduce its cost. By implementing proposed structure the multisource system doesn't include additional DC to DC converters to interface multiple voltage sources but instead allows voltage sources direct integration within converter. The multilevel solution increased number of switches needed for three-phase converter from six to 18. Nevertheless proposed system implementation eliminated need of DC to DC converters that require eight power switches and additionally include expensive and bulky wound components. The second advantage of proposed system is its control that is centralized in one unit when in conventional systems the separate controllers are needed for each voltage conversion stage. It is also worth to mention that since the H-Bridge section is supplied by capacitors with voltage that is 50% lower than main source voltage, then the switches that are used for H-Bridges can be rated with the smaller power what additionally reduces their cost. Base on those assumptions it can be expected that developed system should at last do not exceed price of conventional multisource system.

7.2 Conclusions

The work has presented solutions to several issues and problems that have not been addressed in previous works on multisource multilevel structures. Based on the conducted investigations, the following conclusions can be drawn in this study.

7.2.1 Voltage vectors limitations

The main problem with direct integration of the multiple sources into multilevel inverter structure is the voltage sources variable amplitude. As presented in

Chapter 3 this leads to variation of available voltage vectors and make standard modulation impossible. Based on performed analysis it was possible to find relations between the voltage sources amplitude and available voltage vectors. This allowed identifying modulation modes and their critical parameters. This novel modulation strategy provide fully utilization of available voltage sources and allows to maximize inverter output voltage. The experimental results proved that thanks to constant voltage vectors limits monitoring it become possible to accurately select the modulation mode that is able to generate requested inverter output voltage with the lowest harmonic content.

7.2.2 Phase shift power regulation

The main function of multisource system is to distribute active power between the sources. From active power analysis for defined modes it was possible to find relation between the power distributions and to introduce new power control parameter. Thanks to developed phase shift regulation the active power that each voltage source provides can be accurately controlled. During experimental validation it was confirmed that this method allows having stable capacitor voltage regulation and can alter power delivered by main source by 25%. The method was found to have no advert effects on output voltage quality.

7.2.3 Mixed modulation strategy

It was found that the phase shift power control is limited to only few conditions and do not provide full power regulation. Also since depending on the UCs voltage and reference output voltage it is not always available to modulate the reference output voltage vector through the whole period. The research found that it is possible to alternate between two modulation methods to improve inverter performance. The proposed method was validated through the experimental tests and proves that it is feasible to expand operating range with only small increase in unwanted harmonic and additionally to improve control power distribution between sources. It was found that method allows to accurately regulate power delivered to UCs and to control their reference value.

7.2.4 Control for maximum number of voltage levels

The further inverter analysis defined a novel control method to find UCs reference voltage that is able to provide the maximum number of voltage levels at inverter output in case when the main source delivers only active power. Derived control identifies a new UCs value depending on requested output voltage value and provides its control parameters when motor drive remains in steady state. During experimental test it was confirmed that the calculated UCs value can provide the lowest harmonics and with defined parameters no active power is delivered from the UCs.

7.2.5 Modification to inverter structure

The hybrid cascade multilevel inverter that was implemented into multisource system was found to have lower performance in case the UC voltage is much smaller than the main supply. To overcome this problem the inverter structure was studied to find improvement to its structure. The research found that by integration of the third low power voltage source (electrolytic capacitor) the inverter limits can be improved. The proposed change requires implementation of additional six switches what increases system cost and is the main drawback of proposed solution. Since the additional switches are switched only under zero current, then the modification cost could be not significant.

7.3 Future work

As presented in this thesis, a multilevel topology with multiple sources can be an attractive solution for a drivetrain application, achieving as it does an increase in performance at relatively low cost and without a great increase in complexity. The work focused mainly on its automotive application, while the control method and topology could be easily adapted for other types of units, such as wind turbine generators, solar panels and active filters. The main advantage of connecting such a system to the grid would be the ability to capture or source high values of transient instantaneous power without affecting harmonic distortion in output voltage. For power-generation applications it would allow stabilization of the outputted power and maximization of the energy

produced. The proposed structure could also be beneficial for other low-power high-energy sources such as fuel cells.

This research was limited mainly to the topology of the modified hybrid cascade multilevel inverter. However, as presented in Chapter 2, there are many possibilities for the implementation of a multisource structure with a multilevel inverter. The control strategy that was implemented could be scaled into other structures to meet more specific mission objectives. The work also presented in Chapter 3 potential modifications to the cascade inverter that could further increase drive performance without drastically increasing unit cost.

The analysis of drive performance was limited to a simple load break. Yet by upgrading the motor loading method it would become possible to better validate the system's dynamic performance in four quadrant motor operations. It was also only mentioned that the reference stator flux could be adjusted specifically to the inverter available active and passive power. By implementing a stator reference control strategy, however, it would be possible to increase the efficiency of the motor drive further.

In light of the present analysis the following goals for further work can be identified:

- Modification to the hardware that will allow its connection to the grid. By including additional analogue channels to provide information about grid three-phase voltage and by introducing additional line impedance it would become possible to connect the inverter to a three-phase network. In this case its upgraded control algorithm should allow the compensation of unwanted harmonics in the system and at the same time the capture of rapid power variation providing low THD in the output voltage.

- Adaptation of the developed control method for other multilevel inverter topologies with more source types. By introducing additional low power voltage source the UCs could be used solely for instantaneous power capture when additional source could be tasked to improve system efficiency.

- Upgrading the inverter load by replacing the induction motor torque break for a complete dynamometer setup to allow better validation of the breaking and acceleration profiles. This would generate an improved characterization of the developed system to find its best control strategy and validate the system's efficiency.

- Optimizing motor flux control according to the available active and passive power available from the inverter. This would allow maximizing motor speed in flux weakening region depending on UCs state of charge. Also efficiency of the motor drive could be improved by this method.

The research presented herein proposes a solution that increases inverter performance while overcoming its limitations, not only in the case of a cascade hybrid inverter but which could be implemented in various topologies. Due to the system's unique power transfer capability it could find many applications where load has very dynamic variation and supply voltage source has implemented operational limitations. The modular structure of this inverter and the easily adaptable control system present opportunities to easily access and modify the system structure and energy management.

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APPENDICES

Appendix A Control system design - Labview implementation

The core of the program has been implemented in FPGA on C-RIO platform where the main functions of the code are:

- Interface to power control and flux regulation
- System safety control
- Encoder A, B, Z for speed control
- Analogue inputs interface
- Digital filtering
- Counters and triggers for SVM
- Digital filters for high speed data
- SVM with power transfer control
- P and Q power calculations
- Flux and torque estimation

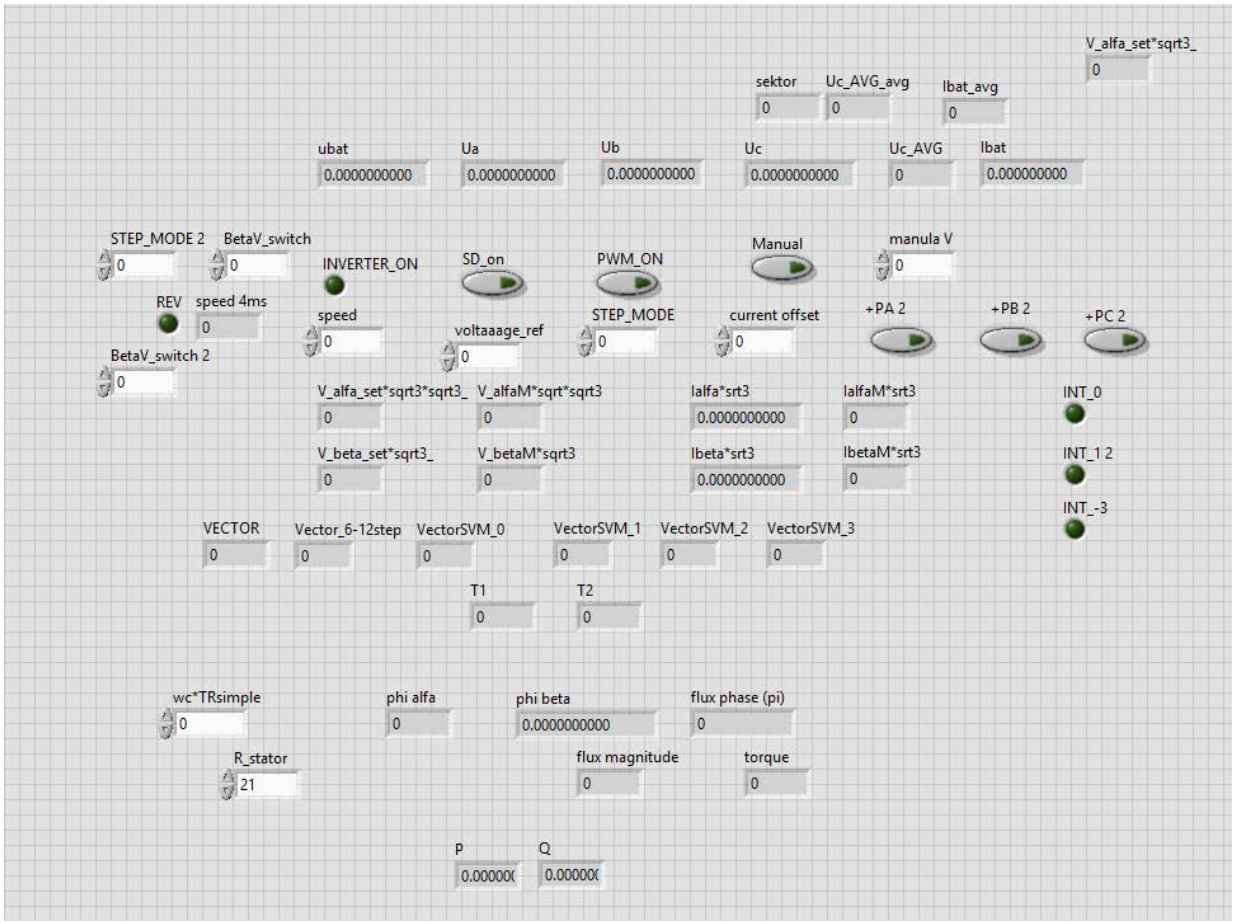

Figure A-1 FPGA code interface

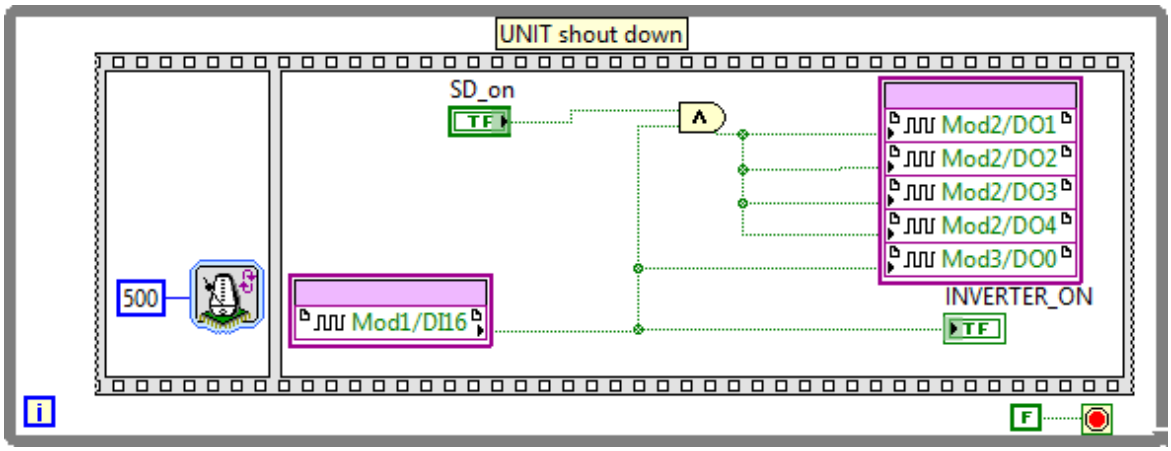

Figure A-2 Safety power ON and OFF switch for cascade inverter

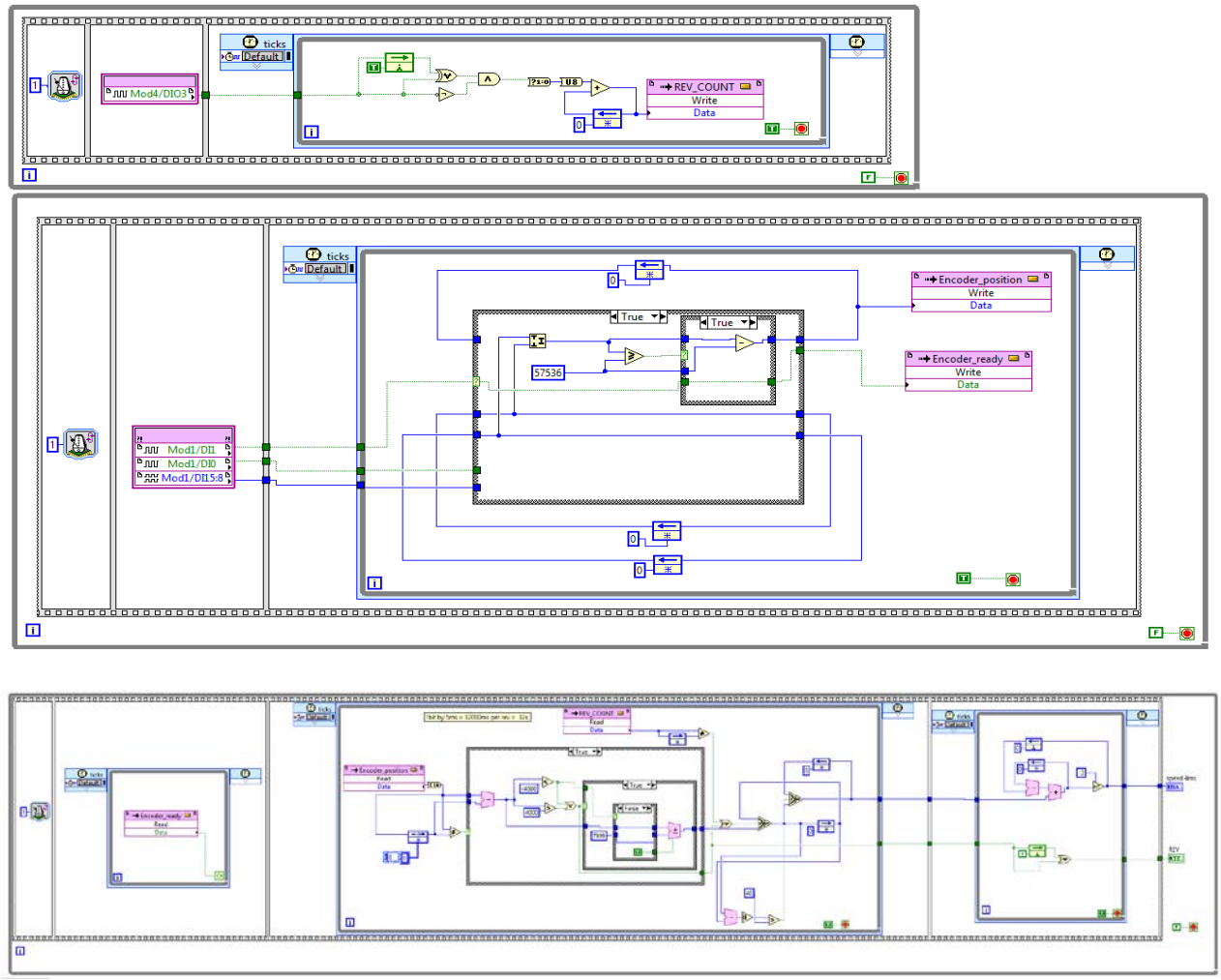

Figure A-3 Encoder interface and speed measurement

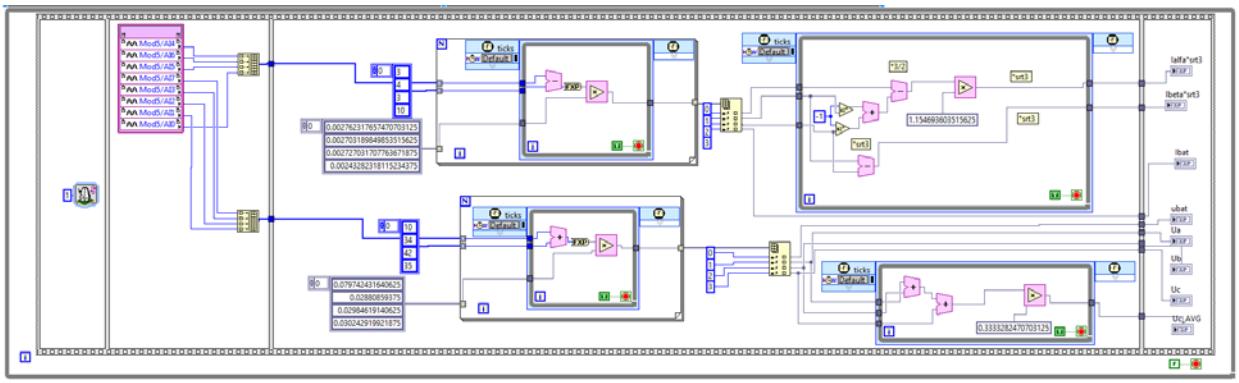

Figure A-4 Analogue input interface for eight ADC channels with 16µs sampling and signal scaling

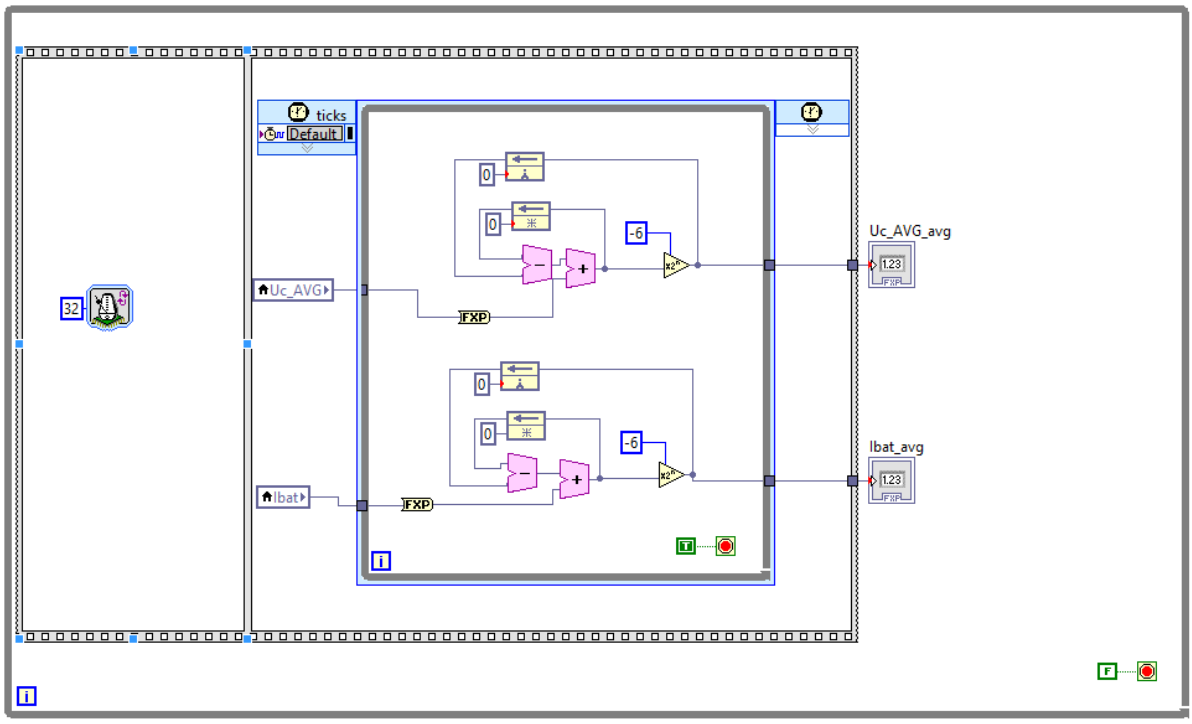

Figure A-5 Low pass filtering for analogue data

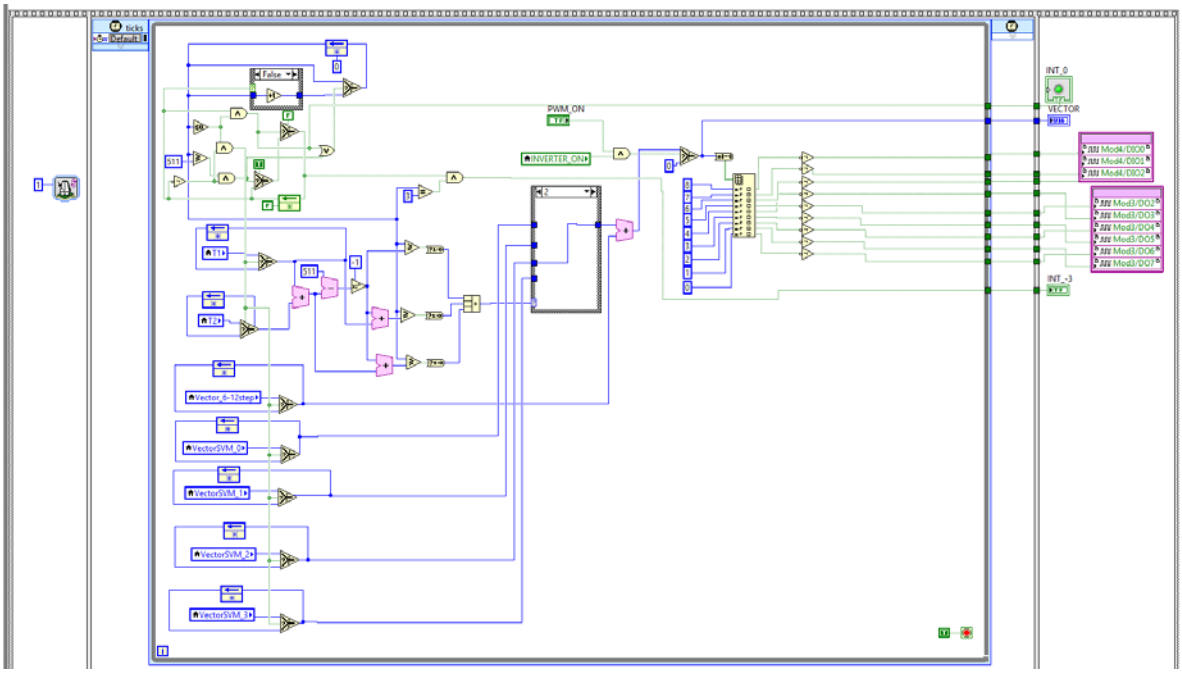

Figure A-6 SVM counter and output triggers for hybrid cascade inverter

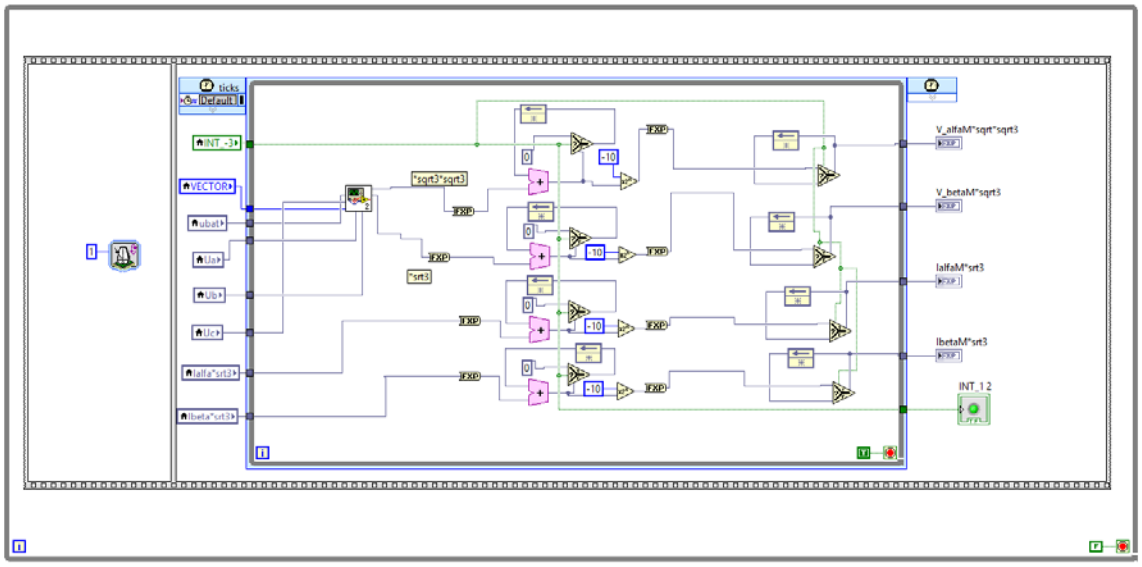

Figure A-7 Digital filtering for high speed data

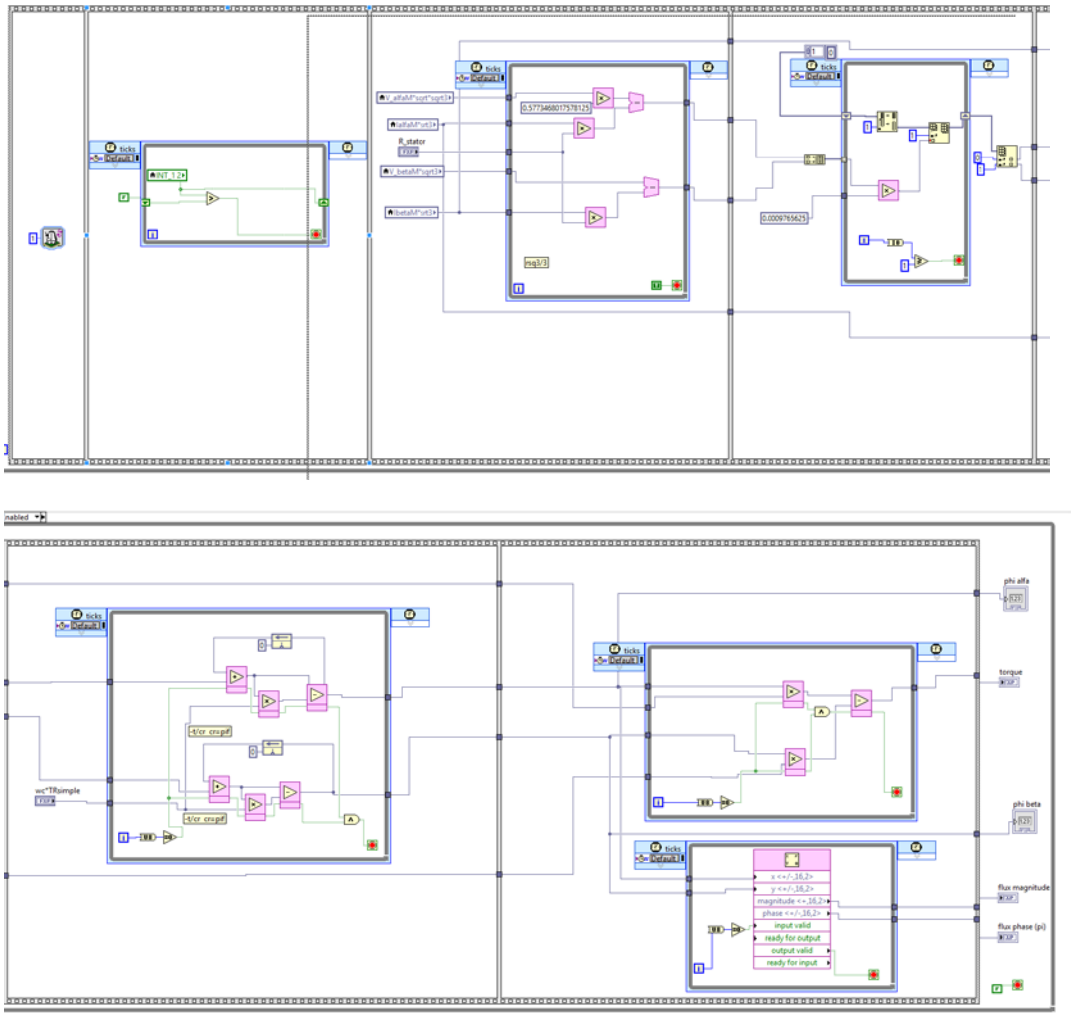

Figure A-8 Flux and torque estimation

Algorithm for SVM dwell time calculation and vector selection to accomplish power transfer is consisting of following stages:

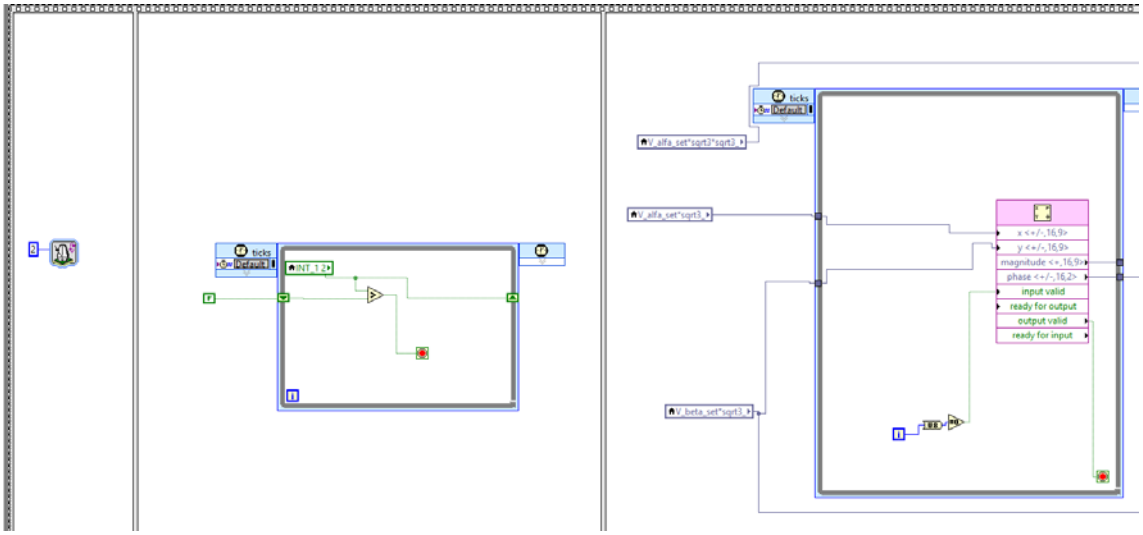

Figure A-9 Calculation of voltage vector phase angle from α β coordinates

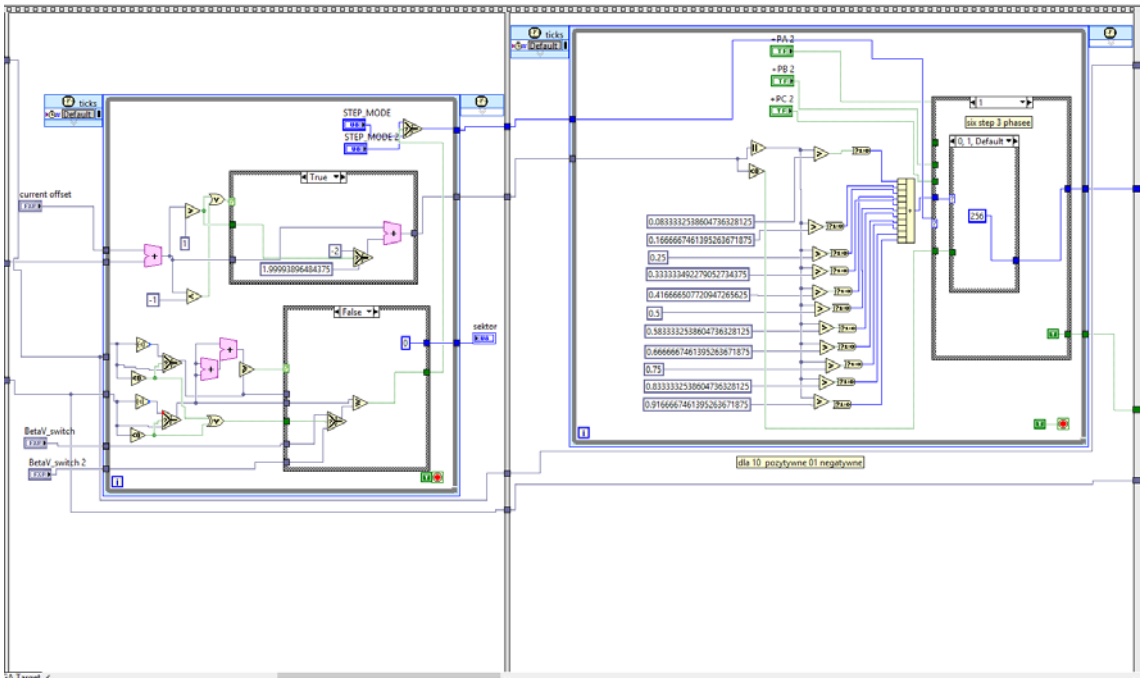

Figure A-10 Comparison of switch angle "α" in with reference voltage in β plane and vector selection for six step switching

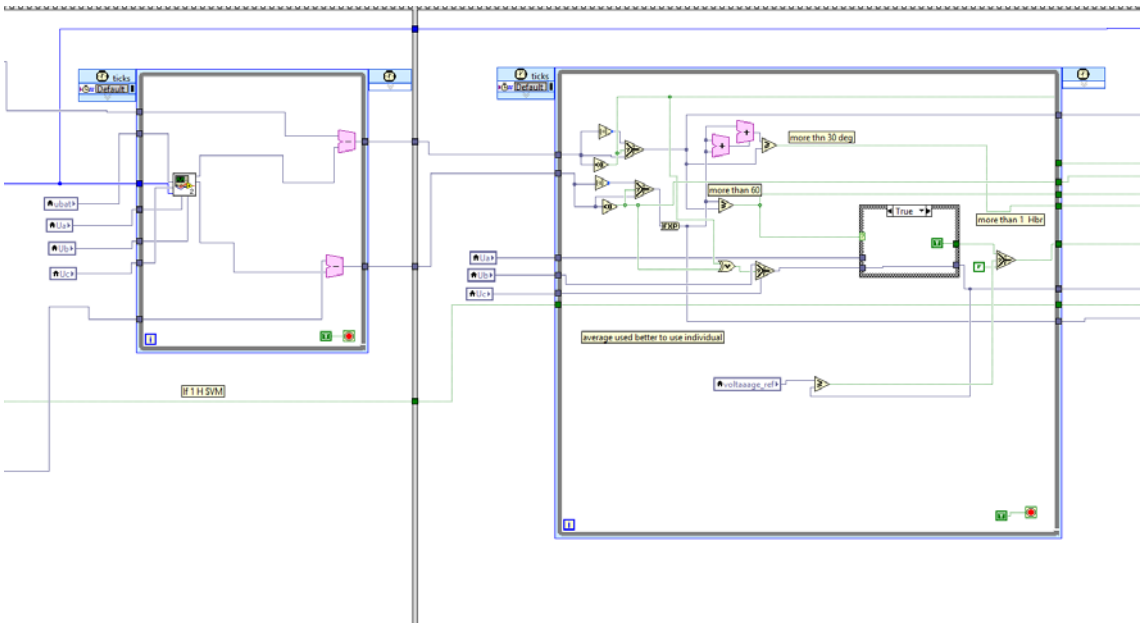

Figure A-11 Subtraction of six-step waveform from reference value in α-β plane and detection of remaining voltage for SVM

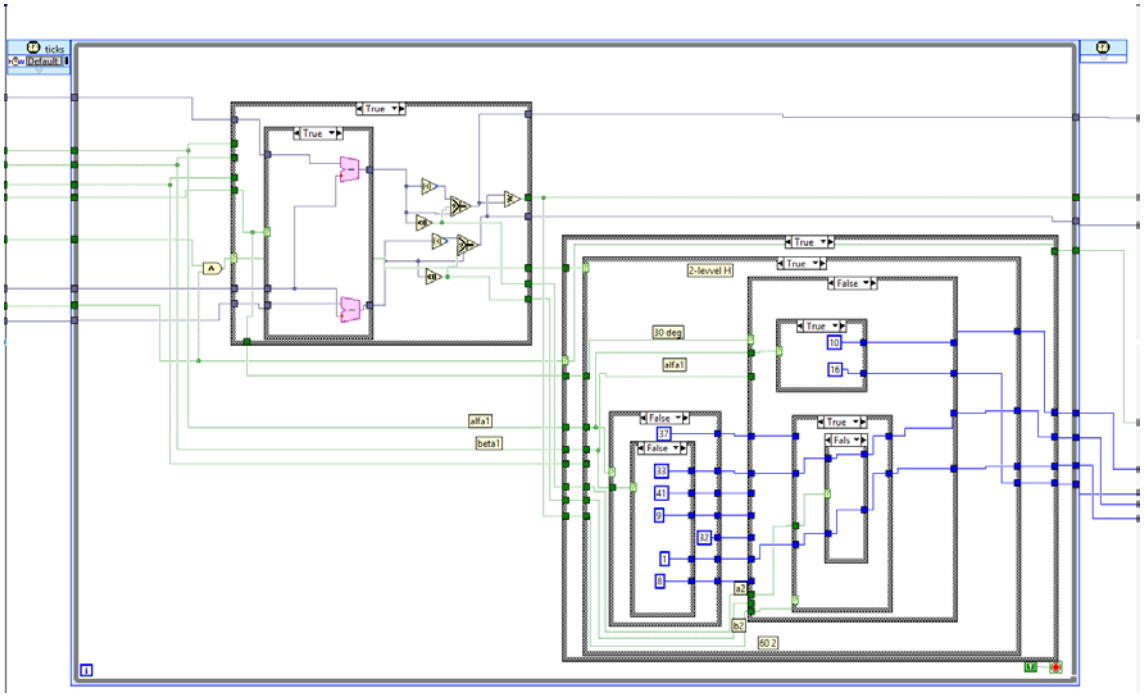

Figure A-12 Calculations of remaining voltage vector for inverter in SVM together with vectors look up tables

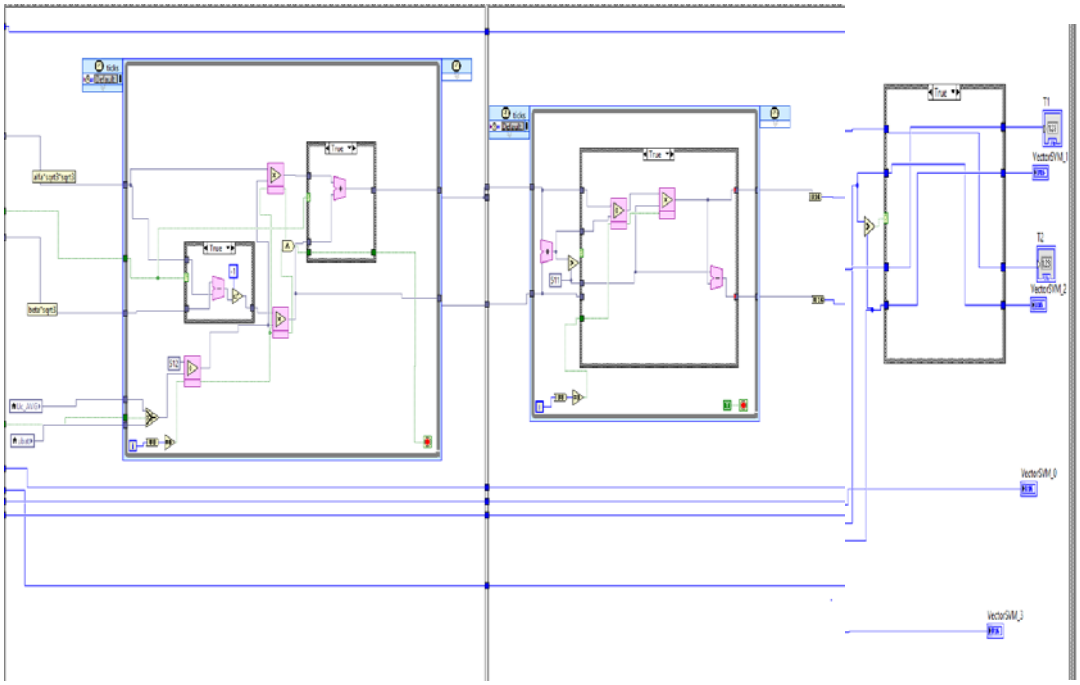

Figure A-13 Dwell times calculation for SVM

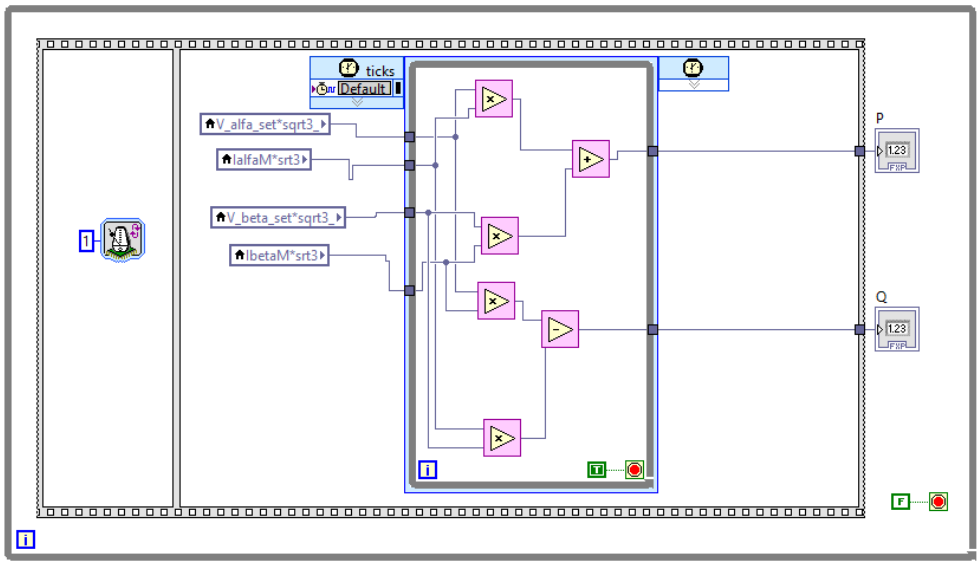

Figure A-14 Active and passive power calculations

Appendix B Simulink model

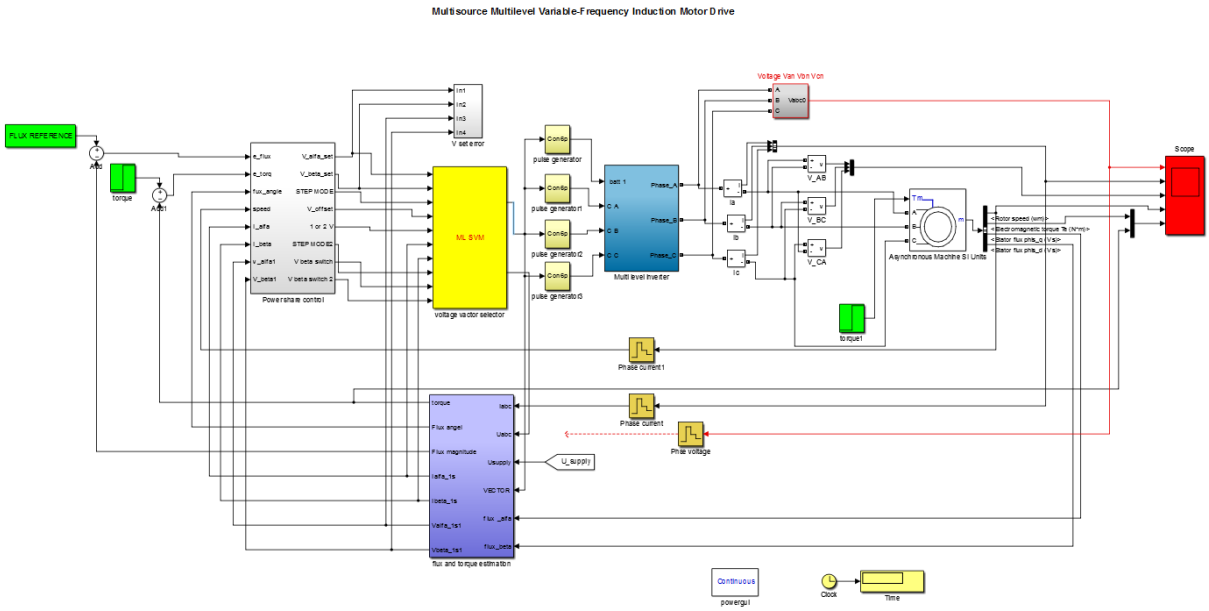

Figure B-1 Matlab/Simulink model of proposed system

Presented system in Figure B-1 consist of five main blocks

- Three-phase induction motor
- Torque and flux estimator
- Torque and flux regulator together with power control
- Space vector modulator with six modulation strategies
- Cascade multilevel inverter

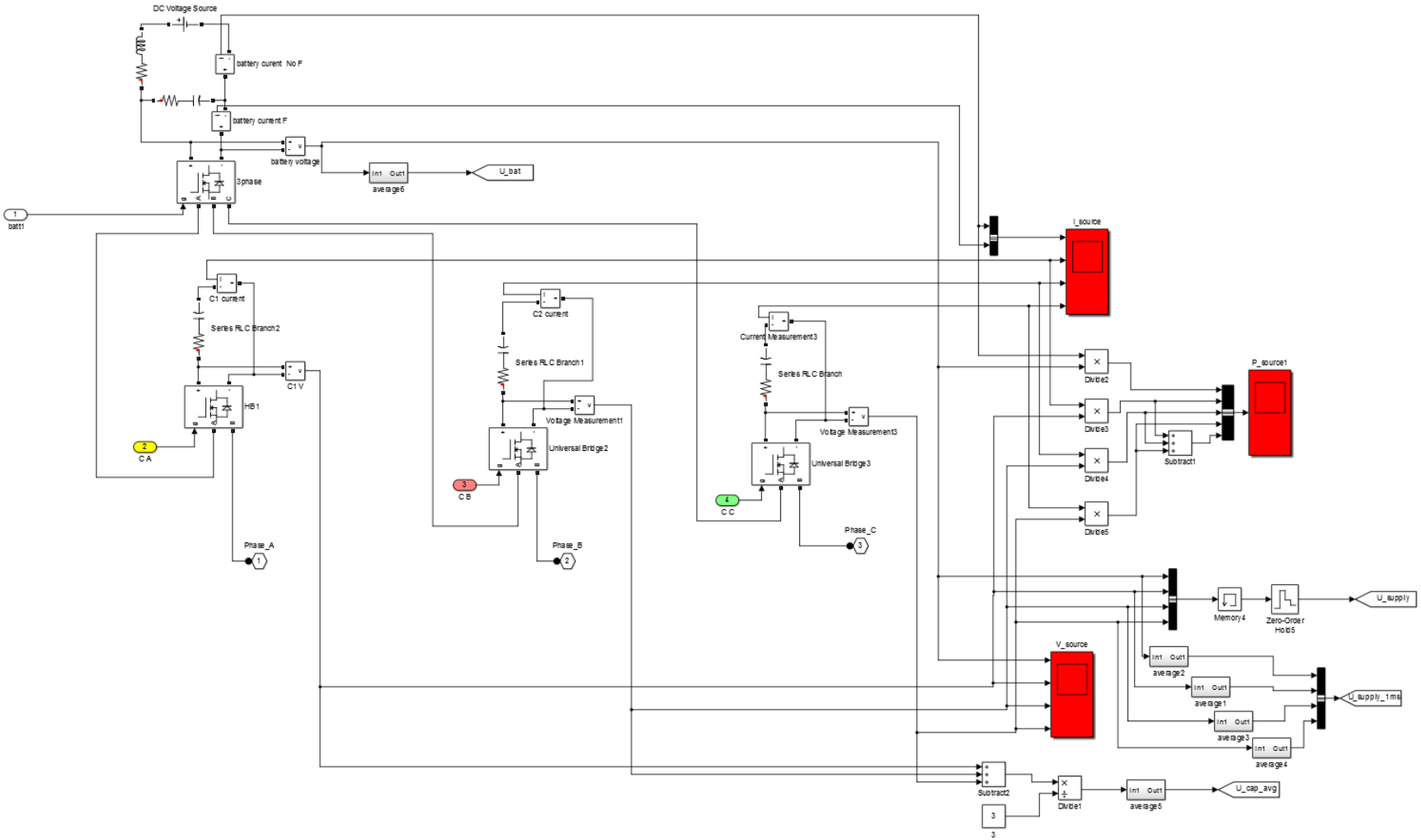

Figure B-2 Multilevel cascade inverter consisting three-phase bridge and three H-Bridges

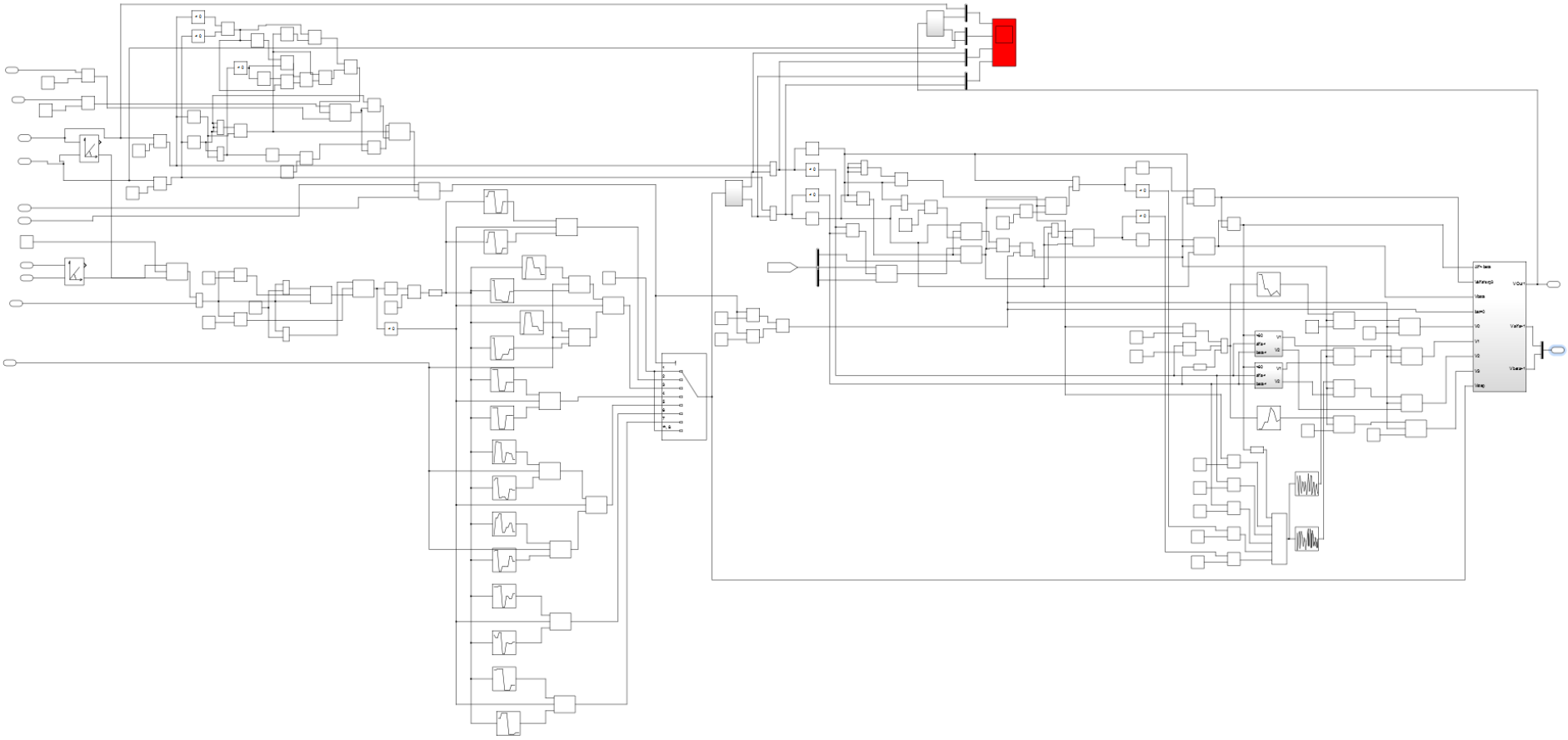

Figure B-3 Space vector modulator with six modulation strategies

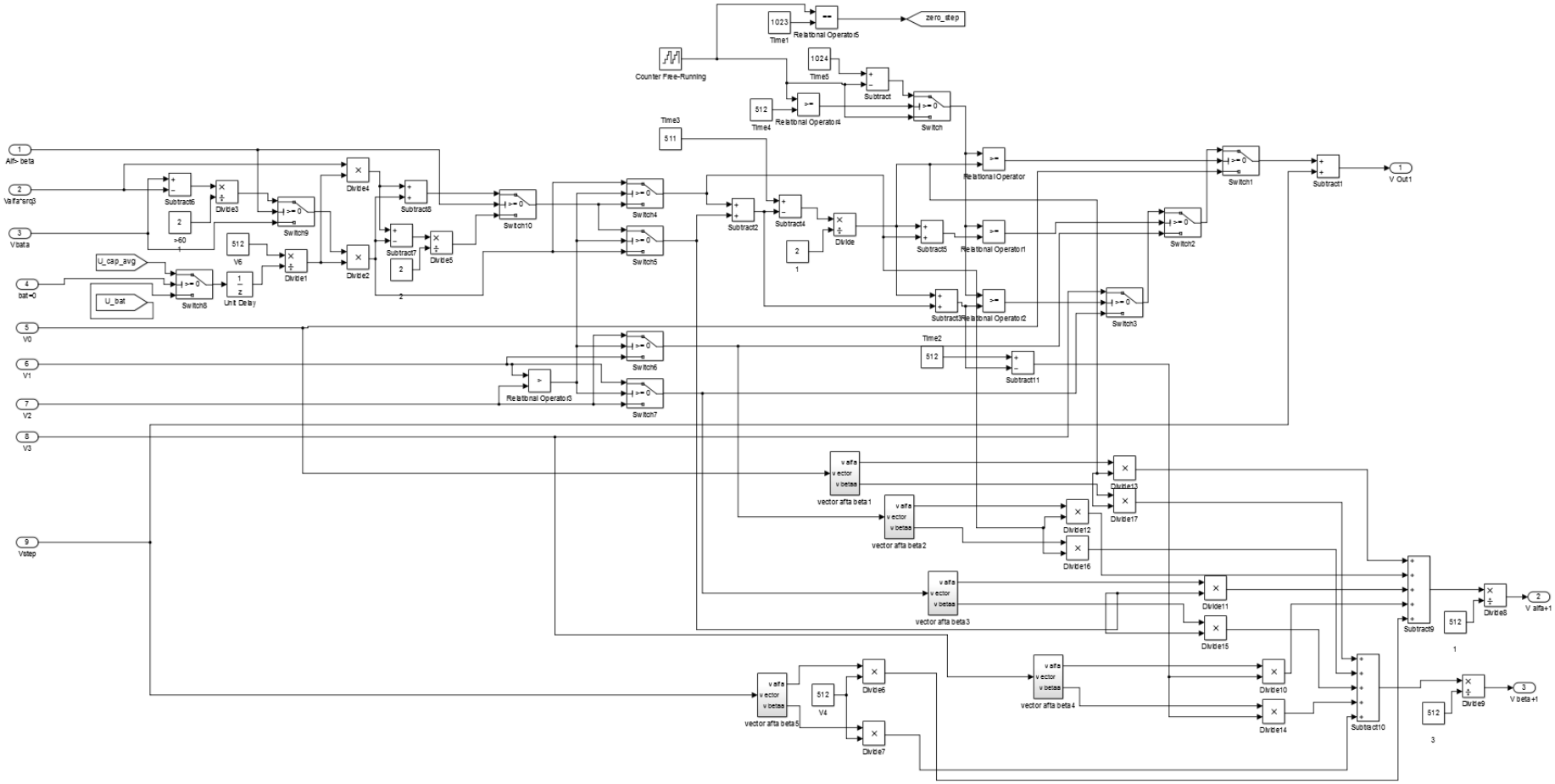

Figure B-4 Space vector modulator- dwell times calculations

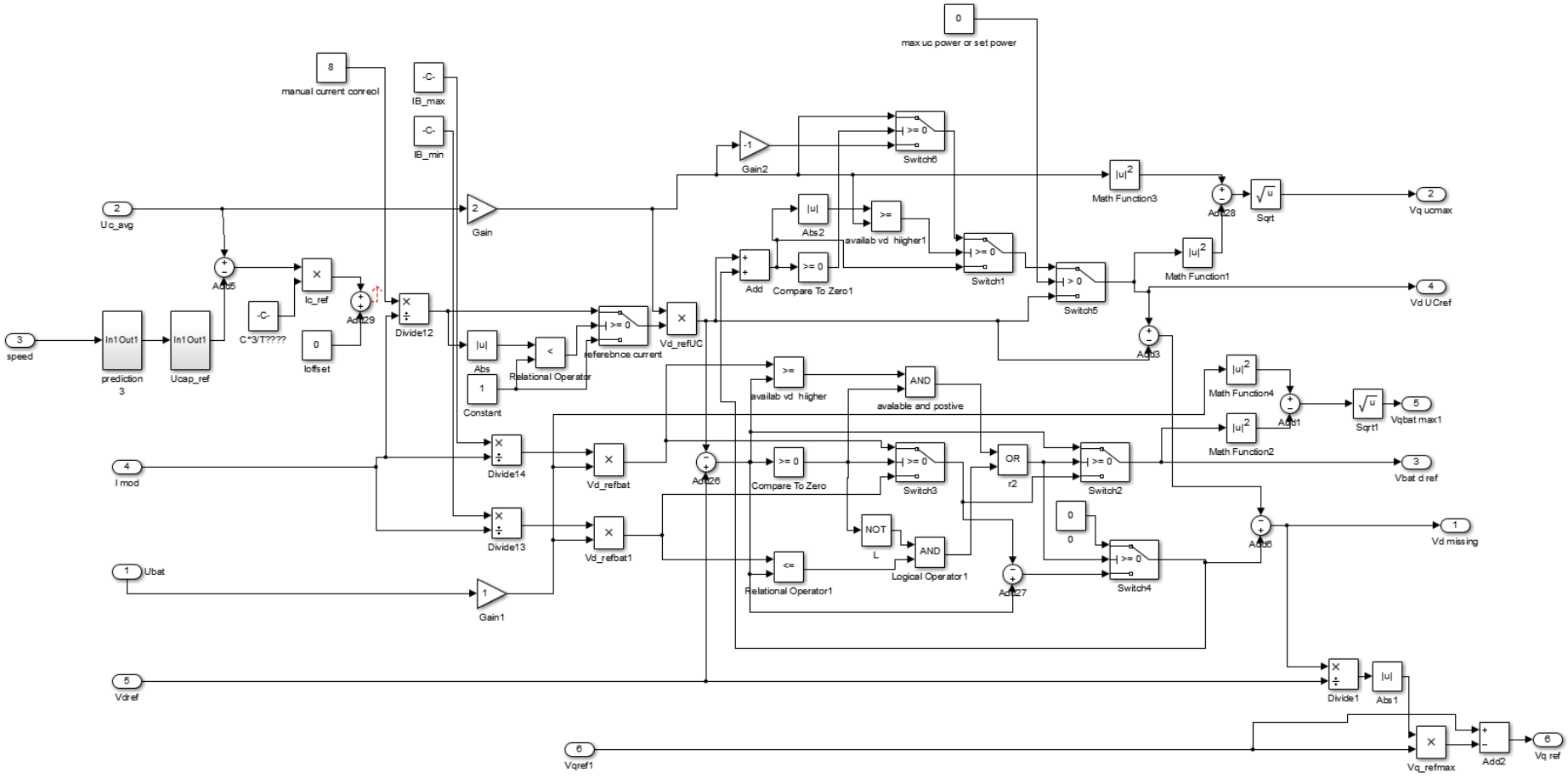

Figure B-5 Torque and flux regulator together with power control

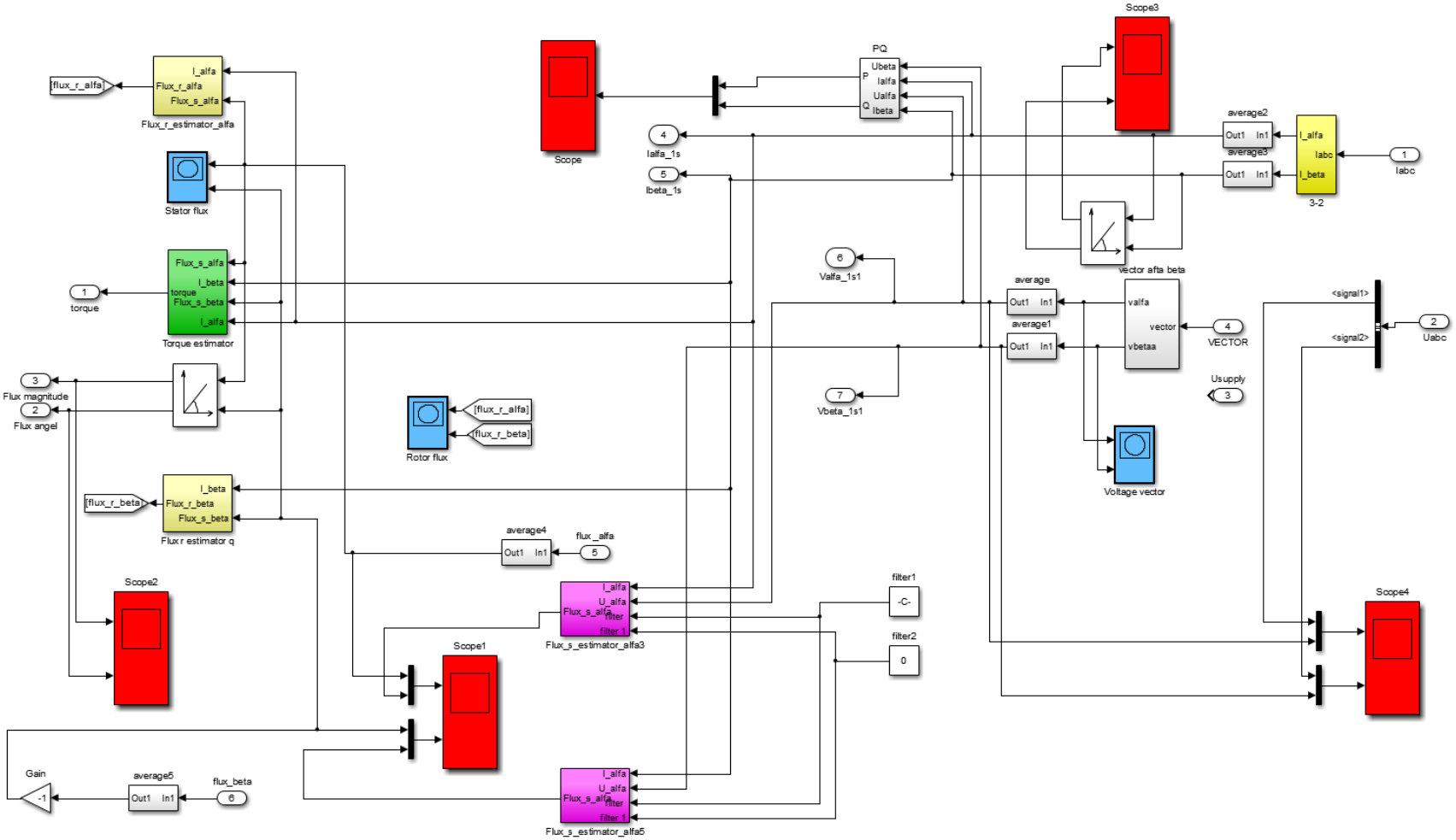

Figure B-6 Torque and flux estimator

Appendix C Control platform configuration

The configuration of the CRIO used for the multilevel inverter under discussion includes following module as presented in Figure C-1:

- NI cRIO-9012 Real-Time controller – The NI cRIO-9012 is a Real-Time Controller with 64MB DRAM and 128MB of Storage. The embedded 400MHz processor runs real-time deterministic control, data logging and analysis.
- NI cRIO-9112 Virtex-5 LX30 cRIO Reconfigurable Chassis with FPGA – The chassis has integrated Xilinx Virtex-5 LX30 FPGA with 19200 flip-flops and 1152kbit embedded RAM. The internal clock operates at 40MHz.
- NI 9425 Digital Input module – is used to read decoded information from the position encoder. Inputs operate with 7us resolution.

  DI0 – bit with information which byte is on the output from HCTL-2017-A00 decoder (1 for low byte or 0 for high byte)

  DI1 – bit with information when data byte is ready to read (1 when data is ready to read)

  DI 15:8 – byte with information about rotor position (16 bit position latch read in two sequential bytes)

- NI 9476 Digital Output module – low-speed digital outputs (500us resolution) are used to control shutdown function for gate drivers (DO0 – enable switch, DO1 – three-phase bridge, DO2 – H-Bridge A, DO3 - H-Bridge B, DO4 - H-Bridge B)
- NI 9474 High-speed digital output – six out of eight digital outputs are used to control the H-Bridges in each phase with a minimum resolution of 1us.

  DO2 and DO3 – gate signals for H-Bridge in phase A (DO2 – A1, DO3 – A2)

  DO4 and DO5 – gate signals for H-Bridges in phase B (DO4 – B1, DO5 – B2)

DO6 and DO7 – gate signals for H-Bridges in phase C (DO6 – C1, DO7 – C2)

- NI 9402 – high-speed digital outputs and Inputs

DIO0, DIO1 and DIO2 are used as digital outputs that form gate signals for the three-phase bridge (DIO0- S1, DIO1 – S2, DIO2 – S3), (since the signal level is 0-5V it has to be additionally amplified to 0-15V for optoisolated circuit)

DIO3 – digital input to detect full rotation from encoder (Z signal from encoded, single pulse per revolution)

- NI 9201 Analogue input module – the analogue input module is used for voltage and current feedback signals. This module comprises eight analogue inputs with +/-10V input range, 12-bit resolution and 500kS/s sampling frequency, giving a highest sampling frequency equal to 16us when all eight channels are used. In the setup above inputs are used to measure the following signals:

  AI0- supply current (I_{bat}) for three-phase bridge (the current is transformed by external hardware from +/- 6A into +/-10V that is connected to AI0),

  AI1- Supply voltage of H-Bridge in phase C (U_C) (converted by external hardware from floating 0-65V into 0-10V),

  AI2- Supply voltage of H-Bridge in phase B (U_B) (converted by external hardware from floating 0-65V into 0-10V),

  AI3- Supply voltage of H-Bridge in phase A (U_A) (converted by external hardware from floating 0-65V into 0-10V),

  AI4- Current in phase A (I_A) (the current is transformed by external hardware from +/- 6A into +/-10V that is connected to AI4),

  AI5- Current in phase C (I_C) (the current is transformed by external hardware from +/- 6A into +/-10V that is connected to AI5),

AI6- Current in phase B (I_B) (the current is transformed by external hardware from +/- 6A into +/-10V that is connected to AI6),

AI7- Supply voltage of three-phase bridge (Ubat) (converted by external hardware from floating 0-160V into 0-10V),

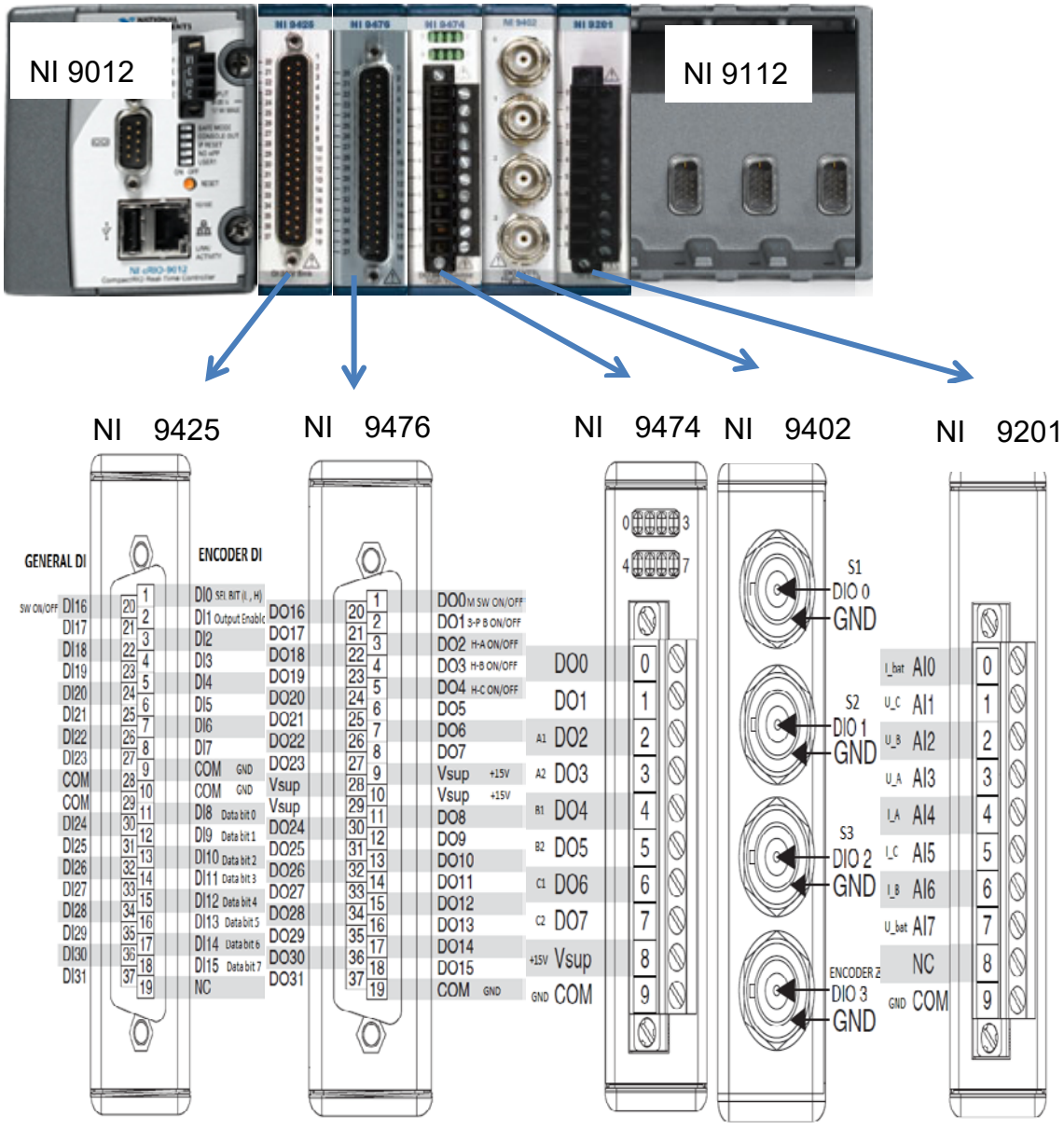

Figure C-1 Configuration of Compact RIO control platform together with input / output allocation