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Toward an Intelligent High Frequency AC Distributed Power System: Part I; Conceptual Design

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Abstract – *High frequency AC (HFAC) distributed power systems (DPS), where electric power is delivered at up to multi-kHz via cables, is an alternative means to conventional centralized power systems. When armed with on-line data, the HFAC DPS can perform intelligent management of power flow and lends itself to a host of emerging applications. The key enabling feature to realizing intelligent management in the DPS is the creation of a communication framework that allows the various sources and loads in the system to communicate their status seamlessly with each other. Whilst data communication over conventional power grid lines has been routinely implemented, there is remarkably no evidence of similar development in DPS where potential benefits would be significant. One key challenge is that DPS systems invariably operate at high frequency, thus squeezing allowable bandwidths for data. This paper explores the means by which real-time information can be achieved without installing additional physical communication channels on an existing 50 kHz current-fed HFAC DPS in lighting applications. A communication protocol is methodologically developed to facilitate robust and efficient inter-device real-time communication. The conceptual design of an intelligent HFAC DPS is proposed and the fundamental requirements and communication challenges of the modem are presented.*

Keywords: *Modems, data communication, intelligent power distribution, energy management, power distribution systems, high frequency AC, lighting systems.*

I. Introduction

High Frequency AC (HFAC) Distribution Power Systems (DPS), in which power is delivered in sinusoidal waveforms at frequency of up to tens of kHz, was first proposed by NASA to power on-board equipment in the space station program in the 80s [1]. The advantages of HFAC DPS over existing DPS, which include simpler system architecture and higher efficiency, are comprehensively discussed in [2] – [5], and have been demonstrated in a variety of applications such as telecommunications, computer systems [6], automotive [7] , [8], multilivel inverters [9], data transmission [10], microgrids [11] – [18]. To date, research in HFAC has been focused on the efficiency of power processing and delivery. Various novel power conversion topologies and control schemes [19] – [25] have been proposed. Whilst these schemes have pushed the efficiency of the overall system to a plateau, future improvements are likely to be coming from intelligent system architecture and power management optimization, where a step change in efficiency and reliability can be envisaged [26] – [30]. Whilst work on HFAC lighting appears limited in scope [31], [32], there has been active research in large-scale lighting involving new power grids [33], [34], and converters [35] - [37]. Although initial works on intelligent distributed lighting have been reported, these systems are based on conventional power using wireless sensors [38], or separate communication networks [39]. In addition, other systems such as Power Line Communication (PLC) or its subset Broadband over Power Line (BPL) at 50/60 Hz have been reported in [40] – [42]. However, the biggest problems facing PLC and BPL that the network is not designed for frequencies other than 60 Hz. Because of this, the network is very inconsistent, and its parameters change over time, location, and load levels. This makes it very difficult to correctly model the attenuation, impedance, and noise on the line. In this paper, an intelligent HFAC DPS for a LED application is realised by retrofitting a communication protocol onto the HFAC bus, showing large-scale distributed lighting as one of the potential applications. Indeed, an intelligent power delivery system offers a host of exciting features including: (i) better utilization of the various power processing structures in the system, (ii) metering power consumption and duty cycle of individual loads, (iii) intelligent scheduling of non-critical loads and (iv) health monitoring and fault reporting. In a system with many dynamic loads with varying power demand and operating duty cycle, the provision of real time instantaneous power demand of the bus could offer a significant opportunity for improving overall system performance. Based on demand, optimal power routing strategies from the numerous front end power converters could be scheduled on a real time basis.

This would enhance system efficiency beyond what is possible by only increasing operational efficiency at individual power converter level. The potential for intelligent management in HFAC DPS is evident.

In this paper a HFAC data modem is proposed to facilitate communication over the HFAC power bus without the need for additional communication channel. Using on a lighting application, the conceptual design of an intelligent HFAC distributed power network is proposed. The fundamental requirements and communication challenges are presented in the following sections, and the design of the modem is described in detail.

II. Fundamental Requirements

The fundamental requirement for an intelligent HFAC system is a communication capability that supports bi-directional flow of data between different subsystems or agents on the bus. In transmit mode, agent 1 will send out modulated data onto the HFAC bus. In receive mode, agent 2 will fetch data from the bus and de-modulate the data to recover the original information. This must be achieved reliably and without interrupting the power flow in the bus.

In a typical HFAC network, it is anticipated that there would be many agents all communicating with each other over the same HFAC bus, causing potential data collision. Bus arbitration mechanism is necessary to ensure that collisions are avoided and detected if they do happen.

As the communication is required mainly for telemetry purposes, the required data bitrate is relatively low. A data rate of less than 1kbps is sufficient for most applications [43], [44]. Another desirable feature is the compatibility of the required modem with both voltage and current-fed HFAC systems. In addition, the modem shall be capable of generating a signal level to the remote terminal that is above the sensitivity of the receiver, with a signal-to-noise ratio (SNR) well above the minimum, so that the receiver can make a correct decision based on the information transmitted.

Before proceeding to the detailed design of the modem, two important design considerations need to be first addressed - data encoding technique and modulation scheme.

II.1. Data Encoding

As the data is transmitted over the existing power bus which consists of only two conductors, the data would need to be asynchronously transmitted. The microcontroller naturally generates the transmit data in Non-return-to-zero (NRZ) format. Without an accompanying clock signal, the detection of NRZ encoded data at the receiving end can be challenging especially when long strings of '1s' or '0s' are transmitted. Any drift in the clock generator at the receiving end could cause a bit slip and corrupt the received data.

To overcome this problem, the HFAC bus voltage frequency is utilized as a synchronizing clock. At the transmit side, the NRZ data is generated in sync with the 50kHz HFAC bus voltage/current waveform. At the receiving end, the clock signal is derived from the bus voltage using a zero-crossing detection circuit which can then be used to 're-time' the received NRZ data. This solution eliminates any bit slip even if frequency deviation exists in the bus.

This simple solution, however, has some limitations. First, the transmission bit rate is dependent on the bus voltage frequency, with absolute maximum achievable bit rate being one bit per period of the bus voltage and lower bit rates (integer ratios of bus frequency) implementable only with additional circuitry. Next, the synchronization of the transmit data with the bus frequency would naturally require that data transmission begin at the zero crossing point of the bus voltage. This greatly increases the probability of data collision in a system with many communication nodes.

An alternate solution is to Manchester encode the NRZ data stream. In a Manchester encoded data a logic '1' is represented by a high to low transition and logic '0' by a low to high transition. These transitions occur at the midpoint of the data bit frame. Therefore there will be a guaranteed transition at the middle of every bit period regardless of the bit pattern of the digital stream being encoded. This method indirectly embeds the clock rate information within the transmitted data and therefore is self-clocking. This has a benefit in the clock recovery process at the receiving end. Using Manchester encoding, the data bit rate is not constrained by the bus voltage frequency and the data transmission need not be aligned with the zero-crossing points of the bus voltage.

II.2. Digital Modulation

To transmit the digital data over the power line, it would first need to be modulated. For low speed power line communication, frequency-shift keying (FSK) or ON-OFF keying (OOK) is often the preferred choice. The primary advantage of using OOK is its simple implementation. OOK can be easily generated using a CMOS astable multivibrator. Detection and demodulation is also simple and can be performed using a rectifier and a peak detector circuit. The OOK implementation approach used for regular 50/60Hz power line communication can also be employed for HFAC [45]. The main disadvantage of OOK is that it is not compatible with multiple bus access systems. This is due to the inability to distinguish between 'no transmission' and logic zero transmission.

The modulation and demodulation circuitry of FSK is more complex than the OOK implementation. However,

it is compatible with multiple bus access systems as a carrier signal is present during the transmission of both logic '1' and '0'. Therefore it is possible to identify if the bus is idle before a node decides to transmit information. Accordingly, the FSK technique is used in this research In the next section the detailed design of the hardware and software aspects of the modem is discussed.

III. Modem Design

A complete block diagram of a proposed HFAC data modem is shown in Fig. 1. At one end, the modem has a serial interface link to communicate with external systems. At the line end a coupling circuit is used to interface to the HFAC bus. In this section the circuit level implementation of the modem is discussed.

III.1. NRZ to Manchester Encoding

The microcontroller generates the data to be transmitted in NRZ format and outputs two signals, NRZ_DATA and NRZ_CLK. The NRZ data is converted into Manchester code by using a XNOR logic gate with NRZ data and clock as inputs.

III.2. Frequency-Shift Keying Modulator

In the proposed FSK design, the carrier frequency shall be selected such that the ratio between the carrier and the bus voltage frequency is as high as possible. The greater the ratio, the more relaxed the requirement for the coupling circuit becomes. In addition, using high carrier frequency reduces the susceptibility of interference form the bus voltage. On the other hand, using too high a frequency imposes constraint on the selection of opamps and power amplifiers in the signal processing chain. To avoid using a high-cost gain bandwidth opamps, a logic '1' and logic '0' carrier frequency of 12.5MHz & 10.5MHz was selected as a balance for the frequency requirements. FSK modulation can be implemented using any voltage controlled oscillator (VCO) with a suitable frequency range. In this design the CD74HC7046A phase-locked loop (PLL) integrated circuit (IC) from Texas Instruments was used. This IC was selected due to its excellent VCO frequency linearity.

III.3. Transmit Low-Pass Filter

The FSK modulated signal from the VCO is a square wave with 50 duty cycle. A low-pass filter is used to filter out all the high order harmonics and to generate a sinusoidal FSK modulated signal. The main requirement of the filter is a steep roll-off rate to ensure the 3rd harmonic is sufficiently suppressed. In addition, a small gain variation at 10.5MHz and 12.5MHz is desired to ensure uniform amplitude of both the carrier frequency. To meet this requirement, a 6th order Butterworth low-pass filter (T-configuration) was used.

III.4. Transmit Amplifier

The modulated FSK data has to be sufficiently amplified before it is injected onto the HFAC bus. A single stage inverting opamp with a class B push-pull output stage is proposed. The impedance of the HFAC bus is inevitably varied depending on the loading condition of the bus. For example, under low impedance conditions, the transmit amplifier can be significantly loaded. Therefore the output stage is necessary to increase the current drive capability of the inverting amplifier.

III.5. Coupling Circuit

In principle the coupling circuit consists of a tuned LC high-pass filter that presents a low impedance path to the carrier frequency but blocks the bus power frequency. The design requirement for the coupling circuit will be discussed in depth in section IV to VII.

III.6. Receive Band-Pass Filter

While the coupling circuit filters out the carrier signal from the bus, further signal processing is required to ensure the received signal can be successfully decoded. Coupling circuit components, are required to be rated to handle the bus voltage levels and therefore are often bulky, expensive and difficult to source in a wide range of values at low tolerances. Therefore a second stage filtering process with a narrower pass-band is used to filter out the high order harmonics of the bus voltage/current frequency that exist in the communication signal.

Direct cascade of the receive band-pass filter to the coupling circuit can pose some problems because the input impedance of the receiver section will be determined directly by the input impedance of the band-pass filter. This is not desirable as the modem input impedance requirement for the current-fed and voltage-fed system is different. Therefore a non-inverting voltage buffer amplifier is used as an interface between the coupling and filter circuit. A common filter configuration can then be used for both the current-fed and voltage-fed systems. A 3rd order Butterworth band-pass filter with a PI-configuration was used.

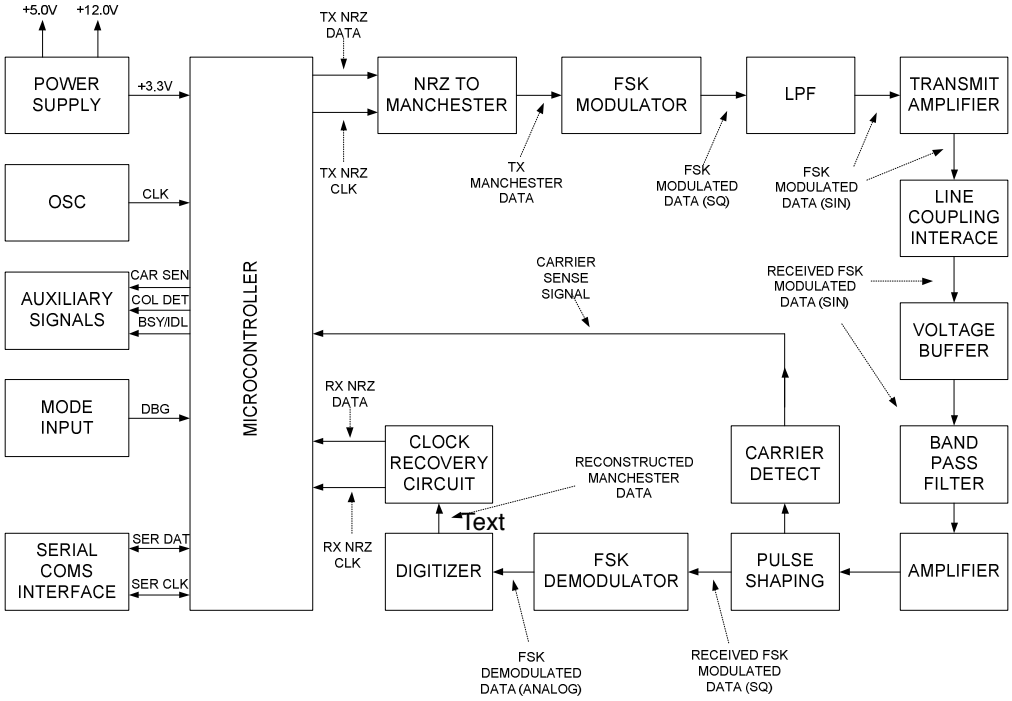


Fig. 1. Block diagram of the HFAC data modem.

III.7. Receive Amplifier

In general the received signal amplitude is quite low, and it can vary broadly depending on the impedance of loads connected to the bus. In this application it is only crucial that the frequency information of the signal is preserved. Actual signal wave shape is not important. Therefore the strategy employed in this design is to use an amplifier with sufficient gain such that at the lowest expected input amplitude, the signal is adequately amplified. With this approach, if the input signal is considerably larger than the minimum value, the high gain amplification could cause signal clipping. This is not a concern as the frequency of the signal remains unchanged even under these conditions. The receive amplifier was implemented using a CMOS inverter operating in linear mode.

III.8. Pulse Shaping

To ensure consistent and accurate decoding irrespective of the amplitude of the input signal, it is necessary to shape the amplified pulse to a square wave. This can be easily done by feeding the output of the amplifier through a logic inverter. The reshaped square wave is identical regardless of the amplitude of the input signal, the frequency matches the original input signal and the duty cycle is 50.

III.9. Carrier Detect

The main purpose of the carrier detection circuitry is to identify if the bus is in the idle state or if it is currently busy with ongoing communication. The presence or absence of a square wave from the pulse shaping circuitry can be used to determine if the bus is idle. The carrier detection circuitry is designed to output a logic high to the microcontroller to indicate a 'busy' state and logic '0' for 'idle' condition. This can be implemented using a simple envelop detection circuitry and non-inverting Schmitt trigger or comparator circuit. The time constant of the peak detector should be approximately 3 to 4 times the period of the carrier frequency.

III.10. Frequency-Shift Keying Demodulator

The output of the pulse shaper is demodulated using a PLL. The PLL locks to the frequency of the input signal and generates an output voltage proportional to the frequency of the input signal. In the ideal case, the frequency profile of the PLL should be designed to match the transmit VCO frequency profile. However temperature drift at the transmit side could cause the frequency output of the VCO to increase beyond the designed value. The PLL should therefore be designed with a narrower profile to ensure robust detection. In general a larger offset frequency and a reduced range is necessary. In this design the CD74HC7046A PLL IC from Texas Instrument was used. The IC was configured

for positive edge-triggered phase and frequency detector (PFD) and passive lead lag low-pass loop filter.

III.11. Digitizer

The demodulated signal is an analog voltage between 0V to 5V proportional to the input frequency. In order to digitally decode the received data, the demodulated signal will need to be digitized to crisp logic levels. This is implemented using a voltage comparator circuit with hysteresis. The output of the comparator is the transmitted Manchester encoded data stream.

III.12. Clock Recovery Circuit

Before the received Manchester encoded data can be decoded, it is first necessary to extract the synchronizing clock information from the Manchester data stream. With the clock signal available, the retimed NRZ equivalent data and the clock signal can be generated and sent to the MCU for further processing. The proposed clock recovery circuit to perform this function is shown in Fig. 2. As described in section II, the Manchester encoded signal has a transition in the middle of every clock period. Therefore, latching the Manchester data stream just prior to the midpoint of the clock signal results in the NRZ representation of the data. This can be achieved using a shifted clock signal which is 90 out of phase with the original clock used to encode the Manchester data.

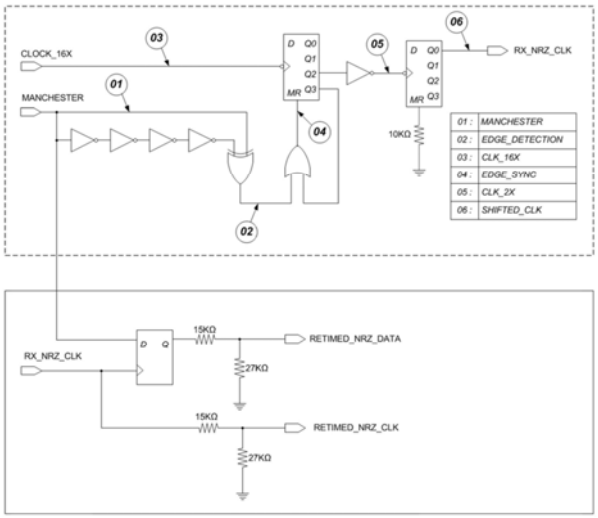


Fig. 2. Simplified clock recovery circuit.

The problem now lies in generating the shifted clock signal. This is performed by the circuit enclosed in the dotted section of Fig. 2. Fundamentally a high frequency clock (16 times the transmitted NRZ clock) and a binary counter operating as a frequency divider is used to derive the phase shifted clock signal. The binary counter is synchronized at every edge of the incoming Manchester data stream and therefore any deviation in the high frequency clock is corrected at every transition.

There are however some limitations with this technique. Although the Q0 output of the binary counter toggles at the right frequency, the state of the Q0 output can either be a logic '1' or '0' at the start of the data stream. In other words, the recovered clock can either lead or lag the transmit clock by 90. In both conditions, the sampling point of the incoming Manchester bit stream differs and can produce different results. Additional synchronization circuitry to reset U2 appropriately could be quite involved. This problem can be solved reasonable easily in software by exploiting the fact that the Manchester encoded data sampled at either +90 or -90 relative to the transmit clock will result in either the correct NRZ data or the inverse of the transmit data. The preamble detection routine in software can be used to identify if the received data is inverted.

IV. Coupling Circuit- Voltage Fed System

In a voltage-fed system, the modems are effectively connected in parallel to the HFAC bus. Fig. 3 shows a simplified equivalent circuit for a number of modems connected to a HFAC bus. In this case it is assumed that no loads are present in the system. Each modem is represented as a voltage source with series impedance Z_{MODEM}. The HFAC inverter that generates the bus voltage is modeled as a Thevenin equivalent circuit. We now assume that MODEM 1 in the system is transmitting information over the bus. All other modems are assumed to be in receive mode. The red dotted lines represent the current flow due to MODEM 1. For maximum communication efficiency, the following conditions are necessary:

1) The impedance of the modem (Z_{MODEM1}) in transmit mode should be as small as possible at the carrier frequency.
2) The impedances of the modems in receive mode (Z_{MODEM2} to Z_{MODEMn}) should be reasonably high at the carrier frequency to avoid loading the transmitter excessively.
3) The impedance of the HFAC inverter (Z_{INVERTER}) should be very high at the carrier frequency.
4) The impedance of Z_{INVERTER} should be very small at the bus voltage frequency for efficient power transfer.

The modem can be represented as shown in Fig. 4, where TA and RA represent the transmit and receive amplifier circuits respectively. The transmit amplifier by design has negligible output impedance and the receive amplifier has a very high input impedance. Therefore the effective input impedance of the receiver circuit is equal

to the value of R_{IN}. The coupling circuit is shown in the figure as an equivalent two port network.

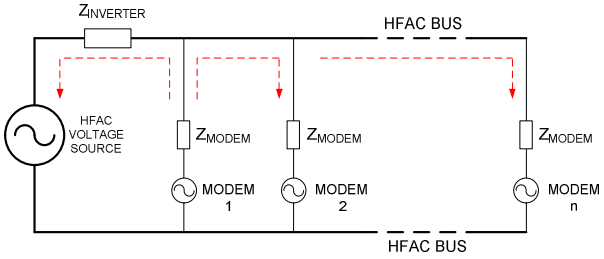


Fig. 3. Multiple modems on a voltage-fed HFAC bus.

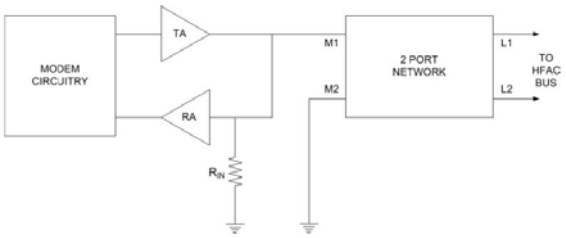


Fig. 4. Simplified representation of the modem line interface stage for a voltage-fed system.

To meet requirement 1, the input impedance of the network seen from terminals M1 and M2 should be very small at the carrier frequency. Requirements 2 & 4 call for the impedance seen from terminals L1 and L2 be equal to the value of R_{IN} at the carrier frequency and at the bus voltage frequency the impedance should be very high. An impedance network with a high-pass or band-pass characteristics would meet these requirements.

In this design a band-pass configuration consisting of a tuned series and parallel resonant circuit was used. An isolation transformer was also used to provide electrical isolation between the HFAC bus and the modem circuitry. The leakage inductance L_P and magnetizing inductance L_{MAG} of the transformer also influence the performance of the circuit and in this design it was intentionally used to form part of the coupling circuit. The coupling circuit is shown in Fig. 5.

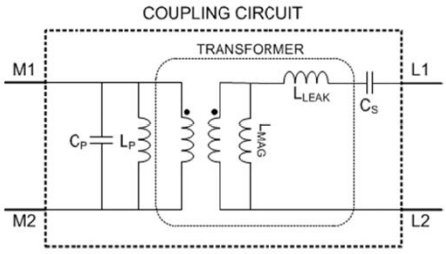


Fig. 5. Modem coupling circuit for voltage-fed system.

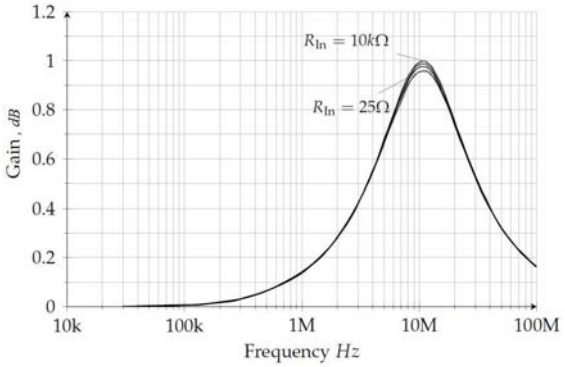
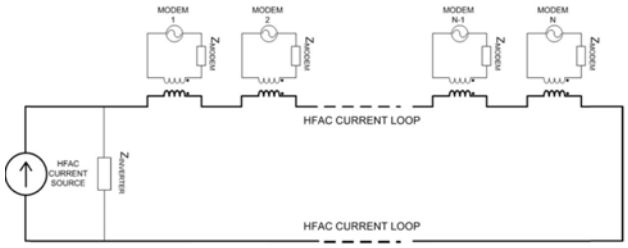


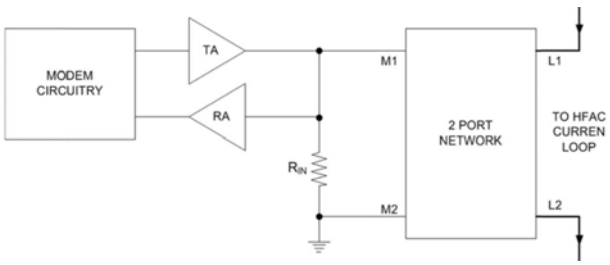
Fig. 6. Frequency response simulation of the coupling circuit- voltage-fed system.

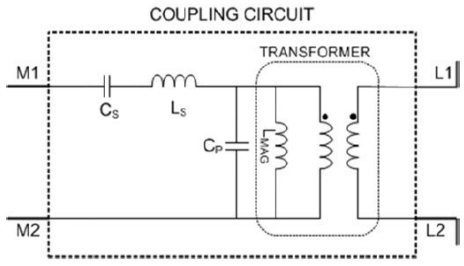
In selecting the coupling transformer, it is important to ensure the operating frequency range is compatible with the carrier frequency [46], [47]. In this design, the T60403-K4031-X008 coupling transformer from Vacuum Schmelze was used. This transformer is rated for operation from 1 to 30. The leakage and magnetizing inductances (line side) were measured to be 620 and 1.458 respectively. The series capacitor C_S value of 330 was selected to be at resonance with L_{LEAK}. At the modem side, a parallel resonant circuit is used. The value of L_P should be selected to be much smaller than the magnetizing inductance. In this design L_P and C_P values were 22 and 10 respectively. The simulated frequency response of the proposed coupling circuit is shown in Fig. 6. It can be observed that the bus voltage frequency (50) is well attenuated. The frequency response curve shows almost no sensitivity to changes in the value of R_{IN}.

V. Coupling Circuit- Current-Fed System

In a current-fed system, the modems are effectively connected in series to the HFAC current loop. Fig. 7 shows a simplified equivalent circuit for a number of modems connected to a HFAC current loop. In this case it is assumed that no loads are present in the system. The inverter generates a HFAC sinusoidal constant current output. To ensure that the impedance of the inverter ($Z_{INVERTER}$) does not attenuate the communication signal, a tuned band-pass filter can be added in parallel with ($Z_{INVERTER}$) to offer an alternate low resistance path for the communication signal. The simplified equivalent modem circuit is shown in Fig. 8. The requirement of the coupling circuit is described as follows:







$V\ n-$. Therefore even under ideal conditions with no line and load impedance, amplitude of the received signal falls as the number of modems increase. In the voltage-fed design, under similar ideal conditions, the amplitude of the received signal remains constant regardless of the number of modems in the system, provided that the transmit amplifier has sufficient current drive capability.

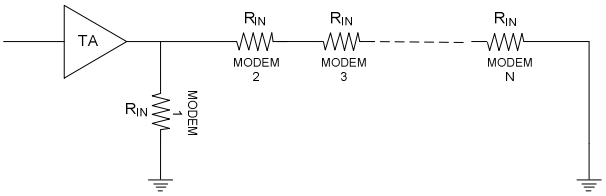


Fig. 10. Transmit mode equivalent impedance model.

Next, consider a similar system but with two modems simultaneously transmitting. This condition is represented in Fig. 11. At the input node of MODEM 1, a signal of amplitude V due to self-transmission will be present. In addition, another voltage component due to the simultaneous transmission of modem N will appear across the input node of MODEM 1. The amplitude of this component will be $V/(N-1)$. Therefore the signal seen at the input of both modems will consist of the sum of both the self-transmission component and the simultaneous transmission by the neighbouring modem. If the number of modems in the system is large, the amplitude of the voltage due to the transmission of the neighbouring modem will be small and may be totally overwhelmed by the self-transmission component. This may potentially impair the collision detection capability. Any load connected to the loop increases the total resistance and further aggravates these problems. Therefore a tuned band-pass bypass filter should always be used across all loads to offer an alternate low resistance path for the communication signals.

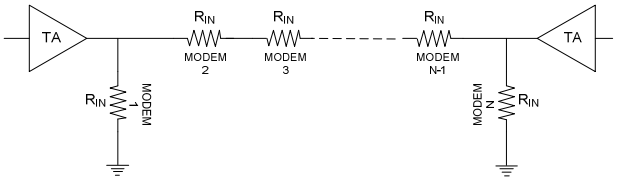


Fig. 11. Multiple transmit mode equivalent impedance model.

VII. Conclusion

HFAC power distribution systems offer some distinct advantages, such as less system components and / or compactness of the components when compared to low frequency AC system. Applications benefiting from HFAC systems are countless. One potential application is the lighting systems. HFAC offers opportunities for energy savings, space reduction, high performance, even lamp brightness, redundancy and reduced EMI noise capability compared to existing lighting systems. This paper proposed a new communication framework by means of which intelligent management of a HFAC distributed power system is advanced. The conceptual design and the requirements of data modem capable of implementing bidirectional communication at a data rate of 38 kbps over a 50 kHz HFAC current-fed power bus in a lighting application is presented. The proposed enabling communication framework showed significant potentials that can be exploited in implementing intelligent power management schemes for HFAC distributed power systems. The presented concept addressed the problems that are associated with the traditional PLC and its subset BPL communication systems such as limitation of the operating frequency and speed of data transfer. Moreover, this paper discussed the main limitations on the coupling circuits of the HFAC system. For example, when using a current-fed design, amplitude of the received signal falls as the number of modems increase. Whereas in the voltage-fed design, the amplitude of the received signal remains constant regardless of the number of modems in the system. It was also demonstrated that a tuned band-pass bypass filter should always be used across all loads to offer an alternate low resistance path for the communication signals. The limitations are even increased when using other types of filters especially if the number of modems in the system is large. If precautions are not considered in the design stage, this may potentially harm the collision detection capability of the system.

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Toward an intelligent high frequency AC distributed power system - Part I: conceptual design

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