CRANFIELD UNIVERSITY

STEVEN LOURDES

HIGH FREQUENCY AC POWER AND DATA DISTRIBUTION SYSTEM

DEPARTMENT OF ENGINEERING & APPLIED SCIENCE
POWER & DRIVE SYSTEMS GROUP

PhD THESIS
Academic Year : 2011 – 2012

Supervisor : Dr. Patrick Chi Kwong Luk
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This thesis is submitted in partial fulfilment of the requirements for the degree of Doctor of Philosophy

ABSTRACT

At present, power delivery issues are becoming a concern with modern state of the art electrical and electronic systems. The existing power networks, namely the centralized power architecture and the DC distributed power systems are struggling to cope with rigorous demands in some application areas. While active research to improve the current system is being relentlessly pursued, a more radical approach proposing a new power distribution system is increasingly drawing attention. High frequency AC (HFAC) power distribution architecture has been identified as a viable alternative to existing and future systems. The HFAC distributed power system (DPS) was initially proposed in the early 80s for space application and since then it has been considered for many modern ground based applications.

This dissertation presents a fresh perspective to the problem by challenging the current notion of viewing the HFAC DPS merely as a passive power distribution system. The possibility of converting the existing system to a more intelligent architecture is investigated. Two fundamental features identified to be crucial for this implementation is the ability to communicate and to control power flow between the various power processing structures in the system. Developing the 'enabling technologies' is the primary focus of this research. A data modem designed to enable bidirectional multi node communication over the HFAC bus satisfies part of this requirement. The ability to control power flow is achieved by introducing digital control in the front end HFAC inverter. It is shown that intelligent management of the HFAC DPS offer potential efficiency benefits previously not possible in the traditional implementation.

At the subsystem level, the front end inverter, the point of load (POL) converter and the communication module are investigated in depth. Extensive mathematical modelling is undertaken to develop optimal design guides to improve performance of the subsystems. Prototypes are constructed and the models are experimentally validated. In the case of the front end inverter, a multi stage inverter with parallel operation capability incorporating digital control is presented. An integral cycle converter is investigated as part of the POL subsystem and optimal synthesis pattern that improves power factor is identified. The communication subsystem constitutes the HFAC data modem described above. The modem emulates Ethernet style communication and interfaces to a host system via a simple serial communication link. All communication over the HFAC bus is performed transparently to the host.

This dissertation contributes to the improvements of HFAC DPS at both the system and subsystem levels. At the system level, implementation of intelligent management of the HFAC DPS is shown to be viable and offers opportunities for improved performance and flexibility not previously possible. At the subsystem level, performance improvement to the individual power processing structures in the system is presented.

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In the course of this research, I have had the opportunity to have met and worked with many talented people who have contributed in some way to this work, to only some of whom it is possible to give particular mention here. I would firstly like to thank my supervisor, Dr. Patrick Luk for his constant support, encouragement and excellent supervision which has been crucial at all times. Although meeting his high expectations has been very challenging, his patient and calm disposition has made this experience very enjoyable and I am very grateful for this. I am also very appreciative of the support of Dr. Ken Jinupun which was very helpful in many aspects of this work.

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Finally I would like to thank my friends and family for all the support and motivation they have given me during this project. Above all I would like to thank my wife, Rina for her love, understanding and help at various levels, without which this thesis would not have been possible.

Nomenclature

Notation	Description	Unit	
A_c	Core Cross Sectional Area	square centimeter	[cm^2]
B	Magnetic Flux Density	tesla	[T]
C_{ac}	Controlled AC Resonant Capacitor	farad	[F]
C_b	Boost Capacitor	farad	[F]
C_f	Filter Capacitor	farad	[F]
C_p	Parallel Resonant Capacitor	farad	[F]
C_r	Resonant Capacitor	farad	[F]
C_s	Series Resonant Capacitor	farad	[F]
D	Duty Cycle	-	-
DCR	Inductor DC Resistance	ohms	[Ω]
f_{boost}	Boost Switching Frequency	hertz	[Hz]
f_{bus}	HFAC Bus Frequency	hertz	[Hz]
f_0	Fundamental Switching Frequency	hertz	[Hz]
f_r	Resonant Frequency	hertz	[Hz]
$H(s)$	Modem Coupling Circuit Voltage Transfer Function	-	-
$i_{bus\_primary}$	HFAC Bus Current Referred to Primary	ampere	[A]
i_C	Boost Capacitor Current	ampere	[A]
i_{cp} / $i_{cp'}$	Parallel Resonant Capacitor Current	ampere	[A]
i_{cp_RMS}	Parallel Resonant Capacitor RMS Current	ampere	[A]
i_L	Boost Inductor Current	ampere	[A]
I_L	Effective DC Inductor Current	ampere	[A]
$\langle I_L \rangle$	Boost Inductor Average Current	ampere	[A]
I_{LMAX}	Boost Converter Maximum Peak Current	ampere	[A]
I_{LMIN}	Boost Converter Minimum Peak Current	ampere	[A]
I_{LOAD}	Load Current	ampere	[A]
i_{lp} / $i_{lp'}$	Parallel Resonant Inductor Current	ampere	[A]
i_{lp_RMS}	Parallel Resonant Inductor RMS Current	ampere	[A]
i_r / $i_{r'}$	Resonant Tank Input Current	ampere	[A]
i_{r_RMS}	Resonant Tank Input RMS Current	ampere	[A]

Notation	Description	Unit	
i_{RIC}	Rectifier Input Current	ampere	[A]
I_{ROC}	Rectifier Output Current	ampere	[A]
I_{SHUNT}	Shunt Regulator Current	ampere	[A]
i_p	Transformer Primary Current	ampere	[A]
i_{p_DC}	Transformer Primary Current DC Component	ampere	[A]
$i_{p\_peak(f=f_{bus})}$	Transformer Primary Peak Bus Frequency Current Component	ampere	[A]
i_{p_RMS}	Transformer Primary RMS Current	ampere	[A]
i_s	Transformer Secondary Current	ampere	[A]
i_{s_RMS}	Transformer Secondary RMS Current	ampere	[A]
k_p	Parallel resonant tuning factor	-	-
k_s	Series resonant tuning factor	-	-
K_{fe}	Core Loss Coefficient	-	[W/cm^{3}T$^\beta$]
K_u	Winding Fill Factor	-	-
L_b	Boost Inductor	henry	[H]
L_f	Filter Inductor	henry	[H]
L_k	Connection Inductance	henry	[H]
L_{leak}	Transformer leakage inductance	henry	[H]
L_{mag} / L_m	Transformer Magnetizing Inductor	henry	[H]
L_p / L_{pr}	Parallel Resonant Inductor	henry	[H]
L_r	Resonant Inductor	henry	[H]
L_s	Series Resonant Inductor	henry	[H]
MLT	Mean Length Turn	centimeter	[cm]
n	Harmonic Number	-	-
n_s	Transformer Primary Turns	-	-
n_p	Transformer Secondary Turns	-	-
N	Transformer Turns Ratio	-	-
N_{FR}	Frame Length	-	-
N_m	Number of Modem	-	-
P_{avg}	Average Output Power	watts	[W]
P_{core}	Transformer Core Losses	watts	[W]
P_{DC_DC}	Average Output Power of DC-DC Converter	watts	[W]

Notation	Description	Unit	
P_{loss}	Total Power Loss	watts	[W]
P_{out}	Output Power	watts	[W]
P_{tx_loss}	Total Transformer Losses	watts	[W]
$P(s)$	Modem Coupling Circuit Impedance Transfer Function	ohms	[Ω]
PF	Power Factor	-	-
Q_s / Q_{sm}	Series Quality Factor	-	-
Q_p / Q_{pm}	Parallel Quality Factor	-	-
r_c	Capacitor ESR	ohms	[Ω]
r_{cp}	Parallel Resonant Capacitor ESR	ohms	[Ω]
r_{cs}	Series Resonant Capacitor ESR	ohms	[Ω]
r_{ds}	Mosfet Drain to Source ON Resistance	ohms	[Ω]
R_{IN}	Modem Input Impedance	ohms	[Ω]
r_L	Inductor ESR	ohms	[Ω]
R_{LB}	Boost Converter Effective Load Resistance	ohms	[Ω]
R_k	Connection Resistance	ohms	[Ω]
r_{lp} / r_{lpr}	Parallel Resonant Inductor ESR	ohms	[Ω]
r_{ls}	Series Resonant Inductor ESR	ohms	[Ω]
R_{eq}	Equivalent Load Resistance	ohms	[Ω]
r_s	Resonant Tank Series Resistance	ohms	[Ω]
R_T	Total Modem Input Impedance	ohms	[Ω]
$r_{winding}$	Transformer Winding Resistance	ohms	[Ω]
R_L / R_{LOAD}	Load Resistance	ohms	[Ω]
T_d	Switching Dead Time	sec	[s]
T_{OCC}	One Cycle Controller Integral Time Constant	sec	[s]
T_s	Switching Period	sec	[s]
v_a	HFAC Resonant Inverter Tank Input Voltage	volts	[V]
v_{a_AC}	AC Component of HFAC Resonant Inverter Tank Input Voltage	volts	[V]
v_{bus}	HFAC Bus Voltage	volts	[V]
V_{AC}	AC Source Voltage	volts	[V]
V_{bus}	RMS HFAC Bus Voltage	volts	[V]
V_{bus_peak}	HFAC Bus Peak Voltage	volts	[V]

Notation	Description	Unit	
$v_{bus\_primary}$	HFAC Bus Voltage Referred to Primary	volts	[V]
v_{cp} / $v_{cp'}$	Parallel Resonant Capacitor Voltage	volts	[V]
v_{cp_RMS}	Parallel Resonant Capacitor RMS Voltage	volts	[V]
v_{cs} / $v_{cs'}$	Series Resonant Capacitor Voltage	volts	[V]
v_{cs_RMS}	Series Resonant Capacitor RMS Voltage	volts	[V]
V_D	Diode Forward Voltage	volts	[V]
V_{DC}	DC Source Voltage	volts	[V]
V_{DS}	Mosfet Drain to Source Voltage	volts	[V]
V_{IN}	Resonant Inverter Input Voltage	volts	[V]
V_{LMAX}	Boost Inductor Max Average Voltage	volts	[V]
V_{LMIN}	Boost Inductor Min Average Voltage	volts	[V]
v_{lp} / $v_{lp'}$	Parallel Resonant Inductor Voltage	volts	[V]
v_{ls} / $v_{ls'}$	Series Resonant Inductor Voltage	volts	[V]
V_m	Modulating Signal	volts	[V]
V_{mdm}	Modem Transmit Amplifier Output Voltage	volts	[V]
V_{OUT} / V_o	Average Output Voltage	volts	[V]
v_p / $v_{p'}$	Transformer Primary Voltage	volts	[V]
$v_{pn'\_RMS}$	RMS Value of the nth Harmonic of Transformer Primary Voltage	volts	[V]
$v_{p1'\_RMS}$	RMS Value of the Fundamental Component of Transformer Primary Voltage	volts	[V]
V_{r_pp}	Boost Capacitor Ripple Voltage	volts	[V]
V_{REF}	Control Loop Reference Voltage	volts	[V]
V_{REF_BUS}	HFAC Bus Reference Voltage	volts	[V]
V_{REF_IN}	Input Reference Voltage	volts	[V]
v_s	Transformer Secondary Voltage	volts	[V]
v_{s_peak}	Transformer Secondary Peak Voltage	volts	[V]
V_{syn}	Synthesized Output Voltage	volts	[V]
v_{th}	Thevenin Equivalent Voltage	volts	[V]
W_A	Core Window Area	square centimeter	[cm^2]
X_{CP}	Reactance of Parallel Resonant Capacitor	ohms	[Ω]
X_{CS}	Reactance of Series Resonant Capacitor	ohms	[Ω]
X_{LP}	Reactance of Parallel Resonant Inductor	ohms	[Ω]

Notation	Description	Unit	
X_k	Connection Reactance	ohms	[Ω]
X_{LS}	Reactance of Series Resonant Inductor	ohms	[Ω]
X_p	Reactance of Parallel LC Branch	ohms	[Ω]
X_s	Reactance of Series LC Branch	ohms	[Ω]
Z_{cpn}	Impedance of Parallel Resonant Capacitor and ESR	ohms	[Ω]
Z_k	Connection Impedance	ohms	[Ω]
Z_L	Load Impedance	ohms	[Ω]
Z_{lpn}	Impedance of Parallel Resonant Inductor and ESR	ohms	[Ω]
Z_{sn} / $Z_{s'}$	Impedance of Series Resonant Branch	ohms	[Ω]
Z_{pn} / $Z_{p'}$	Impedance of Loaded Parallel Resonant Branch	ohms	[Ω]
$Z_{pr'}$	Unloaded Impedance of Parallel Branch of LCLC tank	ohms	[Ω]
Z_{th}	Thevenin Equivalent Impedance	ohms	[Ω]
Z_{txn}	Transformer Series Impedance	ohms	[Ω]
Z_{in} / $Z_{in'}$	Resonant Tank Input Impedance	ohms	[Ω]
α	Phase Shift Angle	radian	[rad]
β	Core Loss Exponent	-	-
ϕ_n	Phase angle of Resonant Tank Input Voltage	radian	[rad]
ω_s / ω_{sm}	Series Resonant Angular Frequency	radians per second	[rad/s]
ω_p / ω_{pm}	Parallel Resonant Angular Frequency	radians per second	[rad/s]
ω_{bus}	HFAC Bus Angular Frequency	radians per second	[rad/s]
ω_o	Fundamental Angular Switching Frequency	radians per second	[rad/s]
λ	Transformer Primary Volt Second	volt-sec	[V-sec]
ℓ_m	Magnetic Path Length	centimeter	[cm]
ρ	Wire Effective Resistivity	ohm-centimeter	[Ω-cm]
η	Efficiency	-	[%]

Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
ATX	Advanced Technology eXtended
BJT	Bipolar Junction Transistor
BPF	Band Pass Filter
CDC	Centralized Direct Current
CMOS	Complementary Metal Oxide Semiconductor
CPS	Centralized Power System
CPU	Central Processing Unit
CS	Checksum
CSC	Current Sharing Controller
CSMA-CD	Carrier Sense Multiple Access with Collision Detection
DA	Destination Address
DC	Direct Current
DCR	Direct Current Resistance
DLF	Data Length Field
DPA	Distributed Power Architecture
DPS	Distributed Power System
DSC	Digital Signal Controller
DSP	Digital Signal Processor
DTF	Data Type Field
EFD	End Frame Delimiter
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EPR	Equivalent Parallel Resistance
ESR	Equivalent Series Resistance
EV	Electric Vehicle
FBICC	Full Bridge Integral Cycle Converter
FET	Field Effect Transistor
FSK	Frequency Shift Keying
HBICC	Half Bridge Integral Cycle Converter
HFAC	High Frequency Alternating Current

HVDC	High Voltage Direct Current
ICC	Integral Cycle Converter
IGBT	Insulation Gate Bipolar Transistor
ISS	International Space Station
LED	Light Emitting Diode
LFAC	Low Frequency Alternating Current
LPF	Low Pass Filter
LVDC	Low Voltage Direct Current
MAG-AMP	Magnetic Amplifier
MCU	Micro Controller Unit
MIMO	Multiple Input Multiple Output
MIPS	Million Instructions per Second
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
M-PSM	Modified – Pulse Shift Modulation
MSI	Multi Stage Inverter
NASA	National Aeronautics & Space Administration
NRZ	Non Return to Zero
OCC	One Cycle Control
OOK	ON OFF Keying
PC	Personal Computer
PCB	Printed Circuit Board
PDA	Power Distribution Architecture
PF	Power Factor
PFC	Power Factor Correction
PFD	Phase Frequency Detector
PI	Proportional - Integral
PID	Proportional – Integral - Derivative
PLL	Phase Locked Loop
POL	Point of Load
PPM	Pulse Phase Modulation
PPU	Power Processing Unit
PRC	Parallel Resonant Converter
PSM	Phase Shift Modulation
PSU	Power Supply Unit
PWM	Pulse Width Modulator

RA	Receive Amplifier
RCD	Resistor Capacitor Diode
RMS	Root Mean Square
SA	Source Address
SFD	Start Frame Delimiter
SMPS	Switch Mode Power Supply
SRC	Series Resonant Converter
SSC	Soft Switching Control
SSI	Single Stage Inverter
TA	Transmit Amplifier
THD	Total Harmonic Distortion
VCO	Voltage Controlled Oscillator
VMC	Voltage Mode Control
VRM	Voltage Regulation Module
ZCS	Zero Current Switching
ZVRT	Zero Voltage Resonant Transition
ZVS	Zero Voltage Switching

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CHAPTER 1

INTRODUCTION

"The beginning of wisdom is found in doubting; by doubting we come to the question, and by seeking we may come upon the truth" – ***Pierre Abelard, 1079-1142.***

This chapter begins with an overview of existing power architectures and presents a logical classification structure to categorize the various power systems. A comprehensive discussion on the general features of a distributed power system is first presented. Following this, the motivation for high frequency AC power distribution is explored as it has been proposed as a potential alternative to existing systems. The scope of the problem as covered by this work is then defined and the main aims and objectives of the research are set out. Next, the research methodology adopted in this work is presented and the key contributions as a result of this research are then outlined. This section concludes with a brief description of the subsequent chapters to give an overview of the entire thesis.

1.1 Overview

This research is motivated by the ever increasing need for efficient means of power processing and distribution in any power delivery system. A power distribution architecture (PDA) refers to a systematic configuration of various power sources, power converters, distribution medium and loads capable of effective and efficient management of power flow from one point in the system to another. Thus the PDA not only refers to the familiar electric power utility grid but covers a broader definition. An example of a local PDA would be power distribution within a personal computer (PC), or the power architecture in vehicles. In land vehicles, the power system consists of a battery as a primary power source and power is distributed via cables to various loads in the vehicle.

Modern state of the art electronic systems place high constraints on the power delivery system. However the basic power architecture until recently remained the same as it was decades ago. Many of the current architectures may no longer be effective in terms of performance and cost [1-3]. PDAs are evolving from the traditional centralized power architectures to more complex distributed power systems (DPS). In a centralized power system (CPS), power is processed in a centralized location where all the required system voltages are generated. These are then distributed via a bus to power loads throughout the system. Distributed power systems have now replaced the centralized power system in many applications. The first widespread use of distributed power systems was in the avionics industry [4]. In a DPS, the power processing function is decentralized and is collectively performed by the many power converters present in the system.

Distributed power systems come in many variants and are generally characterized by the bus voltage type. In general, there are two types of DPS, an AC DPS and DC DPS. In an AC DPS, the front end power processor converts the source power to an AC voltage that is then distributed throughout the entire system. Local point of load (POL) converters converts the AC bus voltage to the required form. Similarly in a DC DPS a DC voltage is generated and distributed to the entire system.

The AC DPS can be further classified by the frequency of the bus voltage. It is broadly categorized as low frequency AC (LFAC) and high frequency AC (HFAC). Low frequency typically refers to AC voltage frequencies of 50Hz and 60Hz. Frequencies

greater than the mains voltage are normally referred to as high frequency AC. Frequencies as high as 1MHz have been proposed for some HFAC applications.

The DC DPS is classified by the voltage level of the bus, as low voltage DC (LVDC) and high voltage DC (HVDC). No universal definition for high and low voltages exists. The distinction is normally made in reference to a particular application. The categorization of power network is shown in Figure 1.1.

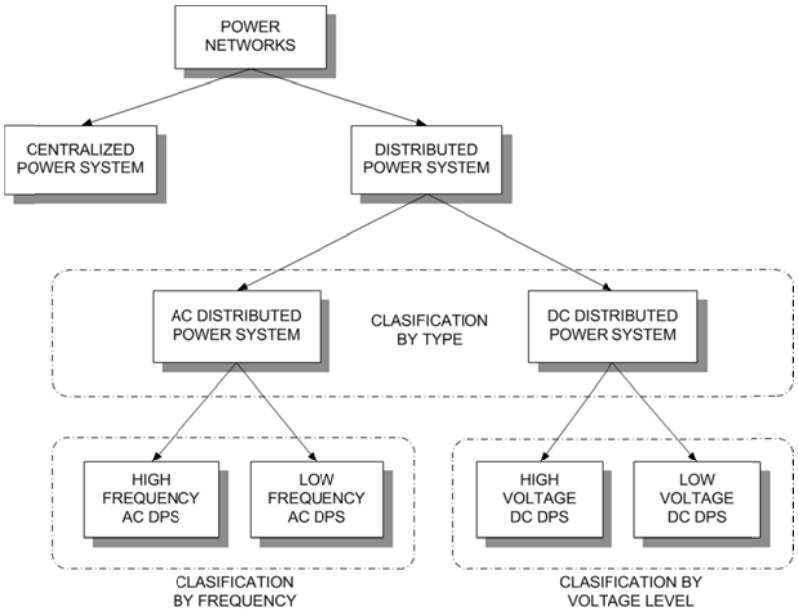


Figure 1.1 : Categorization of power architecture

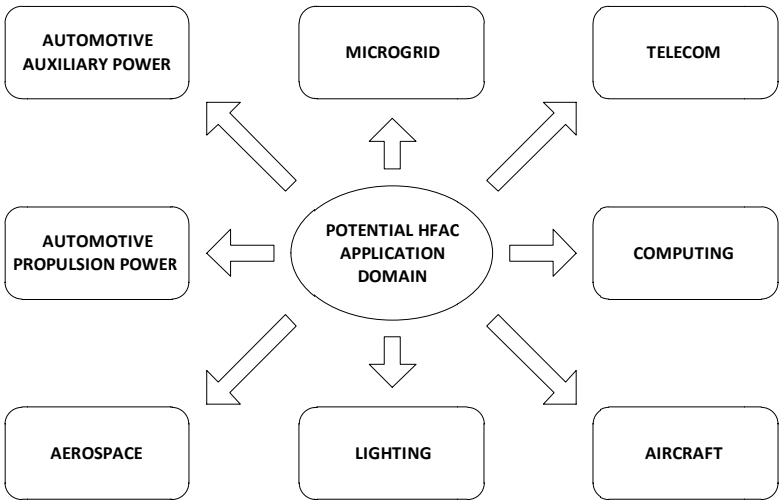


Figure 1.2 : Potential HFAC application domain

HFAC DPS has been considered for a variety of applications as shown in Figure 1.2, due to perceived advantages over DC DPS and LFAC DPS. In the next section the basic concept and features of distributed power system are discussed.

1.2 Background on Distributed Power System

In a distributed power system, the power processing functions are de-centralized and distributed throughout the system. The front end power converter converts the input power source to an intermediated voltage, (usually called the bus voltage) suitable for efficient distribution. This voltage is distributed throughout the power network. Loads are connected to this network through an interfacing power converter that transforms the bus voltage to the form that is required by the load. A typical example of distributed power system is shown in Figure 1.3 which consists of various loads and power sources

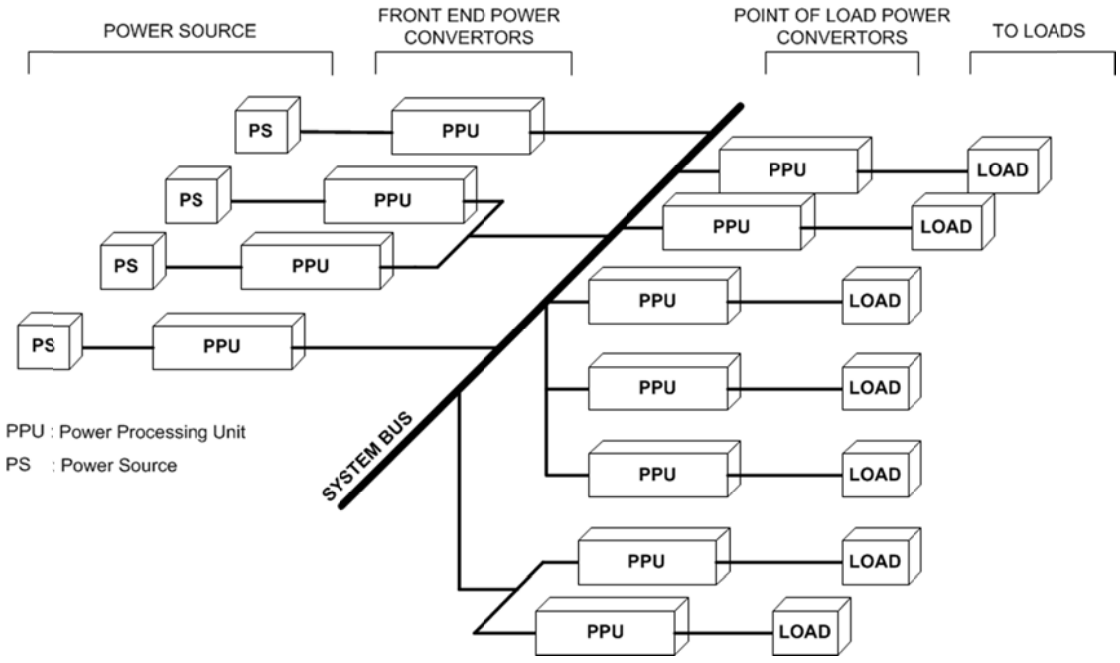


Figure 1.3 : Typical distributed power architecture (extracted from [5])

The building blocks of a complex distributed power architecture is based on basic units called distributed structures. Distributed power systems are built using combinations of these basic structures. The four basic structures are (i) parallel structures, (ii) series or

cascaded structures, (iii) source splitting and (iv) load splitting structures. These structures are shown in Figure 1.4

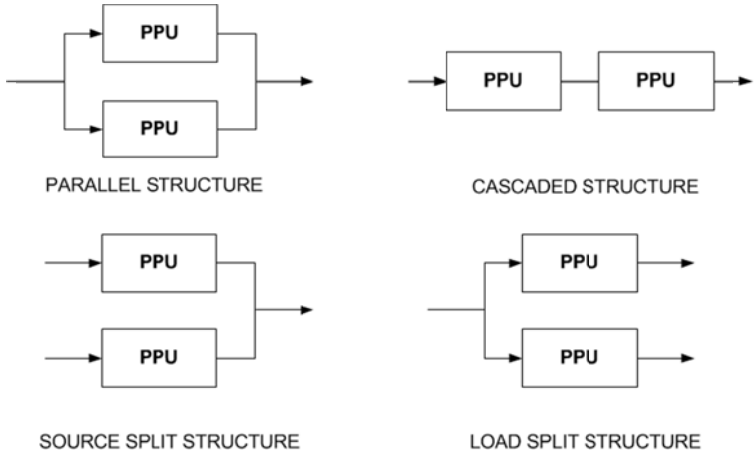


Figure 1.4 : Distributed power structures (extracted from [5])

The characteristics of distributed power systems have been widely described in literature [5-11], the salient features are discussed below.

1.2.1 Simplified Thermal Management

In parallel configuration of power processing units (PPU), the power handling requirement for each unit is lower than the total required power. As each unit only handles part of the total power, the cooling requirement is lower and this translates to smaller heat sinks. Distributing the sources of heat generation allows for more efficient heat sink area utilization and possibly eliminates the need for forced cooling. This further leads to reduced cost and smaller physical size of the power processing units.

1.2.2 Reduced Size & Higher Power Density

Lower operating power level for PPUs offered by the distributed power architecture, leads to PPU design with enhanced power density. This is generally achieved by increasing the switching frequency of the power converter. Higher switching frequencies lead to decrease in physical size of magnetic and filter components. Together with the reduced size of mechanical components such as heat sinks and bus bars, the overall mass and volume of the PPUs will be reduced.

1.2.3 Modularity & Flexibility

The DPS naturally promotes modularity. As opposed to centralized power system, which is typical custom designed for each application, the DPS can be configured using standard power modules. These standard modules can be used to build the basic power structures and subsequently the entire power distribution system to meet specific application requirements. The system can benefit from all the advantages of using standardized modules such as reduced design and engineering cost, faster development cycles, increased reliability and possibly lower unit cost for each standardized module due to economy of scale.

Another important feature is the flexibility of the system to readily accommodate changes in power capacity. Should the power requirement for the system increase, additional PPU modules can be added to provide the additional power. From a cost perspective, this offers an attractive advantage, which can be derived from the "pay as you grow" [10] concept. Conversely, recovering from overly optimistic initial power budget estimates are also possible, as the system can be easily scaled down when necessary.

1.2.4 Reliability

In a DPS, while the number of components may be higher, the thermal and electrical stresses on the PPUs are lower due to lower power handling requirements. In addition, higher switching frequencies in power converters result in higher control bandwidth that enables faster response to system abnormalities and adverse system conditions such as overload and short circuit [8]. These arguments show that the overall reliability of the DPS is higher.

1.2.5 Redundancy

The parallel power structure has inherent support for redundancy. Configuring more PPUs in a parallel fashion than the minimum number necessary to meet load requirements enhances system reliability. Typically (n+m) modules (PPUs) are used, where 'n' is the minimum number of modules required for proper system operation and

'm' is the number of additional redundant modules. This redundant framework enables the system to tolerate 'm' failures without any impact to the system [9]. While redundancy is a desirable feature in most systems, it is mandatory in some high reliability applications.

1.2.6 Maintainability

In a DPS, it is possible to localize and isolate faults more easily due to the distributed nature of the power processing function. Thus a faulty power processing module may only cause part of the distribution network to fail and does not render a complete system failure. DPS can also be specifically designed to allow for on line replacement (hot-swapping) of defective power modules. This provides means for non-interrupting maintenance and repair, a very desirable feature for high reliability systems with low down time tolerance.

1.2.7 Point of Load Regulation

In cascaded power structures, the existence of the point of load power converter in close physical proximity to the load improves voltage regulation and dynamic response. The POL decouples the load and power bus on an instantaneous basis.

1.2.8 Reduced Distribution Losses

Cascading of power processors to introduce intermediate bus voltage has an important implication in enhancing distribution efficiency. Increasing the intermediate bus voltage to a suitable level to reduce the distribution currents will reduce the copper losses (I^2R) in the distribution network. Thus the overall efficiency of the system is improved. The cascading structure allows the front end PPUs to generate a higher voltage that is consistent with low transmission losses without being dictated by load voltage requirements. Load voltages are derived locally by POL convertors. In addition, low current distribution results in simpler, smaller, lighter and less expensive distribution harnesses.

1.2.9 Multiple Power Source Blending

A separate front end PPU is often required for each power source; therefore it is possible to blend multiple power sources to supply power to the bus. This is potentially important in systems that require uninterrupted power supply that often need battery backups. The DPS can be designed to be powered from a several primary and secondary power sources to increase system capacity and provide redundancy.

1.3 Motivation for HFAC Research

Modern loads with sophisticated control systems are placing stringent requirements on the design of power distribution systems. The steadily increasing power level, demand for high current level at low voltages, high current slew rate and stringent transient voltage regulation requirements are becoming more and more common in today's systems. The current power delivery and processing technologies are being pushed to the limits to cope with the rigorous demands of the loads in some applications.

In various domains, the leap from centralized power system to the distributed power system has been made in the past. Most of these systems are currently based on a DC distributed system. Although this has paved the way for more versatile powering means than previously possible, the time has now come to re-assess the viability of the DC distributed power system for some current and future applications. It is widely agreed that improvement or new development in power distribution architecture is vital to ensure that power demands of the future are adequately met.

Whilst the DC DPS has resolved many of the problems and limitation of the centralized power system, scrutinizing the design intricacies of the DC DPS has uncovered potential room for improvement. To begin with, the power processing chain from the source to the load involves many intermediate conversion steps. In general, power processing structures with several conversion steps in series will invariably lead to an inefficient overall power system. The typical block diagram of DC distribution system is shown Figure 1.5. It can be seen that there are a total of 5 conversion stages, three at the front end PPU, and a further two at the POL converter.

In a HFAC system, the number of conversion stages can be reduced. A block diagram of a typical HFAC DPS system is shown in Figure 1.6. The total number of conversion stages is reduced to 3 for the same input and output power configuration compared to a DC DPS. Therefore the HFAC DPS will generally have better efficiency, higher reliability and potentially lower cost. Further, HFAC DPS presents the possibility for directly tapping power from the bus via induction. This presents interesting application opportunity to be explored and dispenses the need for connectors.

It has been reported in literature that current at frequencies higher than 10kHz is safer for human cells compared to DC or low frequency AC [12]. Therefore in applications where human interaction with the distribution system is highly likely, HFAC may be preferred from a safety point of view. Furthermore compared to DC DPS, protection implementation in HFAC DPS could potentially be easier due to the periodic zero crossing in AC current. Implementation of fuseless protection in HFAC power converters is also possible and has been demonstrated to be viable [13, 14].

Emerging applications area such as modern LED lighting, microgrids and contactless charging of EV batteries, could potentially be an attractive application for HFAC DPS. With environmental concerns continuing to be a key issue in the modern economy and together with impending low carbon legislation, the pressure to improve energy efficiency is constantly increasing. This could perhaps pave the way for accelerated adaptation of HFAC technology.

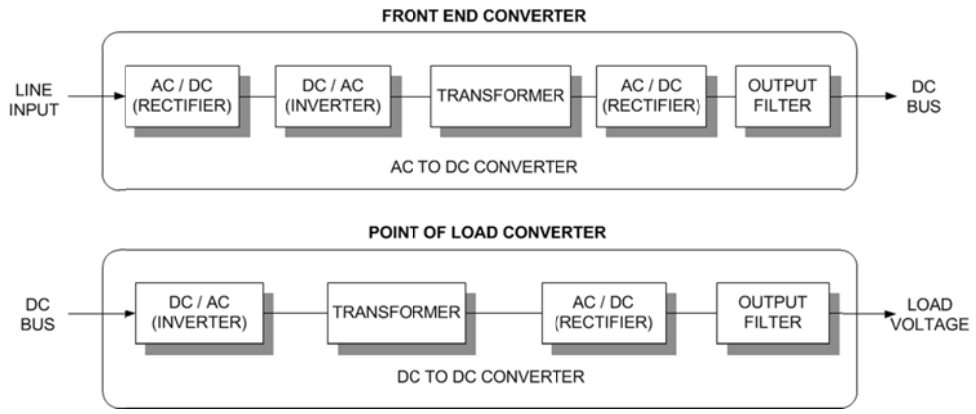


Figure 1.5 : Block diagram of DC distributed power system

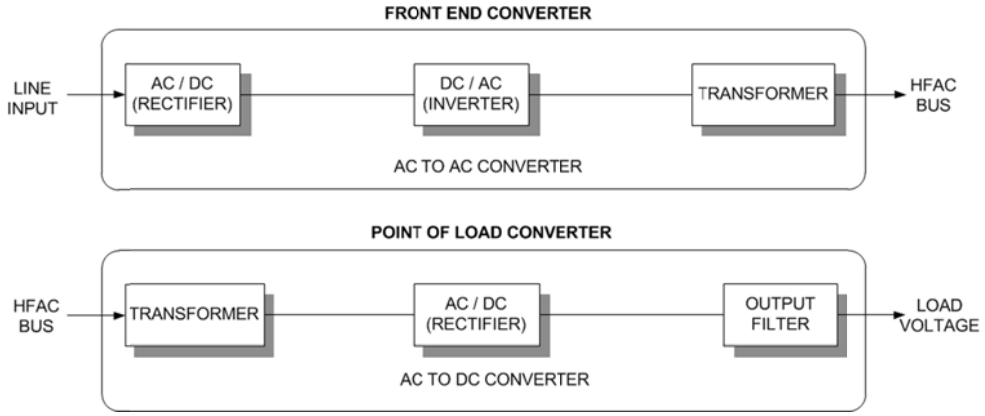


Figure 1.6 : Block diagram of HFAC distributed power system

1.4 Aims & Objectives

In a typical HFAC power distribution system there are 4 stages or subsystems categorized as (i) power generation (ii) power conversion (iii) power distribution and (iv) loads. The scope of this research is limited to the power conversion subsystem. In this category, the research is focused on 2 areas, firstly the front end HFAC inverter and secondly the point of load power converter. The investigation of the power converter is done in the context of a particular application. As such, the input and output power and voltages of the converters are defined specifications. In this research, the converters are designed for a HFAC DPS in automotive application for powering auxiliary loads. The input and output requirements are drawn from recent literature in this area. Additionally, this research introduces the communication subsystem not previously included in a typical HFAC DPS model.

In this research, the HFAC DPS is studied at both the subsystem and the system level to identify potential opportunities for improvement. At the subsystem level, the front end HFAC inverter and the point of load power converter is investigated separately to improve the performance of these individual subsystems. At the system level, intelligent management of the HFAC power network is investigated. More precisely, the aims of this research can be divided into two parts and is expressed as follows.

1. To develop techniques to guide optimal design of HFAC power converters to improve defined performance aspects of the converter.

2. To investigate the possibility of converting the existing HFAC DPS into a more intelligence architecture.

More specifically, the objectives of the research are

1. To undertake a critical review of the current state of the art of HFAC power converters and to identify potential areas for further investigation.
2. To analytically model the behaviour of HFAC power converters and based on these models develop design guide to improve its performance.
3. To validate the predictions of the mathematical model using simulation and experimentation.
4. To identify and develop the necessary 'enabling technologies' to convert the HFAC DPS into a more intelligent architecture.

1.5 Methodology

This research begins by recognizing the potential advantages of taking a holistic system level approach to the investigation of the HFAC DPS. To date, the research in this domain is predominantly focused on improving various aspects of the power processing structures in a typical HFAC DPS. Although improvement at the subsystem level is crucial and contributes to the viability of the overall system, it cannot be assumed that the system level performance depends solely on the performance of the individual subsystems. System level improvements can be attained by intelligent interaction between the various power processing structures in the system in real time. In this research, a top down approach is taken by first identifying the primary features that are necessary to realize an intelligent power architecture that provides a framework for system level improvements. Some of the features require subsystem level implementation and therefore defines part of the requirements of the individual subsystem.

The primary capabilities were identified as (i) the ability for the various power converters in the DPS to communicate and (ii) the ability for the front end inverter to respond based on real time information about the power system. This leads to two important requirements at the subsystem level. Firstly it establishes a need for a suitable communication mechanism and secondly the power converters require some form of digital control capability to manage power flow based on information about the current

state of the system. Additionally, parallel operation capability of the inverter is an important implied feature that could potentially offer a wider range of system level control possibilities. Deriving the necessary enabling features at the outset based on high level system requirements, allows the various technologies to be tightly integrated at the subsystem level and therefore the design of the various subsystem can then proceed independently.

Mathematical modelling is used extensively in the development of the various subsystems. Analytical model derived from first principals are used to precisely describe circuit level behaviour. As the fundamental aim is to develop procedures that enable optimal design, the models need to be sufficiently accurate and comprehensive to capture all significant effects. Conversely, overly complicated model may be counterproductive as important feature may be obscured by mathematical complexity. Approximation and simplifying assumptions are used where possible to yield models that are simpler and computationally efficient. In these situations, the effects on accuracy is carefully considered and quantified where possible.

The mathematical models are used as a starting point for various downstream design processes and therefore require some form of independent validation to ensure the integrity of the models. Circuit simulation software is widely used to validate the mathematical models. In general, circuit simulation tools offer more accurate results as they incorporate physics models of the various components, which are more realistic. In this work, PSPICE software is used to perform circuit simulations and for all critical parts exact models of components used in the physical design are also used in the simulation. The use of generic models is limited to non-critical components.

Finally, proof of concept prototypes are constructed based on the design procedures derived from the mathematical model. Experimental measurement is then used to validate the prediction of the theoretical models. Any discrepancies are investigated and the models are updated as necessary to better reflect physical behaviour.

1.6 Original Contributions

The key contributions of this work can be summarized as follows.

1. The work presents a fresh perspective to the HFAC DPS by introducing 'intelligence' into the power architecture. This challenges the current notion of viewing the HFAC DPS merely as a passive power distribution system. The 'enabling technologies' necessary to realize an intelligent power network is identified and developed. This offers vast potential to implement 'smartgrid' like features, data collection and health monitoring.

2. The viability of enabling multi node bidirectional communication over the HFAC power bus without the need for additional communicational channel is demonstrated in this work. A novel HFAC data modem capable of enabling communication over both current fed and voltage fed HFAC DPS is developed and experimentally validated.

3. In this study a systematic approach to the design of a HFAC MSI is presented. The proposed technique captures operating requirements, desired performance goals, physical design constraints and accounts for component non-idealities. An important consequence of this approach is the selection of the first stage DC-DC converter based on efficiency calculation. In general literature, the first stage DC-DC converter is viewed only as a means to provide independent amplitude control and as such its selection is normally dictated by the input voltage variation range.

4. Digital control technique to achieve independent magnitude and phase angle control in HFAC MSI is established to be viable for low and medium frequency implementation. It is shown that the controller complexity is no greater than what would be necessary for regular DC-DC converter. Independent phase and magnitude control enables parallel operation of inverters. All previous implementation reported in literature are based on analog controllers.

5. This work presents a new mathematical framework to compute the input current harmonic spectrum of an integral cycle converter based on the output voltage synthesis pattern. This model is used to determine optimal synthesis sequence that helps to relax the requirement for the input current shaping filter and therefore have positive effect on power factor.

1.7 Thesis Outline

Chapter 2 begins with background history to understand the reasons behind the arising need for HFAC DPS. To this end the limitations of existing systems and the initial implementation detail of HFAC DPS in space application is discussed. Following this, other application areas of HFAC DPS such as computing, telecommunication, etc. are covered to demonstrate the viability of this new power distribution architecture.

Chapter 3 to 5 is focused on the investigation of the front end DC to HFAC inverter. In Chapter 3 a literature survey of the front end HFAC inverter is first undertaken followed by a detailed comparative study of the various proposed topologies. Resulting from this study the gaps in existing research that presents an opportunity for further research is identified. Chapter 4 covers the modelling of the LCLC resonant inverter which forms the second stage of a multi stage resonant inverter. The modelling and design of the front end DC-DC converter which constitutes the first stage of the multi stage inverter is covered in Chapter 5. In addition control implementation and experimental results are also presented in this chapter.

Chapter 6 covers the point of load converter in a HFAC DPS. A literature survey is first undertaken to gain appreciation of the state of the art. A particular type of POL converter called the integral cycle converter is then examined and a new mathematical model to describe the behaviour of the converter is presented. The validity of the proposed model is verified using circuit simulation techniques.

Chapter 7 presents a novel technique that enables communication over the HFAC power bus without the need for an additional communication channel. A comprehensive discussion on the design aspect of a data modem capable of overlaying communication

signal over the HFAC voltage/ current waveform is given. A proof of concept prototype was constructed to demonstrate the viability of the technology.

Chapter 8 concludes this dissertation with an overall conclusion on the 'enabling technologies' developed in the course of this research to convert the HFAC DPS into an 'intelligent power architecture'. Recommendation for future work is also presented in this chapter.

1.8 Publications and Reports

1. Lourdes S., Luk P. C. K., Bendyk M., (2008). **"An Analytical Model for Harmonic Content Computation of HFAC Power Distribution Systems"**. Cranfield Multi-Strand Conference (CMC), 2008.

2. Lourdes S., Luk P. C. K., Jinupun K., (2009). **"An Alternative Power Grid – High Frequency AC Power Distribution Platforms".** IEEE International Conference on Power Electronic and Motion Control, 2009. IPEMC 2009.

3. Lourdes S., Luk P. C. K., Ng A.S.Y., (2009). **"Unity Power Factor Integral Cycle Converter for High frequency AC Power Distribution Systems".** IEEE International Conference on Power Electronics and Drive Systems, 2009. PEDS 2009.

4. Lourdes S., Luk P. C. K., Jinupun K., (2009). **"Switching Strategy for Integral Cycle Converter in a High Frequency AC Distributed Power System".** IEEE International Conference on Power Electronics and Drive Systems, 2009. PEDS 2009.

5. Lourdes S., Luk P. C. K., (2008) **"Position Paper - HFAC Implementation in Automotive Environment".** Internal HIFPADD Project Report (Restricted).

6. Lourdes S., Luk P. C. K., (2008) **"A Review of HFAC Voltage Regulation Module Topologies".** Internal HIFPADD Project Report (Restricted).

7. Lourdes S., Luk P. C. K., (2009) **"Viability of HFAC as an Alternative Distributed Power System – A Quantitative Approach**". Internal HIFPADD Project Report (Restricted).

8. Lourdes S., Luk P. C. K., (2009) **"AC Voltage Synthesis – Discrete Phase Shift Modulation".** Internal HIFPADD Project Report (Restricted).

9. Lourdes S., Luk P. C. K., (2009) **"Current Fed Integral Cycle Converter for High Frequency AC Power Distribution System".** Internal HIFPADD Project Report (Restricted).

10. Lourdes S., Luk P. C. K., (2009) **"Modelling of Resonant Rectifier Based on Push Pull Parallel Resonant Converter Operating in Inverse Mode".** Internal HIFPADD Project Report (Restricted).

11. Lourdes S., Luk P. C. K., (2010) **"J2 HFAC Data Modem Design Document"**. Internal HIFPADD Project Report (Restricted).

CHAPTER 2

HIGH FREQUENCY AC DISTRIBUTED POWER SYSTEM & ITS APPLICATIONS

"The reasonable man adapts himself to the world. The unreasonable one persists in trying to adapt the world to himself. Therefore, all progress depends on the unreasonable man" - ***George Bernard Shaw, 1856-1950.***

Since its conception in the early 1980s, HFAC distributed power system has been considered for various applications. This chapter begins by exploring the reasons behind the need for a new power distribution architecture in aerospace application and how this gave rise to HFAC technology. Following this, a detailed account of the implementation of HFAC DPS in other application areas such as telecommunication, computing, automotive and lighting are discussed. In each application domain, the various existing power delivery technologies are first examined and are compared to the proposed HFAC architecture. In most cases, the power distribution architecture appears to evolve in a similar trend, starting from centralized implementation and leading to some form of high voltage distributed system. It is shown in the discussions that the next logical step in this progression is the HFAC DPS. Finally future prospect for HFAC DPS is briefly discussed.

2.1 History of HFAC – Aerospace Application

The need for HFAC DPS first arose in the aerospace domain. It was initially proposed by NASA to replace the then existing power distribution system in spacecrafts. This decision was taken in response to a study conducted by NASA in the early 1980s to estimate spacecraft power demand. The study concluded that the projected power requirement for future spacecraft could grow to the megawatt level by the year 2000 [15]. Following this, an appraisal of the existing power distribution system was undertaken in light of predicted future requirements. It was established that the low voltage DC based distribution architecture at that time, could not meet the projected power requirement for future space applications.

The total electrical power in most spacecraft that NASA had launched till then averaged under 1kW. This naturally led to a simple low voltage (28V) DC based power distribution architecture. Copper losses in distribution cables are not significant at these low power levels. At higher power levels, greater than 10kW to 15kW, low voltage distribution would incur large ohmic losses in the distribution system [16], thus becoming less appealing from an efficiency point of view. In addition, DC power distribution has other inherent limitations that impair the flexibility of the distribution system. In the next section, the limitation of the pre-existing LVDC DPS in space application is discussed. This is then followed by a discussion on environmental considerations that impose constraints on the design of the DPS. Finally the justification for HFAC DPS as a viable alternative to the LVDC DPS is addressed.

2.1.1 Limitations of Low Voltage DPS in Spacecraft

The main limitations of LVDC DPS are high distribution losses, inefficient voltage conversion and lack of flexibility. Distribution losses not only impose efficiency penalties but also have financial consequences. Mitigating I^2R losses in the distribution stage requires the use of large distribution cables. This inevitably leads to higher copper mass, thus heavier cables and subsequently higher cost. This is not desirable especially for mass sensitive aerospace application. Typical cable mass per meter as a function of current rating is given in Figure 2.1. Launch cost is estimated to be in the region of $20000 dollars per kilogram [17], therefore payload weight is extremely critical and it is vital that

it be kept as low as possible. In large spacecraft, the transmission distance between the source and the load require long cable lengths and even a small increase in conductor radius can contribute to large increase in mass.

In a DC distribution system, voltage conversion from one level to another involves high power processing overheads. DC voltage conversion is generally more complex and not as efficient as transformers in AC voltage conversion [18]. Inefficient conversion inevitably limits the number of power conversion stages in the system. As such, the choice of the distribution voltage is often strongly influenced by the source voltage. Additionally, loads would generally need to be designed to operate at the bus voltage without intermediate point of load converters. This is not only inconvenient, but also demands high degrees of customization, as standard ground based equipment are not compatible with the bus voltage.

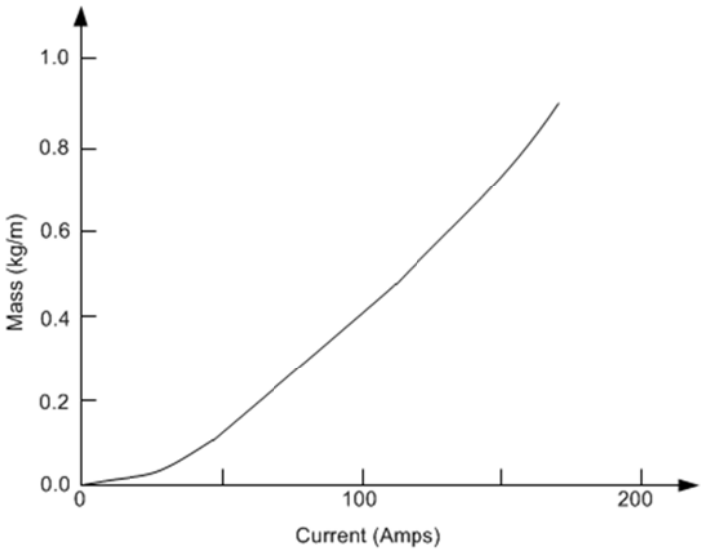


Figure 2.1 : Cable mass vs current rating (extracted from [19])

2.1.2 Environmental Limitation

Plasma interactions in space especially at low earth orbits limit the maximum operating voltage of the solar panels. This is due to the interaction between the exposed interconnections of the solar array and the charged-particles in space environment. Consequently, solar panels are often operated at lower than the desired operating voltage. This is one of the main reasons that led to low voltage power distribution in early

spacecraft. Insulating the solar array could in general allow higher operating voltages, but this was deemed ineffective, as it does not provide sufficient immunity and increases weight [15]. The interested reader is referred to [20] for more information pertaining to the effects of plasma interactions on spacecraft.

2.1.3 Rationale for HFAC Distribution System in Spacecraft

To achieve high overall system efficiency it is important that each stage of the system, the power generation, distribution and consumption (load) be collectively designed to be as optimal as possible without being constrained by the limitation imposed by the preceding or the subsequent stage. The environment imposed limitation on the maximum operation voltage of the solar panel is incompatible with high distribution efficiency. As such, it is vital that the solar array be decoupled from the distribution bus. This enables the solar panel to be operated within the limits permitted by environmental parameters without affecting distribution considerations. The power distribution stage can then be optimized based on the total power demand and transmission distances via selection of appropriate bus voltage.

This naturally gives rise to distributed power architecture with a high voltage distribution bus to reduce distribution losses. Power sources and loads can be connected to the bus via intermediate power converters that can be designed to support sources and loads operating at various voltages, frequency and power levels. The modularity and flexibility offered by such a system would also allow the power network to be readily adapted to meet future power requirement.

In a spacecraft with numerous types of loads, each having different power and voltage requirement for optimal operation, it is critical that the system is capable of effective and efficient voltage transformation at every node. AC voltage conversion can be performed easily and efficiently compared to DC conversion. As such, AC power distribution offers better viability as it can be easily adapted to meet load requirements. It was reported in [21], that AC power appears to be preferable to DC power in almost all cases, with DC competitive only for the shorter cable runs. In the effort to keep overall system mass low, it is conceivable that increasing the bus frequency would improve the power

converter density due to reduction in size of magnetic and filter components. This implication led to the decision to distribute power at high frequency.

It is shown in the discussions above that a train of simple but insightful technical decisions led to the creation of HFAC DPS and its implementation in spacecraft. With HFAC DPS, the bus voltage can be kept high to reduce transmission losses and then locally converted to the required voltage efficiently at the point of use to meet specific load requirements. Besides meeting the requirements stated above, the HFAC DPS offers extra isolation as the network naturally promotes the use of transformers. Another advantage is the reduction in acoustic noise due to transformer hum. Figure 2.2 shows the block diagram of the proposed HFAC power distribution system used in space craft.

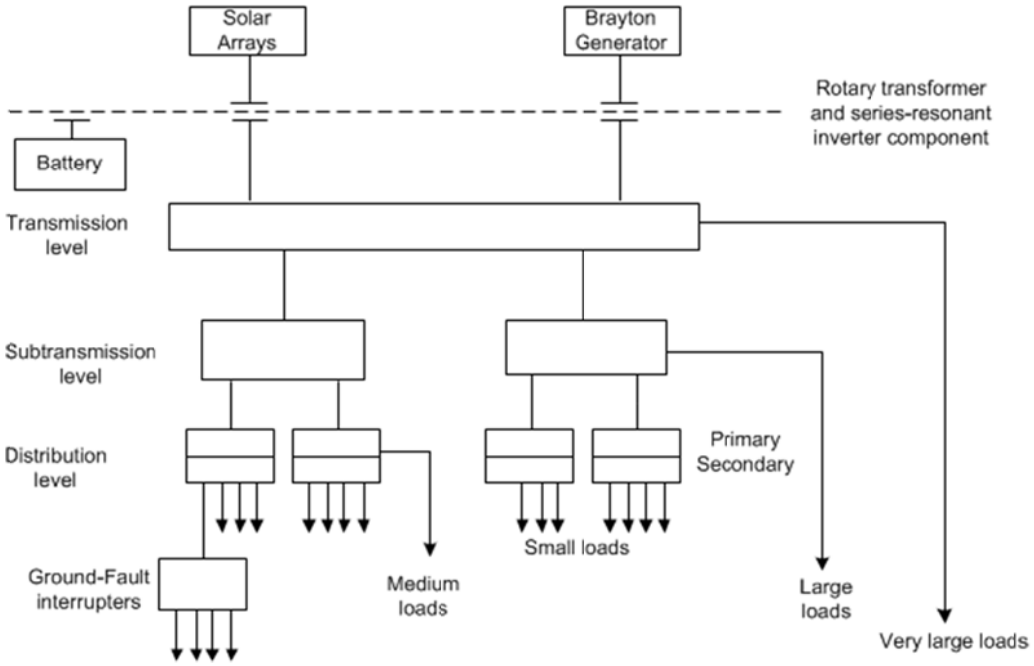


Figure 2.2 : Proposed HFAC power distribution system for spacecraft (extracted from [15])

2.1.4 Implementation Details of HFAC DPS in Space Station

In a later document [22], NASA reported that the power distribution in the space station will be accomplished using a 20kHz sinusoidal, 440Vrms single phase system. A parallel resonant inverter was proposed to generate the bus voltage. This converter was selected as it is suitable for parallel operation due to inherent low source impedance. One of the

major challenges for the HFAC DPS was the cabling harness and interconnects. There was a need for new power distribution cable with low AC resistance and inductance to reduce voltage drop, crosstalk and the external magnetic field of the cables. The simultaneous requirement of high efficiency and low cross talk was achieved by configuring the cables as double sided strip-lines. This helped to keep the inductance of the cable low. To mitigate skin effect, the conductors of the strip-lines were constructed as straps of woven individually insulated copper wire, forming a Litz wire type configuration, which offers low AC resistance [23].

2.2 HFAC in Non-Aerospace Domain

Soon after the application of HFAC DPS in the aerospace domain, the potential performance benefits of HFAC DPS over pre-existing power distribution technologies was beginning to be recognized. It soon stood as a serious contender for other more common ground based applications. HFAC DPS has been proposed for the following applications

1 Telecommunications

2 Computer and Commercial Electronics Systems

3 Aircrafts

4 Automotive

5 Microgrid & Lighting

In the following sections, the challenges faced by the existing power distribution systems in these areas are discussed and the potential benefits offered by HFAC implementation to mitigate these effects are addressed

2.3 HFAC in Telecommunication Application

The telecommunication industry has been particularly receptive to the idea of HFAC DPS. Application of HFAC DPS in the telecommunication domain has been widely discussed in literature [14, 24-27]. One of the early works in this area, by Joseph Drobnik [24] comprehensively covers the system level concerns of telecommunication powering schemes. Drobnik explained that the power distribution architecture in telecommunication system at the shelf or frame level has only been implemented in the DC domain. He goes on to explore HFAC DPS as a new powering scheme for telecommunication systems and demonstrates that it combines all the advantages of the existing DC powering option and in addition brings in new features that are otherwise technically impossible with the DC domain.

The commonly used DC powering scheme in telecommunication systems prior to the proposal of HFAC DPS is the centralized DC (CDC) power system and DC DPS. These are first discussed to identify limitations and to establish the need for a new distribution architecture.

2.3.1 Power Architecture in Telecommunication Application

The centralized DC power system is the most common powering scheme and is shown in Figure 2.3. The converter is fed from a battery (typically 48V) and it generates the required DC voltages for the cards (usually lower voltage) that are then distributed via the backplane. With this approach, besides I^2R losses, high current in the backplane causes the bus voltage to drop proportional to the distance of transmission. Consequently, the bus voltage presented to the system cards that is located further away from the centralized power supply will be lower. Therefore remote voltage sensing is often necessary to compensate for voltage drop across the backplane.

As the centralized power converter processes the total system power, the heat generated in the system is generally concentrated within the power convertor. This creates the need for expensive and bulky cooling systems.

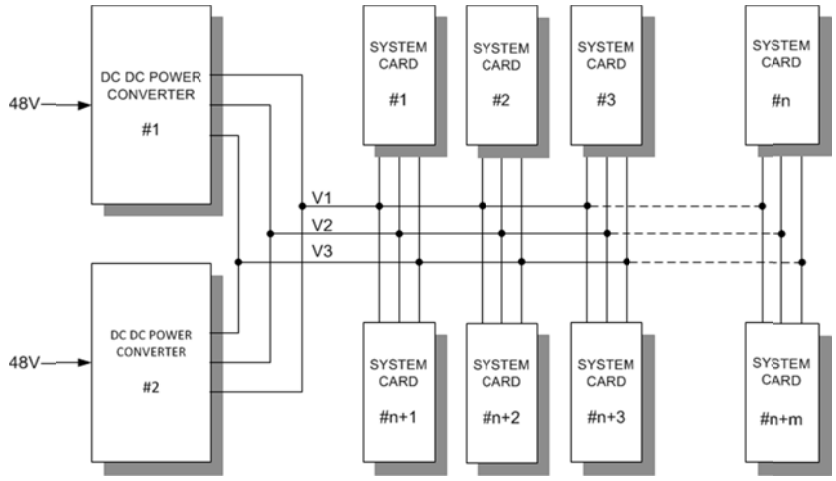


Figure 2.3 : Centralized DC/DC system in telecommunication systems (extracted from [24])

The distributed DC power architecture was later proposed as a better alternative to the centralized power system. A typical block diagram of the distributed DC power system is shown in Figure 2.4. This scheme requires a Point-of-Use Power Supply (PUPS). PUPSs are generally smaller power convertors which are distributed on each system card. The input to the PUPS is the bus voltage (48V) and the required lower output voltages are generated locally by the PUPS.

As the power processing function is shared between the front end power converter and the PUPS, the heat generated is distributed throughout the whole system. This reduces, or in some cases may eliminate the need for forced cooling. Power distribution at a higher voltage (48V) reduces the current levels in the backplane and subsequently decreases the I^2R losses significantly. This results in simpler construction of the backplane. Lower distribution currents also lead to simplified connectors and harnesses. Finally the use of PUPS ensures good voltage regulation and better noise immunity.

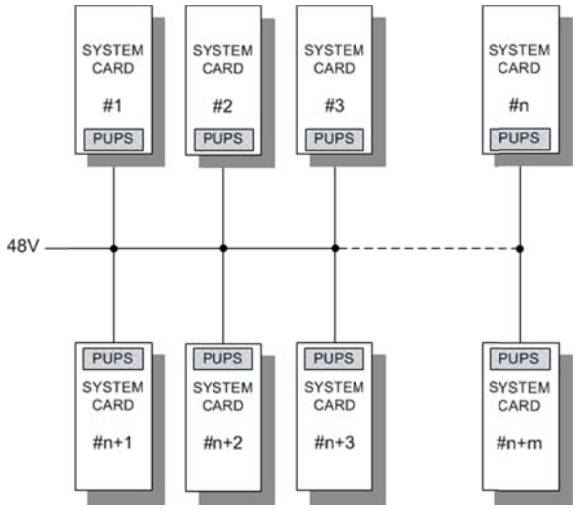


Figure 2.4 : Distributed DC/DC system in telecommunication systems (extracted from [24])

HFAC DPS as shown in Figure 2.5 was first proposed as an alternative to the DC based power system in [24]. A front end DC-AC inverter generates high frequency AC power at 60V RMS at 128kHz. The power is then distributed through the backplane to the various system cards where the required voltages are locally converted. In addition to the advantages offered by the DC DPS such as (i) low loss high voltage distribution, (ii) improved thermal management and (iii) better voltage regulation, the HFAC DPS has other advantages to offer.

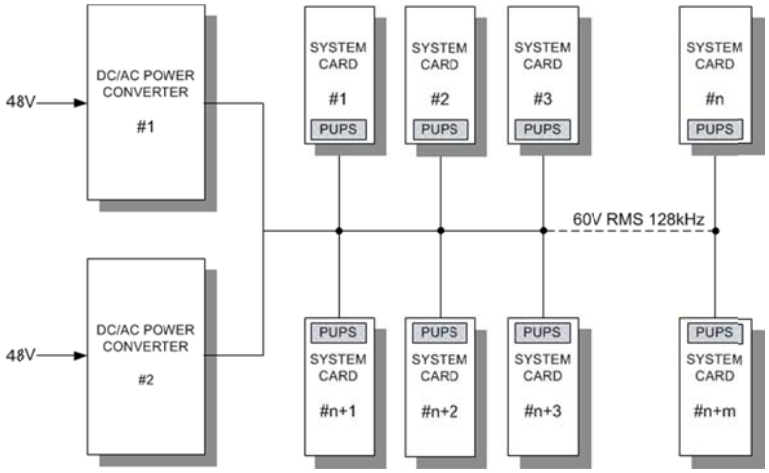


Figure 2.5 : HFAC DPS for telecommunication systems (extracted from [24])

The authors have claimed that the power converter in the HFAC DPS is generally more efficient, less complex and contains lower component count compared to the converters utilized in the DC DPS. The number of components not only effects cost but it is also used in reliability calculations. Therefore, fewer components yield better reliability. Figure 2.6 and Figure 2.7 shows the block diagram of the DC and HFAC power convertors respectively. Due to reduced number of power conversion stages, the HFAC power distribution architecture has higher overall efficiency.

The HFAC power converter is usually based on resonant topologies. Therefore besides the advantage of zero voltage / current switching, inrush current is naturally limited without the need for additional circuits. This makes hot-plugging of cards possible without added cost. Comparing Figure 2.6 and Figure 2.7 it can be noted that the absence of a low pass filter at the output of the HFAC power converter invariably leads to better dynamic response. Additionally, the innate use of transformers in the front end and local convertors in a HFAC DPS allows for the possibility of connector-less power supply. The transformers can be used as a media for magnetic coupling between the backplane and removable cards.

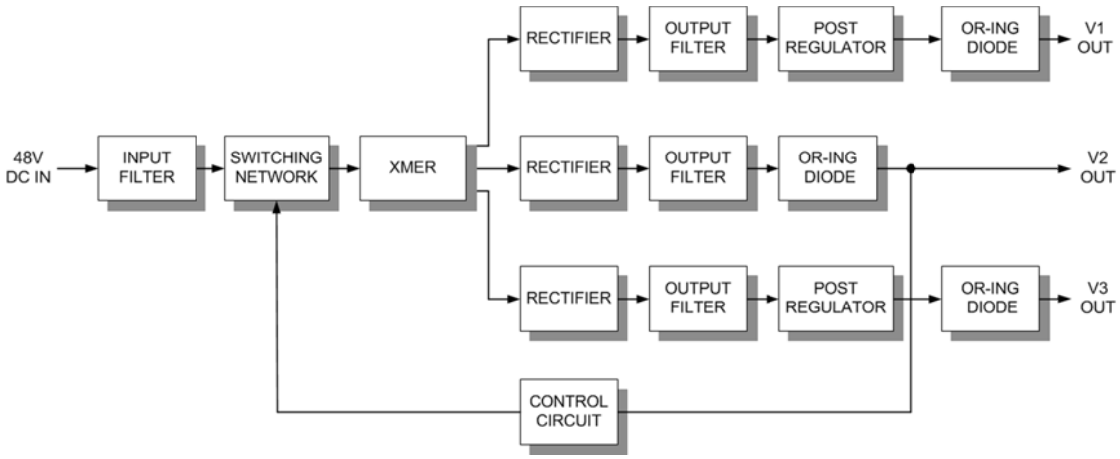


Figure 2.6 : Convertor Block Diagram of DC DPS (extracted from [24])

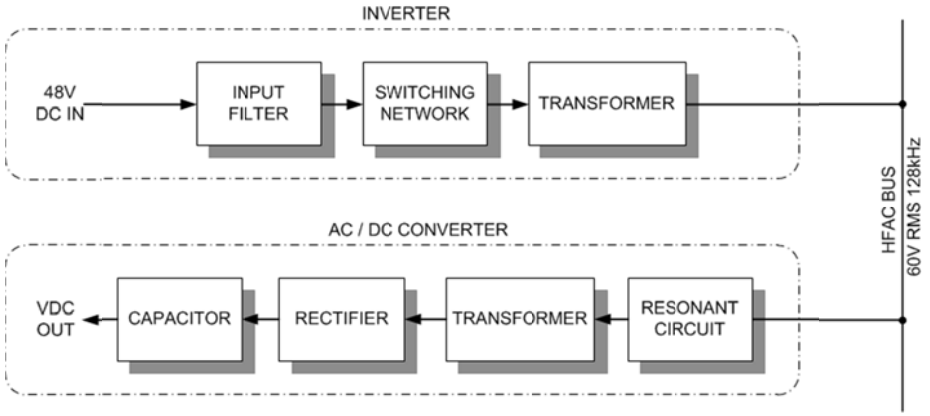


Figure 2.7 : Convertor Block Diagram of HFAC DPS (extracted from [24])

Based on the discussions on the limitations of the DC DPS and the advantages offered by the HFAC DPS, Drobnik argues that HFAC DPS has the potential to increase the reliability and efficiency of the power system without adding unnecessary complexity. He further states that there exists substantial potential for cost and space reduction, thus making it a viable alternative to the current DC DPS in telecommunication systems.

2.4 HFAC in Computing Application

The advances in semiconductor technology have led to dramatic increase in transistor density and clock frequency in modern computer central processing units (CPU). This places great challenges on the power delivery system. Various aspects of HFAC DPS implementation in PC and microcontroller powering application has been considered in literature [3, 28-34]. Drobnik, Huang, Jain and Steigerwald in [29] conducted a survey on the application, challenges and the future direction of PC power distribution systems. The challenges of the personal computer (PC) power delivery system identified by the authors are summarized as follows

1 Low output voltage – Voltage scaling is the commonly used technique to reduce power consumption of CPU. The dynamic power consumption of the CPU is proportional to the transistor gate capacitance, switching speed and the square of the operating voltage. With ever increasing switching frequency and die transistor density, reducing the CPU operating voltage is inevitable to reduce power dissipation.

2 High Output Current – Exponential increase in transistor count in modern CPUs and falling core operating voltages demand high input current

3 High Power Quality – Tight tolerance on the power supply parameters at steady state and transient state.

4 Increase in number of regulated multiple output voltages – PCs require multiple output voltage levels with good regulation (12V, 5V, 3.3V, 2.5V, 1.5V).

5 Fast transient response and high current slew rate – To reduce average power consumption, power management is employed. Systems within the CPU are turned OFF and ON dynamically in the aim to conserve power. To the power delivery system, this translates to dynamically changing load current. It is vital to ensure that the supply voltage is within specified limits when the system load changes from maximum to minimum or vice versa within very short time periods (typically in the region of a few nanoseconds).

In the next section, the existing power distribution system in PCs is briefly explored. The issues faced by existing technologies in meeting the challenges of current and future systems are addressed.

2.4.1 PC Power Architecture

In the past the lowest voltage level used by CPUs were +5V with a modest current requirement of approximately 1A. The voltage regulation requirements were not as stringent as they are on modern systems and were easily achievable. The power delivery architecture for such systems was a simple centralized PSU which generates +5V which is distributed via cables to directly power the CPU

At present, the demands imposed on the CPU power delivery system is very challenging as discussed in the previous section. In current systems, the basic design consist of a power supply unit, which is powered by the mains and generates low voltage DC output typical 12V, 5V and 3.3V which is then distributed. A VRM is then used to reprocess the

output voltage into lower DC voltage required by the CPU core. Figure 2.8 shows typical power delivery architecture of current systems.

One of the disadvantages of this system is the necessity for 3 regulated output voltages, requiring at least 3 DC-AC-DC power processing stage in the front end power converter. This distribution scheme also suffers from higher distribution losses due to distribution of high current at low voltage. Early PC ATX power supply standard had the most of the power delivered via the 3.3V and the 5V line. To reduce distribution losses, specification were amended to allow a higher percentage of the system power to be delivered via the +12V line [35].

Many approaches have been proposed to improve the performance of the current system, including (i) increasing the switching speeds of power converters to improve power density, (ii) using multiple phase interleaved converters, (iii) sophisticated control schemes and (iv) increasing the input voltage to the VRM. Some of these methods did offer incremental performance improvements while others had negative effect on cost and reliability due to the increase in complexity. However an interesting impact on performance was observed by using a higher intermediate voltage (12V) to power the VRM [29]. It was clear that more visible performance improvement could be attained by using even higher intermediate voltage, which led to next powering scheme – High Voltage DC Distribution.

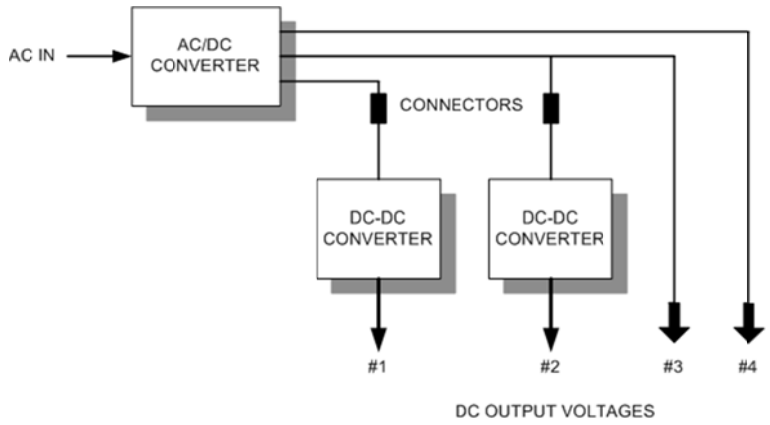


Figure 2.8 : Low voltage DC Distribution System for computer systems (extracted from [29])

In the high voltage DC distribution scheme, the power supply unit generates a single voltage at a much higher level. A simplified block diagram is shown in Figure 2.9. Typically an intermediate voltage of 48V is used. High voltage power distribution has been extensively and successfully used in the telecommunication industry for many years. This scheme is capable of dealing effectively with some of the challenges listed above; however the problem of duplicate power conversion stages and the absence of any provision to effective deal with the high negative di/dt remain. In addition, large voltage step down ratios are required at the point of load converters. High cost is also a concern with this architecture.

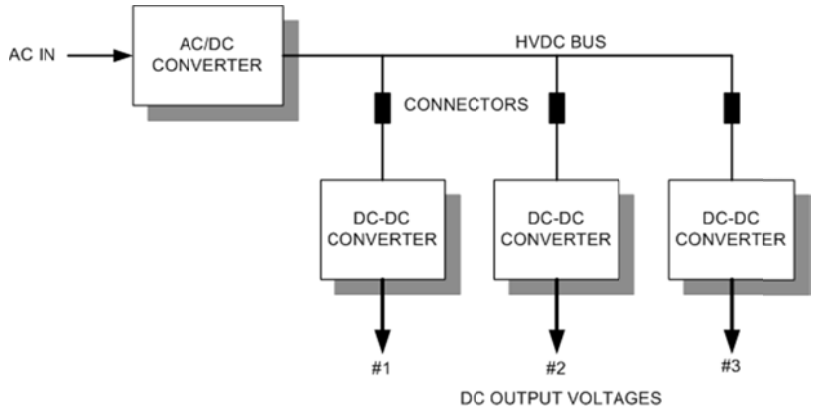


Figure 2.9 : High voltage DC Distribution System for computer systems (extracted from [29])

To overcome most of the problem described above at low cost, HFAC distribution system was proposed. The block diagram of the proposed system is shown in Figure 2.10. The HFAC solution is conceptually the simplest architecture, which deals with most of the power delivery issues, including elimination of duplicate power conversion and active energy steering without additional components, eventually leading to higher overall efficiency.

A prototype high frequency AC distributed power system similar to the architecture shown in Figure 2.10 was reported in [34]. This system was a 48V, 250kHz trapezoid bus voltage rated at 250W. It was reported that the HFAC DPS offered better performance in terms of efficiency, total cost, reliability and flexibility. In [33] and [32] an HFAC inverter and VRM specific for PC application was proposed.

In summary, the authors in [29] and [34] argue that the current multi voltage DC power architecture is inadequate both from an economical and technical considerations. They claim that the single voltage power architecture better meets the requirements of future processors, but HFAC distribution offers the best overall solution and therefore it is the logical step forward to achieve lower cost, higher efficiency and higher reliability than the DC distribution system.

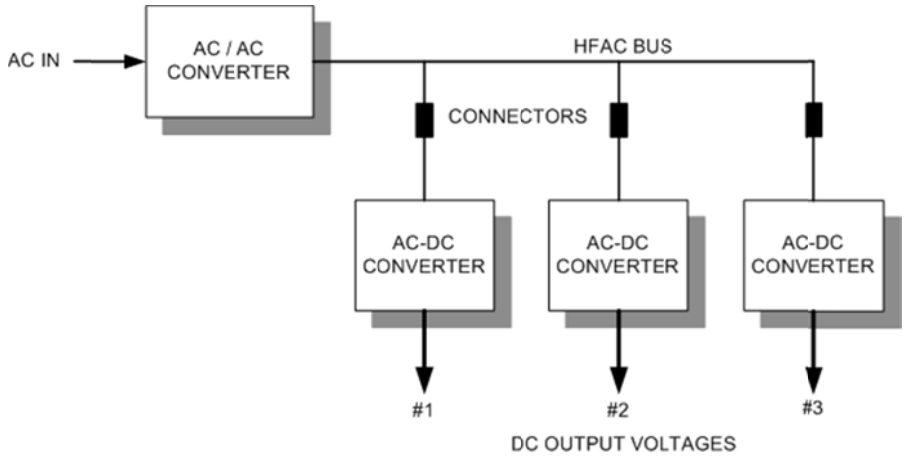


Figure 2.10 : High voltage AC Distribution System for computer systems (extracted from [29])

2.5 HFAC in Aircraft Application

In 1989, Kelly & Owens [36], proposed a HFAC based power distribution system for the inflight entertainment unit in aircrafts. It was suggested that using HFAC, the personalized video entertainment unit could be powered inductively (contactless power transfer) thus eliminating the need for connectors between the seat unit and the cabin floor. The elements of the connector-less power supply consists of a single power track mounted parallel to the seats mounting track in the cabin floor which houses the primary winding. The power pick up unit, consisting of the secondary winding is mounted on the legs of the seat. The power supply unit that locally generated the required power for the entertainment unit is placed under the seat. This configuration of the connector-less power supply allows the circuit to be completely enclosed with no exposed electrical connections.

Ludwig, Weigmen, et al [37], proposed a HFAC based distributed power system for aircraft engine modular control in 1993. This was based on the premise that the present

aircraft engine control systems tend to be highly customized and is usually difficult to expand or modified to be adapted for new engines. They go on to suggest an alternative distributed controller system in which sensed and controlled variables communicate with a central computer via a digital data bus. The sensors and actuators now become modules with sufficient local electronics to perform necessary analog and digital interfacing and to support serial digital communication. In order to realize this modular system, distributed power system architecture was developed to provide power to each smart module in the aircraft engine modular control.

Instead of generating all the required voltages in a centralized power supply, and distributing them via cables to the local control modules, a distributed HFAC architecture was proposed. Local converters in the smart modules will generate the required voltage at the point of use. This helps to reduce overall cable mass and complexity, lower cost and improve voltage regulation. A trapezoid AC bus frequency of 100kHz with 200V peak to peak voltage was proposed for this application.

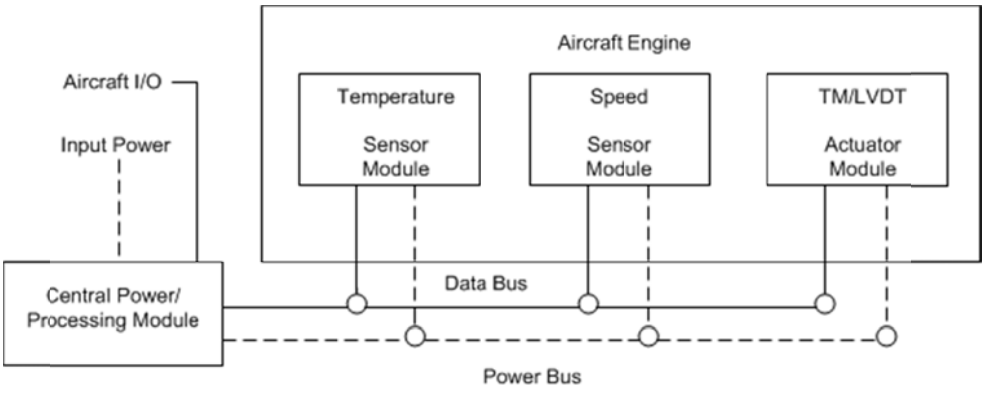


Figure 2.11 : Modular architecture for aircraft engine control (extracted from [37])

2.6 HFAC in Automotive Application

The mention of the potential for HFAC power distribution in automobile application in literature first appeared in a survey paper on electrical vehicles by C.C Chan [38]. In 1994, the Laboratory of Electromagnetic and Electronics System at MIT together with major car manufacturers and suppliers set out to consider the possibility of achieving consensus on the electrical system architecture in luxury vehicles in the 2005 – 2015 timeframe. [39].

As a result of these discussions, it was predicted that the electrical power distribution in a typical luxury automobile in 2005 and beyond would be based on 25 kHz, 48Vrms HFAC system.

The need for a new power distribution system in automobiles is driven by increasing number of electrical loads and the perceived inadequacies of the existing distribution system to cope with demand. The electrical power demand in automobiles have been growing steadily driven by the need for improved safety features, strict regulatory requirements on fuel economy and emission and the increasing number of hotel load for enhanced customer comfort. Figure 2.12 shows the historical and projected average auxiliary (non-propulsion) electrical load in automobiles. Another more recent study [40] has calculated the power demand of a modern vehicle to be approximately 4.7kW. The power demand breakdown by subsystem is given in Table 2.1 Despite this increasing trend, the electrical power architecture in modern vehicles however hasn't changed much from the 12V system proposed in 1950 [41].

To put things in perspective, today's luxury vehicles typically have more than two kilometres of wire in the harness, 2000 terminals and 350 connectors and nearly 1500 different circuits. By contrast, in the mid-fifties, vehicles typically had less than 75 meters of wire, less than 100 terminals and about 30 connectors [42] .

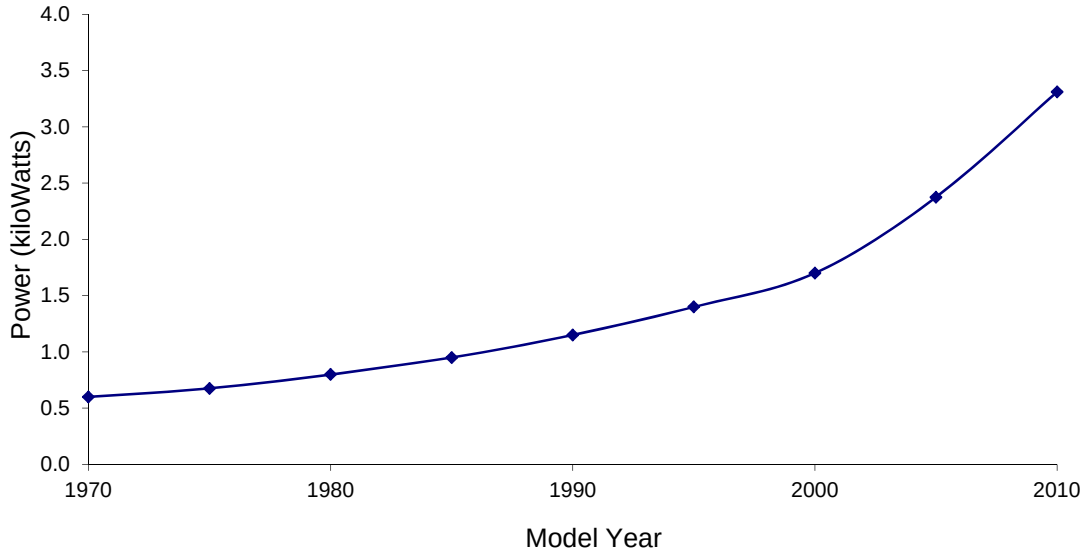


Figure 2.12 : Average automobile auxiliary electrical load(extracted from [42])

Engine Management		Multimedia & HVAC	
Loads	**Power**	**Loads**	**Power**
Fuel Pump & Injectors	135 W	High End Audio System	300 W
Ignition System	60 W	Navigation & GPS	150 W
Electronic Throttle System	60 W	Driver Information Display	30 W
Sensors & Actuators	110 W	Cabin Climate Valves	75 W
Solenoids & Relays	20 W	Blower Motor + ECU	370 W
Sub Total Engine	**385 W**	**Sub Total Cabin System**	**925 W**
Amps @ 14.2 V = 27.11A		Amps @ 14.2 V = 65.14A	
Body Electrical		**Chassis Electrification**	
Loads	**Power**	**Loads**	**Power**
Power Windows (4)	560 W	Electric Assisted Steering	300 W
Power Door Locks (4)	200 W	ABS Braking System	200 W
Wipers & Washers	140 W	Air Suspension Valves	50 W
Heated Backlight	500 W	Air Compressor	500 W
Power Seats (2)	460 W		
Sub Total Body System	**1860 W**	**Sub Total Chassis**	**1050 W**
Amps @ 14.2 V = 130.99A		Amps @ 14.2 V = 73.94A	
Lighting (Exterior & Interior)		**Future Systems**	
Loads	**Power**	**Loads**	**Power**
Headlamps (2)	120 W	DVD & In-Seat Displays	N.A
Running / Park Lights (4)	130 W	Micro/Mild Hybrid Functions	N.A
Turn Signal Lamps	130 W	Active Suspension	N.A
Center High Mounted Stop	65 W	Front / Rear Radar	N.A
Backup / Interior	45 W	Obstacle Detection & Airbags	N.A
		Active Cruise Control	N.A
Sub Total Lighting	**490 W**	**Sub Total Future Systems**	**0 W**
Amps @ 14.2 V = 34.51A		Amps @ 14.2 V = 0A	
Total Power (All Systems)			**4710 W**

Table 2.1 : Power demand of modern automobile subsystem (extracted from [40])

2.6.1 Limitations of Current Power System in Automobiles

The conventional 12V point to point wiring leads to heavy and complex wiring harness. This requires complicated, time consuming and expensive assembly process, and has a negative impact on serviceability. With increasing power demand, high gauge cables are required to mitigate ohmic losses. This negatively impact cost and increases weight. In addition, bulky harnesses and interconnects also place constraint on the vehicle body design as wire routing is difficult in tight cavities. Coupled with the requirement for fuses and the need to place those in easily accessible location, the wiring in modern vehicles can be very complex.

The system voltage (battery voltage) varies over a wide range depending on the state of charge and temperature of the battery. The battery voltage can typically vary from 11V to 15.5V [41]. This requires that all loads be designed to tolerate wide voltage fluctuations and be rated to withstand continuous operation at the maximum voltage and current to ensure reliability. This potentially adds mass and cost to the distribution system and on all loads. Further, all electrical systems in the vehicles are constrained to operate at the battery voltage, (typically 12V) as opposed to being designed to operate in a fashion that allow for maximum efficiency.

2.6.2 Advantages of HFAC in Automotive Application

The block diagram of the HFAC DPS as proposed in [39] is shown in Figure 2.13. In this system, a 25kHz, 48Vrms sinusoidal bus voltage is distributed to power various loads in the system. At point of load, local power converters are used to convert the HFAC bus voltage to the form required by the load. The local power converters ensure tight voltage regulation and high power quality and therefore all loads need not be over-rated to handle wide variations in operating voltage and high transients present in the current system.

The point of load power processing allows the freedom for loads to be designed to operate at voltages optimal for efficient performance of the load without the need to be constrained by battery or the bus voltage. Further motor and actuators used in the system need not be limited to DC brushed motor. Motor selection can be based on suitability

for a particular application and other criteria such as cost, size, weight and efficiency. In [43] it was reported that motors and actuators in general benefit from higher voltage and in HFAC DPS this is a possibility.

Perhaps the most obvious benefit offered by HFAC DPS is reduction in distribution losses. The battery voltage can be boosted up by a power converter to reduce distribution current. In addition to enhancing distribution efficiency, low current distribution results in simpler, smaller, lighter and less expensive distribution harnesses. Any reduction in vehicle mass will translate to improvement in fuel efficiency. In electric vehicles, this could lead to increase in range. Reduced size of wiring harnesses eases constraints on vehicle body design. This is especially important for small vehicles with limited cabin space. HFAC also offers the possibility of non-contact power transfer which potentially can further reduce wiring harness complexity.

The HFAC DPS is inherently modular in nature and can be easily scaled to meet varying power requirements. Therefore a common base design can be used in various vehicle models. This often leads to more cost effective designs that can benefit from economies of scale. HFAC DPS also potentially enjoy higher voltage conversion efficiency compared to competing systems such as 42V DC systems.

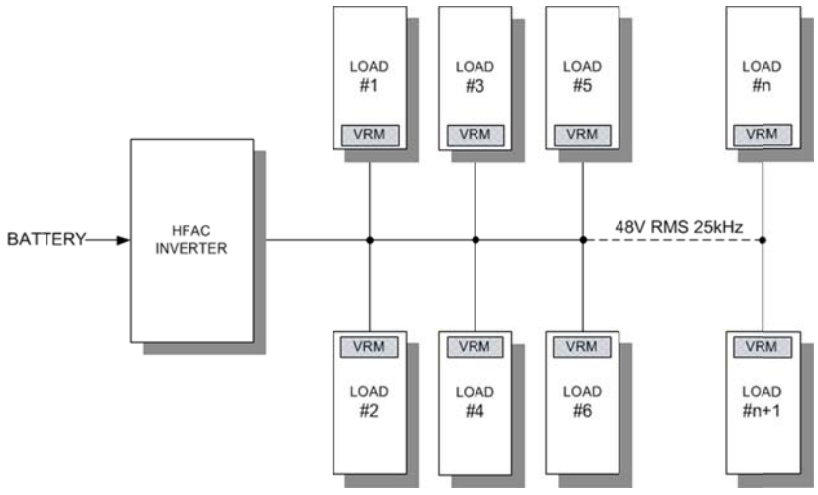


Figure 2.13 : HFAC power distribution architecture for automotive application

Up to this point, the discussion on HFAC DPS in automotive application has been limited to powering auxiliary loads. At this stage, it is perhaps worth noting that HFAC

DPS was also considered for propulsion power applications. In 1996, Bose, Kim & Kankam [44] addressed the viability of HFAC for propulsion power in series hybrid electric vehicle (EV). In their paper, 4 power distribution topologies were investigated (i) DC (ii) resonant link DC, (iii) single phase HFAC and (iv) polyphase HFAC. It was reported that the single phase HFAC system was superior compared to the other schemes. The comparison was based on technical and economic considerations such as performance, cost and weight. In 2004, a 300V 20kHz HFAC DPS was proposed for propulsion power in EV by Xiamin [45].

2.7 Other HFAC Application

With the drive toward integrating renewable energy source in distributed generation systems, HFAC based microgrids have been proposed in [46-49]. Operating frequencies of 400Hz to 20kHz have been reported. It is not uncommon for microgrids to contain a combination of several types of different sources, such as micro wind turbines, solar panels and fuel cells. Each of these sources generates power at different voltage levels and frequencies. Integrating these sources naturally requires some form of power electronic interface equipment. HFAC implementation in this application does not require additional power conversion stages that would not have been otherwise necessary. This provides a lower entry barrier for HFAC based solutions from an economic point of view.

Lighting application has recently expressed interest in HFAC distribution system. In 2010, Andy Ng in his PhD dissertation [50] demonstrated the viability of using constant current HFAC DPS to power distributed fluorescent lighting systems. In [51], HFAC application for LED based lighting system was reported. Commercial application of HFAC for lighting application is beginning to appear in the market. One such solution is Juice J-Drive technology developed by Juice Technology Ltd UK, based on a constant current HFAC system operating at 50kHz.

Commercial implementation of HFAC DPS has also appeared in other electronic systems. For example, the HP70000 series modular measurement system manufactured by Hewlett-Packard is based around a voltage fed HFAC system operating at 40kHz.

2.8 Concluding Remarks

The power distribution architecture for the various applications discussed in the preceding sections appears to follow a similar course of evolution. In most systems, the leap from centralized to distributed power architecture has already occurred. At present, increasing numbers of applications either have or are currently in the process of making transition towards high voltage distribution. Only minorities have embraced HFAC DPS to date, nevertheless this appears to be the next logical step in the evolution of the power architectures. Industry inertia and natural risk aversion to emerging technology have been cited as the impeding forces to the adaptation of HFAC [52]. It is evident that low risk non safety critical application areas will be the potential early adopters of HFAC DPS. This is beginning to show to some degree in certain areas. For example, although the HFAC technology was considered for lighting application relatively recently, commercial exploitation in this domain has begun to occur. It is anticipated that growing interest in emerging application such as EV inductive battery charging technology and distributed generation would lead to renewed interest in HFAC DPS. In summary the potential advantages of HFAC DPS over existing system is evident in a growing number of application areas and future prospect of HFAC remains promising,

CHAPTER 3

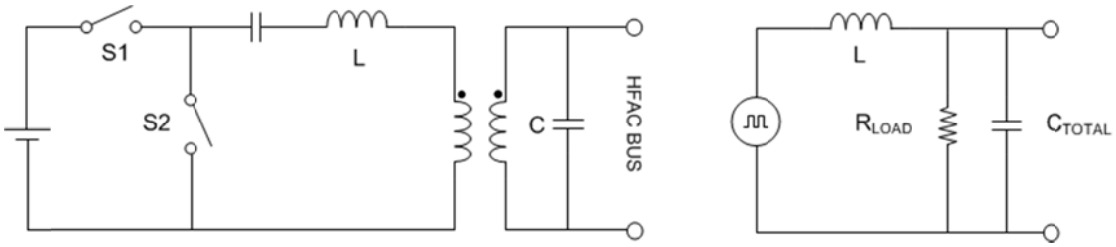
HFAC INVERTER – LITERATURE SURVEY

*"Many precede and many will follow" - **anonymous***

The front end inverter is perhaps the most important component of a HFAC DPS and it has a strong influence on the overall performance of the system. This chapter begins with a critical review of existing HFAC inverters to identify advantages and drawback of various approaches. The key observations are then presented and discussed. The HFAC resonant inverter is divided into three main building blocks, the switching stage, the tank circuit and control loop. Each of these blocks is discussed in detail and a comparative study of available topologies is presented. Based on these discussions, gaps in the literature that presents opportunity for further research is identified. Finally a suitable HFAC inverter is then proposed for automotive HFAC application.

3.1 Review of Existing HFAC Inverter Topologies

The first HFAC inverter to appear in literature was proposed by NASA in [15]. The design is shown in Figure 3.1. This inverter was designed to generate a HFAC bus voltage at a frequency of 20kHz. Switches S1 and S2 are switched at the bus frequency to generate a square wave voltage which is then presented to the LC resonant tank. The circuit can be simplified as in (b) to resemble a parallel resonant inverter. The LC resonant circuit is tuned to the bus frequency and it serves as a low pass filter, allowing a sinusoidal current to flow to the load. The switches 1 and 2 are switched at the current zero crossing point to eliminate switching losses.



(b) HFAC inverter (b) Simplified equivalent circuit

Figure 3.1 : Parallel resonant HFAC inverter (extracted from [15])

In 1988, Jain & Tanju [53] proposed a HFAC inverter to be potentially used for the International Space Station (ISS). The inverter was required to operate at 20kHz sinusoidal output with very high efficiency (> 95%) , tight voltage and frequency regulation and low harmonic distortion (<2.5%). To meet all these requirements while keeping the control simple, the authors proposed a new hybrid doubly tuned resonant stage. The HFAC inverter was based on a full bridge switching stage constructed using mosfet switches with RCD snubber. A 4 element resonant tank consisting of a series and parallel tuned LC branch was used. The circuit diagram of the inverter is shown in Figure 3.2.

The control scheme employed in this design is phase shift modulated voltage mode control. The phase shift in the output of the switching stage is proportional to the voltage error and is used to regulate the bus output voltage magnitude. In this design, it was proposed that both the series and parallel LC branches be tuned to the bus frequency. Besides meeting the stringent requirement described above, perhaps the most interesting feature of this converter is the ability to maintain consistently high efficiency

over a wide variation in load. The major contribution of this work is the proposal of the novel doubly tuned resonant tank circuit, which is the preferred configuration in modern HFAC inverters.

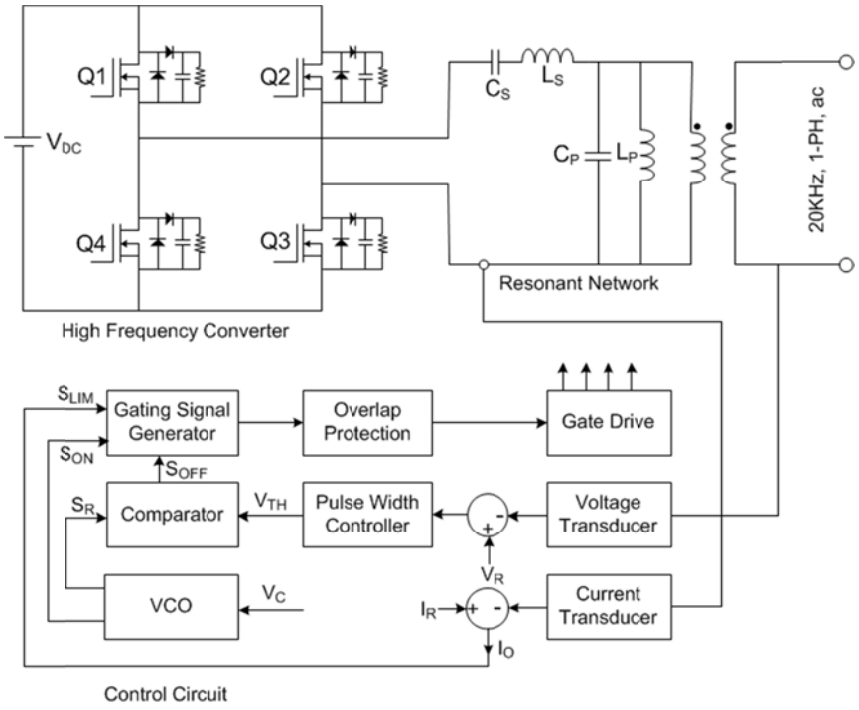


Figure 3.2 : 20kHz Hybrid resonant inverter (extracted from [53])

Ray and Stuart proposed a 2 stage cascaded series resonant HFAC inverter in [13]. The reported inverter consists of a front end series resonant DC-DC converter with variable frequency control. The output of this first stage is a regulated DC voltage which feeds a second series resonant inverter. This second stage operates at a fixed frequency equal to the desired HFAC bus frequency (20kHz). This configuration allows a system with fixed bus frequency with independent regulation of the output amplitude. In [54], a modification to the circuit was proposed to enhance light load efficiency. This was achieved by adding a voltage clamp circuit to the original circuit in Figure 3.3.

As will be shown in later designs, the idea of implementing cascaded converters to decouple the control of the amplitude and phase of the bus voltage has important application in paralleling of HFAC inverters.

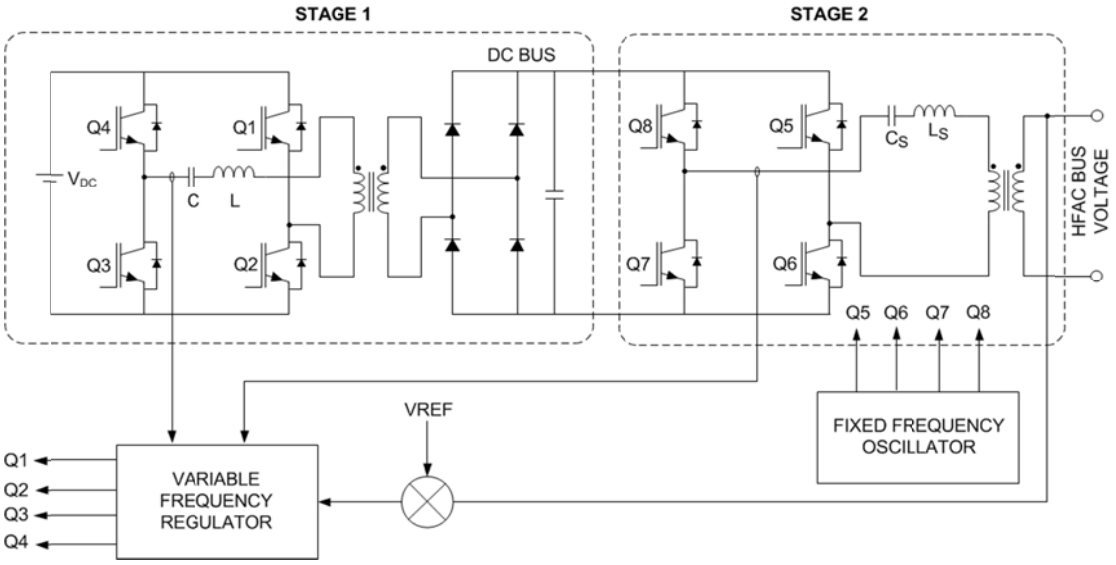


Figure 3.3 : Cascaded Schwarz converter (adapted from [13])

In a NASA supported research, Tsai and Fred Lee in [55], presented a Mapham inverter to generate a 20kHz HFAC voltage at 440Vrms. Figure 3.4 illustrates the circuit configuration of the inverter. In this proposed design, thyristors with antiparallel diode were used as switches. To avoid shoot through, the inverter was switched at a frequency lower than the resonant frequency thus allowing the resonant current to reverse before the thyristor switching transition. It was shown, with proper control, soft switching for both the turn ON and OFF transition can be achieved. The Mapham inverter was also proposed by Jain & Botrill, [56] for space HFAC application. This paper addressed the starting commutation failure of the Mapham inverter under full load condition. An improved inverter with additional starting commutation circuit was presented to alleviate the problem.

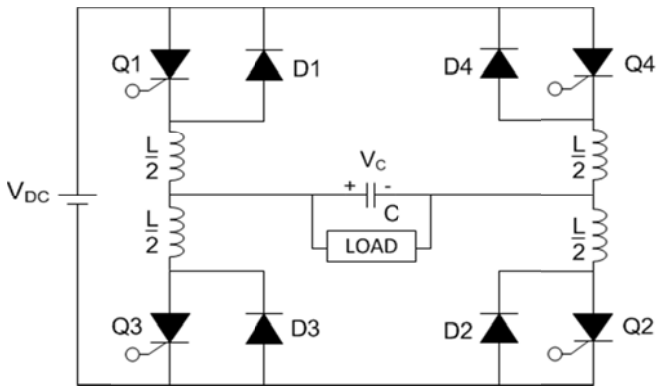


Figure 3.4 : Mapham Inverter (extracted from [55])

In [37], a HFAC inverter operating at 100kHz was proposed for aircraft application. This converter outputs a trapezoid bus voltage. As the input DC voltage had large fluctuation (between 15 to 50Vdc) a front end boost converter was used to generate a regulated 60VDC output. The regulated DC output was then fed to a half bridge AC inverter as shown in Figure 3.5. A transformer is then used to step up the bus voltage to 200V peak to peak. It was claimed that this half bridge AC inverter is zero voltage switched but it is not obvious how this was achieved from the given schematic. It can however be deduced that this is attained by the resonant interaction between the transformer leakage / magnetizing inductance and parasitic capacitance across the switches.

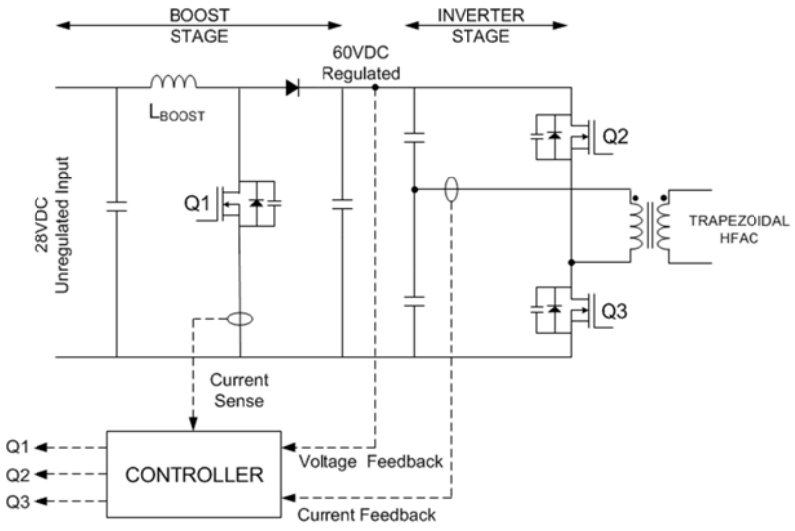


Figure 3.5 : HFAC inverter for aircraft (extracted from [37])

Sabate, Jovanovic et al in 1995 [57], presented an LLC resonant inverter for a 20kHz HFAC distributed power system. They first analysed the performance of the existing series and the parallel resonant inverter that was commonly used. The LLC resonant tank was proposed to combine the benefit offered by both systems. In a series resonant converter (SRC), the transistor current is equal to the load current. As the load is in series with a resonant tank there is no circulating current. The quality factor of the SRC is inversely related to the value of the load resistance. At light load the output current has high THD and as the load become heavier, the THD improves. Therefore in applications where wide variation in load is anticipated, the SRC is not a suitable option.

The parallel resonant converter (PRC) on the other hand can tolerate wide load variation. It can generally be designed to provide output voltage with low THD from no load to

full load. This however is achieved at the expense of increased circulating current. In a PRC, the transistor has to conduct the sum of the load current and the circulating current through the parallel capacitor, thus increasing conduction losses.

The inverter propose in [57] consists of a full bridge switching stage and a LCC resonant tank. The inverter was operated above the resonant frequency with phase shift control. To reduce the circulating current, a new switching sequence was proposed. Under this switching condition, mosfets Q1 and Q3 operates under ZVS and mosfet Q2 and Q4 under ZCS. However fast recovery diodes were required across mosfet Q2 and Q4 as the switching sequence consist of a D2 to Q4 and D4 to Q2 switching transition. During these transitions, the diode reverse recovery becomes a problem thus the need for external fast diodes. However the reduction in conduction losses (due to circulating current) offered by the switching strategy outweighed the increase in the switching losses and total efficiency between 92% (capacitive load) to 96% (inductive load) was reported. The simplified circuit diagram and the switching waveform are shown in Figure 3.6 and Figure 3.7 respectively.

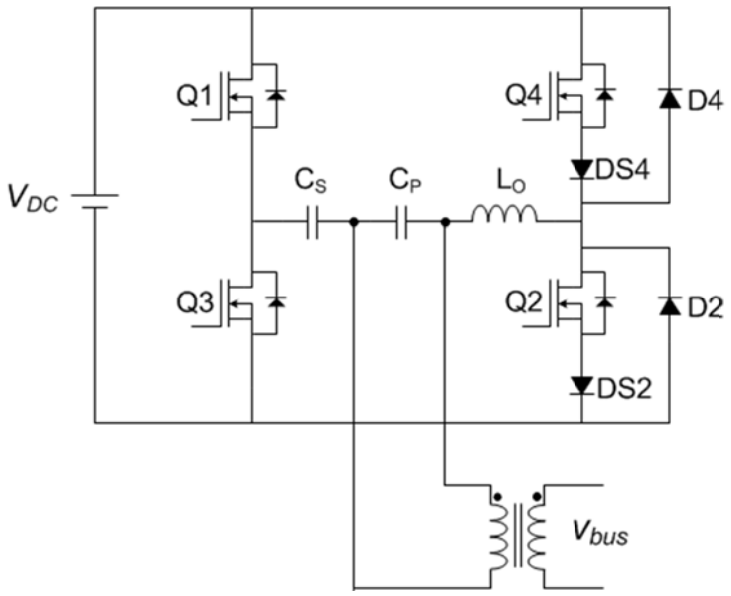


Figure 3.6 : LCC resonant inverter (extracted from [57])

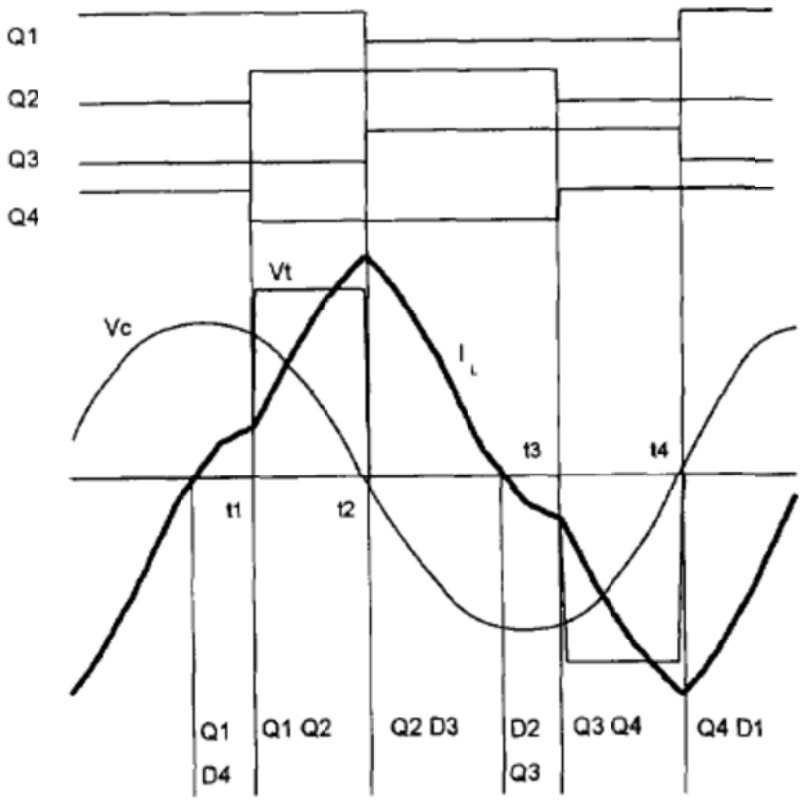


Figure 3.7 : LCC resonant inverter switching waveform (extracted from [57])

In [44] Bose et al investigated the viability of HFAC distribution system for electric vehicle propulsion power. As can be seen from Figure 3.8, the proposed inverter is similar to the doubly tuned resonant inverter proposed in [53]. Phase angle modulation was implemented to control the HFAC bus voltage amplitude. A two phase and three phase HFAC system was also investigated. In the 2 phase design, 2 set of the single phase HFAC converter operating at 90° phase difference was proposed. It was reported that the 2 and 3 phase converters were not economical and inefficient compared to the single phase design mainly due to significant triplen harmonic current in the neutral connection. A qualitative assessment on the optimal selection of the bus frequency and voltage was also addressed. In general, it was reported that higher bus frequency is desired due to the reduction in size of the magnetic and passive filter components. The maximum frequency is however constrained by physical limitation, mainly the switching speed and the dv/dt rating of the switching devices. In addition electromagnetic interference (EMI) could potentially be a problem at high switching frequencies and these effects should be considered when selecting the switching frequency. A higher bus voltage is also generally preferred due to improved distribution efficiency. Further, motor

load operating at higher voltages were reported to be generally more economical and efficient. On the down side, higher bus voltage would require switches that have high voltage withstanding capability. The single phase converter proposed in this paper was also later proposed in [58] again for automotive propulsion application.

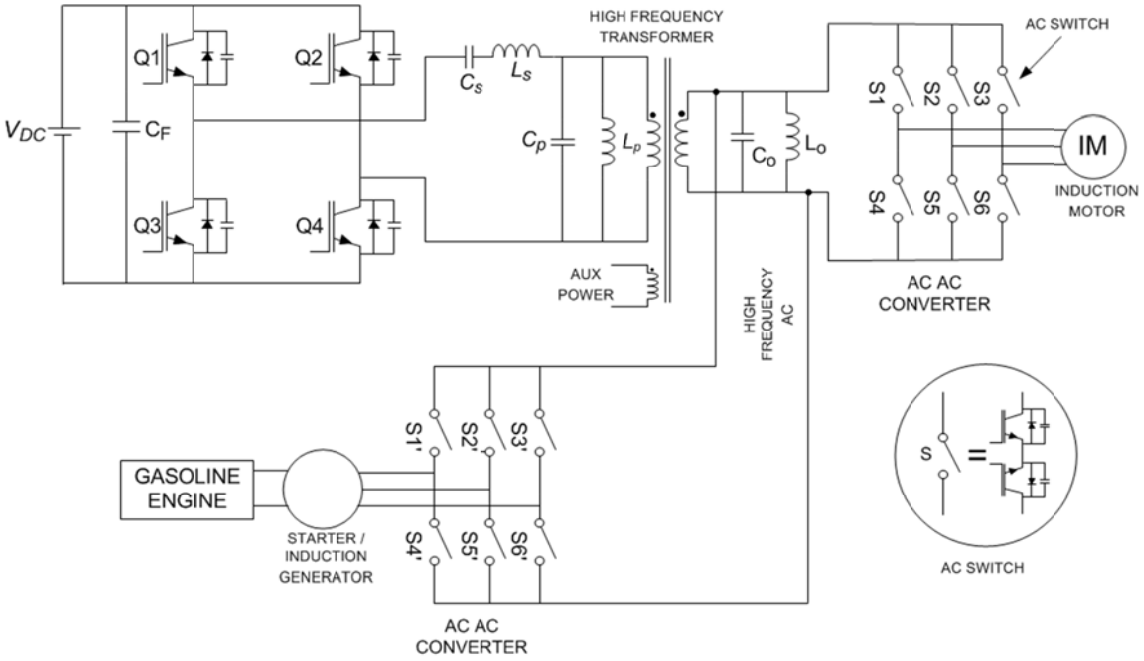


Figure 3.8 : HFAC inverter for automotive propulsion (extracted from [44])

The use of square wave HFAC DPS was suggested previously by Ludwig et al in [37] and by Arduini in [59]. The first paper in literature to decisively advocate square wave HFAC DPS is [28]. It was acknowledged that most of the previous work on HFAC DPS has proposed a sine wave bus waveform. The authors claimed that this was due the selection of the bus waveform being based only on the noise propagation perspective. From this point of view, the sine wave distribution is favourable as the frequency spectrum is free of high frequency harmonics. The propensity for capacitive or inductive noise coupling grows with increasing frequency, making the square wave distribution, with its extensive harmonic composition unattractive.

To alleviate this problem, the authors proposed that the rising and falling time of square wave be increased, effectively approaching a trapezoidal shape. It was reported that increasing the rise and fall time to between 10 – 15% of the switching period sufficiently reduces the high frequency harmonics. The transitions are 'softened' by exploiting the leakage inductance and parasitic capacitance of the switches allowing for a resonant

transition and subsequent achieving ZVS switching. The transition times are load dependent and at very light loads require a gapped core transformer to increase the energy forced to circulate in the leakage inductance.

The authors argue that from the perspective of power converter design, the sinusoidal converters are more complicated and due to the presence of the resonant tank, the converter performance exhibits high load dependent properties. Maintaining THD and efficiency for wide load variation is difficult and require complex closed loop control and point of load converters with good power factor. On the other hand, the absence of the resonant tank in PWM square wave converters, dispense the need for closed loop control if the input is sufficiently regulated. This is possible as the conversion ratio of PWM converters can be made to be independent of loading conditions. The proposed HFAC square wave inverter is shown in Figure 3.9. It can observed that this design is similar to the design proposed in [37] with the exception of the circuitry in the shaded region. This additional circuitry is added to improve holdup requirement (during line voltage drop outs) as the converter is intended to be operated in open loop mode and therefore is unable to regulate the output when the input voltage falls.

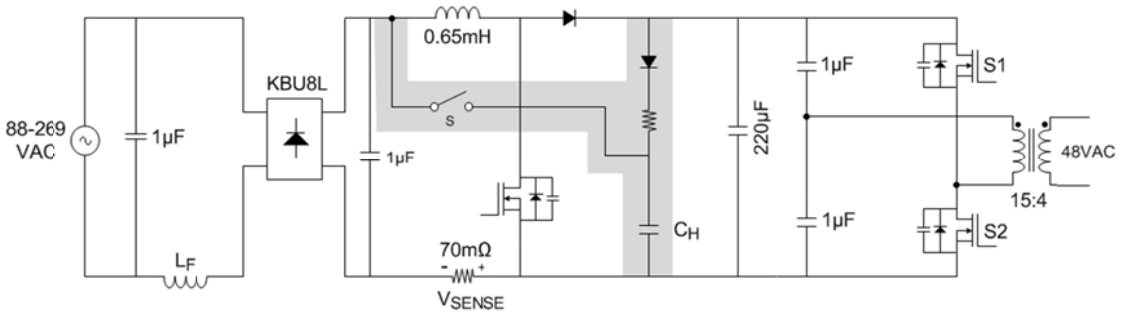


Figure 3.9 : HFAC square wave converter (extracted from [28])

A similar 2 stage converter with a front end DC-DC converter followed by a capacitor split half bridge DC-AC inverter was proposed in [34] and [29]. The design in [29] however had a flyback DC-DC stage instead of a boost converter. The performance of the converter is similar to the one described in [28] in all other respects. Another converter proposed for square wave HFAC DPS is described in [30] & [3]. This converter too has a front end boost DC-DC regulator for power factor correction and to provide a regulated DC output voltage. A second stage 2 switch forward converter was proposed to generate a high frequency square wave bus voltage. The transformer

however has multiple secondary winding configured for different voltage levels. Multiple voltages are distributed as opposed to a single bus voltage as commonly used. To understand the need for multiple bus voltage, it is important to consider the point of load converters in the proposed system. A Magnetic amplifier (mag-amp) based load converter was used in this system and depending on the level of the regulated output voltage selecting a suitable AC voltage enables the mag-amp to operate more efficiently by decreasing the magnetic blocking area. In systems with multiple output requirements, the overall efficiency will be enhanced if multiple AC bus voltage approach is used

In 1999, Jain et al proposed a doubly tuned series parallel full bridge resonant inverter with phase shift control to be used as a front end sine wave HFAC inverter for telecommunication application [14]. This inverter is similar to the one proposed before by Jain for space application in [53]. This inverter was again preferred due to the high efficiency performance from full to reduce load and load independent nature of the output voltage. A similar converter was also proposed to power hybrid fiber / coax multimedia service systems (cable TV with telephony service) in [26].

After almost 2 decades since HFAC first appeared in literature, Luo, Batarseh, et al in year 2000 conducted a study to assess the current state of the HFAC DPS technology and to identify the major technical issues. In this paper a simplification to the 2 stage converter as proposed in [28] was presented. The basic idea was to combine the boost front end stage with the back end DC-AC stage into a single stage converter as shown in Figure 3.10. This simplification does however come with some compromises. Firstly the wider capacitor voltage range in the single stage design require component with larger rating. Additionally there will be regulation performance penalty and this converter is generally limited to low power levels.

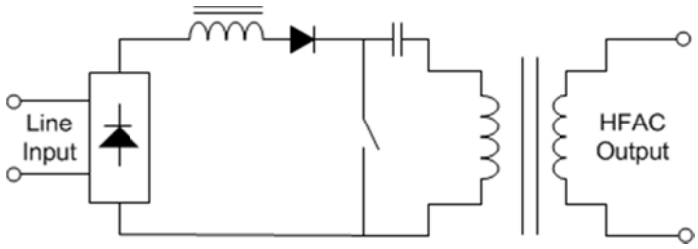


Figure 3.10 : Single state HFAC inverter (extracted from [2])

Guo & Jain in [60] and [61], proposed a full bridge series parallel HFAC inverter for telecom and computing application. As the converter was designed to be powered by the mains supply, a front end power factor correction and dc bus regulation stage was required. This was achieved using a boost converter in the front end. The authors decided to use the 2 stage approach as opposed to integrating the PFC stage into the resonant inverter. The single stage design leads to high DC bus voltage at low loading condition thus exceeding the requirement of commercially available capacitors. This similar concern was also reported in [2].

In this work, the authors proposed a simple unified control for both stages. Phase shift control was implemented for the DC-AC resonant inverter stage. The gate drive for the boost mosfet was derived from the bridge gate drive signal using combination logic and a monostable multivibrator circuit. In essence the gate drive for the boost is generated whenever the opposite pairs (Q1 & Q3) or (Q2 & Q4) of the inverter is driven. However a pulse skipping mechanism was implemented to skip some of the gate drive pulse to limit the DC bus voltage. In this design, whilst the boost mosfet is hard switched, all the inverter mosfets are soft switched. To achieve ZVS it is imperative that the inverter be switched higher than the resonant frequency of the tank circuit. This inverter enjoys the same benefit as other doubly tuned resonant inverter reported previously. The proposed converter is shown in Figure 3.11

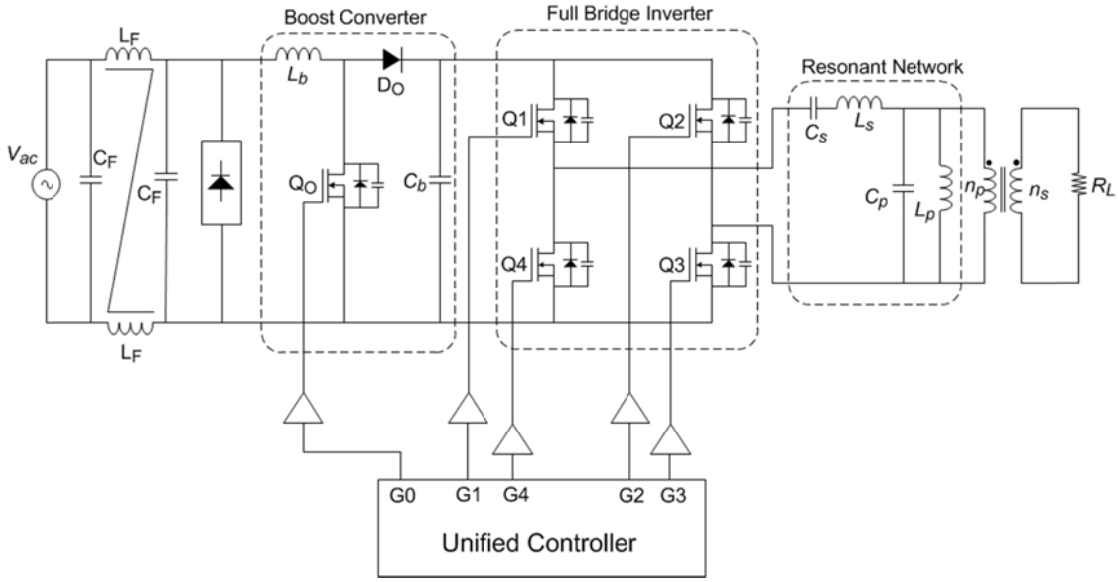


Figure 3.11 : HFAC inverter with PFC (extracted from [60])

In a later publication, Guo & Jain [62] & [63] proposed some improvement to their earlier work [60] & [61] to further reduce the DC bus voltage under worst case operating condition. This was achieved by replacing the front end boost converter with a buck boost converter. A set of design curve were generated and these were used to select optimal values for key design parameter and to understand the resulting trade-off between the competing requirements. A prototype converter operating at bus voltage of 30Vac and 100kHz rated at 250W was built and tested. Total overall efficiency of more than 85%, with maximum DC bus voltage of less than 400V was reported.

Qui, Jain et al in 2002 [64], proposed an asymmetrical PWM controlled resonant inverter. The switching stage consisted of a half bridge mosfet arrangement followed by a series parallel resonant network (Figure 3.12). This design is a simple single stage design operated with DC input. By controlling the duty cycle of the mosfet, a varying square wave is presented to the resonant tank. As the duty cycle is not symmetrical, (for D not equal 0.5) even harmonics will be present at the output of the switching stage. Therefore the resonant tank includes a 2^{nd} harmonic trap consisting of L2 & C2 to improve the THD of the output voltage.

The simplicity of the design, lends itself to some drawbacks. The phase angle and the amplitude of the output voltage cannot be controlled independently; therefore this converter is not suitable for parallel operation. As in most resonant inverters, the THD, soft switching range and efficiency exhibits load and control input dependant behaviour. However the authors have shown that with careful design the inverter can be made to operate with high efficiency and low THD for a wide range of loading, input voltage and control input. This converter has fast transient response due to the feed forward and feedback based control system, as shown in Figure 3.13 making it particularly suitable for computer application.

The proposed converter was later used as a front end DC-AC HFAC converter to study the system level performance of the HFAC distribution system in [65] & [66]. Even at the system level, with multiple point of load converters and varying loading condition, it was reported that the inverter exhibited excellent performance as discussed in [64].

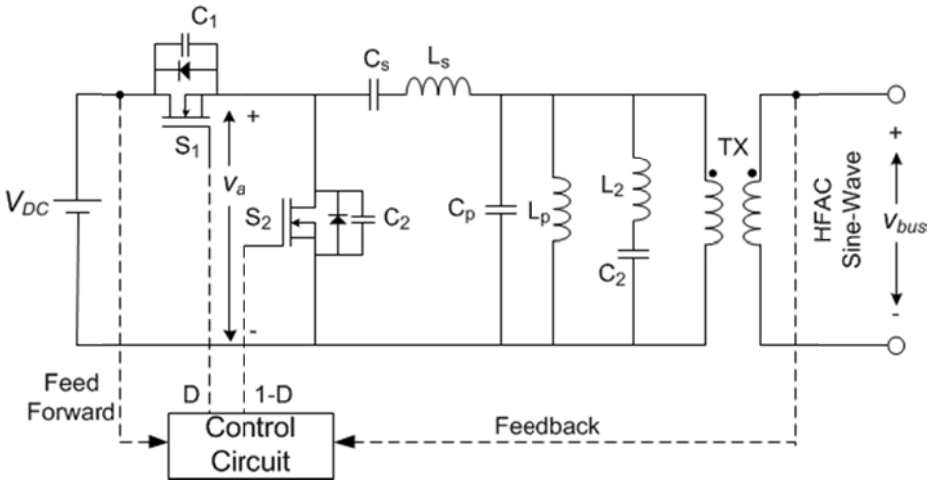


Figure 3.12 : Asymmetrical PWM resonant inverter (extracted from [64])

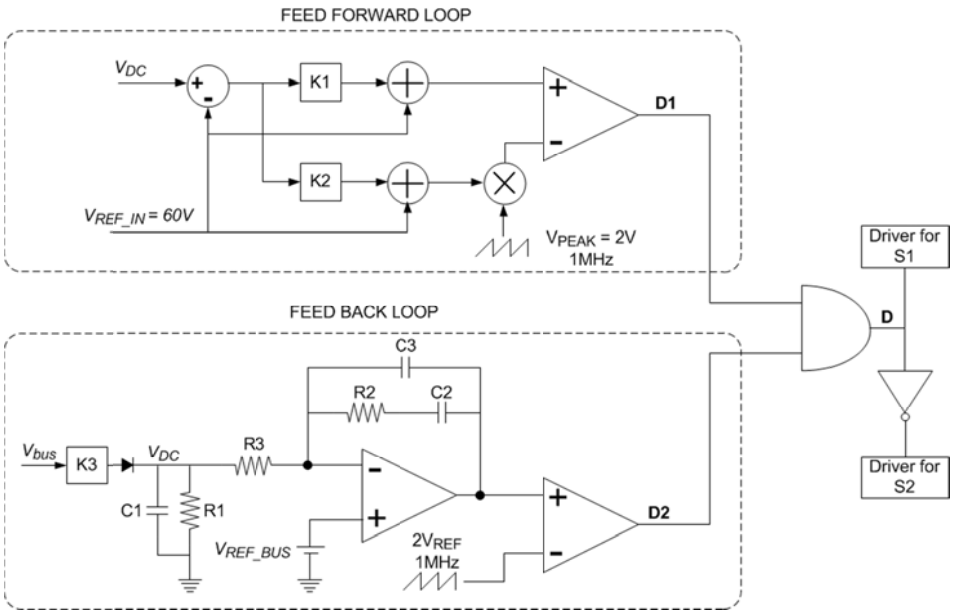


Figure 3.13 : Feedback & feedfoward control (extracted from [64])

The converter was again proposed in [32] by the same authors with a modified control system. The new control system shown in Figure 3.14, uses modulated integral control as a feedfoward loop to provide pre regulation for the feedback loop. The feedback loop is based on a type II error amplifier and is essentially similar to the initial design. A thorough discussion on the design of the control loop is given in [67]. A combination of the feedfoward and feedback provides excellent transient response and completely removes steady state error. It was reported that the output voltage reaches the steady state value within 3 to 5 cycle during a step change in load from 50% to 100% and vice versa. Excellent rejection to input voltage fluctuation was also reported.

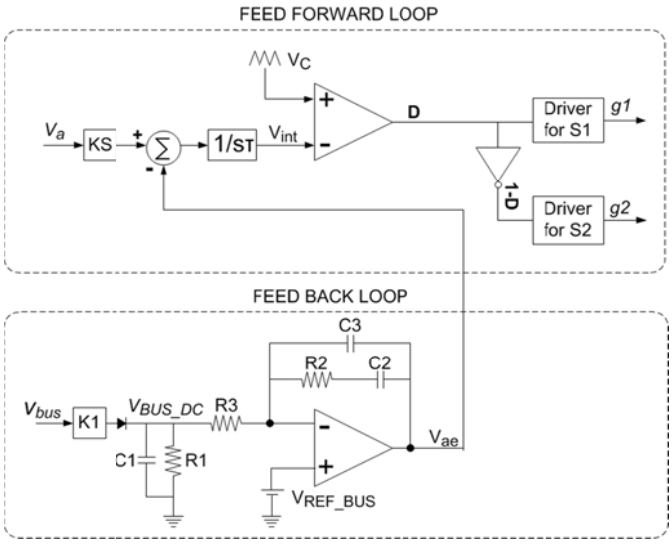


Figure 3.14 : Improved control system (extracted from [32])

To date, all literature on HFAC has proposed constant bus frequency, although the ideal bus waveform shape has been disputed, no record exist on the proposal for the continuously varying bus frequency. The first work to propose such a system is [68]. The authors argued that HFAC inverter being based on resonant topology suffer from load sensitivity problems. Changes in the load alter the effective RLC values in the tank circuit and this leads to changes in the resonant frequency, THD and soft switching range. A full bridge series resonant inverter switching at variable frequency was proposed as a potential solution to mitigate the discussed drawback in regular resonant inverters (Figure 3.15). The switching frequency is kept lower than the tank resonant frequency. Under this condition, the tank circuit presents an effective capacitive load to the full bridge switching stage and therefore ZCS switching can be achieved. The switching frequency is controlled in a manner such that amplitude of the resonant current is maintained close to a desired reference value. However this work does not address the implications of the varying bus frequency on noise propagation and EMI.

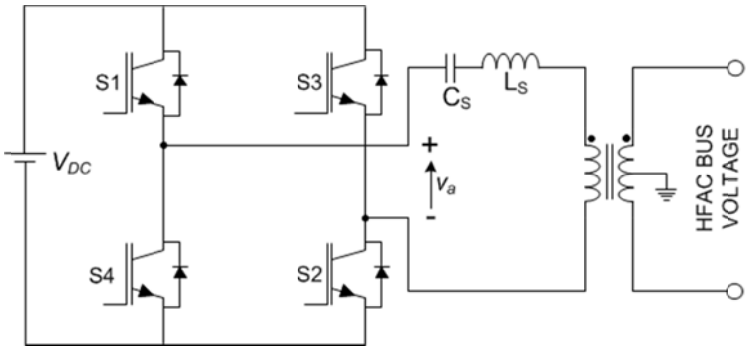


Figure 3.15 : Varying frequency resonant inverter (extracted from [68])

Peretz and Ben-Yaakov in [69] proposed a self-adjusting current fed push pull resonant inverter to generate a sinusoidal HFAC output voltage. This circuit configuration is popularly used in electronic ballast for fluorescent lighting. The proposed circuit is shown in Figure 3.16. When the push pull stage is switched at the resonant frequency, the inverter operates under ZVS condition. In steady state, the output voltage is independent of loading and is only dependent on the input DC voltage and transformer turns ratio. The mosfet gate drive voltage is generated by a soft switching control circuit (SSC) that switches the mosfets every time the center tap voltage crosses zero. This ensures that the switching frequency always equals the tank resonant circuit. The resonant tank frequency however is load dependent. In order to ensure fixed frequency operation, the tank inductor is varied. This is accomplished by using a variable inductor configuration as proposed in [70]. The inductance is controlled by varying the bias current in the auxiliary coil based on the difference between the tank frequency and the desired reference bus frequency.

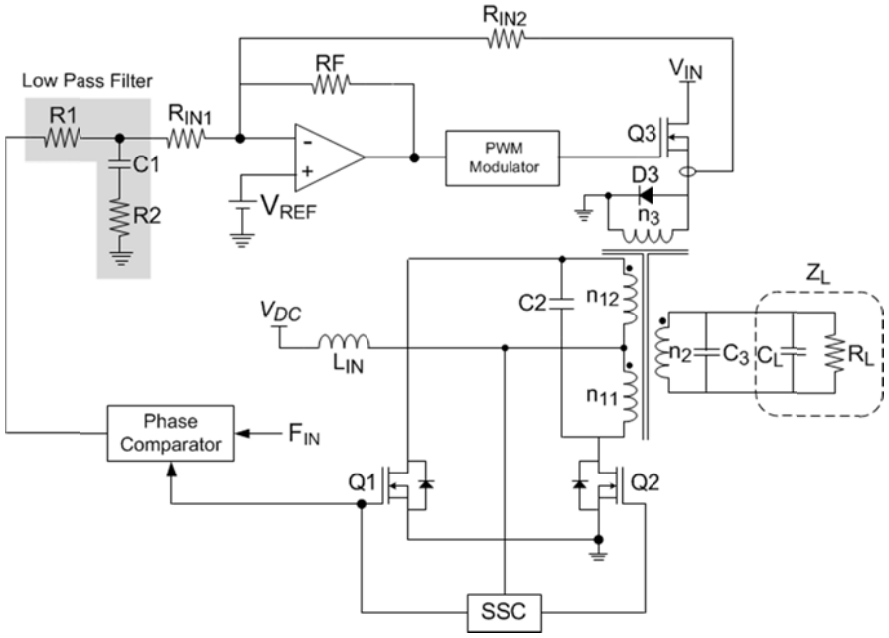


Figure 3.16 : Self adjusting CFPPRI (extracted from [69])

In [71-73], a cascaded 2 stage resonant inverter was proposed. The main aim of the converter was to decouple the control of the amplitude and the phase angle of the output. This allows the converters to be paralleled and thus multiple front end inverters can be used in a HFAC system to increase the power capacity. This is achieved by adding a standard buck converter between the DC input voltage and the resonant inverter (Figure 3.17). In [72] & [73], a zero voltage quasi resonant buck converter was proposed to achieve soft switching in the first stage. Although topologically similar to a standard buck converter, a smaller inductor is used, allowing the inductor current to go negative for a portion of the switching cycle. The presence of the front end DC-DC converter effectively allows the input voltage to the resonant stage to be controlled and consequently the amplitude of the output voltage can be controlled. The second stage resonant inverter is similar to the inverter proposed in [32]. At steady state, the second stage will be operated at fixed frequency equal to the bus frequency and at 50% duty cycle. However when the bus frequency is out of phase with the reference phase, the frequency of the PWM will be changed proportional to the phase error until the error is eliminate. Therefore during this transient period, the bus frequency will vary. A PI controller was proposed in this paper to generate the PWM control signal based on the phase error. The second harmonic trap in the resonant tank is not necessary as the input voltage to the tank only contains odd harmonics due to symmetric duty cycle. The design requires 2 controllers. An outer loop voltage mode control (VMC) was implemented to

regulate the amplitude and an inner phase angle control loop to synchronize the output phase to the reference bus waveform.

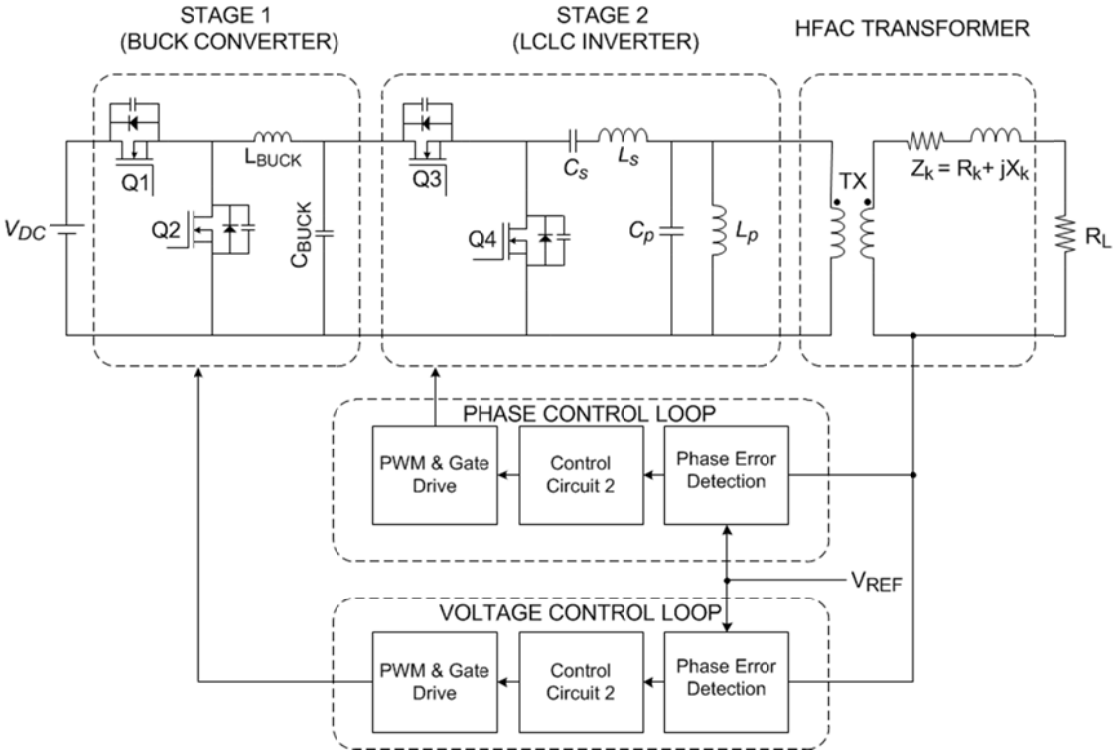


Figure 3.17 : Cascaded 2 stage resonant inverter (extracted from [71])

A full bridge resonant inverter with a series parallel resonant tank with phase shift modulation was investigated in [74]. The proposed circuit is shown in Figure 3.18. To achieve ZVS switching during turn on, the resonant tank was tuned to be inductive at the resonant frequency. Soft turn off was achieved using lossless snubber capacitor across the mosfet. The drawback of regular phase shift control was addressed in this paper and a modified version of PSM was later proposed. The main problem with conventional PSM when applied to the proposed converter is the dependence of the phase angle of the bus voltage on the VMC input. The typical waveform and control circuit of conventional PSM is shown in Figure 3.19. To mitigate this problem, a novel modified symmetrical phase shift was proposed. As can be seen from Figure 3.20, the new circuit is very similar to the conventional PSM control circuitry with the exception of 4 additional AND gate and 1 NOT gate. One other difference is the modified version requires a symmetrical triangular carrier signal as opposed to a ramp carrier for the conventional circuit. Figure 3.21 shows the comparison between the new proposed

scheme and conventional PSM for 2 different control effort. It is evident that the proposed solution enables output voltage of different amplitudes to remain synchronized.

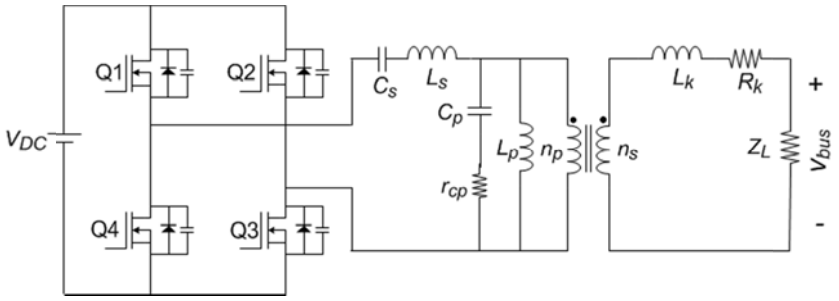


Figure 3.18 : Full bridge series parallel resonant inverter (extracted from [74])

With the new scheme, the phase of the output voltage is independent of the voltage control and it remains at a fixed phase offset from the clock signal. Therefore using a common clock signal, it is possible to synchronize multiple converters and thus this converter is suitable for multiple input, multiple output (MIMO) configuration. However the small variation in the phase angle that may exist due to the tolerance in the values of the components in the tank circuit is not compensated by the proposed control scheme.

In later papers [75, 76], using the same converter and control scheme proposed in [74], the authors focused on the design of the resonant tank and the resulting tradeoffs. A set of performance curves were provided in the paper, to aid the design of an optimal converter. In [77], the feasibility of the full bridge resonant inverter with modified PSM for multiple paralleled inverter configuration with weighted current sharing was demonstrated.

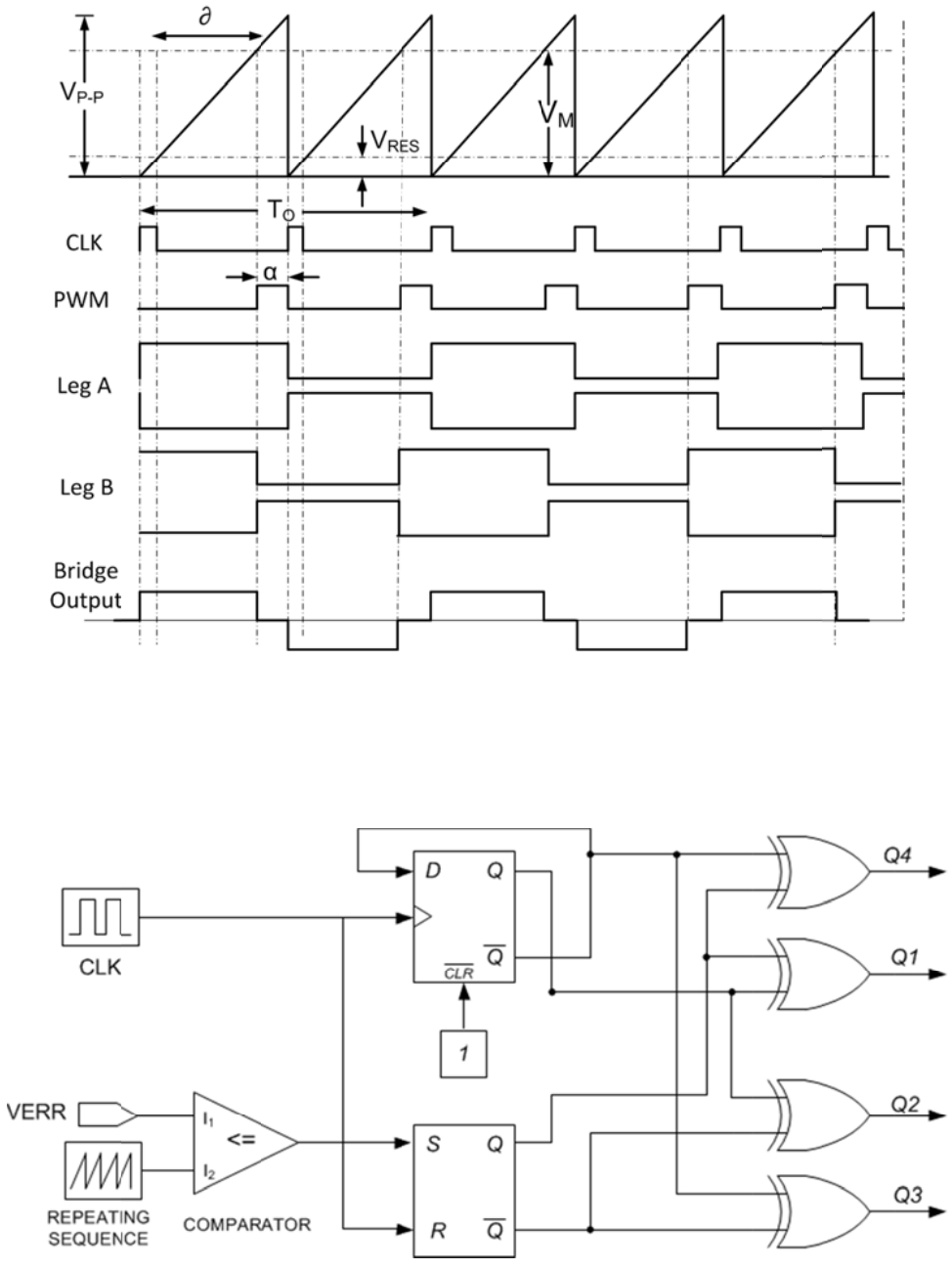


Figure 3.19 : Phase shift modulation waveform & circuitry (extracted from [74])

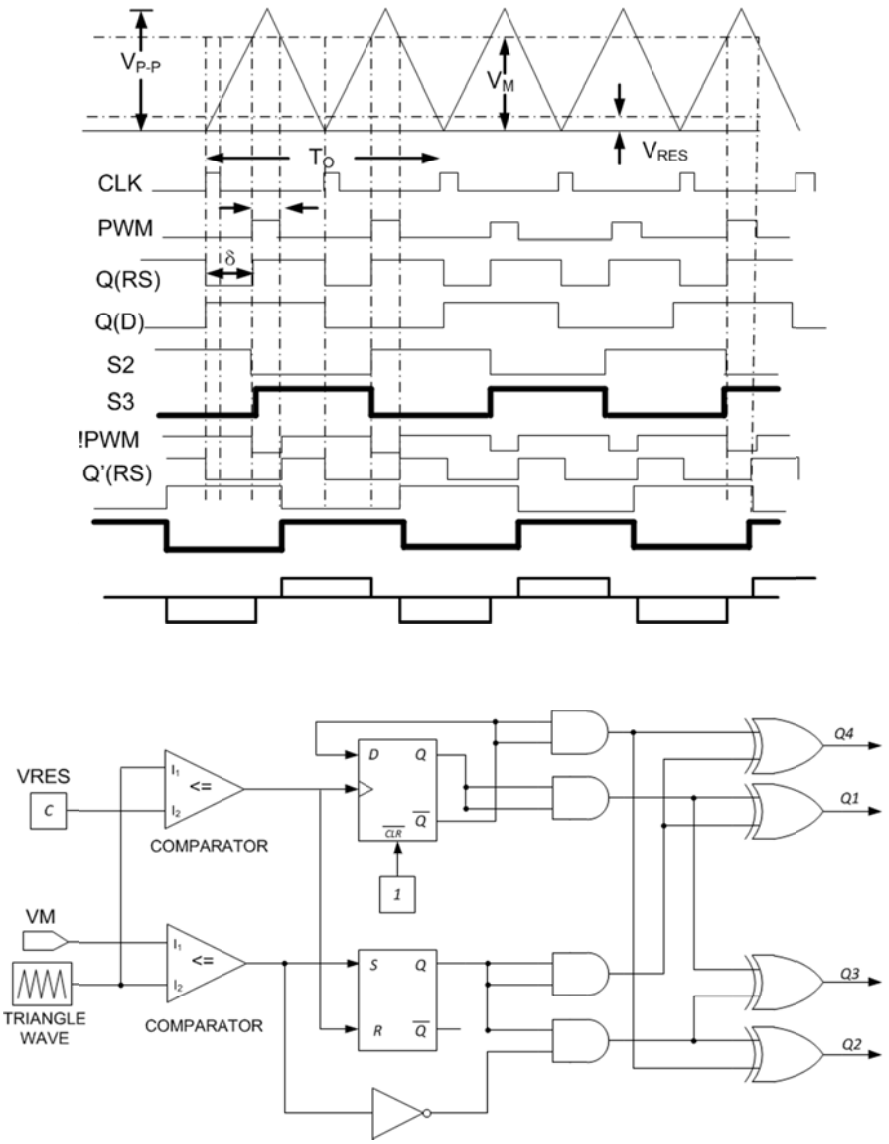


Figure 3.20 : Modified phase shift modulation waveform & circuitry (extracted from [74])

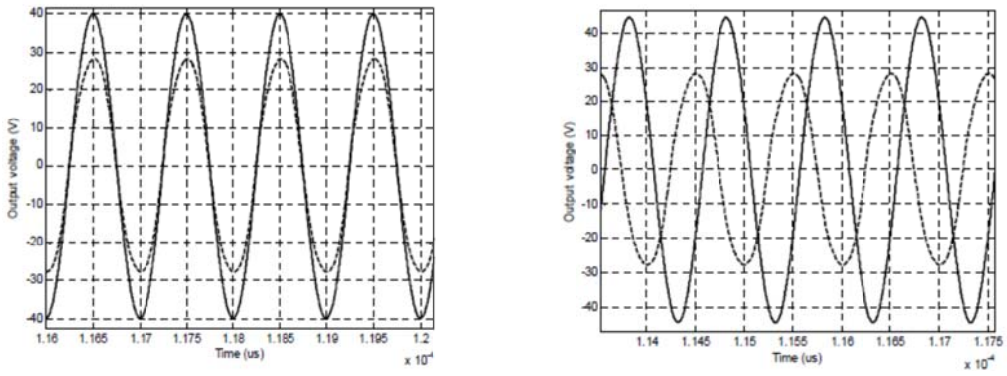
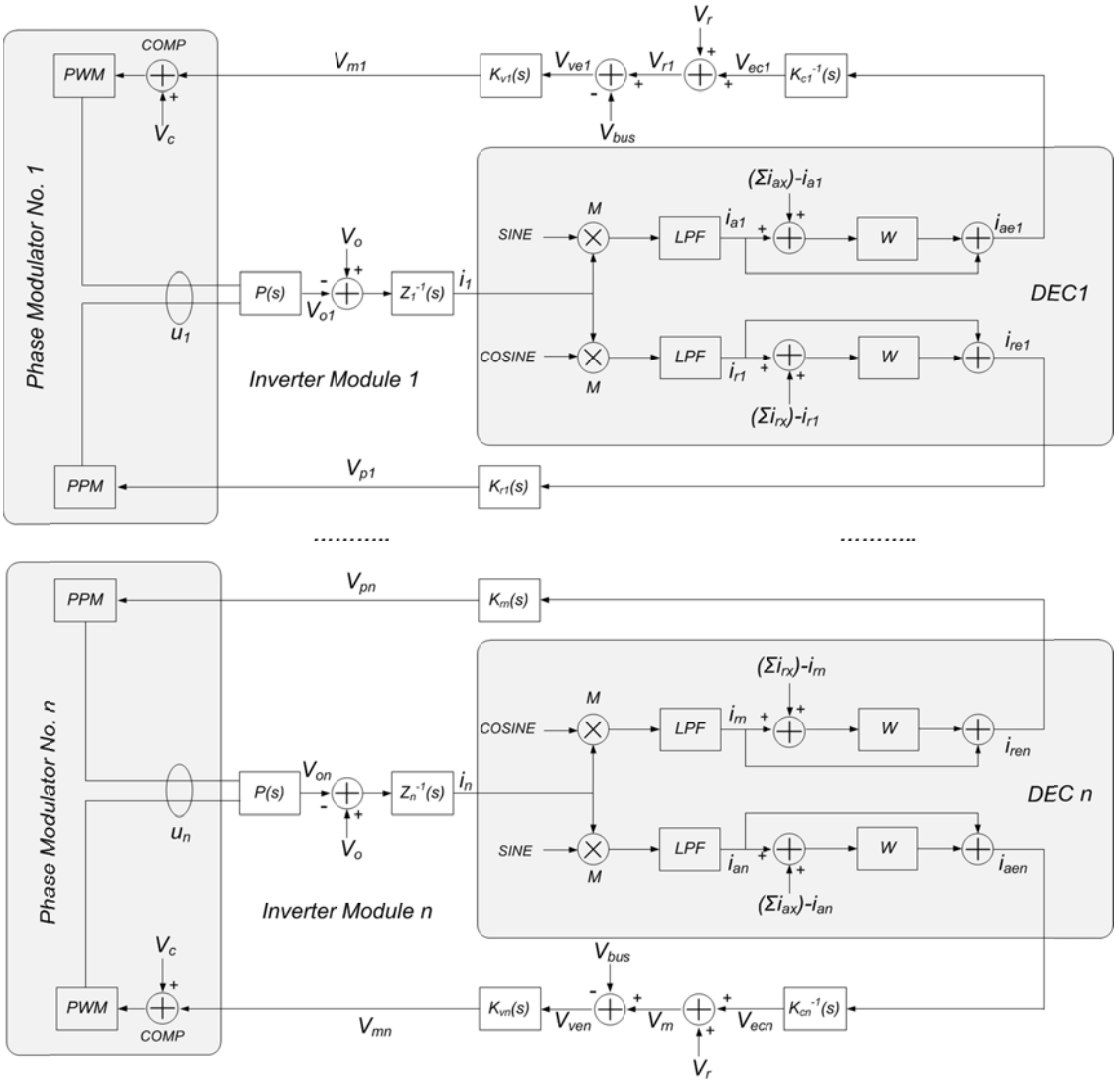


Figure 3.21 : Comparison between modified and conventional PSM (extracted from [74])

A 2 stage converter was proposed in [78-80], which has a similar power stage topology as the converter proposed previously in [71]. In this work however a novel control scheme based on current phasor decomposition technique was proposed. In a system with multiple parallel converters, it is vital that the load current is equally shared by all converters in the system. Current imbalance could cause uneven and excessive loading of some converters and cause circulating current between the converters in the system. The main idea of the proposed control scheme is based on the sensing of the output current of the power converter and decomposing it into the 'in phase' (active current) and quadrature component (reactive current) using Fourier analysis. It was shown that for effective load sharing and to reduce circulating current, the control objective is to keep the active current of all the inverters in the system to be equal and at the same time keeping the reactive component as small as possible.

This is equal to reducing the phasor error of the output current in each inverter in the system. The active current information together with the bus voltage feedback signal is used to regulate the magnitude of the bus voltage by controlling the front end buck converter. The reactive current is used to control the phase of the bus voltage via a pulse phase modulator (PPM). The proposed method was reported to be very effective in reducing the circulating current in multiple inverter systems. Maximum circulating current of less than 5% of load current was measured in an experimental prototype of 2 inverters in parallel with phasor control.

Comparatively, the same experiment setup was used to measure the percentage of circulation current under the following conditions, (i) without magnitude or phase, (ii) only magnitude control and (iii) only phase control. The measured circulating current for the 3 conditions are 25%, 11% and 12.5% respectively. This remarkable improvement in performance comes at the expense of very complex control system. Besides, the control system requires the average active and reactive current inputs of all the other inverters in the system and this can be challenging if the inverters are spatially distributed. The control structure of the current phasor control is shown in Figure 3.22.



$K_{V(x)}$	Voltage Controller of Module x
$K_{R(x)}$	Reactive Current Controller of Module x
$K_{C(x)}$	Active Current Controller of Module x
Z_X	Connection Impedance of Module x
P(s)	Small Signal Model of Inverter Module x
PPM	Pulse Phase Modulator
DEC	Current Decomposition Algorithm
OFG	Orthogonal Frame Generator
LPF	Low Pass Filter
W	Weighting Function

V_C	Carrier Signal
V_M	PWM Modulation Signal
V_P	PPM Modulation Signal
V_{bus}	Output Bus Voltage
$i_{(x)}$	Current of Module x
$i_{(rx)}$	Reactive Current of Module x
$i_{(ax)}$	Active Current of Module x
$i_{(aex)}$	Active Current Error of Module x
$i_{(rex)}$	Reactive Current Error of Module x
u_x	Pulse Modulation Signal of Module x

Figure 3.22 : Phasor control block diagram (extracted from [80])

In [81, 82], an inverter topology previously proposed in [74], (see Figure 3.18) was presented with a new control scheme. One cycle control (OCC) with phase shift modulation was proposed for this design. The controller block diagram is shown in Figure 3.23. Some structural similarity can be observed between this controller and the

controller in Figure 3.14. The OCC block (F_{OCC}) is fundamentally an integrator circuit that computes equation (3.1), where v_k is the output signal of the voltage controller $K_v(s)$, and $|v_b(t)|$ is the rectified bridge voltage. The PSM block (F_{PSM}) implementation is shown in Figure 3.19. In this paper, H_∞ robust control design techniques were used to design the voltage controller $K_v(s)$ to ensure stability under large uncertainties in resonant tank component tolerance, input voltage and load variation.

$$v_m(t) = \frac{1}{T_{occ}} \int_0^t (v_k(\tau) - |v_b(\tau)|) d\tau \tag{3.1}$$

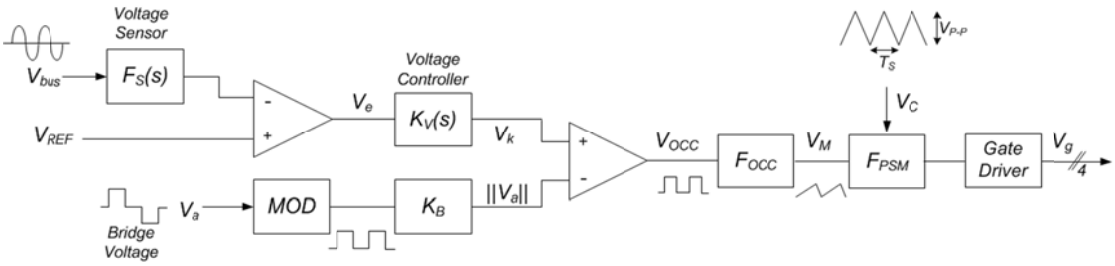


Figure 3.23 : OCC with PSM controller block diagram (extracted from [81])

A half bridge resonant inverter with pulse phase modulation was presented in [83-86]. The design and the proposed control system are shown in Figure 3.24. Pulse phase modulation allows the phase of the output voltage to be controlled. This design is in fact similar to the second stage inverter proposed in [71], (see Figure 3.17). The phase error was derived by multiplying the reference sine wave signal with the bus voltage waveform and filtering the resulting high frequency term (twice the bus frequency). A PI phase controller was designed to provide the phase modulation signal for the PPM module. The PPM timing waveform and circuitry is illustrated in Figure 3.25. As the phase modulation signal changes, the phase shift signal changes proportionally. During this transient duration, the frequency of the gate drive changes corresponding to the change in phase shift angle. This ensures the phase angle of the output voltage is adjusted to match the reference phase angle during the following cycle.

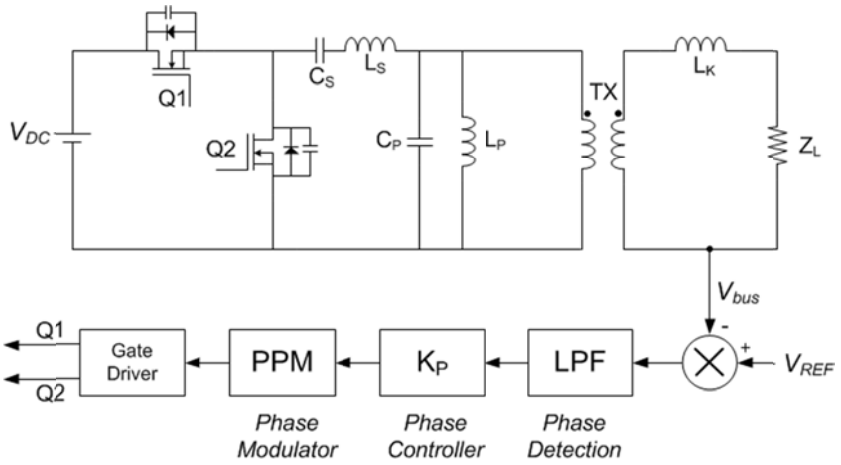


Figure 3.24 : Half bridge inverter with PPM (extracted from [83])

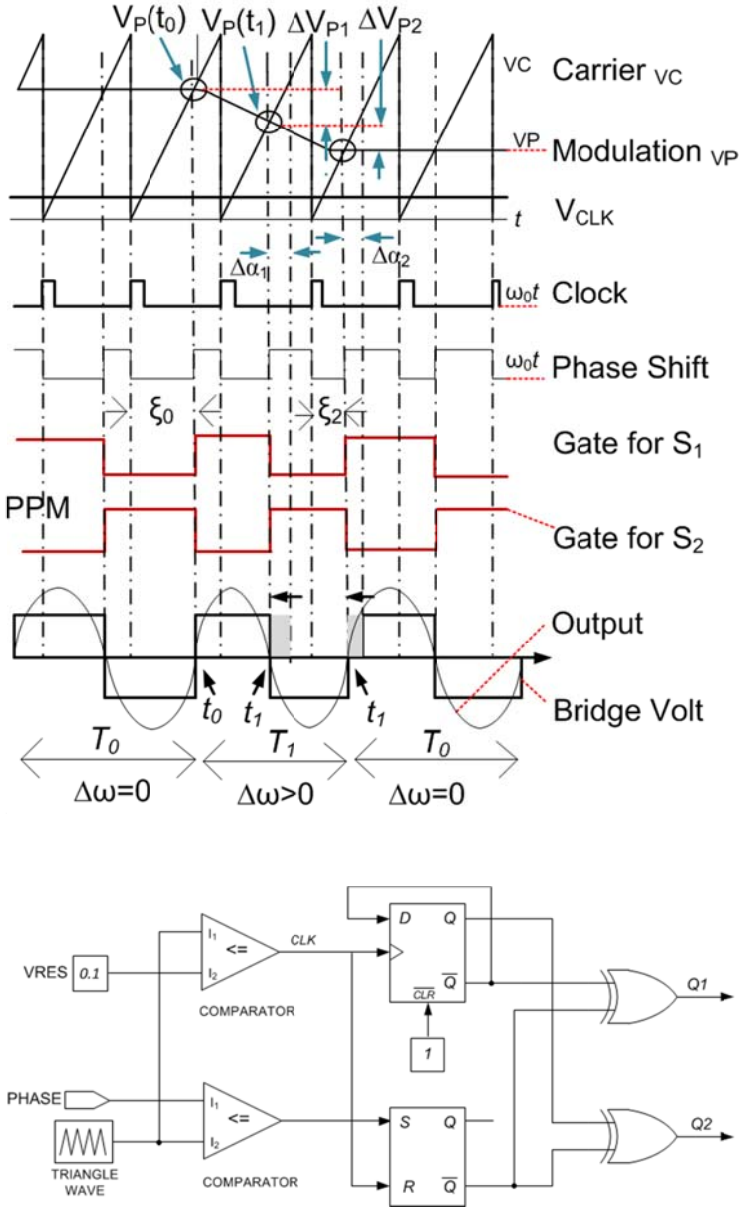


Figure 3.25 : PPM waveform & circuitry (extracted from [83])

3.2 Observations & Summary

As discussed in the previous section, the research in HFAC has spanned for more than 3 decades and there are numerous HFAC inverter topologies proposed in literature. In this section the system level concerns such as the selection of the HFAC bus voltage frequency and waveform are critically addressed. Then the proposed inverters in literature are classified in logical groups and a comparative study of the main building blocks of the inverter is attempted.

3.2.1 Bus Waveform

Two difference approaches are reported in literature, sinusoidal and square/trapezoidal bus waveform. The main argument for the selection of the sinusoidal bus is reduced noise propagation and EMI due to the absence of high frequency harmonics. Proponents of square wave bus [28, 37, 59], have argued that sine wave HFAC inverters are generally more complex and exhibit load dependent properties. Further the square wave approach benefits from the vast amount of research reported in literature and existing mature designs [1]. In principal, DC-DC converters are combination of high frequency square wave switching stage followed by a rectifier. Therefore the various switching stage of the existing DC-DC converters can be used as square wave HFAC inverter.

However in square wave converters, in order to achieve soft switching, resonant transition techniques are often employed. Whilst this can be achieved by relying on parasitic inductances and capacitance without the need for additional component, the transition times are load dependent properties. It is possible that under certain loading condition, soft switching ability may be lost.

Another drawback of square wave HFAC bus waveform not often addressed in literature is increased distribution losses. It can be shown that for a fixed load power and resistance, the distribution losses of a the square wave HFAC bus due to skin effect can be as high as 36% greater than that of a comparable sinusoidal bus distribution. (Refer appendix A). Therefore square wave HFAC bus waveform is particularly not suitable for system where long distribution distances are required.

Modern HFAC inverters in literature almost exclusively propose sinusoidal bus waveform and are reported to have high efficiency over a wide load range. In [77] it was demonstrated that in systems with multiple parallel inverter with weighted current sharing, high efficiency can be achieved from full load down to 10% or less. It is anticipated that the sinusoidal HFAC bus waveform will remain the preferred choice for the foreseeable future.

3.2.2 Operating Frequency & Voltage

The selection of optimal HFAC bus voltage and frequency is application specific. In general a single fixed voltage and frequency is the preferred solution. Variable frequency bus has been proposed in [68], but in most application the poor noise performance and EMI problems caused by continuously varying frequency is not acceptable. The selection of the bus voltage is often driven by the need to increase distribution efficiencies. Therefore there is a tendency to select the highest possible voltage as far as other considerations such as regulatory & safety compliance, insulation requirements and voltage stresses in power converters allow.

The bus frequency is selected with the aim to improve the power density of the power processing structures in the system. Increasing the frequency reduces the size of capacitors, inductors and transformer used in the HFAC DPS and therefore more compact power converters are possible. On the other hand, switching losses and skin effect increase with frequency and have detrimental efficiency consequences. In addition higher frequency increases the propensity for capacitive noise coupling. Determining the ideal bus voltage and frequency is a complex multi objective optimization problem depending on many factor such as distribution distances, total power handling requirement, number of power converters in the system and load duty cycle. The HFAC bus voltage and frequency for various application reported in literature is graphically illustrated in Figure 3.26.

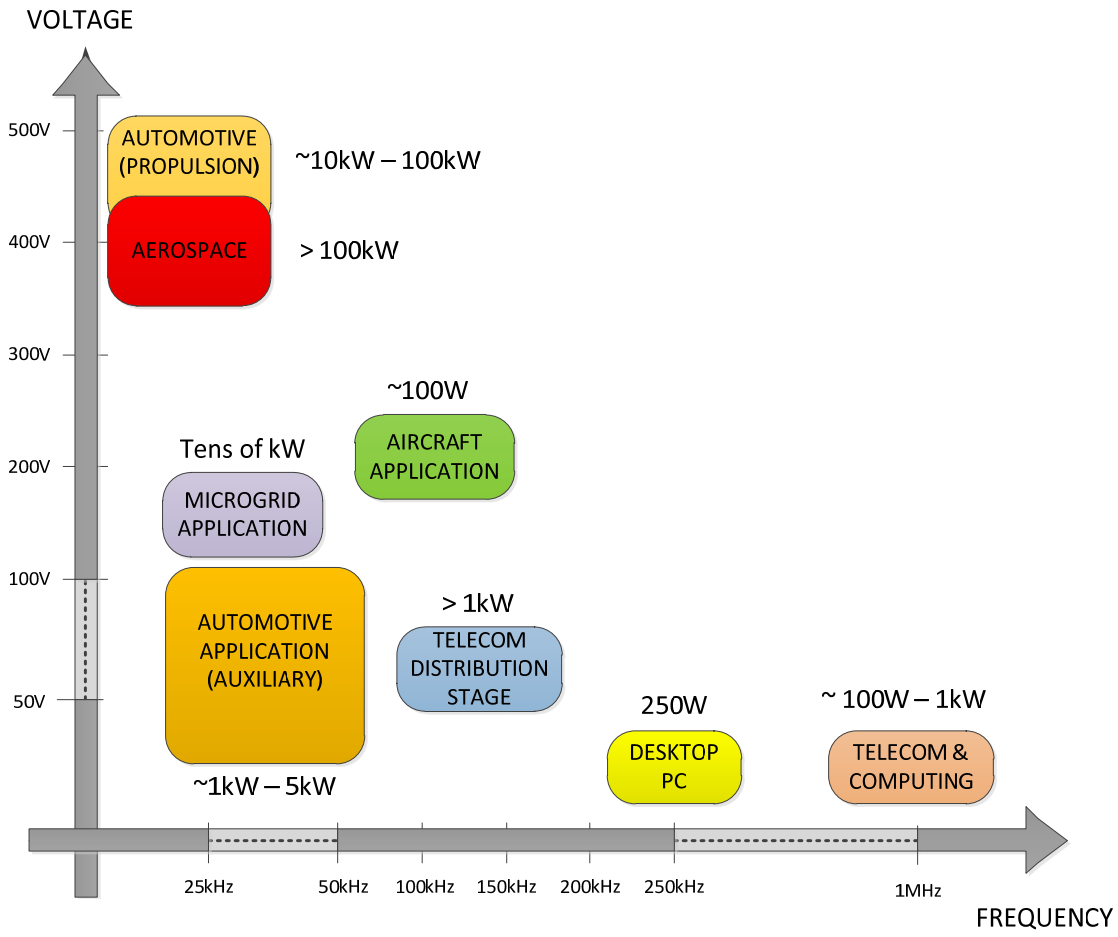


Figure 3.26 : HFAC bus voltage & frequency for various applications

3.2.3 Single & Multi Stage Inverters

HFAC inverters can generally be classified into two groups (i) single stage inverters (SSI) and (ii) multi stage inverter (MSI). A generic block diagram for both the SSI and MSI is shown in Figure 3.27. In this case, it is assumed that the inverters are fed with a DC input voltage and the HFAC output voltage is sinusoidal. If the input is AC mains voltage, then a preceding PFC stage will be required. For the case of a square wave HFAC bus, the resonant tank block shown in Figure 3.27 will not be necessary.

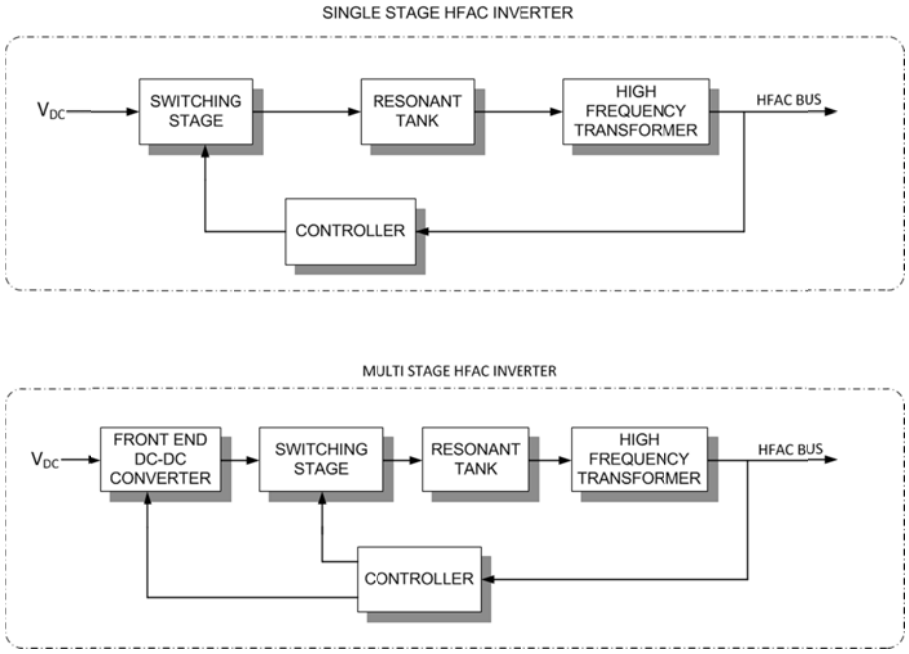


Figure 3.27 : Block diagram of HFAC inverter

Single stage HFAC inverters generally consist of a switching stage followed by a resonant network. The main appeal of the SSI is in its simple topology and control requirements. This however comes at the expense of coupled control of magnitude and the phase angle of the HFAC bus voltage. This is a problem in systems with multiple inverters operating in parallel where synchronization of both voltage magnitude and phase angle is required. An exception to this rule is the full bridge inverter with modified phase shift control. This SSI is capable of independent control of both magnitude and phase angle. However in this design, the ability of all the switches to achieve ZVS is a function of the effective pulse width (δ) of the PSM. It is therefore possible that for certain control input, ZVS ability may be lost leading to high switching losses. In general, all SSI inverters have more restricted ZVS requirements in terms of tolerance to input voltage and load variations.

Multi stage inverters (MSI) consists of a SSI HFAC inverter proceeded by another power converter, normally a DC-DC converter. The main purpose of the first stage converter is to regulate the DC input voltage to the second stage HFAC inverter and thus allowing direct control of the amplitude of the output voltage. The phase angle of the output can be independently controlled by the second stage. In mains powered inverters, the front end PFC converter can be can exploited to additionally serve the function of a pre regulator to the HFAC inverter. However in such design, some restriction in the range of control exists. In a truly independent MSI, the front end DC-DC converter solely serves

the purpose to regulate amplitude of the output voltage, and the second stage is operated at fixed frequency at 50% duty cycle. The phase of the output is dependent only on the phase of the PWM signal of the inverter and the resonant tank elements. Therefore by controlling the phase of the PWM signal in the second stage the phase of the output can be regulated. MSI offer more relaxed constrains for soft switching of the inverter switches and therefore can tolerate a wider variation in input voltage and load.

Further the design of the second stage inverter in MSI is not constrained by the available input voltage. As will be shown later, the efficiency of the resonant inverter is strongly related to the input voltage. Therefore the front end DC-DC converter can be selected such that the second stage inverter is operated at the most optimal voltage for best overall efficiency.

The fully decoupled control of the phase and magnitude of the output voltage make the MSI suitable for parallel operation. Whilst it could be argued, that the addition of another power conversion stage will have efficiency penalties, it is important to consider the efficiency gained due to the reduction in circulating current between multiple inverters which can be very significant.

3.2.4 Tank Circuit

Four types of resonant tank configuration have been proposed in literature for a sinusoidal HFAC inverter. The series resonant circuit [13, 68], parallel resonant circuit [15, 55, 56], LCC resonant circuit [57] and series parallel resonant circuit [44, 53, 58, 60-63, 71-86]. In generally the desired properties of the tank circuit are (i) inductive input impedance for wide range of loading condition. (ii) tank input current proportional to load current, (iii) reduced circulating current & (iv) output voltage with low THD for wide range of load.

The resonant tank current in a series resonant circuit is equal to the load current as no circulating current is present. As the switching devices conduct the tank input current, the losses are therefore proportional to the load current. The harmonic distortion of the tank output voltage is inversely related to the load; at light load the THD is poor. At no

load condition, the terminal voltage is simply equal to the voltage of switching stage and no control on the output is possible even with frequency control

The output voltage of the parallel resonant tank when operated above the resonant frequency is less sensitive to load variation as compared to the series resonant inverter. This however is achieved at the expense of increased circulating current in the tank circuit, especially at light load. Therefore the tank current is not proportional to the load current; at light load the input current can be higher than the load current and thus leads to poor efficiency. Another desirable feature of the parallel resonant tank is the inherently short circuit protection due to the impedance of the resonant inductor. The resonant tank is not normally operated at the resonant frequency as the output voltage is load dependant and under no load condition, the output voltage can be prohibitively high.

The LCC and the series parallel resonant tanks (LCLC) combines the benefits of both the series and parallel resonant tank with the LCLC resonant tank offering better performance over the LCC tank. The LCLC resonant tank can be designed to operate over a wide load range with reduced circulating current. Under this condition, the proportionality of the tank and load current characteristics of the series resonant tank is inherited and thus high efficiency can be attained. The series parallel resonant inverter exhibits load independent output voltage when operated at or near the tank resonant frequency.

The series parallel resonant tank offers the best balance between controllability, efficiency and load insensitivity and therefore is the preferred resonant tank configuration in almost all modern HFAC inverters. In Appendix B, PSPICE frequency response simulation of the all the 4 type resonant tank is presented.

3.2.5 Switching Network

Fundamentally all HFAC inverters consist of a switching stage followed by a resonant tank. There are 3 common switching configurations, the full bridge, half bridge and capacitor split half bridge as shown in Figure 3.28.

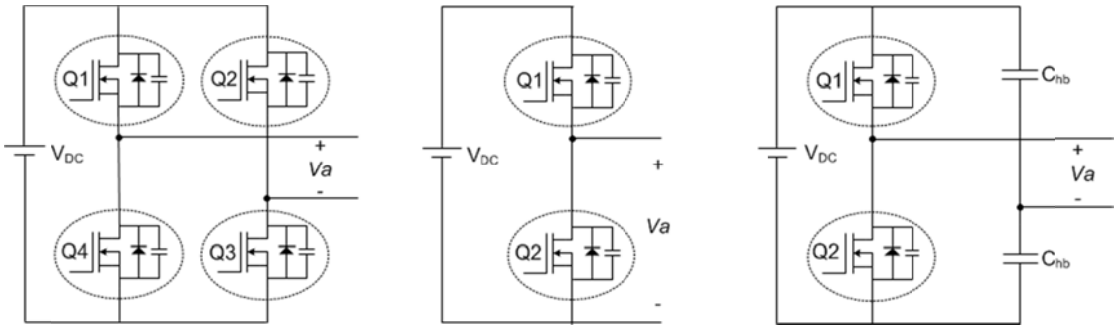


Figure 3.28 : HFAC inverter switching network

The full bridge inverter has high power handling capability and therefore is the preferred choice for high power application. The switches are subjected to the input voltage and the output voltage swing extends from $+V_{DC}$ to $-V_{DC}$. Therefore compared to both the half bridge version, the full bridge configuration requires only half the current to deliver the same load power. Consequently, the conduction losses are lower and the efficiency is generally higher than the half bridge versions. The full bridge switching network is normally phase shift modulated and therefore generates symmetrical switching waveforms which consist only of odd harmonics.

The half bridge switching stage also called the DC chopper is normally used in lower power application. This is the simplest configuration, requiring only 2 switches and therefore is the lowest cost solution of the three switching configuration. The switches should be rated to handle the full input voltage. The half bridge switching stage is normally pulse width modulated, generating a unipolar output voltage with a swing of 0 to +Vin. As the switching waveform has a DC component, a series capacitor is required to avoid saturation of the HFAC transformer. This series capacitor may be present in the form of the resonant network.

The split capacitor half bridge has similar characteristics as the DC chopper but the output voltage is bipolar with a voltage swing of $+ V_{DC}/2$ to $- V_{DC}/2$. Therefore the voltage stress on the switches is similar to that of the full bridge. If the switches are switched at 50% duty cycle, no DC offset is present in the output. The half bridge split capacitor switching stage is often used in the square / trapezoidal wave HFAC inverter.

As can be seen from the literature review of existing inverters presented in section 3.1, various types of semiconductor power switches have been used in the design of the switching stage. In some early design, thyristors and bipolar junction transistors (BJT) were used but most newer designs utilize IGBTs or mosfets with the latter being more popular. The choice of switching devices is application specific, depending on the switch voltage and current stresses and the switching frequency. Figure 3.29 shows the map of power semiconductor device capability and can be used to aid the selection of a suitable switch.

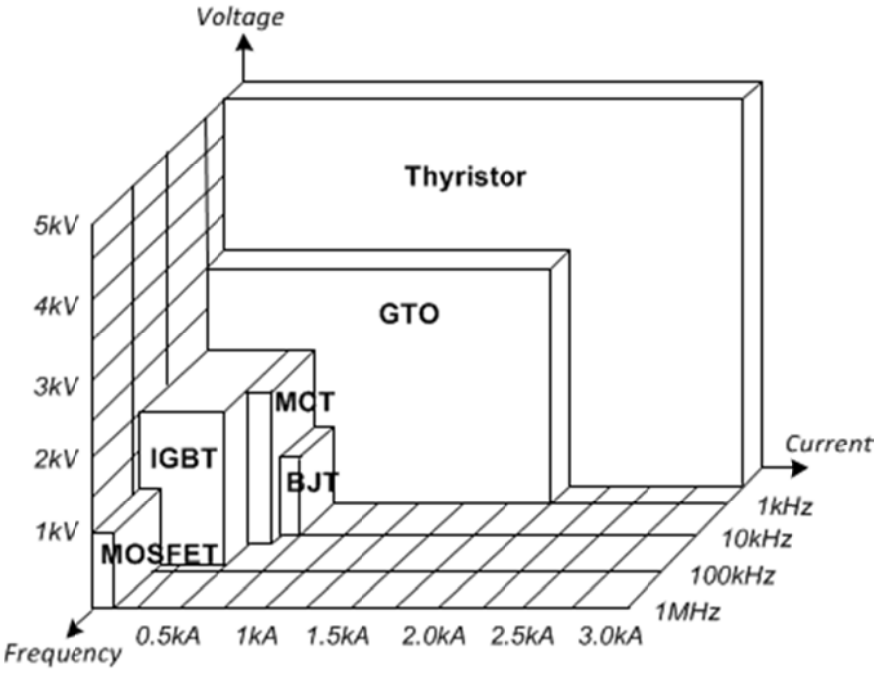


Figure 3.29 : Summary of power semiconductor device capabilities (extracted from [87])

3.2.6 Control Loop

All proposed HFAC inverter in literature employ analog control techniques. In the most basic from the control loop normally consists of voltage/current feedback followed by a compensator network and finally a modulator (PWM, PSM, M-PSM, or PPM) that generates the gate drive signal. A generic form of this type of control structure is represented by the block diagram in Figure 3.30. It shall be shown later that more complex control structures used in other HFAC inverters can be expressed as combination of the basic structure.

This basic control structure in its original form as shown in Figure 3.30 is used only in SSI. In voltage amplitude control, the measured output quantity is the inverter peak or RMS output voltage. In this case, the error signal computation block is simply a subtractor circuit that generates a voltage error signal by subtracting the measured output voltage from the reference voltage. A simple controller such a PI or a type II controller is used to generate the control output. In amplitude control normally a PWM modulator is used to generate the gate drive signal in half bridge designs and PSM / M-PSM is used in full bridge configuration.

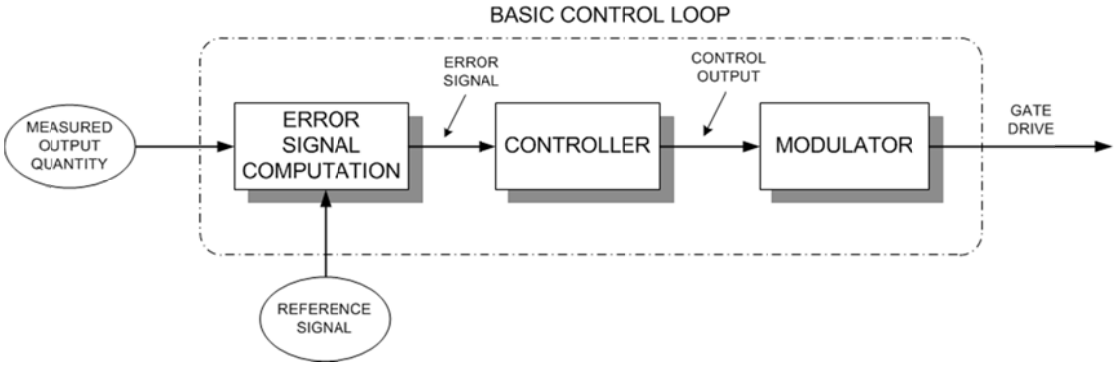


Figure 3.30 : Basic HFAC inverter control block diagram

The same control structure has been used in [83] for phase angle control of the HFAC output voltage. The measured output quantity in this case is still the HFAC output voltage; however the desired error signal is the difference in the phase of the output voltage. The error computation block is therefore more complicated. It consists of a multiplier and a low pass filter circuit to derive the phase error signal from voltage measurement. A PI control is then used to generate the control output. Phase pulse modulation is used to generate the gate drive. Using PPM, under steady state condition with zero error, the gate drive signal is symmetrical (50% duty cycle) and is maintained at a fixed angle from the clock signal. Therefore PPM modulation is the best available technique for phase angle control especially in half bridge inverter design.

In MSI, dual loop control consisting of 2 individual control loop for both amplitude and phase angle control are used [71-73]. One control loop is used to control the magnitude of the output voltage by varying the duty cycle of the front end DC-DC converter. A second loop is used to control the second stage of the inverter using PPM for phase angle control. Each of the individual control structures are exactly same as the voltage

and phase angle controller in SSI described above. Figure 3.31 shows the dual loop control structure typically used in MSI

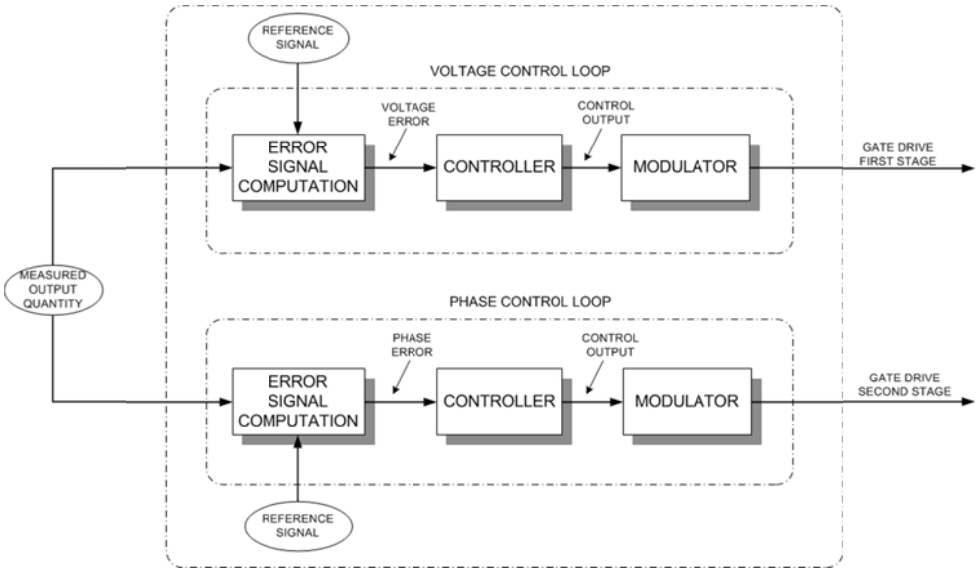


Figure 3.31 : Dual loop HFAC inverter control block diagram

In parallel operation of MSI with current sharing [78-80], a current sharing controller (CSC) is used together with the dual loop control described above. The CSC module senses the output current of the inverter, and the voltage reference & phase error signals are derived from the measured current. A simplified block is shown in Figure 3.32. The details of the CSC block can be seen in Figure 3.22.

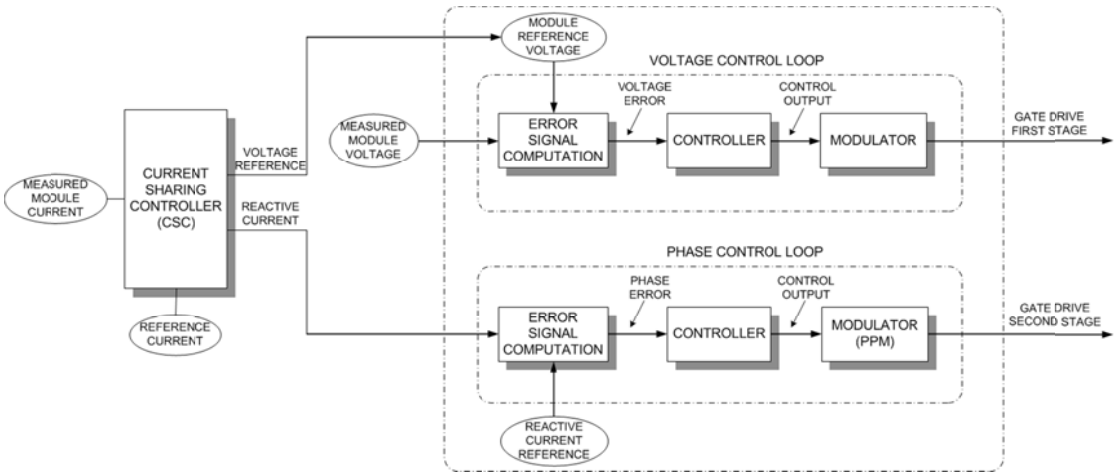


Figure 3.32 : HFAC inverter control block diagram with current sharing control

Feed forward techniques to improve line disturbance rejection have been implemented in HFAC inverter [32, 81, 82]. Feed forward control allows the system to react to changes in the input before it is reflected at the output. Used in conjunction with voltage feedback control, better transient and dynamic performance can be achieved. The implementation block diagram of the feed forward + feedback control loop is shown in Figure 3.33. It can be seen that it is similar to the basic control structure in Figure 3.30 with the exception of the blocks in the shaded area. A type II compensator is typically used to implement the feedback control. A PWM modulator is used to generate the gate drive signal in half bridge designs and PSM / M-PSM is used in full bridge configuration.

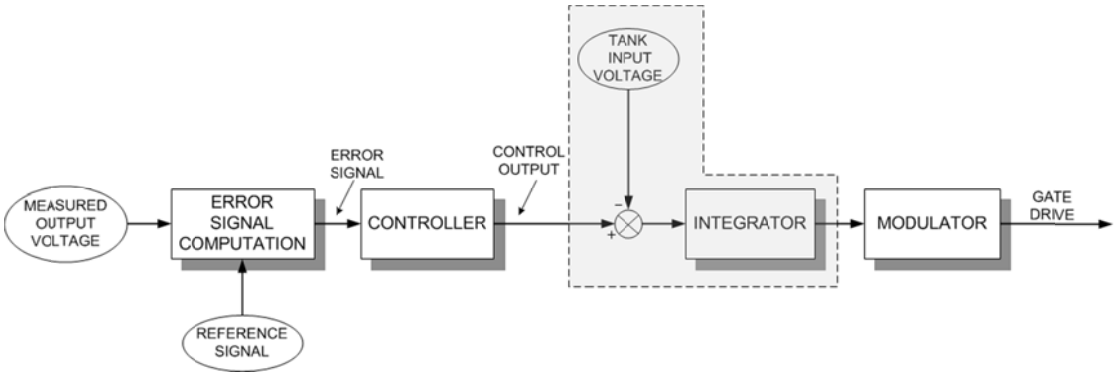


Figure 3.33 : HFAC inverter control block diagram with feedfoward

3.2.7 Further Research Opportunities

In most 2 stage inverters proposed in literature, the front end DC-DC converter is often viewed only as a means to provide independent amplitude control. Therefore in most designs a buck converter is used to step down the input voltage to slightly lower than minimum expected input voltage [71-73, 78-80]. For example in [72, 73], the available input voltage range varies from 45V to 75V and a front end buck converter was used to step down the voltage to 38V to be presented to the HFAC resonant inverter. On the other hand in [37], input voltage variation of 15V to 50V was expected and in this case a boost converter was proposed to step up the voltage to 60V, close to the maximum input voltage. The winding ratio of the transformer is then selected to achieve the required bus voltage level.

It is perhaps necessary to evaluate what the ideal input voltage for the second stage (resonant inverter) should be to in order to achieve maximum efficiency whilst meeting performance goals. Too high or low an input voltage will inevitably leads to high voltage and current stress on the components of the resonant inverter. In the next section we attempt to model the behaviour of the resonant inverter considering the input voltage as a design variable and then using optimization techniques to identify the most suitable design. Performance requirement and constrains imposed by physical component limitation are accounted for in the modelling & optimization process.

As explained in the previous section, all control implementation in HFAC inverter reported so far are analog controllers. In most designs simple controllers such as PI or type II compensators (second order) are used and have been shown to have good transient & steady state performance. On the physical level the controllers are implemented using analog opamp circuitry.

Using a digital signal controller to implement the control of HFAC inverters offer some interesting possibilities. Firstly in MSI, regulating the output phase of the second stage can be achieved by simply synchronizing the PWM duty cycle to a reference signal. Most modern DSP/DCSs have PWM synchronization input signal pins and providing a reference square wave reference input to this pin ensures that the generated PWM signal is in phase with the reference. In effect, this is similar to the behaviour of M-PSM modulator used in full bridge inverters. The front end DC-DC converter can be controlled using standard digital PID or a digital version of typically used analog compensator. In addition, the presence of the digital processor in the HFAC inverter coupled with the capability to communicate over the HFAC bus (see chapter 7), presents the possibility for intelligent management of the HFAC power system.

3.3 Proposal of a HFAC Inverter for Automotive Application

In a study by Antaloae et al in 2010 [88, 89], the authors set out to investigate the system level viability of HFAC power distribution system for powering automotive auxiliary electrical loads. A single phase sinusoidal HFAC bus operating at 50 kHz was reported to be an optimal compromise between transmission efficiency and conductor weight. The HFAC bus voltage level of 100Vrms was proposed. Besides efficiency considerations, the

proposed frequency and bus voltage was selected to be in compliance with SAE J2232 standard on vehicle system voltage and the safety norm DIN VDE 0800 Part 1 which specifies the maximum allowed AC voltage for a range of frequencies.

Here we propose a resonant inverter based on the operating parameters proposed above. The design specification for the HFAC inverter is summarized in Table 3.1.

Parameter	**Notation**	**Value**
Input DC Voltage	V_{DC}	$42V_{DC}$
HFAC Bus Voltage	v_{bus}	$100V_{RMS}$
HFAC Bus Frequency	f_{bus}	50kHz
Output Power (per module)	P_{out}	100W

Table 3.1 : HFAC inverter specification for automotive application

A 2 stage resonant inverter capable of parallel operation is proposed. Either a buck or boost front end will be used for amplitude control followed by a second stage half bridge series parallel resonant inverter. The control loop will be implemented using a suitable digital signal controller. The second stage HFAC inverter is operated at 50kHz at a fixed PWM duty cycle of 50%. The switching frequency of front end DC-DC converter will generally need to be higher than the HFAC bus frequency for improved dynamic performance. A switching frequency of 4 times the bus frequency (200kHz) is proposed. At 200kHz, a maximum of 5μs is available for the computation of the digital control loop and this can be comfortably implemented using existing DSC available in the market. Table 3.2 shows the number of instruction cycle that can be executed within 1 PWM period for various PWM frequency and processor speed. At 200kHz, a 40 MIPS processor is able to execute 200 instructions in 1 PWM period. A 2P2Z (2 poles and 2 zero) controller algorithm takes approximately 26 cycle and 3P3Z (3 poles and 3 zero) take approximately 36 instruction cycles to execute. Therefore at this frequency implementation of fairly complex digital compensators is a possibility. A block diagram of the HFAC inverter is shown in Figure 3.34

PWM Frequency	Interval per cycle (μs)	Number of Instruction Cycles		
		40 MIPS	100 MIPS	150MIPS
50 kHz	20.0	800	2000	3000
100 kHz	10.0	400	1000	1500
200 kHz	5.0	200	500	750
250 kHz	4.0	160	400	600
300 kHz	3.3	133	333	500
500 kHz	2	80	200	300
750 kHz	1.3	53	133	200
1000 kHz	1.0 μs	43	100	150

Table 3.2 : DSP instruction cycles vs PWM frequency

(source : Texas Instruments digital power supplies software solution)

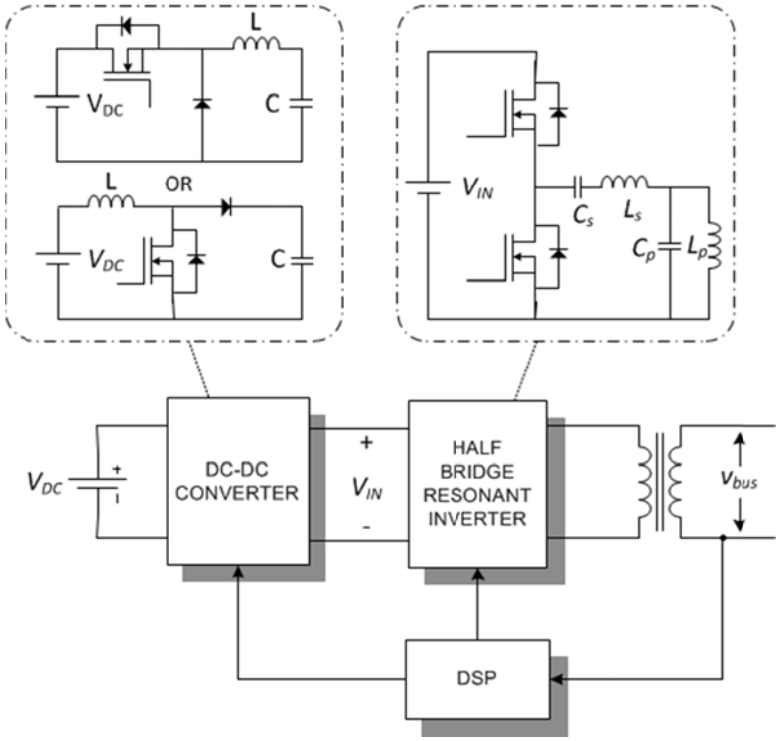


Figure 3.34 : Block diagram of proposed HFAC inverter

3.4 Concluding Remarks

In this chapter, a thorough literature survey of the front end HFAC inverter was presented. The various building blocks of the HFAC inverter were critically reviewed and comparisons between various proposed approaches were drawn. A multi stage resonant

inverter was recommended as a suitable front end inverter for automotive application. Further it was recommended that the input voltage to the second stage resonant inverter should be selected based on efficiency considerations as opposed to being dictated by input voltage variation range. In addition digital control was proposed as an alternative to existing analog control loop. This chapter lays the ground work for the design of a suitable resonant inverter and a preceding DC-DC converter stage in the implementation of a MSI. These are covered in chapter 4 and chapter 5 respectively.

CHAPTER 4

MODELLING OF HFAC RESONANT INVERTER

"All exact science is dominated by the idea of approximation" – ***Bertrand Russell, 1872-1970.***

The primary focus of this chapter is the modelling and optimization of the series parallel resonant inverter that forms the second stage of the multi stage inverter proposed in the previous chapter. Mathematical analysis of the resonant inverter is undertaken to study the complex relationship between the desired performance specification and various design parameters. Graphical frequency domain representation of the important transfer functions is used to provide intuitive insights to the operation of the resonant inverter. Performance curves of the inverter are also generated to complement the frequency domain analysis to yield further qualitative understanding. Following this, a set of assumptions are then proposed to significantly simplify the analytical model and a requirement driven approach is presented to express the relationship between the various design and performance parameters. This simplified model can be efficiently computed to determine optimal design parameters.

4.1 Series Parallel Resonant Inverter – Steady State Modelling

The schematic of the second stage series parallel resonant inverter is shown in Figure 4.1. This circuit represents a realistic model of the resonant inverter, which includes the loss elements in the form of the ESR of passive element, the RDS(on) resistance of the mosfets and transformer non idealities.

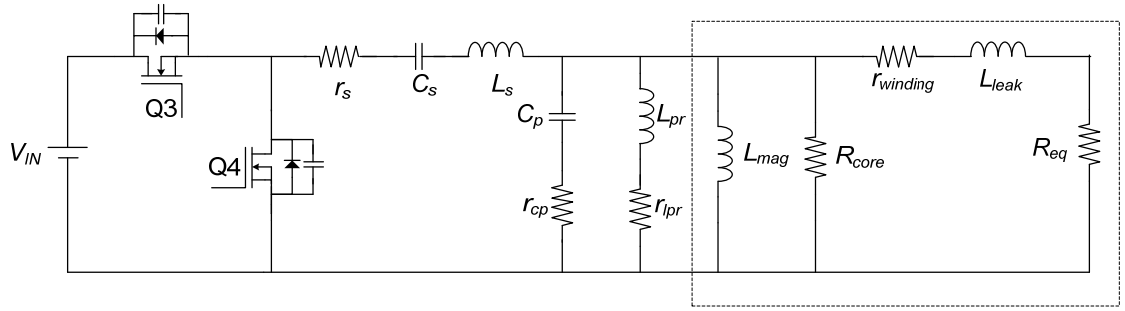


Figure 4.1 : Schematic of half bridge LCLC inverter

The elements within the dotted region in Figure 4.1 represent the approximate equivalent circuit of the HFAC isolation transformer referred to the primary winding. To simplify analysis, the core loss resistance is omitted and the parallel resonant inductor and the transformer magnetizing inductance are combined into a single element. The impedance of the parallel combination of the resonant inductor and the magnetizing inductance is given by (4.1).

$$Z_{p\_eff} = \left(\frac{r_{lpr} {L_{mag}}^2 \omega^2}{r_{lpr}^2 + (L_{mag} + L_{pr})^2 \omega^2} \right) + j \left(\frac{\omega L_{mag} \left(r_{lpr}^2 + L_{pr}(L_{mag} + L_{pr}) \omega^2 \right)}{r_{lpr}^2 + (L_{mag} + L_{pr})^2 \omega^2} \right) \tag{4.1}$$

The effective series resistance and the resonant inductor is a frequency dependent variable. However if the quality factor of the resonant inductor is high $(X_{lpr} >> r_{lpr})$, equation (4.1) simplifies and Z_{p_eff} can be represented as a series combination of an effective resistor r_{lp} and inductor L_p as given by (4.2) and (4.3).

$$r_{lp} = \left(\frac{L_{mag}}{L_{mag} + L_{pr}} \right)^2 r_{lpr} \tag{4.2}$$

$$L_p = \frac{L_{mag} L_{pr}}{L_{mag} + L_{pr}} \tag{4.3}$$

The new simplified equivalent circuit that shall be used for subsequent analysis is shown in Figure 4.2.

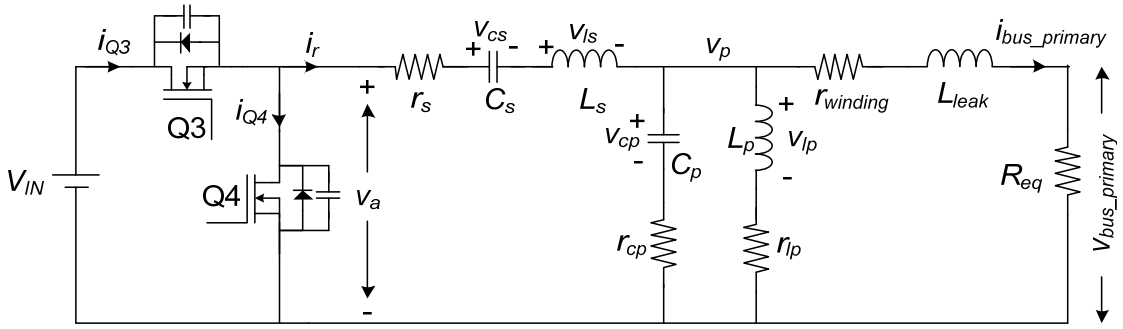


Figure 4.2 : Simplified half bridge LCLC inverter

4.1.1 Circuit analysis

In the simplified circuit, v_a the voltage across Q4 is a function of the switching state. v_a can be expressed in the time domain by (4.4)

$$v_a = \begin{cases} V_{IN} : & t_k < t < t_k + DT_s \\ 0 : & t_k + DT_s < t < t_k + T_s \end{cases} \tag{4.4}$$

Taking the Fourier transform of (4.4), v_a can be expressed as a sum of the constituting harmonic component given by (4.5) and (4.6). With D = 0.5, it can be observed that all the even frequency component become zero. It therefore evident the harmonic distortion will be minimum with D = 0.5.

$$v_a = DV_{IN} + \sum_{n=1}^{\infty} \frac{\sqrt{2} V_{IN} \sqrt{1 - \cos(2\pi n D)}}{n\pi} \sin(n\omega_o t + \phi_n) \tag{4.5}$$

$$\phi_n = \tan^{-1}\left(\frac{\sin(2\pi nD)}{1-\cos(2\pi nD)}\right) \tag{4.6}$$

To keep the analytical expression simple, it is desirable to express the circuit elements in terms of the quality factors and tuning ratio of the tuned branches. The following definitions are proposed. The symbols and notation used here are kept in line with recent literature for the sake of consistency.

The angular resonant frequency of the series and parallel branches are respectively given by (4.7) and (4.8)

$$\omega_s = \frac{1}{\sqrt{L_s C_s}} \tag{4.7}$$

$$\omega_p = \frac{1}{\sqrt{L_p C_p}} \tag{4.8}$$

The ratio of the resonant frequency to the drive (source) frequency ω_o, is an important design parameter. The series and parallel tuning factors are defined as follows

$$k_s = \frac{\omega_s}{\omega_o} \tag{4.9}$$

$$k_p = \frac{\omega_p}{\omega_o} \tag{4.10}$$

The load reflected across the transformer winding (referred to primary) can be expressed as in (4.11) where N is the ratio of the transformer primary winding n_p to the secondary n_s.

$$R_{eq} = N^2 R_L \tag{4.11}$$

The quality factor of the series and parallel resonant branches are defined as follows

$$Q_s = \frac{X_{LS}}{R_{eq}} = \frac{\omega_o L_s}{R_{eq}} \tag{4.12}$$

$$Q_p = \frac{R_{eq}}{X_{LP}} = \frac{R_{eq}}{\omega_o L_p} \tag{4.13}$$

At this stage, using (4.7) to (4.13), the circuit elements can be expressed in terms of the tuning factor, quality factor and reflected load impedance. The reactance of the inductors and capacitors in the series and parallel branches computed at the drive frequency is given as

$$X_{LS} = jnQ_s R_{eq} \tag{4.14}$$

$$X_{CS} = \frac{-jk_s{}^2 Q_s R_{eq}}{n} \tag{4.15}$$

$$X_{LP} = \frac{jnR_{eq}}{Q_p} \tag{4.16}$$

$$X_{CP} = \frac{-jk_p{}^2 R_{eq}}{nQ_p} \tag{4.17}$$

4.1.2 Definition of Impedances

The impedance of the series branch Z_{sn} is given as

$$Z_{sn} = r_s + j\left[nQ_s R_{eq} - \frac{k_s^2 Q_s R_{eq}}{n}\right] \tag{4.18}$$

The impedance formed by the transformer leakage inductance, winding resistance and any connection impedance can be represented by (4.19).

$$Z_{txn} = r_{winding} + jn\omega L_{leak} \tag{4.19}$$

The impedance of the parallel inductive and capacitive branch is given by

$$Z_{lpn} = r_{lp} + j\frac{nR_{eq}}{Q_p} \tag{4.20}$$

$$Z_{cpn} = r_{cp} - j\frac{k_p{}^2 R_{eq}}{nQ_p} \tag{4.21}$$

The effective impedance presented by the parallel inductive branch, capacitive branch and the sum of the transformer and connection impedance and the load resistance is given by (4.22).

$$Z_{pn} = \left(\frac{1}{Z_{lpn}} + \frac{1}{Z_{cpn}} + \frac{1}{Z_{txn} + R_{eq}}\right)^{-1} \tag{4.22}$$

4.1.3 Circuit element current & voltages

The voltage across the parallel tuned branch represented by v_p will need to be first calculated before the expression for the load voltage can be determined. v_p can be determined using the voltage divider rule applied to the combination of the impedance formed by Z_{sn} and Z_{pn} and is given by (4.23)

$$v_p(t) = \sum_{n=1}^{\infty} G_{an} \frac{\sqrt{2}V_{IN}\sqrt{1-\cos(2\pi nD)}}{n\pi} \sin\left(n\omega_o t + \phi_n + \chi_{an}\right) \tag{4.23}$$

Where G_{an} is magnitude of the impedance divider network given by (4.24) and χ_{an} is the phase angle and is given by (4.25). Both these parameters are functions of the harmonic number n and therefore need to be calculated for all harmonic component of v_a.

$$G_{an} = \left|\frac{Z_{pn}}{Z_{sn} + Z_{pn}}\right| \tag{4.24}$$

$$\chi_{an} = Arg\left[\frac{Z_{pn}}{Z_{sn} + Z_{pn}}\right] \tag{4.25}$$

The bus voltage referred to the primary winding can now be computed from the voltage divider network formed by Z_{txn} and the reflected load R_{eq} driven by source v_p. The resulting expression for $v_{bus\_primary}$ is

$$v_{bus\_primary}(t) = \sum_{n=1}^{\infty} G_{an} G_{bn} \frac{\sqrt{2} V_{IN} \sqrt{1-\cos(2\pi n D)}}{n\pi} \sin\left(n\omega_o t + \phi_n + \chi_{an} + \chi_{bn}\right) \tag{4.26}$$

Where G_{bn} and χ_{bn} are defined as follows.

$$G_{bn} = \left|\frac{R_{eq}}{Z_{txn} + R_{eq}}\right| \tag{4.27}$$

$$\chi_{bn} = Arg\left[\frac{R_{eq}}{Z_{txn} + R_{eq}}\right] \tag{4.28}$$

The input current to the resonant network i_r can be computed by dividing the voltage across the resonant tank v_a by the input impedance of the loaded resonant network. This can be expressed as shown in (4.29)

$$i_r(t) = \sum_{n=1}^{\infty} \frac{1}{G_{cn}} \frac{\sqrt{2} V_{IN} \sqrt{1-\cos(2\pi n D)}}{n\pi} \sin\left(n\omega_o t + \phi_n - \chi_{cn}\right) \tag{4.29}$$

Where G_{cn} is the magnitude of the input impedance given by (4.30) and χ_{cn} is the phase angle of the input impedance of the loaded resonant network as given by (4.31)

$$G_{cn} = \left|Z_{sn} + Z_{pn}\right| \tag{4.30}$$

$$\chi_{cn} = Arg\left[Z_{sn} + Z_{pn}\right] \tag{4.31}$$

The circulating current in the parallel inductor can be computed by dividing the voltage across the parallel elements v_p computed previously by the impedance of the inductive branch. The current into the parallel inductor L_p is given by (4.32) where $\angle Z_{lpn}$ is the phase angle of inductive branch.

$$i_{lp}(t) = \sum_{n=1}^{\infty} \frac{G_{an}}{\left|Z_{lpn}\right|} \frac{\sqrt{2}V_{IN}\sqrt{1-\cos\left(2\pi nD\right)}}{n\pi} \sin\left(n\omega_o t + \phi_n + \chi_{an} - \angle Z_{lpn}\right) \tag{4.32}$$

The current into the parallel capacitor C_p can be computed in a similar manner and is given by (4.33) where $\angle Z_{cpn}$ is the phase angle of the parallel capacitive branch.

$$i_{cp}(t) = \sum_{n=1}^{\infty} \frac{G_{an}}{\left|Z_{cpn}\right|} \frac{\sqrt{2}V_{IN}\sqrt{1-\cos\left(2\pi nD\right)}}{n\pi} \sin\left(n\omega_o t + \phi_n + \chi_{an} - \angle Z_{cpn}\right) \tag{4.33}$$

The voltage across the parallel inductor L_p and parallel capacitor C_p can be computed by using (4.32) and (4.33) and is given as follows

$$v_{lp}(t) = \sum_{n=1}^{\infty} \frac{\left|X_{LP}\right| G_{an}}{\left|Z_{lpn}\right|} \frac{\sqrt{2}V_{IN}\sqrt{1-\cos\left(2\pi nD\right)}}{n\pi} \sin\left(n\omega_o t + \phi_n + \chi_{an} - \angle Z_{lpn} + \frac{\pi}{2}\right) \tag{4.34}$$

$$v_{cp}(t) = \sum_{n=1}^{\infty} \frac{\left|X_{CP}\right| G_{an}}{\left|Z_{cpn}\right|} \frac{\sqrt{2}V_{IN}\sqrt{1-\cos\left(2\pi nD\right)}}{n\pi} \sin\left(n\omega_o t + \phi_n + \chi_{an} - \angle Z_{cpn} - \frac{\pi}{2}\right) \tag{4.35}$$

The voltage across the series inductor L_s and series capacitor C_s can be computed by multiplying the input resonant tank current computed previous with the impedance of L_s and C_s and is given by (4.36) and (4.37).

$$v_{ls}(t) = \sum_{n=1}^{\infty} \frac{\left|X_{LS}\right|}{G_{cn}} \frac{\sqrt{2}V_{IN}\sqrt{1-\cos\left(2\pi nD\right)}}{n\pi} \sin\left(n\omega_o t + \phi_n - \chi_{cn} + \frac{\pi}{2}\right) \tag{4.36}$$

$$v_{cs}(t) = DV_{IN} + \sum_{n=1}^{\infty} \frac{|X_{CS}|}{G_{cn}} \frac{\sqrt{2}V_{IN}\sqrt{1-\cos(2\pi nD)}}{n\pi} \sin\left(n\omega_o t + \phi_n - \chi_{cn} - \frac{\pi}{2}\right) \quad (4.37)$$

The current into mosfets Q3 and Q4 can be expressed as a piecewise function, where during the ON phase of the mosfet, the resonant tank current i_r flows through it and during the off phase the current is 0. Remembering that Q3 and Q4 are switched in a complementary fashion and ignoring the dead time, the mosfet current can be expressed as shown below

$$i_{Q3}(t) = \begin{cases} \sum_{n=1}^{\infty} \frac{1}{G_{cn}} \frac{\sqrt{2}V_{IN}\sqrt{1-\cos(2\pi nD)}}{n\pi} \sin\left(n\omega_o t + \phi_n - \chi_{cn}\right) : & t_k < t < t_k + DT_s \\ 0 : & t_k + DT_s < t < Ts \end{cases} \quad (4.38)$$

$$i_{Q4}(t) = \begin{cases} 0 : & t_k < t < t_k + DT_s \\ -\sum_{n=1}^{\infty} \frac{1}{G_{cn}} \frac{\sqrt{2}V_{IN}\sqrt{1-\cos(2\pi nD)}}{n\pi} \sin\left(n\omega_o t + \phi_n - \chi_{cn}\right) : & t_k + DT_s < t < Ts \end{cases} \quad (4.39)$$

4.1.4 Time Domain Waveforms

From the mathematical model developed in the previous section, the current and voltage waveform across various circuit element are plotted. This is compared against PSPICE simulation results to verify the accuracy of the analytical model. The parameters used for modelling and simulation are shown in Table 4.1.

The plot generated from the mathematical model was obtained by numerically computing the values of equations (4.5) to (4.39) to the first 100th harmonics. The ringing seen especially in Figure 4.10 and Figure 4.11 are not due parasitic LC oscillation (although such effects do exist in actual circuits) but rather due to the Fourier series approximation as mentioned above. The transformer turns ratio is calculated using equation (4.59) and V_{bus} and V_{IN} value from Table 4.1. For the PSPICE simulation, Mosfet IRFS4229PBF from International Rectifier was used. Further a 150ns dead time between the Q3 and Q4 gate drive signals was implemented. From Figure 4.3 to Figure

4.11 it appears that there is very good correlation between the mathematical model and PSPICE simulation. This correlation stands to validate the accuracy of the analytical model.

Parameter	**Notation**	**Value**
Mosfet RDS(on) Value	r_{ds}	48 mΩ
ESR Series Resonant Capacitor	r_{cs}	10.11 mΩ
ESR Series Resonant Inductor	r_{ls}	45 mΩ
ESR Parallel Resonant Capacitor	r_{cp}	7.73 mΩ
ESR Parallel Resonant Inductor	r_{lp}	41 mΩ
Transformer Effective Series Resistance (referred to primary)	$r_{winding}$	110 mΩ
Transformer Effective Series Inductance (referred to primary)	L_{leak}	2.2uH
Duty Cycle	D	0.5
Input DC Voltage	V_{IN}	88V
HFAC Bus Frequency	f_{bus}	50kHz
Series Tuned Quality Factor	Q_s	1.2
Parallel Tuned Quality Factor	Q_p	1.4
Series Tuning Factor	k_s	1
Parallel Tuning Factor	k_p	1.1
HFAC Bus Voltage (RMS)	V_{bus}	100V
HFAC Bus Output Power	P_{out}	100W

Table 4.1 : Inverter simulation and modelling parameters

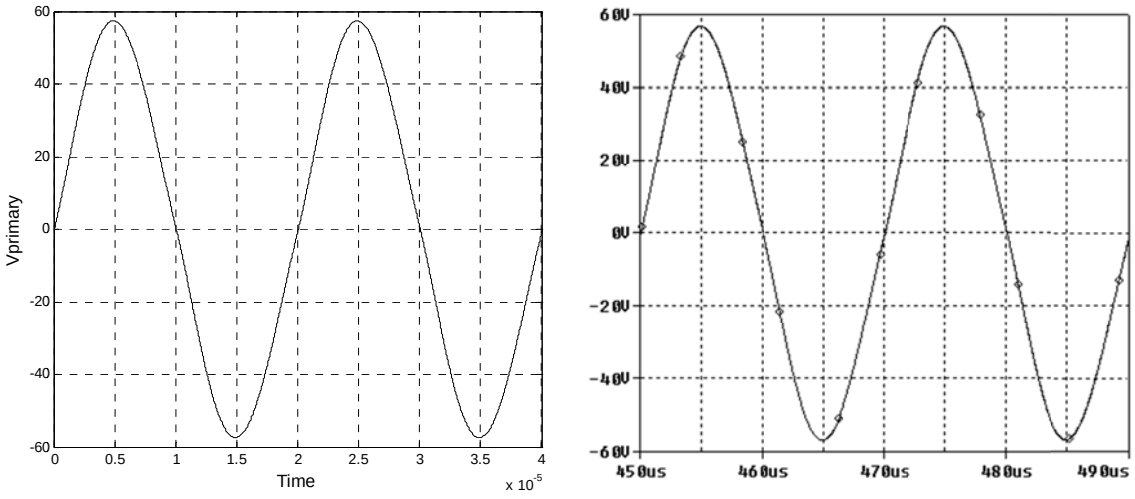


Figure 4.3 : Bus voltage referred to primary (a) analytical (b) P-SPICE

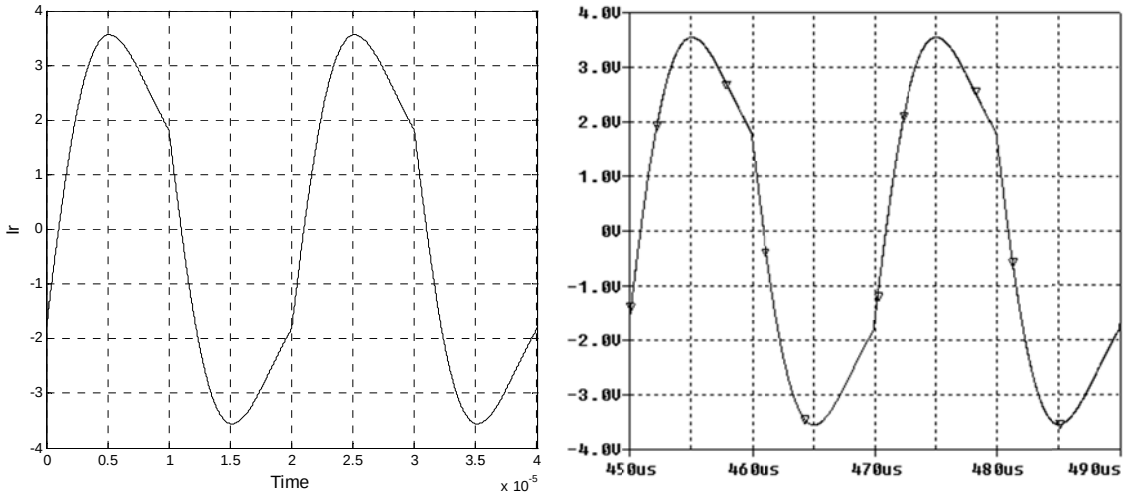


Figure 4.4 : Resonant tank input current (a) analytical (b) P-SPICE

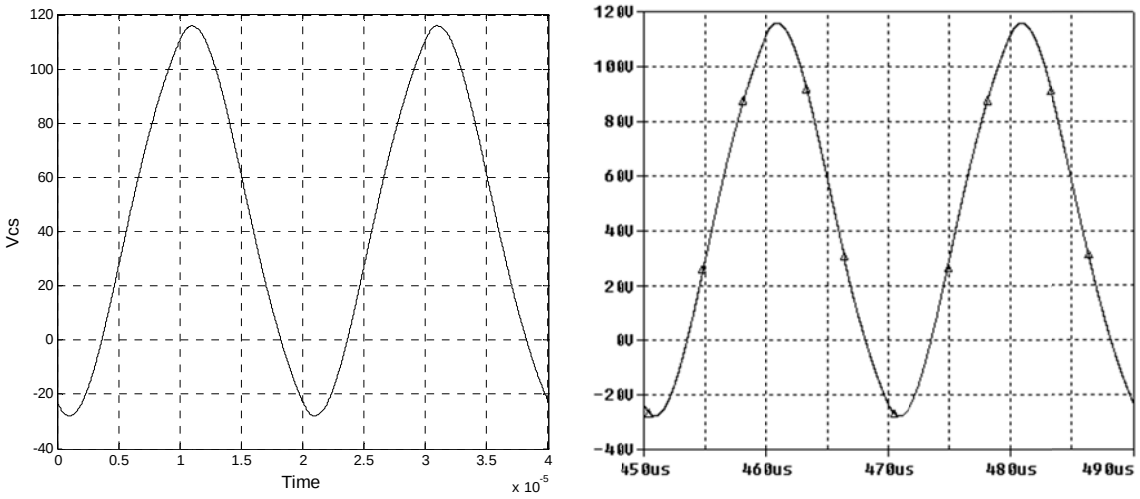


Figure 4.5 : Series capacitor voltage (a) analytical (b) P-SPICE

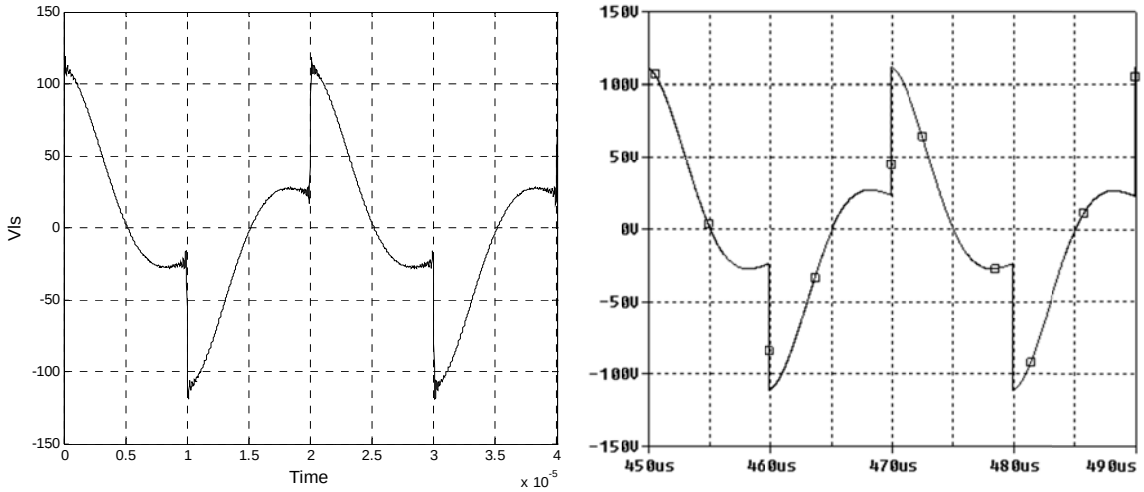


Figure 4.6 : Series inductor voltage (a) analytical (b) P-SPICE

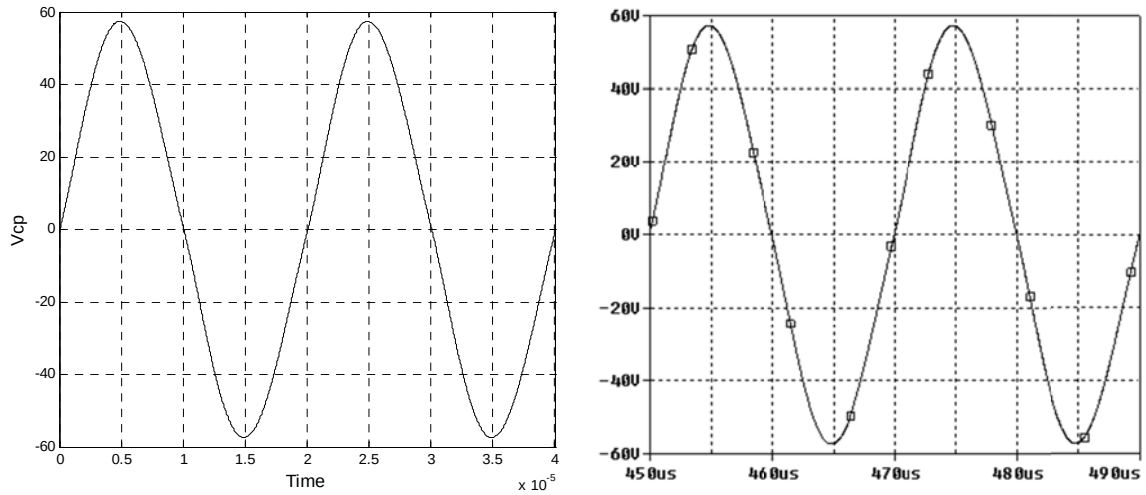


Figure 4.7 : Parallel capacitor voltage (a) analytical (b) P-SPICE

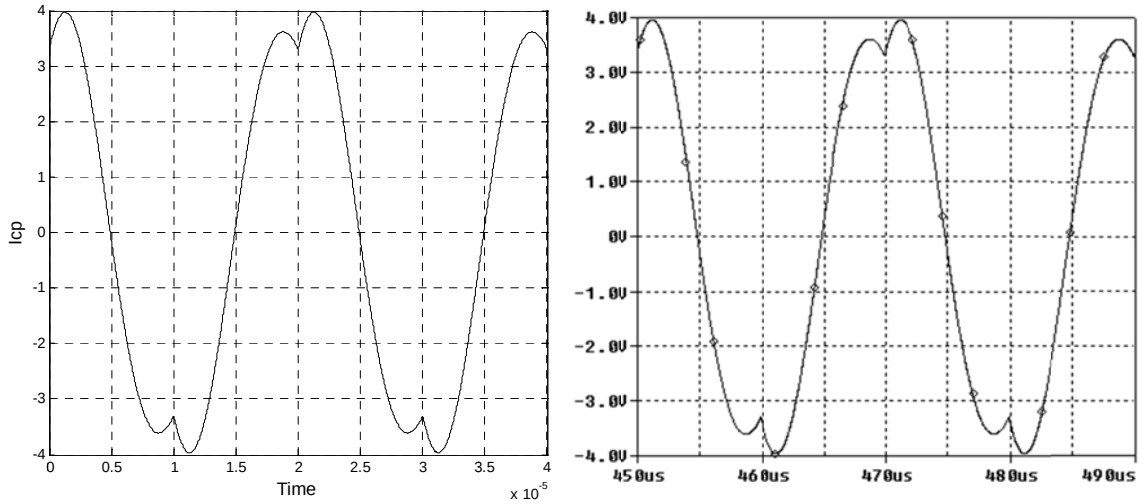


Figure 4.8 : Parallel capacitor current (a) analytical (b) P-SPICE

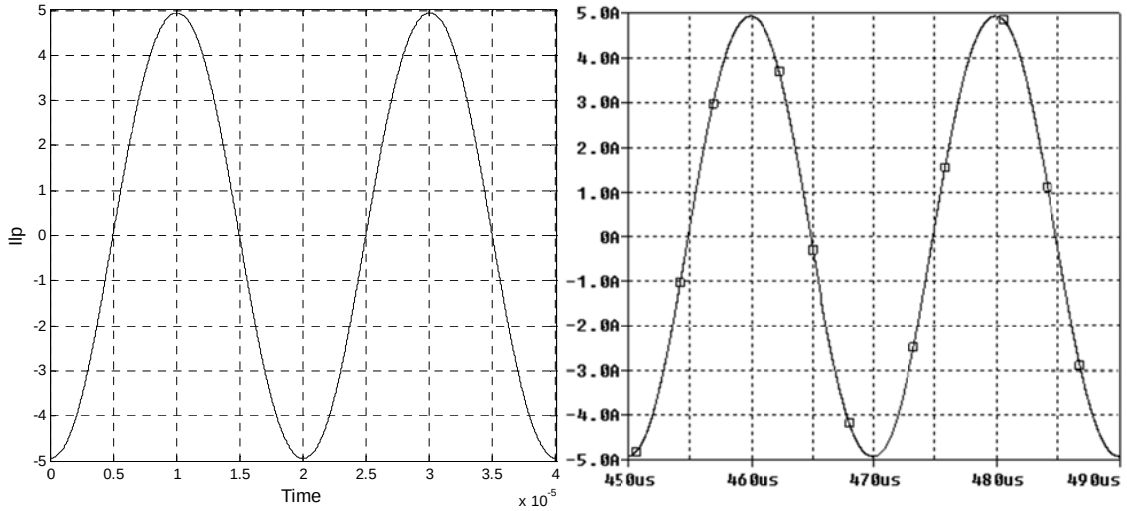


Figure 4.9 : Parallel inductor current (a) analytical (b) P-SPICE

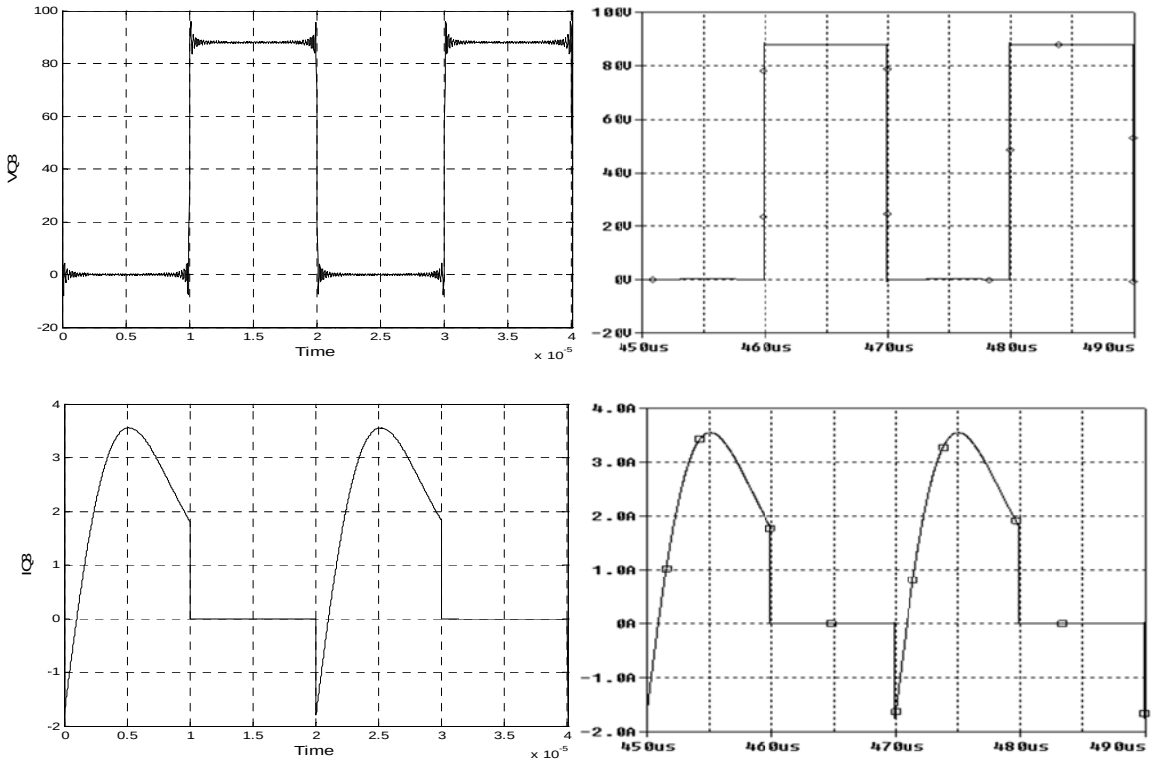


Figure 4.10 : Mosfet Q3 current & voltage waveform (a) analytical (b) P-SPICE

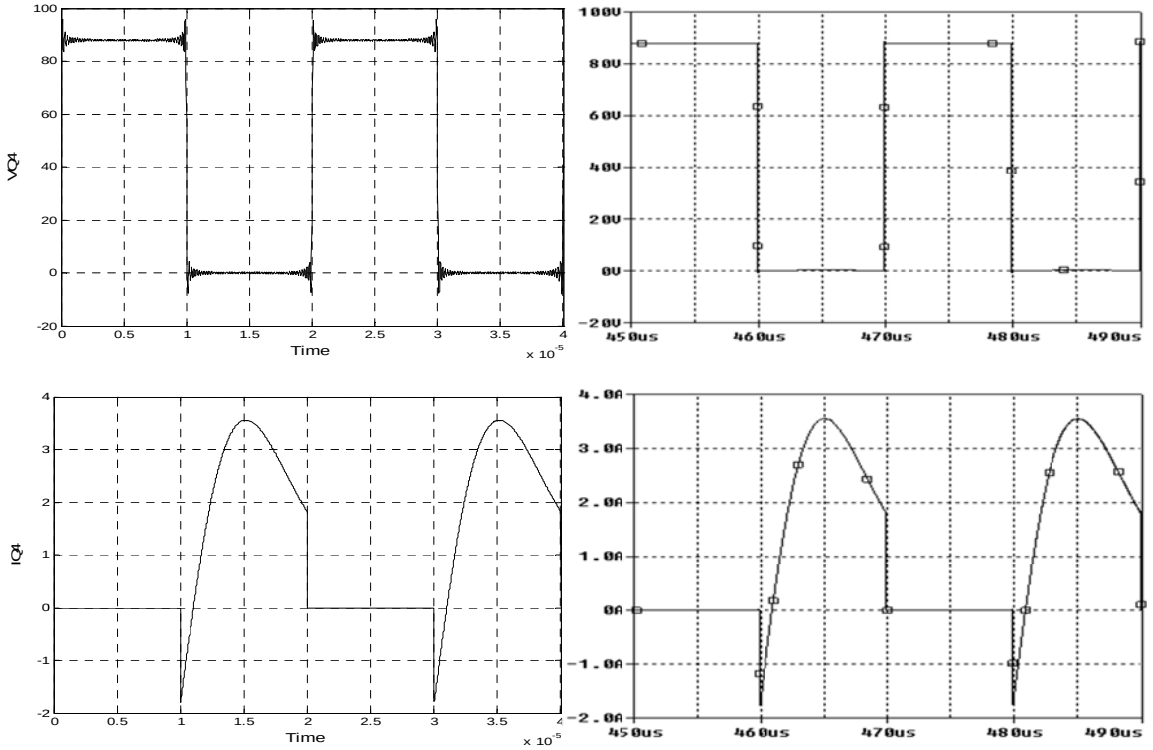


Figure 4.11 : Mosfet Q4 current & voltage waveform (a) analytical (b) P-SPICE

4.2 Frequency Domain Analysis

From the mathematical model developed in the previous section, it is not directly obvious how the various design parameters affect the current and voltage across any circuit element. In the attempt to better understand this relationship, it is beneficial to look at the problem form a frequency domain perspective. This approach allows the relationship to be graphically represented and thus give a general idea on how variation of a design variable might change the performance of the inverter.

From fundamental network theory, it is known that the steady state response of a linear time invariant system, $G(s)$ to a sinusoidal excitation of the $V\sin(\omega t+\phi)$ is given by (4.40)

$$y_{ss}(t) = \left|G(s)\right|_{s=j\omega} V\sin(\omega t+\phi+\angle G(s)\big|_{s=j\omega}) \tag{4.40}$$

The mathematical expression for the various circuit current and voltages derived in section 4.1.3 were deliberately represented in the form similar to (4.40). The input excitation was taken to be the voltage across Q_4, (which is across the input of the resonant tank). Taking (4.26) as an example, the input and the system components of the steady state output equation are shown in
Figure 4.12.

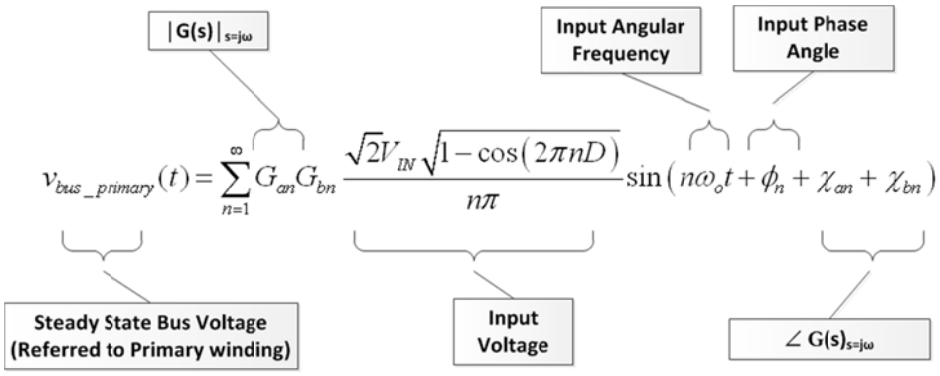


Figure 4.12 : Steady state expression of analytical equations

Having determined the magnitude $|G(s)|_{s=j\omega}$ and phase $\angle G(s)|_{s=j\omega}$, the transfer function $G(s)$ between the output variable and the input can be computed using (4.41)

$$G(j\omega) = |G(j\omega)|e^{j\angle G(j\omega)} \tag{4.41}$$

The bode plot of (4.41) gives a graphical representation of the influence of the system transfer function on the input. As the transfer function itself is a function of the various design parameters, by performing a sweep of these variables, it may be possible to shed some light on the complex relationship between the output and design parameters.

It is important to remember that whilst the bode plot is continuous, it is only meaningful at the harmonic frequencies of the input voltage $n\omega_o$, where $n \in \{1,3,5,7\ldots\ldots\infty\}$. In the next section the two most important transfer functions $[i_r(s)/v_a(s)]$ and $\left[v_{bus\_primary}(s)/v_a(s)\right]$ are analysed.

4.2.1 Resonant Tank Input Current – Transfer Function Analysis

The bode plot of the transfer function between the input resonant current and the voltage across Q_4 , $i_r(s)/v_a(s)$ is given in Figure 4.13 to Figure 4.17. In Figure 4.13, for fixed values of V_{IN} , k_p, k_s and Q_s the effect of Q_p on the resonant current is shown. It can be observed that at the resonant frequency, higher value of Q_p lead to higher gain in the amplitude of the fundamental component. At the harmonics frequencies, the gain for various value of Q_p is similar. Therefore higher Q_p will result in higher resonant current with lower total harmonic distortion. In addition the phase angle at the resonant frequency generally gets more inductive with increase in Q_p .

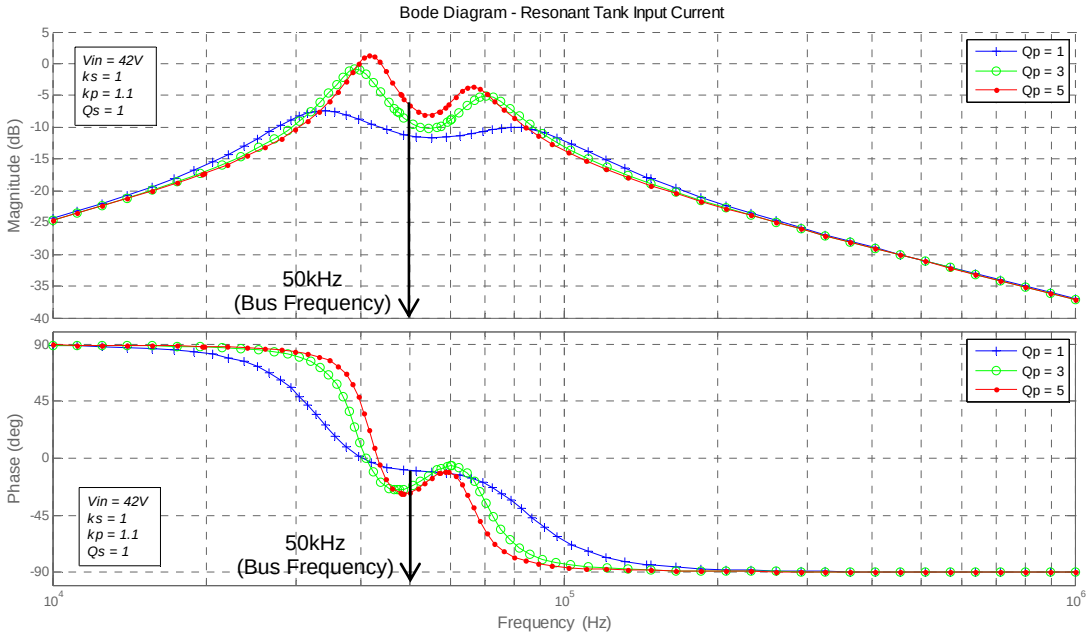


Figure 4.13 : Bode Plot - resonant tank input current (variation in Qp)

Increase in Q_s has no effect on the fundamental component of the resonant current or phase angle. However at the harmonic frequencies, the gain of the resonant tank input current reduces with increase in the value of Q_s, therefore the THD will be improved.

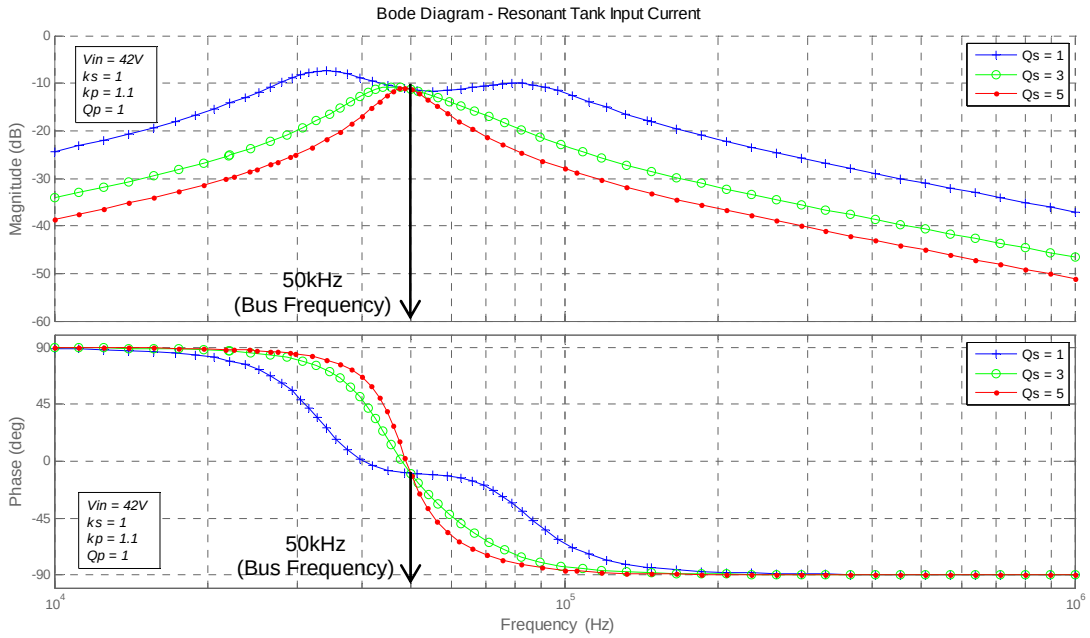


Figure 4.14 : Bode Plot - resonant tank input current (variation in Qs)

The parallel tuning ratio k_p has no effect on the magnitude of the fundamental and harmonic component of the resonant tank input current. However at the resonant fundamental frequency, the phase angle of tank resonant current is affected by the value of k_p. When k_p is unity, the phase angle is zero and thus the resonant tank appears resistive. For value of k_p less than unity, the resonant tank appears capacitive and for k_p greater than unity the tank is inductive. It will be shown in later sections, to ensure the mosfets Q_3 and Q_4 are soft switched, it's imperative that the resonant tank appear inductive and it is evident from Figure 4.15 that k_p should be selected to be greater than unity to ensure soft switching.

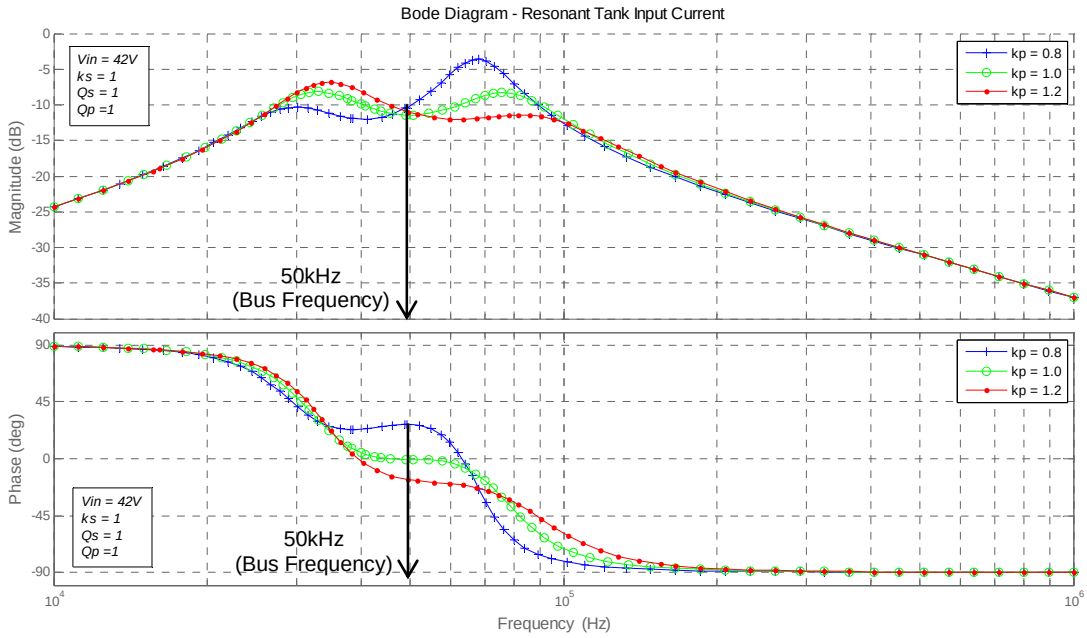


Figure 4.15 : Bode Plot - resonant tank input current (variation in kp)

Variation of the series tuning ratio k_s has no appreciable effect on either the magnitude or the THD of resonant tank current. However when k_s is more than unity, it is possible for the resonant tank to appear capacitive even when k_p is greater than unity.

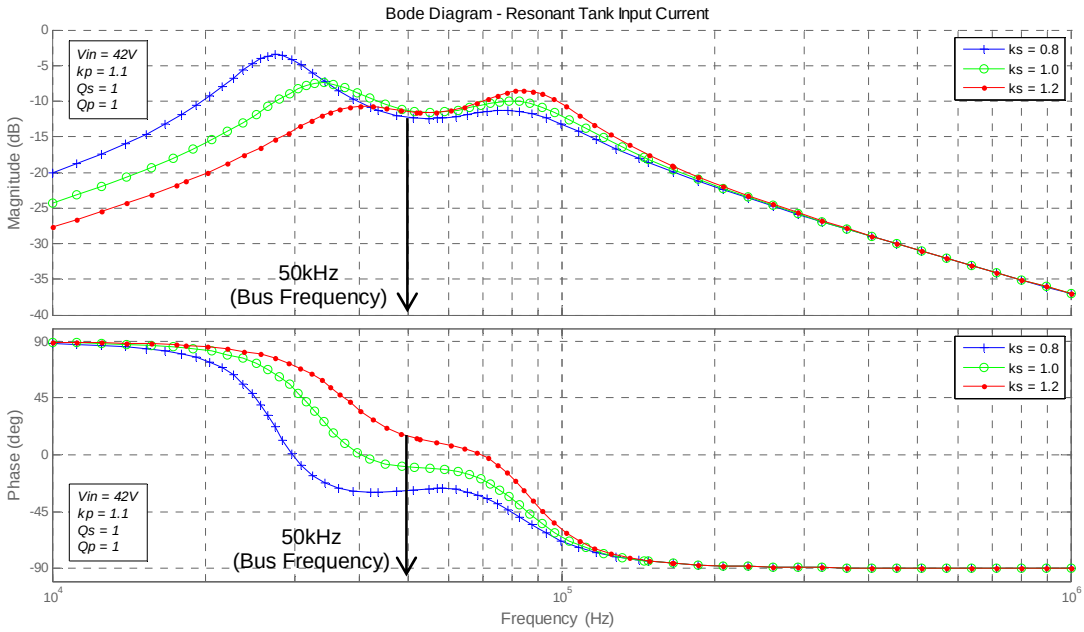


Figure 4.16 : Bode Plot - resonant tank input current (variation in ks)

Increasing V_{IN} vertically shift the magnitude bode plot down, therefore reducing the magnitude of the resonant tank current. As all frequency components are attenuated by the same factor, there will be no change in THD. Changes in V_{IN} has no effect on the phase angle of the resonant current.

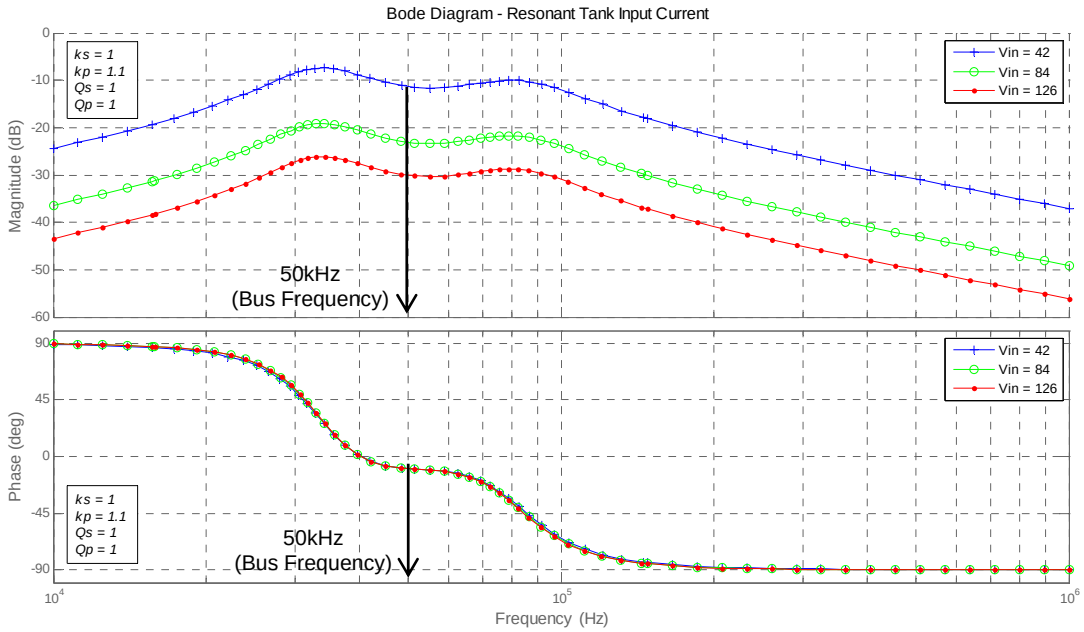


Figure 4.17 : Bode Plot - resonant tank input current (variation in V_{IN})

The effects of the series and parallel tuning factor, quality factor and input voltage on the resonant tank input current as discussed above is summarized in Table 4.2 .

Parameter	Conditions	Transfer Function Summary $i_r(s)/v_a(s)$	
		Magnitude Response	**Phase Response**
k_s	$V_{IN}=42V$ $k_p=1.1$ $Q_s=1$ $Q_p=1$	1. No appreciable effect	1. Larger the value of k_s the more capacitive the resonant tank appears at the fundamental frequency
k_p	$V_{IN}=42V$ $k_s=1.0$ $Q_s=1$ $Q_p=1$	1. No appreciable effect	1. k_p < 1, the resonant tank appears capacitive at the fundamental frequency 2. k_p > 1, the resonant tank appears inductive at the fundamental frequency
Q_s	$V_{IN}=42V$ $k_p=1.1$ $k_s=1.0$ $Q_p=1$	1. THD of resonant tank current is inversely proportional to Q_s	1. Unchanged at fundamental frequency
Q_p	$V_{IN}=42V$ $k_p=1.1$ $k_s=1.0$ $Q_s=1$	1. THD of the resonant tank current is inversely proportional to Q_p 2. The magnitude of the fundamental component of the resonant tank current is proportional to Q_p	1. Larger the value of Q_p the more inductive the resonant tank appears at the fundamental frequency
V_{IN}	$k_s=1.0$ $k_p=1.1$ $Q_s=1$ $Q_p=1$	1. The magnitude of the resonant tank current is inversely proportional to V_{IN}	1. No effect

Table 4.2 : Summary of resonant current to tank input voltage transfer function

4.2.2 Output Voltage – Transfer Function Analysis

The bode plot of the transfer function between the transformer primary voltage and the voltage across Q_4 , $v_{bus\_primary}(s)/v_a(s)$ is given in Figure 4.18 to Figure 4.22. In Figure 4.18, for fixed values of V_{IN} , k_p, k_s and Q_s the effect of Q_p on the output voltage is shown. Q_p has no effect on the fundamental component of the output voltage, however at the harmonic frequencies, higher values of Q_p tend to attenuate the harmonic components better thus resulting in lower THD.

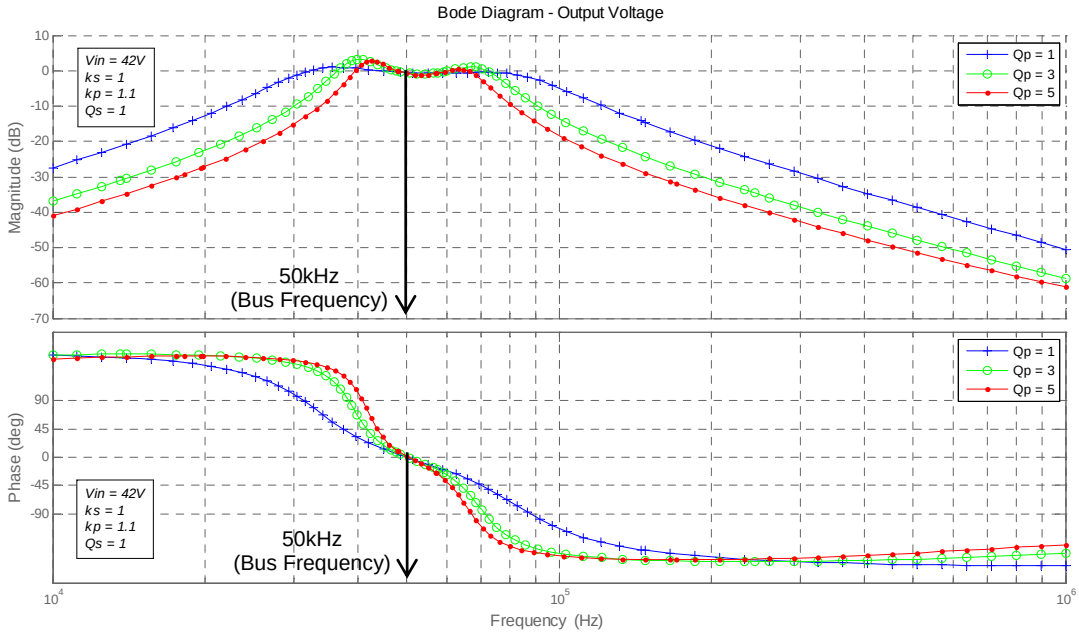


Figure 4.18 : Bode Plot - bus voltage (variation in Qp)

Similarly, variation in Q_s does not appear to have any effect on the fundamental component of the output voltage. Increasing Q_s has the same effect as Q_p at the harmonic frequencies. Therefore higher values of Q_s will yield lower THD of the output voltage.

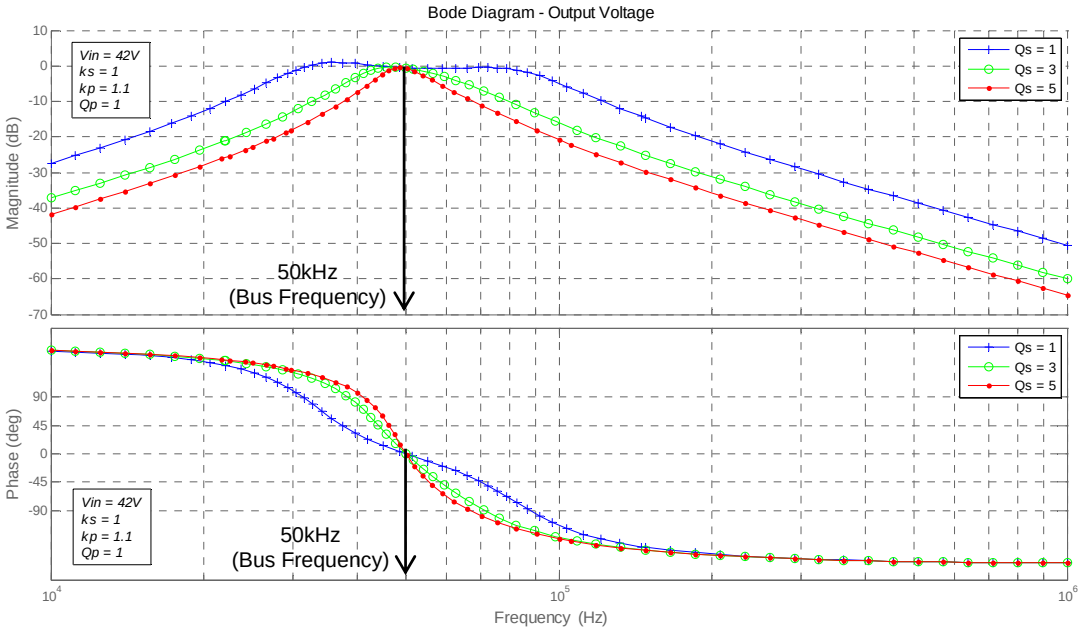


Figure 4.19 : Bode Plot - bus voltage (variation in Qs)

The parallel tuning ratio k_p has no effect on the magnitude or phase of the fundamental component of the output voltage. However lower values of k_p will improve the THD.

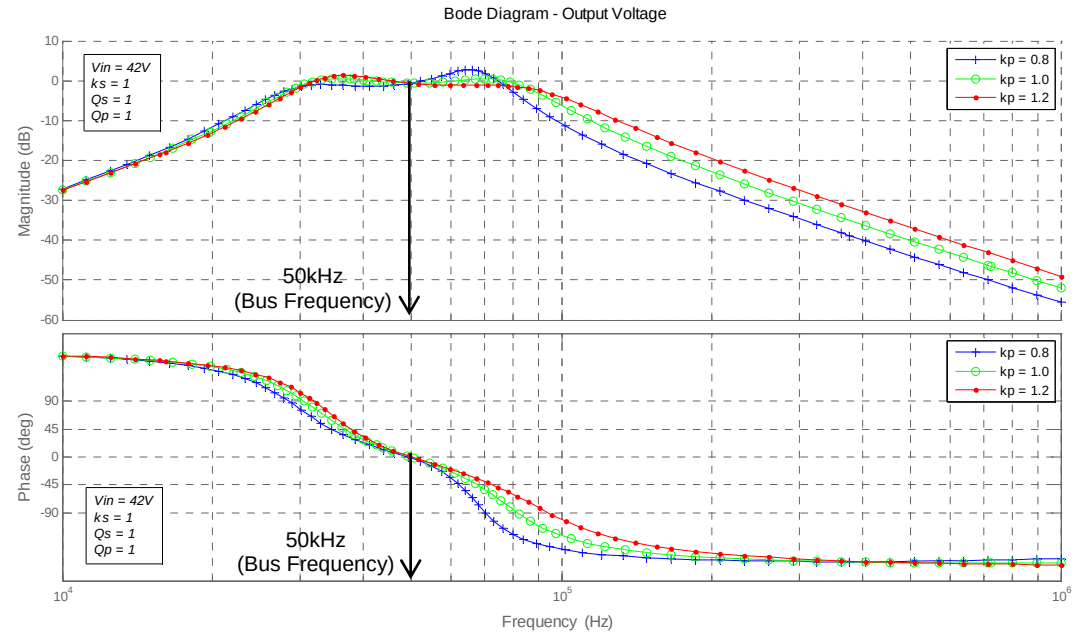


Figure 4.20 : Bode Plot - bus voltage (variation in kp)

Variation in the series tuning ratio k_s has no effect on the magnitude of the fundamental or the harmonic components of the output voltage. Therefore no change in the amplitude or THD is expected as a result of variation in k_s. However k_s is the only parameter that can alter that phase shift of the output voltage. As shall be discussed in later sections, it is important to ensure that the output voltage is in phase with the voltage

across Q_4 to simplify phase angle control of the output voltage. As can be seen is Figure 4.21, to meet this requirement a k_s value of unity is required.

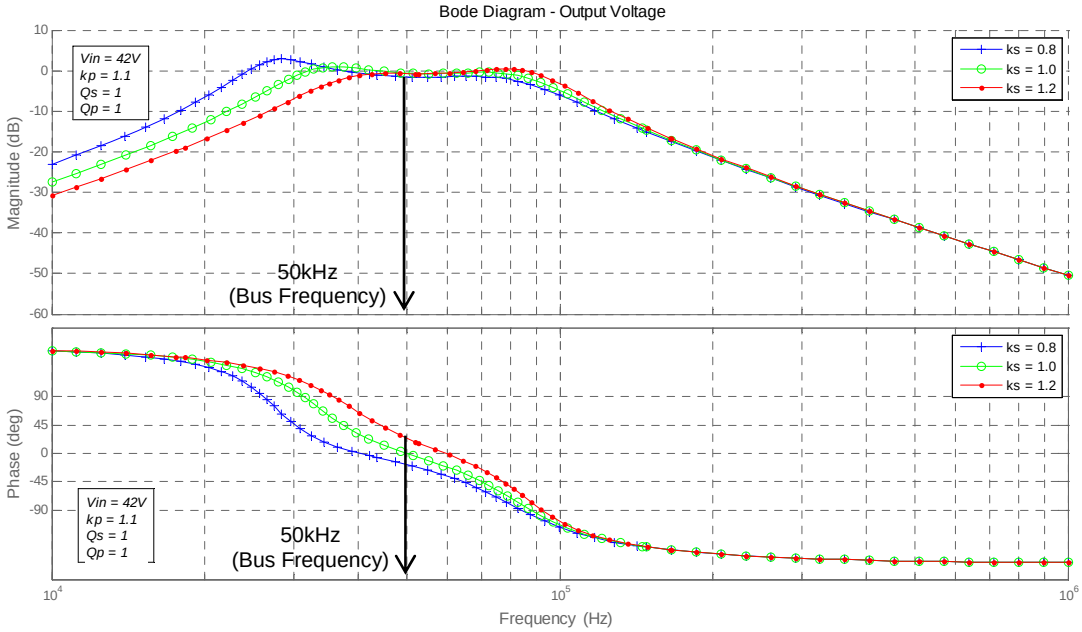


Figure 4.21 : Bode Plot - bus voltage (variation in ks)

Finally Figure 4.22 shows the effect of the variation in the tank input voltage on the converter output voltage. It can be seen that the output voltage magnitude is constant regardless of the tank input voltage, with no change to the THD. This only true if the transformer turns ratio calculated according to equation (4.59).

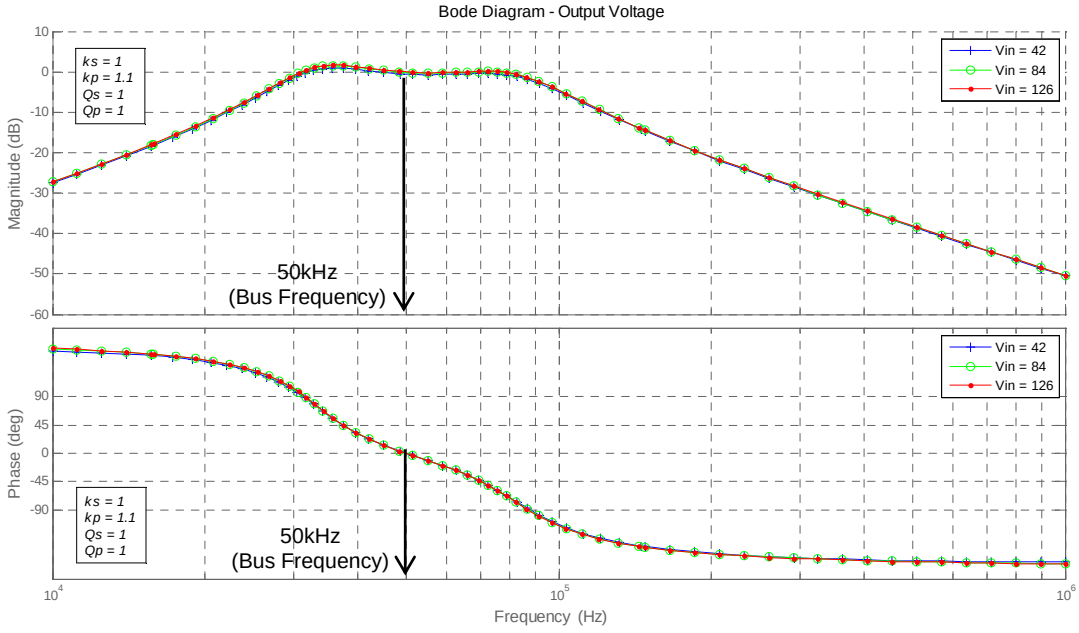


Figure 4.22 : Bode Plot - bus voltage (variation in V_{IN})

The effects of the series and parallel tuning factor, quality factor and input voltage on the bus voltage as discussed above is summarized in Table 4.3.

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Parameter	Conditions	Transfer Function Summary $v_{bus\_primary}(s) / v_a(s)$	
		Magnitude Response	**Phase Response**
k_s	$V_{IN} = 42V$ $k_p = 1.1$ $Q_s = 1$ $Q_p = 1$	1. No appreciable effect on amplitude of bus voltage at fundamental frequency 2. No appreciable effect on THD of bus voltage	1. $k_p <$ 1, the fundamental component of the bus voltage lags the tank input voltage 2. $k_p >$ 1, the fundamental component of the bus voltage leads the tank input voltage
k_p	$V_{IN} = 42V$ $k_s = 1.0$ $Q_s = 1$ $Q_p = 1$	1. No effect on amplitude of bus voltage at fundamental frequency 2. THD of bus voltage is proportional to k_p	1. Unchanged at fundamental frequency
Q_s	$V_{IN} = 42V$ $k_p = 1.1$ $k_s = 1.0$ $Q_p = 1$	1. No effect on amplitude of bus voltage at fundamental frequency 2. THD of bus voltage is inversely proportional to Q_s	1. Unchanged at fundamental frequency
Q_p	$V_{IN} = 42V$ $k_p = 1.1$ $k_s = 1.0$ $Q_s = 1$	1. No effect on amplitude of bus voltage at fundamental frequency 2. THD of bus voltage is inversely proportional to Q_p	1. Unchanged at fundamental frequency
V_{IN}	$k_s = 1.0$ $k_p = 1.1$ $Q_s = 1$ $Q_p = 1$	1. The magnitude of the bus voltage is proportional to V_{IN} 2. THD of the bus voltage is unaffected.	1. No effect

Table 4.3 : Summary of bus voltage to tank input voltage transfer function

4.3 Performance Curves of Resonant Inverter

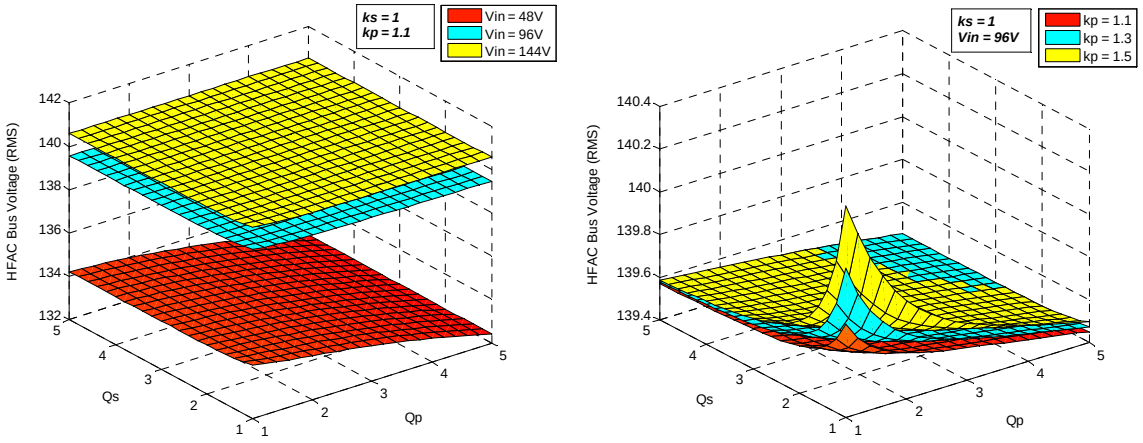
The mathematical model developed in section 4.1.3 contains all the necessary information to accurately determine all inverter current and voltage waveforms. However further information is necessary to concisely describe some performance goals. For example to accurately describe the output voltage requirement for the resonant inverter, often specification for the frequency, RMS value and the total harmonic distortion is required. Further when selecting component for the physical design, in addition to the current and voltage waveform across the component, it is often necessary to know the RMS values.

In this section, we set out to study the important performance parameters of the inverter and how these parameter vary with the design variables namely Q_p, Q_s, k_p, k_s, and V_{IN}. To some extent, the frequency domain analysis in the previous section has shed some light on how some of the performance parameters namely THD. We now proceed to systematically study the relationship between the design and performance parameters

4.3.1 HFAC Bus Voltage

The variation of the RMS HFAC bus voltage as a function of the input DC voltage and the parallel tuning factor is depicted in Figure 4.23. In general, the HFAC bus voltage is proportional to the input voltage of the resonant inverter. The series and parallel quality factor Q_s and Q_p appear to have a negligible effect on the RMS value of the bus voltage especially at high input voltage. However at low input voltage, the bus voltage appears to drop marginally (approximately 2V) as the value of Q_p increases.

The higher the input DC voltage, the closer the calculated HFAC bus voltage approaches the actual peak value of 141.42V ($100V_{RMS}$). At 144V input there is error of approximately 0.6% and at 96V the error is approximately 1.36%. However at 42V the input voltage is error is more than 5.2%.

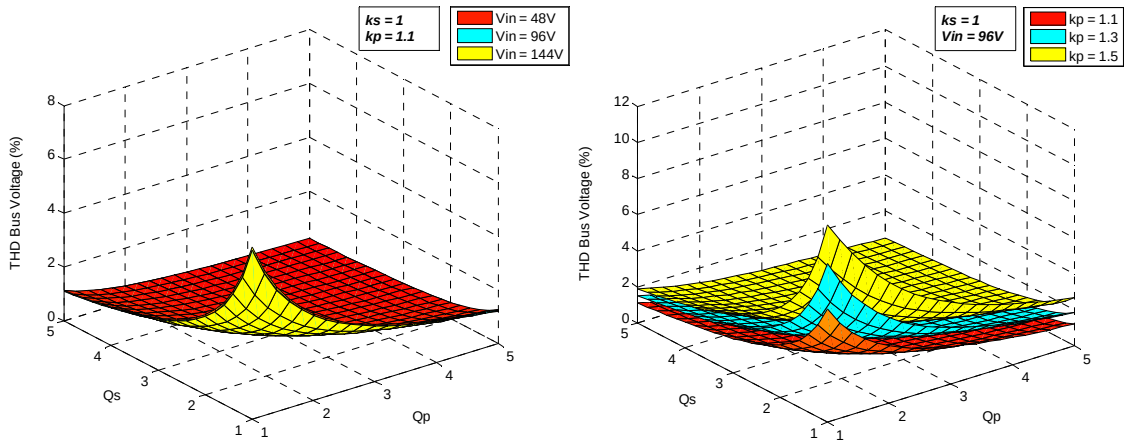


(a) V_{IN} variation (b) kp variation

Figure 4.23 : HFAC bus voltage variation (RMS)

The difference in the magnitude of the HFAC bus voltage for various value of V_{IN} is due to the voltage drop across the parasitic resistances. It will be shown later that for lower input voltage values, the magnitude of the resonant current is higher and therefore the magnitude of the voltage drop will be greater. Subsequently the effective peak voltage across the primary of the transformer is less than $2V_{IN}/\pi$. From Figure 4.23 (b) the parallel tuning factor k_p appears to have a very small, almost insignificant effect on the magnitude of the bus voltage.

As discussed in section 4.2.2, the fundamental component of the output voltage remains unaffected by changes in the values of Q_s, Q_p and k_p. However all these parameters affect the gain at the other harmonic frequencies. Higher values of Q_s and Q_p attenuate the harmonics better and will lead to improved THD. As for k_p, lower values leads to better THD. The THD curve of the output voltage in Figure 4.24 shows the variation of THD with respect to of Q_s, Q_p and k_p. Simultaneous value of low Q_s, Q_p and high k_p can lead poor THD and operation under such condition should be avoided. The input voltage has no effect on the THD of the bus voltage.



(a) V_{IN} variation

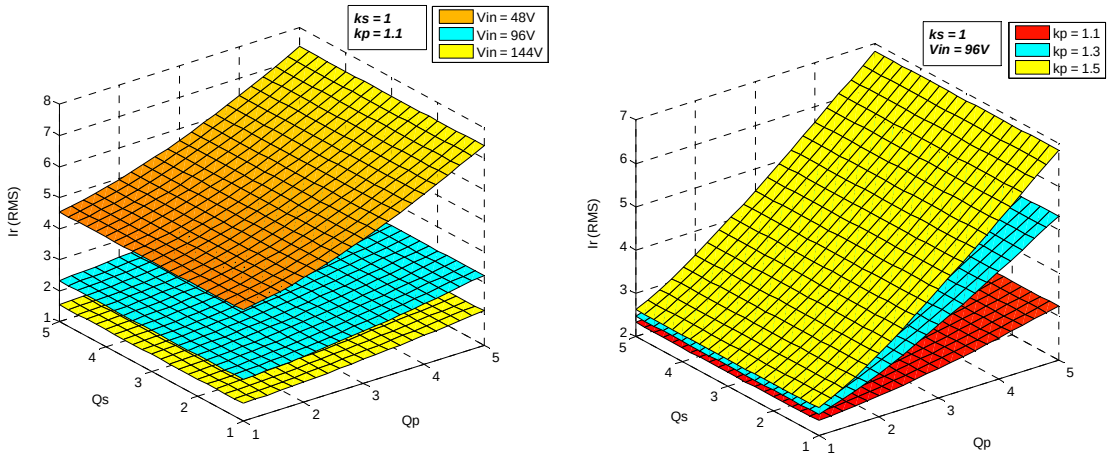
(b) kp variation

Figure 4.24 : THD of the HFAC bus voltage

4.3.2 Resonant Tank Input Current

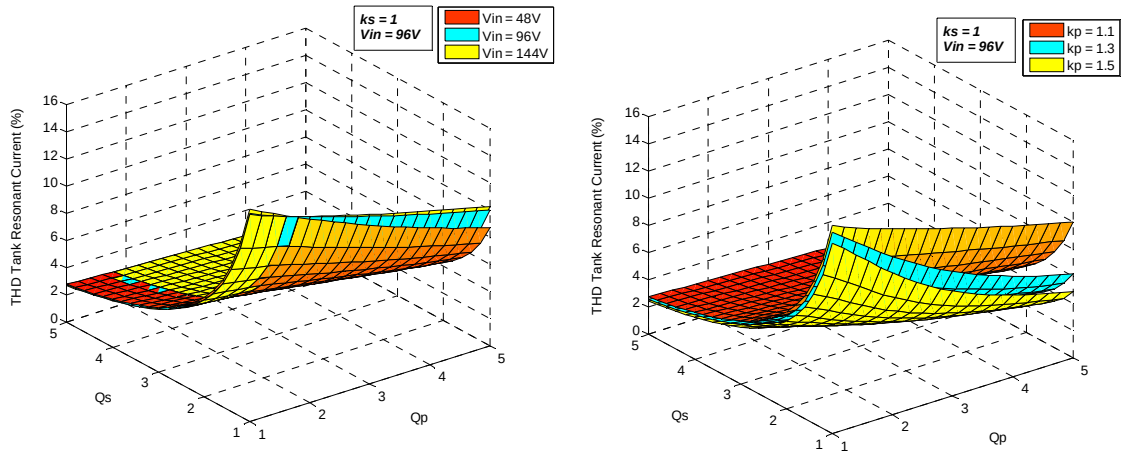
The RMS value of the input resonant tank current increases quickly with drop in input voltage. The series quality factor Q_s does not have any significant effect on the resonant tank current. The magnitude of the tank current increases with Q_p and the rate of increase is higher at lower DC input voltage. This explains the variance in the HFAC output bus voltage at low DC input voltage as shown in Figure 4.23 (a).

From Figure 4.25 (b) at small values of Q_p, the parallel tuning factor k_p does not appear to have any significant effect on the magnitude of the input resonant current. This is consistent with the observation made from the bode plot in Figure 4.15. However as Q_p increases, the effect of k_p on the magnitude of the resonant current becomes more pronounced. At high Q_p values, increasing k_p tends to increase the magnitude of the resonant current. This observation accentuates the limitation of bode plot representation used in the previous sections, as it is difficult to clearly characterize simultaneous effects of various design parameters. A surface plot of the parameter of interest with respect to the design variable as used in this section provides a better means to visualize and to draw qualitative conclusions that are more accurate.



(a) V_{IN} variation (b) kp variation

Figure 4.25 : Resonant tank input current variation (RMS)



(a) V_{IN} variation (b) kp variation

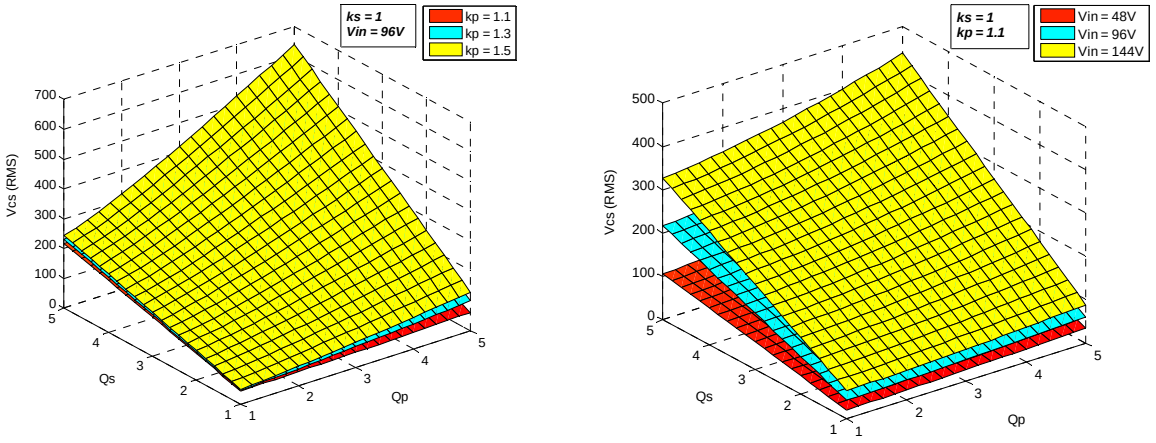
Figure 4.26 : THD of resonant tank input current

The THD of the input resonant current improves with increase in either Q_p or Q_s. As Figure 4.26(a) indicates, higher value of Q_s appears to improve the THD by a larger margin compared to high Q_p. This can be explained by examining the bode plot in Figure 4.13 and Figure 4.14. Both Q_p and Q_s employ different strategy to improve the THD. It can be observed that Q_p improves the THD by increasing the gain of the fundamental component while keeping the amplitude of the higher harmonic components unchanged. Increasing Q_s on the other hand attenuates all harmonic

components except the fundamental. Although both strategies essentially increase the ratio of the fundamental component to the harmonics, the latter technique offers better performance. The effect of k_p on the THD of the resonant tank input current is only noticeable at high Q_p values, where increase in k_p causes a drop in the THD. Figure 4.26(b) show the relationship between k_p and the THD of the resonant current.

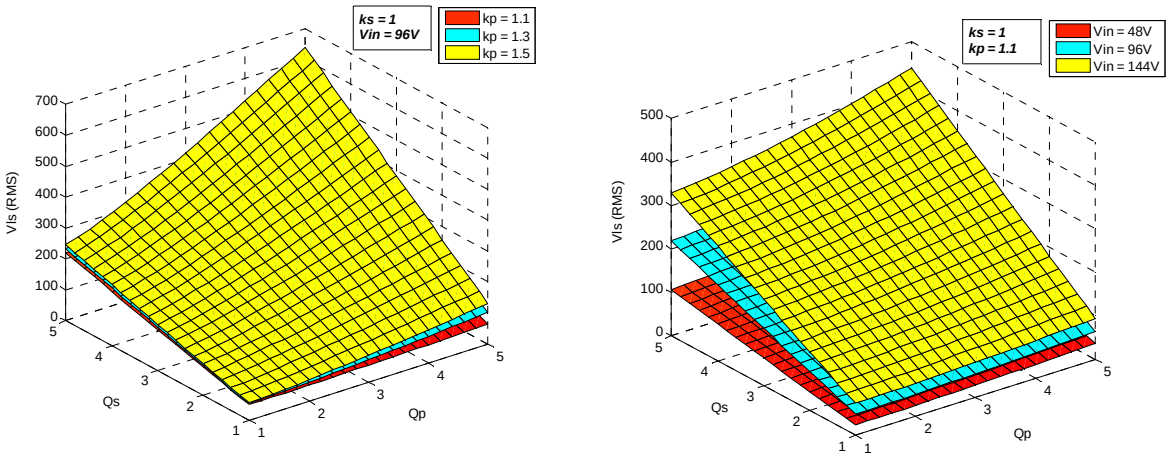
4.3.3 Series Capacitor & Inductor Voltage Stress

The RMS voltage stress across the series capacitor increase with the increase in the values of Q_s, Q_p and k_p. The series quality factor Q_s appears to have a greater effect on the RMS voltage compared to the parallel quality factor. The capacitor voltage also increases with higher input DC voltage. The voltage stress across the series inductor has similar properties as the voltage across the series capacitor and is shown in
Figure 4.27 and Figure 4.28 respectively.



(a) V_{IN} variation (b) kp variation

Figure 4.27 : Series capacitor voltage stress (RMS)

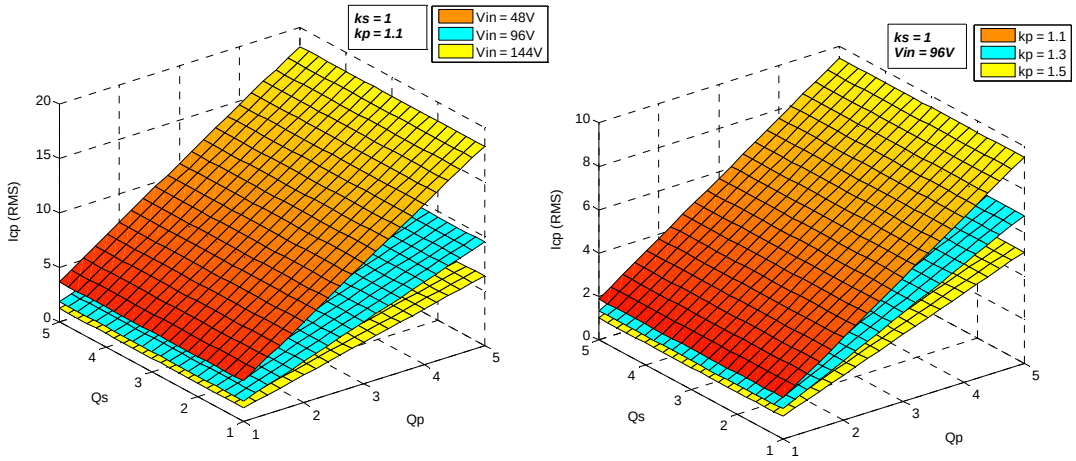


(a) V_{IN} variation (b) kp variation

Figure 4.28 : Series inductor voltage stress (RMS)

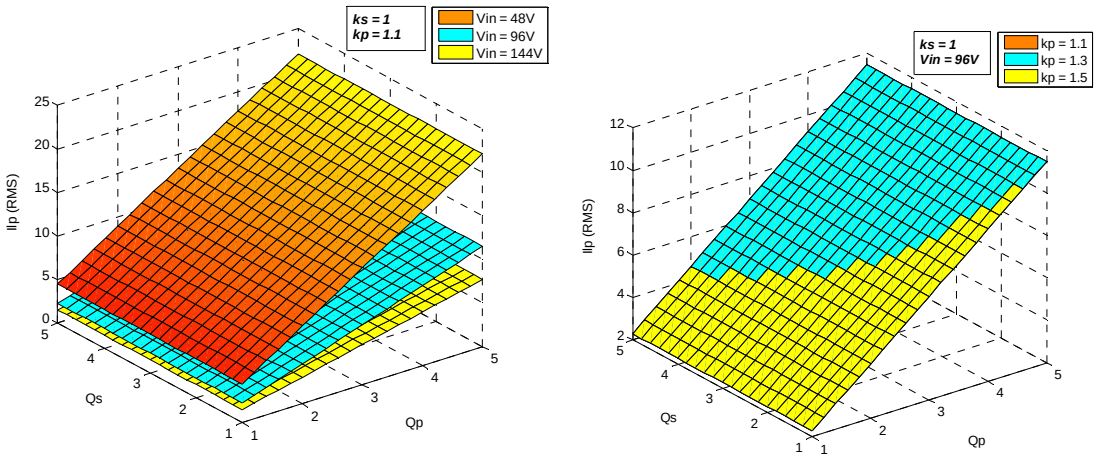
4.3.4 Parallel Capacitor & Inductor Current

The RMS current into the parallel capacitor and inductor behave almost identically to variations in V_{IN}, Q_s and Q_p. The magnitude of both the inductor and capacitor currents decreases as the input DC voltage V_{IN} increases. The RMS current magnitude is linearly proportional to Q_p and appears invariant to changes in Q_s. In addition the parallel capacitor current is inversely related to the parallel tuning factor k_p, but the inductor current however is not affected by variations in k_p. Figure 4.29 shows the RMS parallel capacitor current curve and the inductor current curves are shown in Figure 4.30.



(a) V_{IN} variation (b) kp variation

Figure 4.29 : Parallel capacitor current (RMS)

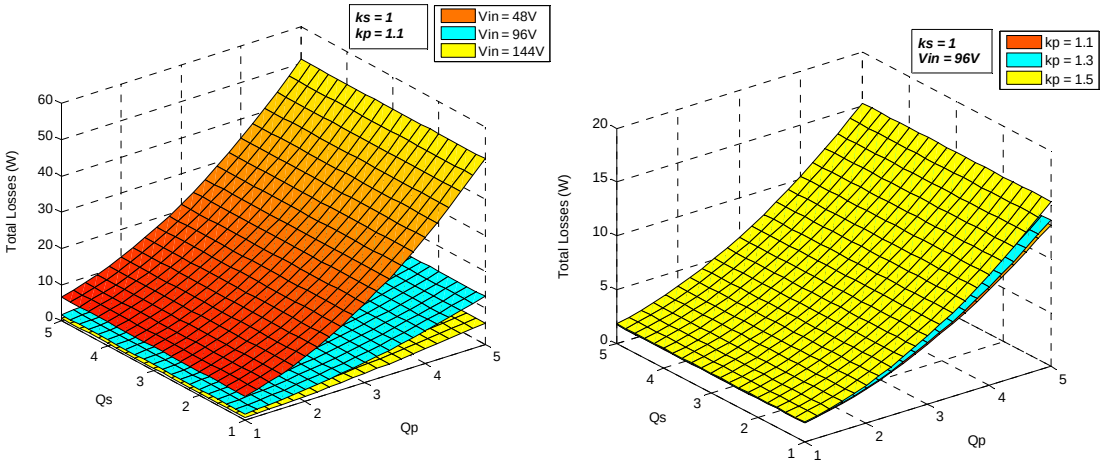


(a) V_{IN} variation (b) kp variation

Figure 4.30 : Parallel inductor current (RMS)

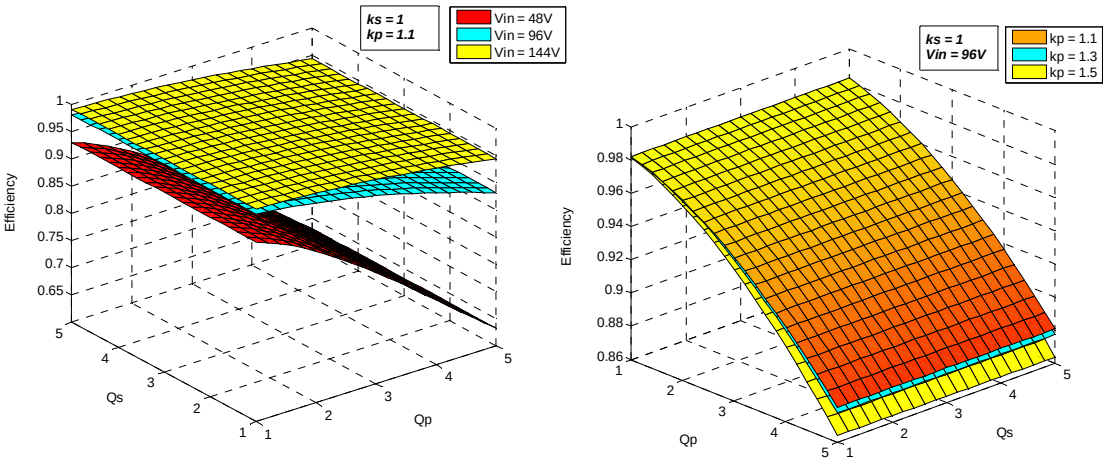
4.3.5 Total Conduction Losses & Efficiency Curves

The total conduction loss curve is shown in Figure 4.31. The total losses are calculated by taking the sum of the I^2R losses in r_s, $r_{winding}$, r_{cp} & r_{lp}. It can be concluded that the input voltage V_{IN} and the parallel quality factor Q_p are the two most important parameters that have significant contribution to the conduction losses. Higher V_{IN} or lower Q_p reduce the total losses significantly. Variance is k_p also has some bearing on the losses, however the effect is not as pronounced as the contribution of V_{IN} and Q_p. The efficiency of the converters can be determined easily from the total losses and the rated output power. The efficiency curves are shown in Figure 4.32. As expected, the efficiency is the highest when the input DC voltage V_{IN} is made as high as possible and the parallel quality factor Q_p is made as low as other considerations allows.



(a) V_{IN} variation (b) kp variation

Figure 4.31 : Total conduction losses in resonant inverter



(a) V_{IN} variation (b) kp variation

Figure 4.32 : Efficiency of resonant inverter

4.4 A Quantitative Approach

In the previous sections, the relationship between the important performance parameters and the design variable we graphically presented. From the design curves in section 4.3, we are able to qualitatively understand the effect a particular design variable has on some performance aspect of the resonant inverter. It is also possible to visualize the simultaneous effect of more than one design variable and draw qualitative conclusion on how it might affect the converter.

It can also be observed that manipulating a certain design parameter to achieve a desired effect in one aspect of the performance might adversely affect another performance factor. For example increasing the parallel resonant quality factor Q_p, to improve the THD of the HFAC bus voltage will lead to unfavourable efficiency penalties. Whilst the performance curves offer great insights, it is challenging to optimally determine the design parameters to meet competing performance requirements.

In the next few sections we tackle the problem on how the various design parameters should be selected such that a set of desired performance goals are optimal met. To achieve this goal, it is necessary to quantitatively describe the performance goals as well as the physical limitations that constraint the selection of the design variables in a concise mathematical framework. It is certainly possible to derive all the required analytical expression from the equations obtained from the steady state analysis of the resonant inverter. Although accurate, the resulting equations will be complex and mathematically intractable to be physically meaningful. An alternative approach to be explored is to identify possible simplifying assumption that can be reasonably applied to yield solution are mathematically simple and intuitive. This can for example be achieved by neglecting small effects that lead to unnecessary mathematical clutter with only marginal accuracy improvements.

In the next section, a simplified analysis method together with the underlying assumption will be discussed. In section 4.5, a requirement driven approach is proposed to define a set of criteria that constraint the selection of the design variable. Finally computer optimization method will be explored, that enable optimal selection of design parameter for a given set of operation constrains and converter specification.

4.4.1 Simplified Analysis – Sinusoidal Approximation

In this section a simplified analysis of the series parallel tuned high frequency resonant inverter is introduced. The simplified analysis relies on a series of simplifying assumption that allows for relationship between the various circuit performance and design variable to be expressed by a simple set of equations. The fundamental assumption in this analysis is that the resonant tank is tightly tuned around the drive frequency and all frequency component other that the fundamental are sufficiently attenuated. As such, sinusoidal approximation is made, where only the fundamental component of all circuit current and voltages are considered in this analysis. Further simplification is made by ignoring the mosfet r_{ds} on resistance and the equivalent series resistance of the inductors and capacitors used in the circuit. The transformer is assumed to be ideal with zero winding resistance and leakage inductance. The magnetizing inductance is lumped into the parallel resonant inductor. Including these elements in the mathematical analysis yields complex equations that obscure the intuitive relationship between various parameters. The simplified equivalent circuit used in the analysis is shown Figure 4.33.

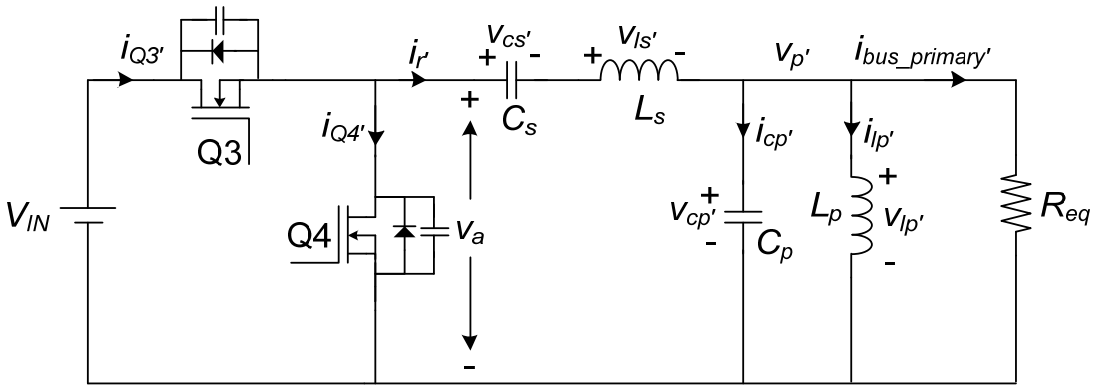


Figure 4.33 : Simplified resonant inverter

4.4.2 Validity of Sinusoidal Approximation

The accuracy consequences of the sinusoidal approximation proposed in the previous section to simplify analysis in investigated. In particular the difference between the true RMS and the RMS value of the fundamental component of the relevant resonant tank current and voltages are identified.

Consider a periodic waveform $x(t)$ with angular frequency ω. $x(t)$ can be expressed as a Fourier series as shown below (4.42)

$$x(t) = X_0 + \sum_{k=1}^{\infty} X_k \sin(n\omega t + \phi_n) \tag{4.42}$$

The RMS value of $x(t)$ expressed in terms of the amplitude of the harmonic component is defined in (4.43), where T is the period of $x(t)$

$$x(t)_{RMS} = \sqrt{X_0^2 + \frac{1}{2}\sum_{k=1}^{\infty} X_k^2} \tag{4.43}$$

The THD of $x(t)$ with no DC component ($X_0 = 0$) can be state as

$$THD = \frac{1}{X_1}\sqrt{\sum_{k=2}^{\infty} X_k^2} \tag{4.44}$$

The ratio of the RMS of the fundamental component of $x(t)$ to the true RMS can be computed form (4.43) and (4.44) and is stated as

$$X_{1\_RMS} = \frac{1}{\sqrt{THD^2 + 1}}\, x(t)_{RMS} \tag{4.45}$$

The more complete analysis accounting for contribution of the harmonic components and other non-idealities to the operation of the inverter as carried out previously in the section 4.3 can now be used to gauge the extend of correlation between the simplified analysis and the more accurate model. From Figure 4.26 and Figure 4.24 it can be seen that for the range of k_p between 1.1 to 1.5, Q_p between 1 to 5 and Q_s between 1 to 5, the maximum THD value of $i_r(t)$ and $v_{bus}(t)$ does not exceed 16% and 12% respectively.

Under the worst case condition within the prescribed domain, using (4.45) it can be shown that the RMS value of the fundamental component of $i_r(t)$ is approximately

98.74% of the true RMS value. Similarly the RMS value of the fundamental component $v_{bus}(t)$ is about 99.28% of the true RMS value. It will be shown later in the following sections that $i_{cp}(t)$, $i_{lp}(t)$, $v_{cp}(t)$ and $v_{cs}(t)$ are all calculated from $i_r(t)$ and $v_{bus}(t)$. It is therefore expected that the RMS value of the fundamental component of these variables will be reasonably close to the true RMS values. This shows that for the ranges of k_p, Q_p and Q_s stated above, the RMS value computed using the sinusoidal approximation method yields results that are very close to the actual values.

4.5 Design Objective

The half bridge switching network will be operated at fixed duty cycle of 50%. This will yield minimum harmonic distortion with only odd harmonic component. The problem now remains in finding values of the tuning factor k_s & k_p and the quality factors Q_s & Q_p for a given set of specification of input voltage V_{IN}, load impedance R_L, HFAC bus voltage v_{bus} and frequency f_{bus}. As the inverter is preceded by a DC-DC converter; the input voltage to the inverter V_{IN} can be controlled and thus can be considered as a variable to be optimized. As the bus voltage is fixed, the transformer turns ratio will depend on V_{IN}, therefore the turns ratio N is also a variable in the optimization process. The selection of these values are limited by a set of design constrains which are described below. In the following analysis the sinusoidal approximation technique introduced in the previous section is employed.

4.5.1 Low Output Impedance

The circuit in Figure 4.33 can be represented as Thevenin equivalent circuit as shown in Figure 4.34. From this representation, it is evident that only when Z_{th} is very small, the resonant inverter approach an ideal voltage source. When Z_{th} is zero, the entire input voltage appears across the load. The Thevenin voltage V_{th} and impedance Z_{th} can be computed using (4.46) and (4.47).

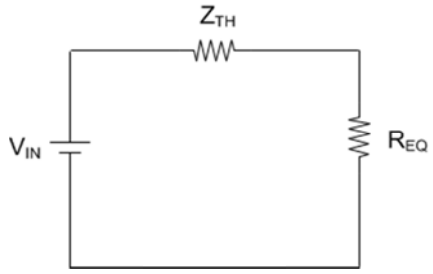


Figure 4.34 : Thevenin equivalent circuit of resonant inverter

$$v_{th} = \frac{Z_{pr'}}{Z_{pr'} + Z_{s'}} v_a \tag{4.46}$$

$$Z_{th} = \frac{Z_{pr'} Z_{s'}}{Z_{pr'} + Z_{s'}} \tag{4.47}$$

Where $Z_{pr'}$ is the unloaded impedance of the parallel branch and $Z_{s'}$ is the impedance of the series branch. Given by (4.48) and (4.49) respectively.

$$Z_{pr'} = \frac{jk_p{}^2 R_{eq} n}{Q_p (k_p{}^2 - n)} \tag{4.48}$$

$$Z_{s'} = jR_{eq} Q_s \left(\frac{n^2 - k_s{}^2}{n} \right) \tag{4.49}$$

The expression for the magnitude of Z_{th} considering only the fundamental component $(n=1)$ is given by (4.50). As k_p, Q_s and R_{eq} cannot equal to zero, the minimum impedance condition is attained when $k_s = 1$.

$$\left| Z_{th} \right| = \frac{k_p{}^2 Q_s R_{eq} \sqrt{(k_s{}^2 - 1)^2}}{\sqrt{(k_p{}^2 - (k_p{}^2 - 1)(k_s{}^2 - 1) Q_p Q_s)^2}} \tag{4.50}$$

In summary, to satisfy the constraint imposed by the requirement of minimum output impedance, condition (4.51) must be met. Referring to Figure 4.21, notice that equation (4.51) also fulfils the requirement for simplified phase angle control of the bus voltage.

$$k_s = 1 \tag{4.51}$$

4.5.2 Soft Switching of Resonant Inverter

The mosfet switching losses are proportional to the switching frequency and can be significant at high frequencies. Therefore it is necessary to ensure that the mosfets are soft switched during the turn ON and OFF transitions. In the resonant inverter, the mosfet current waveform is determined by the impedance of the resonant tank. The resonant tank can appear either resistive, capacitive or inductive depending on the switching frequencies relative to the tank resonant frequency. The 3 modes of operation are considered in further detail below for symmetric duty cycle.

Case I : Operation below the resonant frequency

This mode of operation is characterized by the switching frequency ω_o being lower than the tank resonant frequency ω_r. The resonant tank presents a capacitive impedance to the switching circuits and thus the current waveform leads the voltage. Figure 4.35 shows an ideal switching wave in this condition.

During the turn on transition, the current commutates from the body diode of one mosfet to the mosfet that is being turned ON (D3 → Q4 or D4 → Q3 transition). The mosfet therefore conducts the full resonant current at the turn ON instant leading high instantaneous losses. In addition during the turn ON transition, the mosfet also conducts the reverse recovery current of the diode, further contributing to the losses. The mosfet Cds capacitor charge is also dissipated in the switching device and is not transferred to the load. During the turn OFF transition however, the mosfets are turned OFF when its anti-parallel diode are conducting therefore ZCS is achieved during the turn OFF transition. In summary operation below the resonant frequency generally contributes to high turn ON losses which are difficult to mitigate and consequently leads to poor switching efficiency.

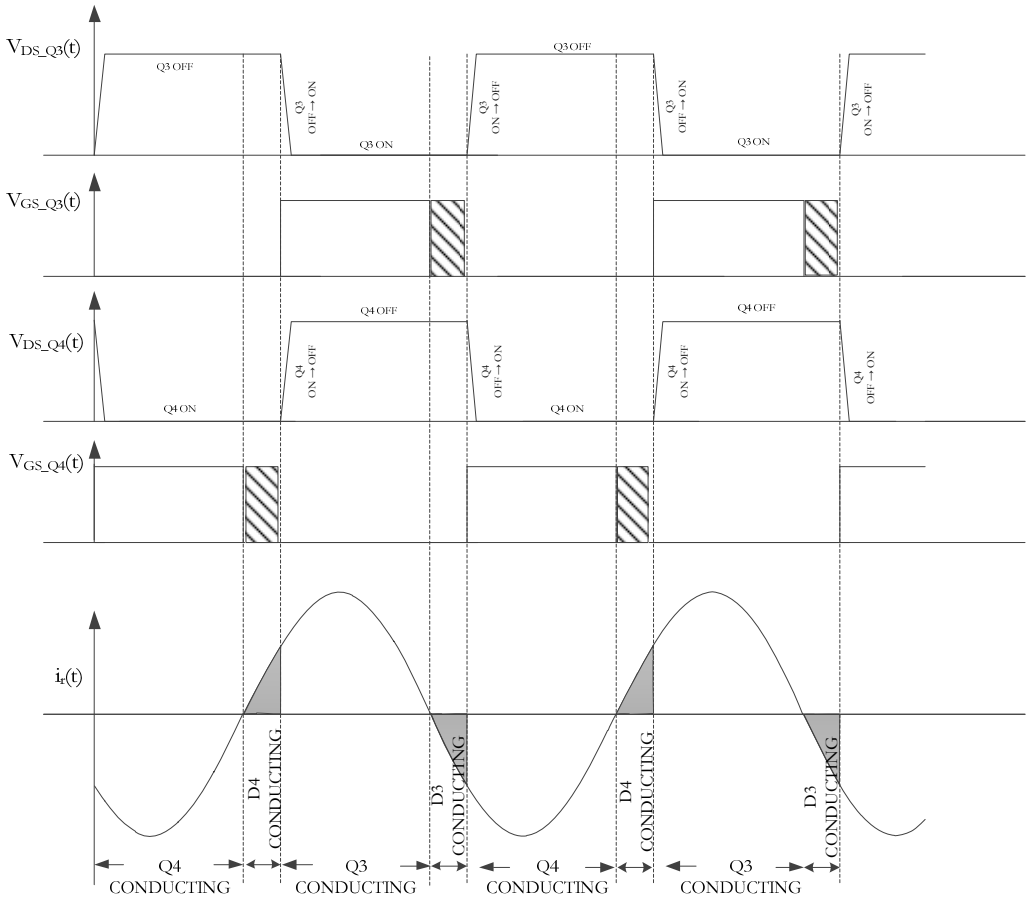


Figure 4.35 : Switching diagram - operation below resonance

Case II : Operation above the resonant frequency

This mode of operation is characterized by the switching frequency ω_o being higher than the tank resonant frequency ω_r. The resonant tank presents an inductive impedance to the switching circuit and thus the current waveform lags the voltage. Figure 4.36 shows an ideal switching waveform in this condition.

During the turn ON transition, the body diode of the mosfet is conducting and therefore the mosfet is turned ON under zero drain to source voltage. The D4 → Q4 or D3 → Q3 transition has a further benefit of eliminating the reverse recovery losses at turn ON. Further the mosfet Cds capacitor charge is transferred to the load and not dissipated in the mosfet. During the turn OFF transition, the mosfet still conducts the tank current and at the same time the drain to source voltage starts to increase. The current and voltage across the mosfet is not simultaneously zero thus losses occur during the turn

OFF transition. However the turn OFF loss can be reduced by slowing the rate of rise of the drain to source voltage of the mosfet when turned OFF. This can be achieved by adding a capacitor across the mosfet. In some cases the mosfet intrinsic Cds capacitance may be sufficient. At the instant of turn OFF, there is short commutation interval where all the mosfets are OFF and thus the tank current starts to charge the drain to source capacitor. If the mosfet turn OFF time is sufficiently fast, then it turns OFF fully before the voltage across its drain to source terminal rises significantly above zero.

Therefore operating above the resonant frequency is a very attractive option with ZVS at the turn ON and OFF transition and consequently leading to very high switching efficiency. The shaded area in Figure 4.36 represents the circulating energy. It is desirable to reduce this area as the circulating current contributes to increase in conduction losses but does not transfer energy to the load [90].

Case III : Operation at the resonant frequency

This mode of operation is characterized by the switching frequency ω_o being equal to the tank resonant frequency ω_r. The resonant tank presents a resistive impedance to the switching circuit and thus the current waveform is in phase the voltage. In this operating mode, as the switching is performed near the current zero crossing points, both the turn ON and turn OFF switching losses are low.

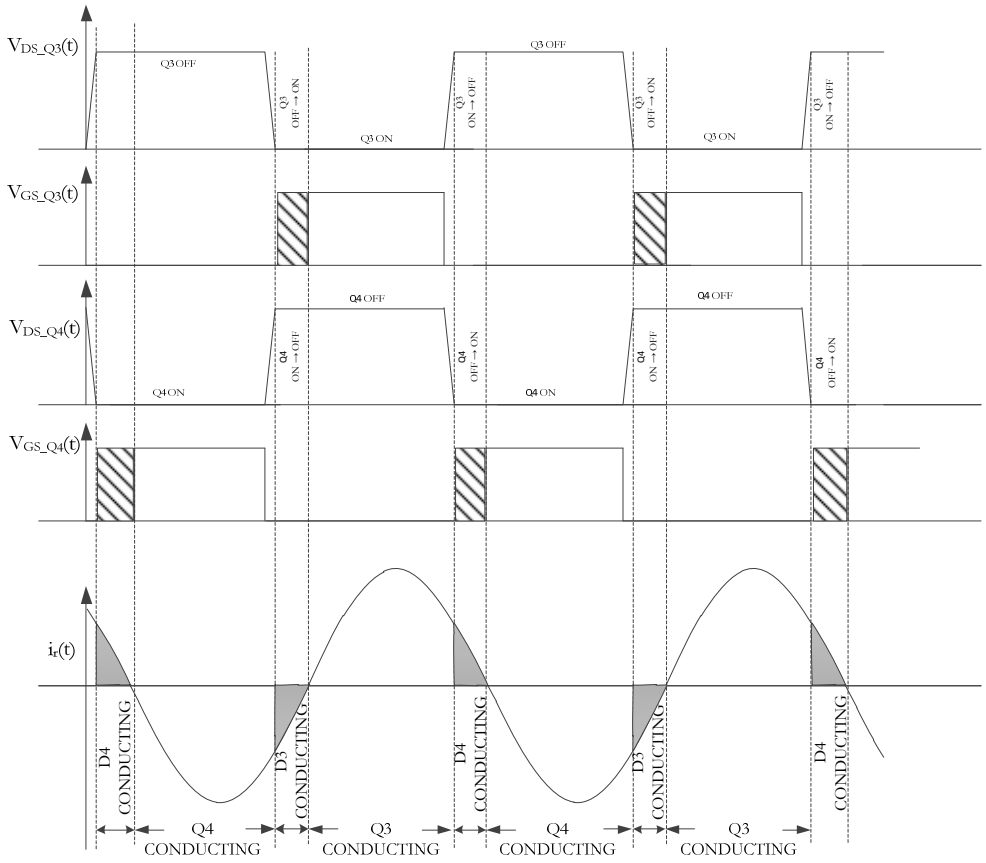


Figure 4.36 : Switching diagram - operation above resonance

Preferred Operating Mode

From the discussion above, it is evident that operating at or above the resonant frequency is attractive from switching efficiency standpoint .However in practice operating at the resonant frequency is not preferred as it may be difficult to tune the resonant tank exactly as inductor and capacitor value normally have large tolerances and come in fixed range of values. Further when the resonant tank is exactly tuned, any capacitance in the load can shift the operating mode to Case I and lead to high losses. It is therefore prudent to ensure operation above the resonant frequency as described in Case II.

This requirement can be captured in a quantitative form by first computing the input impedance of the resonant tank at the switching frequency. The input impedance can be computed using (4.52).

$$Z_{in'} = Z_{p'} + Z_{s'} \tag{4.52}$$

Where $Z_{p'}$ is the impedance of the parallel resonant network given in (4.48) taken in parallel with R_{eq}, and is given in a simplified form in (4.53).

$$Z_{p'} = \frac{nk_p{}^2 R_{eq}}{nk_p{}^2 - jQ_p(k_p{}^2 - n^2)} \tag{4.53}$$

Using (4.49), (4.52) and (4.53) the phase angle of $Z_{in'}$ can be expressed as in (4.54)

$$\angle Z_{in'} = \tan^{-1}\left[\left(\frac{Q_p\left(k_p{}^2 - n^2\right)}{k_p{}^2 n}\right)\left(1 - \frac{\left(k_p{}^2 - n^2\right)\left(k_s{}^2 - n^2\right)Q_p Q_s}{k_p{}^2 n^2}\right) - \frac{Q_s\left(k_s{}^2 - n^2\right)}{n}\right] \tag{4.54}$$

To satisfy the constraint imposed by the requirement for soft switching, inductive resonant tank impedance can be attained when the phase and of Z_{in} is positive. Taking into consideration the condition imposed by (4.51) and using the sinusoidal approximation, (4.54) can be simplified and the requirement for inductive input impedance of the resonant tank can be expressed by (4.55).

$$\tan^{-1}\left[\frac{Q_p\left(k_p{}^2 - 1\right)}{k_p{}^2}\right] > 0 \tag{4.55}$$

In summary, to satisfy the constraint imposed by the requirement of soft switching of mosfets Q3 & Q4 , condition (4.56) needs to be fulfilled

$$k_p > 1 \tag{4.56}$$

4.5.3 Meeting HFAC Bus Voltage Requirement

To compute the output bus voltage, the magnitude of the voltage transfer function of the loaded resonant tank is calculated as in (4.57)

$$\frac{v_{p'}}{v_{a\_AC}} = \left| \frac{Z_{p'}}{Z_{p'} + Z_{s'}} \right| \tag{4.57}$$

Where $v_{p'}$ is the voltage across the primary side of the transformer and v_{a_AC} is the ac component of v_a. The DC component of v_a is blocked by the series capacitor C_s and thus does not appear across the transformer. The expression for v_{a_AC} is given in (4.58).

$$v_{a\_AC} = \sum_{n=1,3,5,....}^{\infty} \frac{\sqrt{2}V_{IN}\sqrt{1-\cos(2\pi nD)}}{n\pi} \sin(n\omega_o t + \phi_n) \tag{4.58}$$

Using (4.51) and considering only the fundamental harmonics, it can be shown that for symmetric duty cycle operation the magnitude of the voltage transfer function of the resonant tank is unity and the phase angle is zero. Therefore the HFAC bus voltage can be expressed as

$$v_{bus} = \frac{2V_{IN}}{N\pi} \sin(\omega_o t) \tag{4.59}$$

In this equation, ω_o is the HFAC bus frequency, and it is equal to the mosfet switching frequency. N represents the transformer turns ratio. In the equivalent circuit used to derive (4.59), the transformer winding resistance and sum of the ESR of the series resonant circuit and mosfet r_{ds} were ignored. In practice, there will be voltage drop across these elements that cause the actual bus voltage to be lower than that predicted by (4.59). The deviation is generally small as the magnitude of the series resistance is normally in the range of not more than a few hundred miliohms, however for large resonant tank current, the actual bus voltage may differ significantly.

4.5.4 Optimizing Resonant Tank Input Current

The input current to the resonant tank i_r, consist of the load current and the circulating current in the resonant tank. For a given bus voltage and output power specification, it is desirable the input current to be as low as possible. The conduction losses in the mosfet and the ESR of C_s and L_s is proportional to the square of the input resonant current. The expression for input resonant current can be computed using (4.60)

$$i_{r'}(t) = \frac{v_{a\_AC}(t)}{Z_{in'}} \tag{4.60}$$

The input impedance of the resonant tank $Z_{in'}$ can be represented in the phasor form with the magnitude given by (4.61) and the phase angle given previously in (4.54)

$$\left|Z_{in'}\right| = \frac{R_{eq}\sqrt{k_p{}^4 n^2 (k_s{}^2 - n^2)^2 Q_s{}^2 + \left(k_p{}^2 n^2 + (k_p{}^2 - n^2)(n^2 - k_s{}^2) Q_s Q_p\right)^2}}{n\sqrt{k_p{}^4 n^2 + (k_p{}^2 - n^2)^2 Q_p{}^2}} \tag{4.61}$$

Using previously obtain result in (4.51) and making further substitution using (4.11) and (4.59) the expression for the input resonant current can be expressed solely as a function of the optimizable variable and design specification. The resulting expression is given below.

$$i_{r'}(t) = \left(\frac{\sqrt{k_p{}^4 + (k_p{}^2 - 1)^2 Q_p{}^2}}{V_{DC}\, k_p{}^2}\right)\left(\pi P_{out}\right)\sin(\omega_o t - \varphi) \tag{4.62}$$

$$\varphi = \tan^{-1}\left[\frac{Q_p\left(k_p{}^2 - 1\right)}{k_p{}^2}\right] \tag{4.63}$$

In summary, to satisfy the constraint imposed by the requirement to minimize the input resonant tank current and consequently reduce conduction losses, it is desirable to minimize the RMS value of (4.62) while meeting other design requirements.

4.5.5 Minimizing Circulating Current

In the parallel branch of the resonant tank there will be circulating current between the inductor L_p and capacitor C_p. This circulating current incurs conduction loss in the ESR of the inductor and capacitor. It is therefore necessary to reduce the RMS value of these currents.

The current flowing into the inductor L_p can be expressed as

$$i_{lp'}(t) = \frac{v_{p'}(t)}{X_{LP}} \tag{4.64}$$

Using equations (4.11), (4.16), (4.51) and (4.59) the fundamental component of the parallel inductor current can be expressed as

$$i_{lp'}(t) = \left(\frac{Q_p}{V_{IN}}\right)(\pi P_{out})\sin\left(\omega_o t - \frac{\pi}{2}\right) \tag{4.65}$$

Similarly the current flowing into the capacitor C_p can be calculated using the following equation.

$$i_{cp'}(t) = \frac{v_{p'}(t)}{X_{CS}} \tag{4.66}$$

Using equations (4.11), (4.17), (4.51) and (4.59), the fundamental component of the parallel capacitor current can be expressed as in (4.67).

$$i_{cp'}(t) = \left(\frac{Q_p}{V_{IN}k_p^{\,2}}\right)(\pi P_{out})\sin\left(\omega_o t + \frac{\pi}{2}\right) \tag{4.67}$$

From (4.65) and (4.67) it can be observed that peak capacitor current is equal to the peak inductor current divided by the square of the parallel tuning ratio. Also both this currents are 180° out of phase.

In summary, to satisfy the constraint imposed by the requirement to minimize the circulating current in the parallel resonant branch, it is necessary to minimize the RMS value of equations (4.65) and (4.67)

4.5.6 Meeting Bus Voltage THD Requirement

The total harmonic distortion on the bus voltage is an important parameter and the maximum tolerable value is often specified as a design requirement. The total harmonic distortion in percentage can be computed using (4.68) for the case where the duty cycle is symmetric.

$$\%THD = \frac{100\sqrt{\sum_{n=3,5,7..}^{\infty} v_{pn'\_rms}{}^2}}{v_{p1'\_rms}} \tag{4.68}$$

Where $v_{pn'\_rms}$ is the RMS value of the nth harmonic component of the primary of the HFAC isolation transformer. The harmonic composition of $v_{p'}$ can be computed using (4.57). The expression for THD given in terms of the optimizable variables and specification parameters is as follows

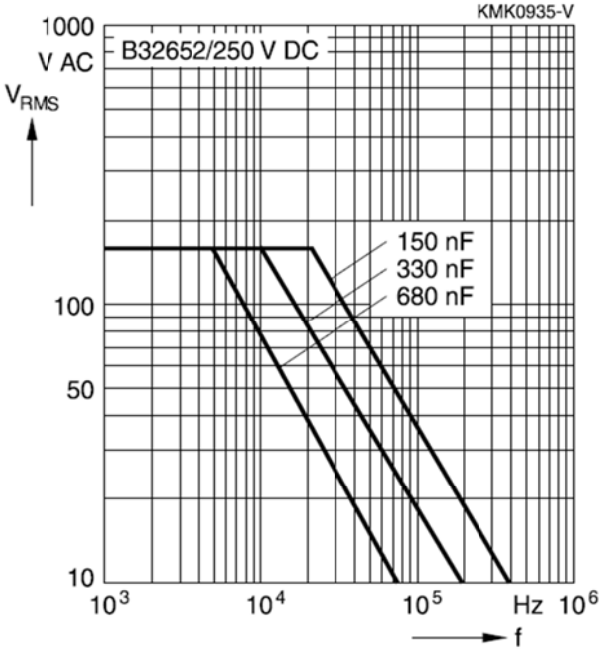
$$THD = 100k_p{}^2\sqrt{\sum_{n=3,5,7..}^{\infty} \frac{n^2}{k_p{}^4 n^2 (n^2-1)^2 Q_s{}^2 + \left(k_p{}^2 n^2 + (k_p{}^2 - n^2)(n^2-1)Q_s Q_p\right)^2}} \tag{4.69}$$

In summary, to satisfy the constraint imposed by the requirement to minimize the total harmonic distortion, it is necessary to minimize equation (4.69).

4.5.7 Minimizing Resonant Capacitor Voltage

Metalized polypropylene film capacitors are often the preferred choice for use in resonant application. Film capacitor have very low dissipation factor and are suitable for high power high frequency application. However the maximum RMS voltage that film capacitors can generally withstand falls quickly as the frequency increases. The rated

voltage rating of film capacitors are normally specified at low frequency typically 1 kHz. A typical RMS voltage vs frequency for metallized polypropylene film capacitor is shown in Figure 4.37.



Specifications			
Part No	B32652A3224K		
Capacitance	220nF		
Rated DC Voltage	250V_{DC}		
Rated AC Voltage	160V_{RMS}		
Dimensions (mm)	W	H	L
	6	11	18
Pitch(mm)	15		
Max dV/dt	200V/μs		
Capacitor type : Metallized Polypropylene Film Capacitors (MKP) *Graph represents permissible AC voltage VRMS versus frequency f (for sinusoidal waveforms, TA ≤90 °C)			

Figure 4.37 : Polypropylene film capacitor voltage vs frequency curve

High voltage stresses may require series connected capacitors to increases the voltage withstanding capability. In the interest to reduce the overall volume of the inverter, it is necessary to minimize the voltage across the capacitor while simultaneously ensuring other performance conditions are satisfied.

The voltage across the series capacitor C_s, can be expressed as

$$v_{cs'}(t) = i_{r'}(t) X_{CS} \tag{4.70}$$

Substituting equations (4.62) and (4.15) into (4.70) and simplifying yield (4.71). Where φ is defined in (4.63).

$$v_{cs'}(t) = \left(\frac{2V_{IN}Q_s}{\pi} \right) \left(\frac{\sqrt{k_p{}^4 + (k_p{}^2 - 1)^2 Q_p{}^2}}{k_p{}^2} \right) \sin(\omega_o t - \varphi - \frac{\pi}{2}) \tag{4.71}$$

The voltage across the parallel capacitor is equal to the voltage on the primary side of the isolation transformer and is given by (4.72)

$$v_{cp'}(t) = \frac{2V_{IN}}{\pi}\sin(\omega_o t) \tag{4.72}$$

In summary, to satisfy the constraint imposed by the requirement to minimize the resonant capacitor voltage stress, it is necessary to minimize equation (4.71) and (4.72).

4.5.8 Estimating Transformer Losses

In this section, we set out to investigate how the design parameters affect the transformer losses. The isolation transformer losses are complex and are difficult to model accurately. In general the losses in the transformer can be classified into core and winding losses. The core losses can be further divided into hysteresis and eddy current loss which are both frequency dependant properties. The winding losses are due to the (i) static copper loss (I^2R), (ii) the eddy current related losses in the winding and (iii) proximity losses which essentially decrease the effective cross section area of the wire.

The total core loss can be approximated by an empirical function of the form shown in (4.73) [90]. This approximation is made on the assumption that the applied waveform is sinusoidal. The loss data for Epcos N87 ferrite core operating at 50kHz at 25°C, 50°C and 80°C is shown in Figure 4.38. Curve fitting using Matlab was performed on the raw data and the resulting equations are also plotted in Figure 4.38.

$$P_{core} = K_{fe}(\Delta B)^{\beta} A_c \ell_m \tag{4.73}$$

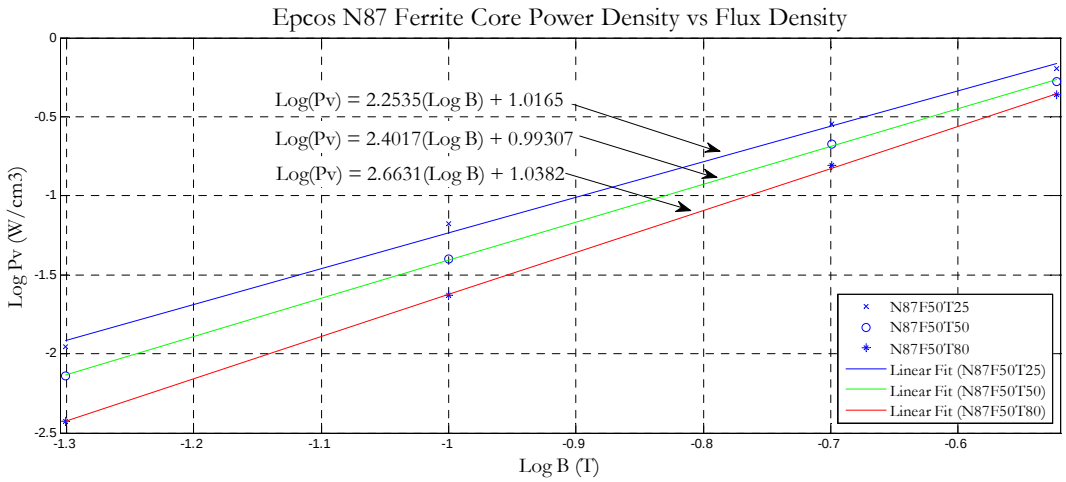


Figure 4.38 : Matlab curve fitting of ferrite core loss data

From the plot above, the value of the K_{fe} and β can be computed and is given in Table 4.4

Core	Frequency	Temperature	K_{fe}	β
Epcos N87	50kHz	25°C	10.387	2.254
		50°C	9.842	2.402
		80°C	10.919	2.663

Table 4.4 : Epcos N87 core loss parameters

The total copper loss in the winding can be calculated using (4.74). This equation accounts for static losses in both the primary and secondary winding. Conduction losses due to proximity and skin effect are not captured by this equation.

$$P_{cu} = \left(\frac{\rho \lambda_1^2 I_{total}^2}{4K_u}\right)\left(\frac{MLT}{W_A A_c^2}\right)\left(\frac{1}{\Delta B}\right)^2 \tag{4.74}$$

The primary voltage sec λ_1 calculated appropriately over the positive region of v_{bus} is given in (4.75)

$$\lambda_1 = N\int v_{bus}\, dt = \frac{2NV_{bus\_peak}}{\omega_0} \tag{4.75}$$

The sum of the RMS winding current I_{total} referred to primary side is computed using (4.76)

$$I_{total} = i_{p\_RMS} + \frac{n_s}{n_p} i_{s\_RMS} = \frac{\sqrt{2} V_{bus\_peak}}{N R_L} \tag{4.76}$$

The total power loss of the transformer can be computed by summing both the core and copper loss as defined by equations (4.73) and (4.74). After some mathematical manipulation the optimal total power loss can be expressed as (4.77). The full derivation can be found in [90].

$$P_{tx\_loss} = \left[A_c \ell_m K_{fe} \right]^{\left(\frac{2}{\beta+2}\right)} \left[\left(\frac{\rho MLT}{K_u W_A A_c^2} \right) \left(\frac{2 P_{out}^2}{\pi^2 f_o^2} \right) \right]^{\left(\frac{\beta}{\beta+2}\right)} \left[\left(\frac{\beta}{2} \right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2} \right)^{\left(\frac{2}{\beta+2}\right)} \right] \tag{4.77}$$

Note that (4.77) is only a function of the selected core material, core geometry, the total load power and the operation frequency. The losses in the transformer are not affected by any of the design parameters, including the turns ratio N. However very large or small values of N may lead to increased leakage inductance.

4.5.9 Estimation of RDS ON & ESR

To calculate the total conduction losses, it is necessary to estimate the mosfet r_{ds} ON resistance and the capacitor and inductor ESR. The r_{ds} ON resistance generally increases exponentially with increase in the V_{DS} rating of the mosfet. In Figure 4.39 the r_{ds} ON resistance vs V_{DS} rating of several commercial mosfets is shown. Curve fitting techniques are used to find a mathematical relationship between ON resistance and voltage rating.

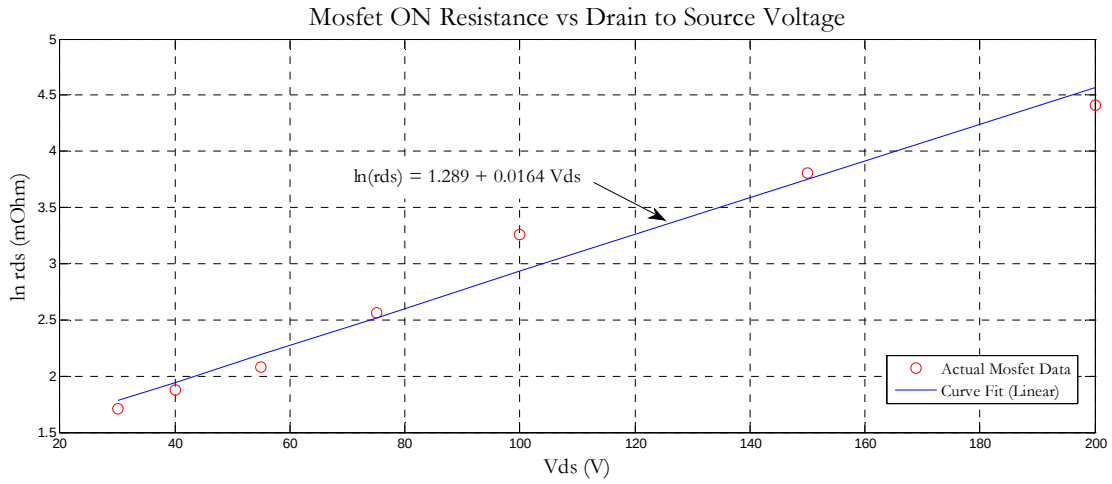


Figure 4.39 : Typical mosfet on resistance vs drain to source voltage curve

The relationship is given in equation (4.78), the r_{ds} ON value is expressed in mΩ and the V_{DS} in Volts.

$$r_{ds} = 3.6292e^{0.0164\,V_{DS}} \tag{4.78}$$

In a similar fashion, the DC resistance vs inductance curve for commercially available power inductors rated to handle the range of current expected in the resonant inverter circuit is shown in Figure 4.40.

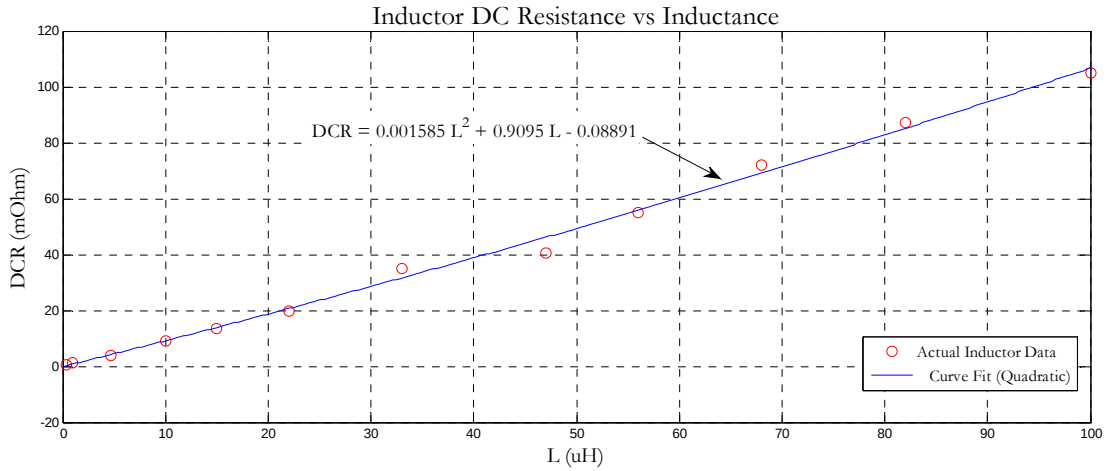


Figure 4.40 : Inductor DCR vs inductance curve

The relationship between the DCR and inductance can be expressed as in (4.79), where L is the inductance in μH and DCR is the resistance in mΩ.

$$DCR = 0.001585L^2 + 0.9095L - 0.08891 \tag{4.79}$$

The film capacitors used in the resonant circuit generally have very low ESR. Figure 4.41 show the typical ESR value for polypropylene film capacitor vs frequency of operation. From this curve, it can be observed that the ESR between frequency ranges of 10kHz to 100kHz is below 10mΩ. A conservative value of 20mΩ shall be used in the optimization process in the next section.

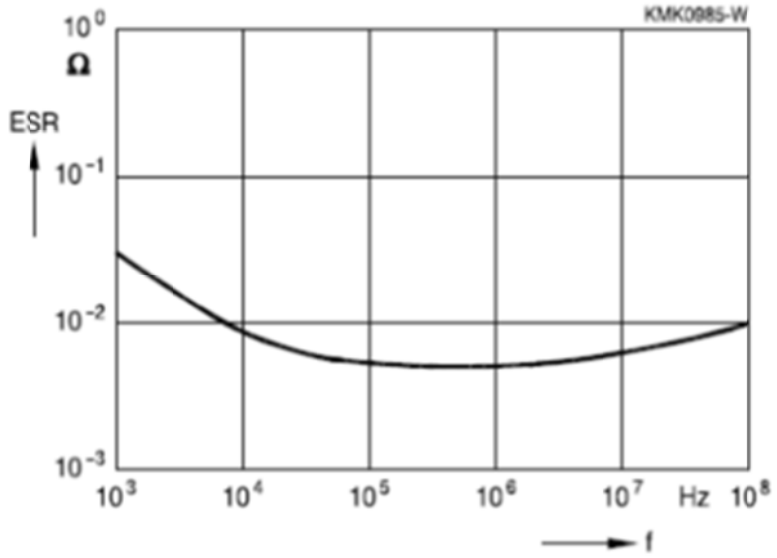


Figure 4.41 : Film capacitor ESR curve (extracted from Epcos datasheet)

4.6 Optimization

Using the constraints derived in the previous section, optimal design parameters that satisfy a set of desired objective functions can be found by using computer optimization. A computer program developed in Matlab was used in the optimization process. Firstly, the value of the objective function is computed for a range design parameters within a prescribed domain. Next from the computed data set, a subset consisting of all operating conditions that meet or exceed the desired requirements are selected. Table 4.5 summarized that data used for in the optimization process.

Converter Operating Specification			
Parameter		**Notation**	**Value**
HFAC Bus Voltage (RMS)		V_{bus}	100V
HFAC Bus Frequency		f_{bus}	50kHz
HFAC Bus Output Power		P_{out}	100W
Design Parameters			
Parameter	**Notation**	**Range**	**Step Size**
Parallel Tuning Factor	k_p	1.1 – 1.6	0.1
Input DC Voltage	V_{DC}	12V -104V	4V
Parallel Tuned Quality Factor	Q_p	1 - 5	0.2
Series Tuned Quality Factor	Q_s	1 - 5	0.2
Objective Function			
Parameter		**Notation**	**Condition**
Efficiency		η	> 97%
THD HFAC Bus Voltage		THD	< 4%
Series Capacitor RMS Voltage		v_{cs_RMS}	< 50V
Parallel Capacitor RMS Voltage		v_{cp_RMS}	< 40V

Table 4.5 : Resonant inverter optimization parameters

The efficiency in Table 4.5 is calculated considering only conduction losses. As the inverter is soft switched, the switching losses are assumed to be negligible. The efficiency is calculated using (4.80).

$$\eta = \frac{100 P_{out}}{P_{out} + P_{loss}} \tag{4.80}$$

Where P_{out} is the converter output power specification as given in Table 4.5. P_{loss} is calculated as shown in (4.81).

$$P_{loss} = i_{r\_RMS}^2 (r_{ds} + r_{cs} + r_{ls}) + i_{lp\_RMS}^2 (r_{lp}) + i_{cp\_RMS}^2 (r_{cp}) + P_{xmer} \tag{4.81}$$

Where P_{xmer} is total losses in the isolation transformer and is calculated using (4.77) for a preselected core geometry. The values of the mosfet r_{ds} and ESR of the inductor and capacitor is estimated as described in the previous section. An Additional 1W was added

to account for other losses such as inductor core loss and transformer proximity and skin effect losses.

4.6.1 Optimization Results

The result of the optimization process is given in Table 4.6 and Table 4.7. Based on the design parameters, the values of the resonant components can be computed using equations (4.82) to (4.85). The calculated physical component values are; L_s = 59.94uH, C_s = 169.03nF, L_p = 35.68uH and C_p = 234.69nF.

Design Parameter	**Notation**	**Value**
Parallel Tuning Ratio	k_p	1.1
Series Tuning Ratio	k_s	1.0
Parallel Tuned Quality Factor	Q_p	1.4
Series Tuned Quality Factor	Q_s	1.2
Input DC Voltage	V_{IN}	88 V
Transformer Turns Ratio	N	0.3961

Table 4.6 : Optimization results - design parameters

Performance Parameter	**Notation**	**Value**
Tank Input Resonant Current	i_{r_RMS}	2.60 A_{RMS}
Parallel Inductor Current	i_{lp_RMS}	3.53 A_{RMS}
Parallel Capacitor Current	i_{cp_RMS}	2.92 A_{RMS}
Series Capacitor Voltage	v_{cs_RMS}	48.92 V_{RMS}
Parallel Capacitor Voltage	v_{cp_RMS}	39.61 V_{RMS}
Efficiency	η	97.15%
Total Harmonic Distortion	THD	3.69%

Table 4.7 : Optimization results - performance parameters

$$L_s = \left(\frac{2}{\pi^2} \frac{Q_s}{\omega_o} \frac{V_{IN}^2}{P_{out}} \right) \tag{4.82}$$

$$C_s = \left(\frac{\pi^2}{2} \frac{1}{\omega_o k_s^2 Q_s} \frac{P_{out}}{V_{IN}^2} \right) \tag{4.83}$$

$$L_p = \left(\frac{2}{\pi^2} \frac{1}{\omega_o Q_p} \frac{V_{IN}^2}{P_{out}} \right) \tag{4.84}$$

$$C_p = \left(\frac{\pi^2}{2} \frac{Q_p}{\omega_o k_p^2} \frac{P_{out}}{V_{IN}^2} \right) \tag{4.85}$$

4.7 Concluding Remarks

In this chapter, the complex relationship between the various design parameters of the resonant inverter and the circuit current and voltage variables were derived based on exact mathematical modelling. It was then shown that the resulting model agrees well with circuit simulation. However, whilst accurate, the mathematical complexity obscures the relationship between the design and performance parameters. The proposed simplifying assumptions and the requirement driven approach presented in this chapter leads to simplified models that can be easily and efficiently optimized to yield designs that meet prescribed performance goals. Finally as a result of the optimization process, the requirement for the first stage DC-DC converter is determined.

CHAPTER 5

MULTI STAGE INVERTER DESIGN & VALIDATION

"The truth is ever to be found in the simplicity, and not in the multiplicity and confusion of things" - ***Isaac Newton, 1642-1727.***

The optimization of the second stage resonant inverter of a MSI as covered in the previous chapter dictates the operating requirement for the first stage DC-DC converter. In this chapter, a zero voltage resonant transition boost converter is proposed as a suitable option. Steady state analysis and small signal modelling of the converter is undertaken to determine operating points and transient behaviour of the converter. Additionally, a digital controller is proposed to implement the control function of a two stage HFAC resonant inverter. It is demonstrated that phase synchronization of the inverter can be implemented easily with this approach and thus is an attractive option for parallel operation of HFAC inverters. The parallel operation capability of HFAC inverters enable a flexible and scalable HFAC DPS to be realized. Finally a prototype HFAC MSI was constructed and experimental measurements are presented.

5.1 Design of Front End DC-DC Converter

The front end DC-DC converter enables independent control of the HFAC bus output voltage. The primary purpose of the DC-DC converter can be viewed as a means to deliver a fixed amount of power ($P_{DC-DC} = P_{out}$) at a suitable voltage to the second stage resonant inverter. In the previous sections, it has been demonstrated that a higher input voltage to the resonant inverter stage will result in higher efficiency. Therefore for the DC-DC converter to deliver a fixed amount of output power at a higher voltage will require less load current and subsequently less transistor and inductor current and potentially higher efficiency.

Based on the optimization process of the resonant inverter, it has been identified that an input voltage of 88V DC will be required to meet the requirements set out in Table 4.5. Therefore the front end DC-DC converter will require a boost converter to convert the input voltage of $42V_{DC}$ to $88V_{DC.}$ A zero voltage resonant transition (ZVRT) boost converter is proposed as a suitable front end DC-DC converter. In a ZVRT converter, the inductor current has large ripple and the current is allowed to flow in the reverse direction. This presents the opportunity to turn ON the mosfets under zero voltage condition. Turns off losses are minimized by using a capacitor across the mosfet to slow down the rate of rise of V_{DS}. Diode reverse recovery losses are eliminated in the ZVRT boost converter and the use of the synchronous diode reduces the conduction losses.

5.2 Steady State Modelling of ZVRT Boost Converter

A simplified circuit of the synchronous boost converter is shown in Figure 5.1. Mosfet Q1 and Q2 are assumed to be ideal with exceedingly small transition time. Therefore no dead time is modelled and subsequently the resonant switching transition due to the interaction between the boost inductor and the soft switching capacitor C_{ss} is ignored. Mosfets Q1 and Q2 are switched on in a complementary fashion. The 2 modes of operation of the circuit are shown in Figure 5.2 (a) and (b). The former represented the state where Q1 is ON and Q2 is OFF (state 1) and latter with Q2 ON and Q1 OFF (state 2).

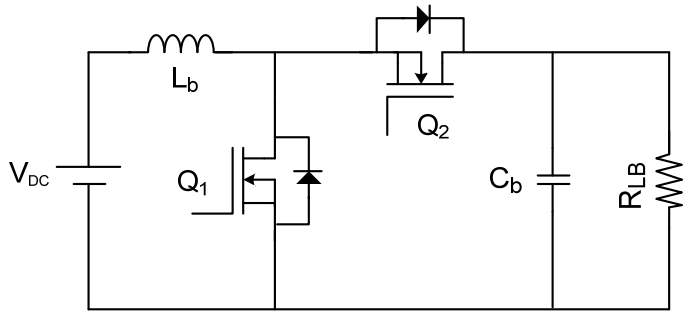


Figure 5.1 : Simplified ZVRT synchronous boost converter

In steady state it is assumed that the output voltage of the converter is fairly constant and therefore the small ripple approximation is employed. However this assumption cannot be applied to the inductor current. The inductor volt-sec and capacitor charge balance principle is used to derive steady state operating parameters.

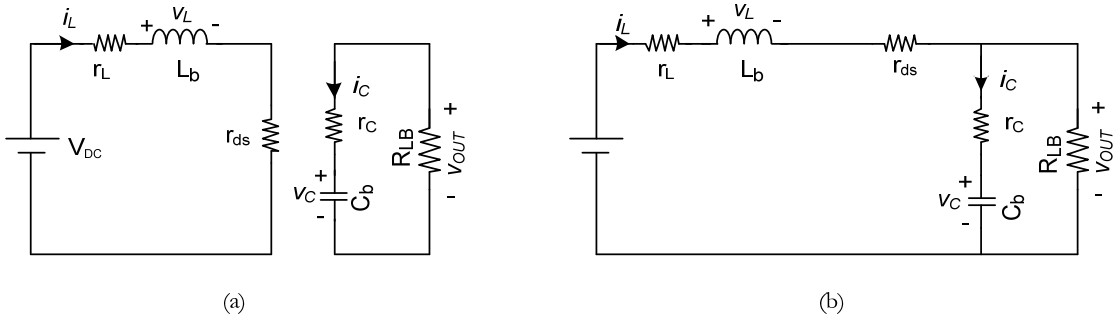


Figure 5.2 : Steady state modes of operation of ZVRT synchronous boost converter

The expression for the inductor voltage and capacitor current in state 1 derived based on the equivalent circuit in Figure 5.2 (a) is given as

$$v_L(t) = V_{DC} - i_L(t)\left[r_L + r_{ds}\right] \tag{5.1}$$

$$i_C(t) = \frac{-V_{OUT}}{R_{LB}} \tag{5.2}$$

Similarly, the expression for state 2 based on Figure 5.2 (b) is given as

$$v_L(t) = V_{DC} - V_{OUT} - i_L(t)\left[r_L + r_{ds}\right] \tag{5.3}$$

$$i_C(t) = i_L(t) - \frac{V_{OUT}}{R_{LB}} \tag{5.4}$$

Applying the voltage-sec balance principal to the inductor voltage as shown in (5.5) an expression for the average inductor current is obtained (5.6).

$$\int_0^{T_s} v_L(t)dt = \int_0^{DT_s} v_L(t)dt + \int_{DT_s}^{T_s} v_L(t)dt = 0 \tag{5.5}$$

Simplifying (5.5) yields

$$\frac{1}{T_s}\int_0^{T_s} i_L(t) = \langle I_L \rangle = \frac{V_{DC} - V_{OUT}(1-D)}{(r_L + r_{ds})} \tag{5.6}$$

Applying the charge balance principal to the capacitor current (5.7) and simplifying yields (5.8)

$$\int_0^{T_s} i_C(t)dt = \int_0^{DT_s} i_C(t)dt + \int_{DT_s}^{T_s} i_C(t)dt = 0 \tag{5.7}$$

$$\int_{DT_s}^{T_s} i_L(t) = \frac{V_{OUT}T_s}{R_{LB}} \tag{5.8}$$

When the value of the inductor resistance r_L and the mosfet ON resistance r_{ds} are small, the inductor current resembles a triangular waveform as shown in Figure 5.3. From the figure, the average inductor current can be expressed as in (5.9)

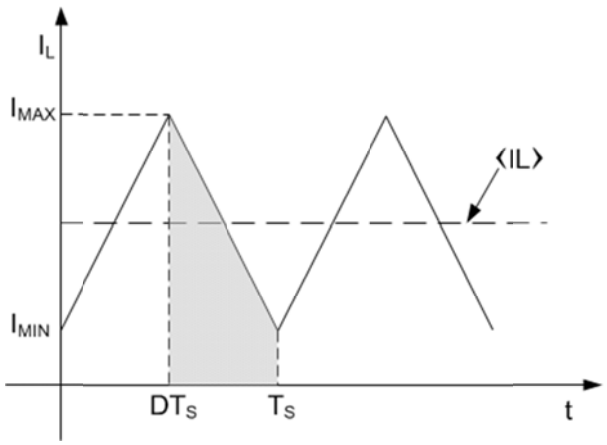


Figure 5.3 : Inductor current waveform

$$\langle I_L \rangle = \frac{I_{LMAX} + I_{LMIN}}{2} \tag{5.9}$$

The inductor voltage waveform is shown in Figure 5.4. Replacing the value of $i_L(t)$ in (5.1) and (5.3), with the average inductor current (5.6), $v_L(t)$ can be approximated to resemble the dotted waveform. This assumption is reasonable so as long as the difference between $I_{LMAX}(r_L + r_{ds})$ and $I_{LMIN}(r_L + r_{ds})$ is small.

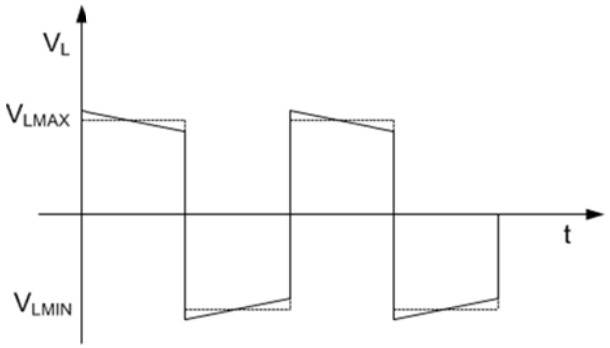


Figure 5.4 : Inductor voltage waveform

The expression for V_{LMAX} and V_{LMIN} can be computed using (5.1), (5.3) and (5.6) and is given as

$$V_{LMAX} = V_{OUT}(1-D) \tag{5.10}$$

$$V_{LMIN} = -DV_{OUT} \tag{5.11}$$

Computing the area of the shaded section in Figure 5.3 and equating it to (5.8) an alternate expression for the average inductor current results as shown in (5.12)

$$\langle I_L \rangle = \frac{V_{OUT}}{R_{LB}(1-D)} \tag{5.12}$$

The voltage gain of the converter can be calculated by equating (5.12) and (5.6) and the resulting expression is given in (5.13)

$$\frac{V_{OUT}}{V_{DC}} = \frac{1-D}{\frac{(r_L + r_{ds})}{R_{LB}} + (1-D)^2} \tag{5.13}$$

The capacitor current waveform is shown in Figure 5.5. With triangular inductor current waveform and using (5.2) and (5.4) the expression for I_{C_PEAK1}, I_{C_PEAK2} and I_{CMIN} is given below in (5.14) to (5.16)

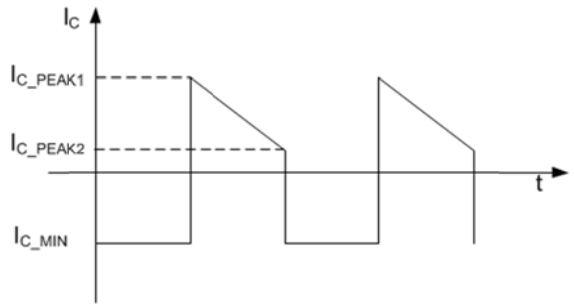


Figure 5.5 : Capacitor current waveform

$$I_{C\_PEAK1} = I_{LMAX} - \frac{V_{OUT}}{R_{LB}} \tag{5.14}$$

$$I_{C\_PEAK2} = I_{LMIN} - \frac{V_{OUT}}{R_{LB}} \tag{5.15}$$

$$I_{CMIN} = -\frac{V_{OUT}}{R_{LB}} \tag{5.16}$$

The peak to peak capacitor ripple voltage can be computed from Figure 5.5 and equation (5.16) and is given as (5.17). This equation can be used to select a suitable C_b value.

$$\Delta V_{r\_pp} = \frac{V_{OUT}}{R_{LB} C_b} D T_s \tag{5.17}$$

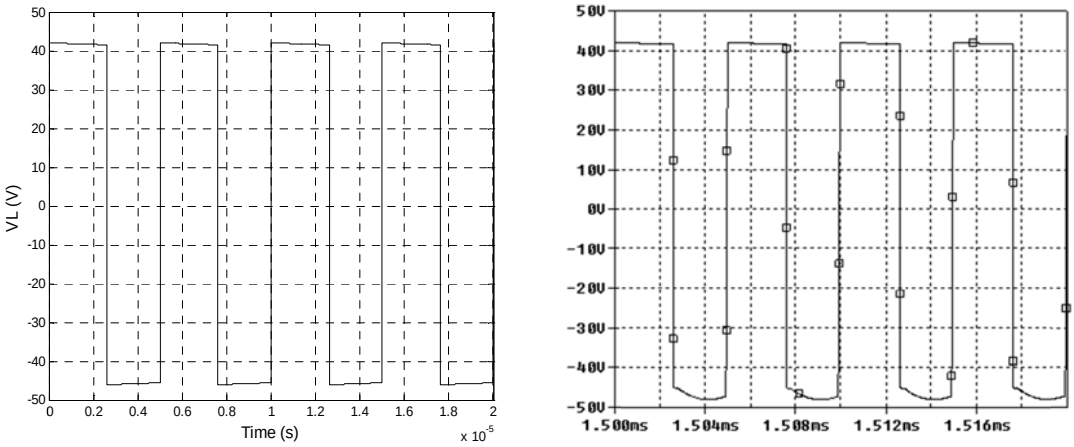
To enable soft turn ON of mosfets Q1 and Q2, the value of I_{LMIN} should be negative. The expression for I_{LMIN} is given in (5.18).

$$I_{LMIN} = V_{OUT}\left[\frac{1}{R_{LB}(1-D)} - \frac{(1-D)DT_s}{2L_b}\right] \tag{5.18}$$

Solving the inequality $I_{LMIN} < 0$, the constraint imposed on the value of the boost inductor is stated as follows

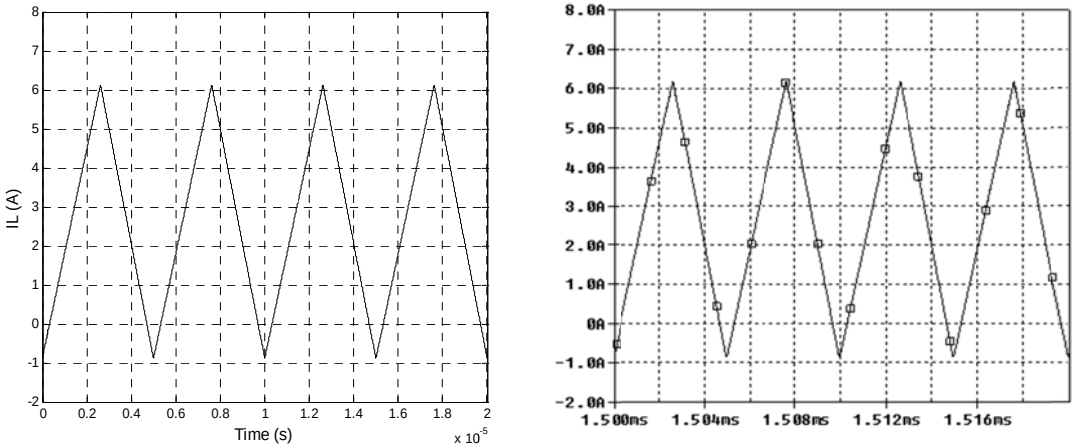
$$L_b < \frac{(1-D)^2 DT_s R_{LB}}{2} \tag{5.19}$$

The inductor current and voltage waveform based on the mathematical modelling is compared with simulation results and are found to be in good agreement. Figure 5.6 to Figure 5.9 below show the comparison between the two.



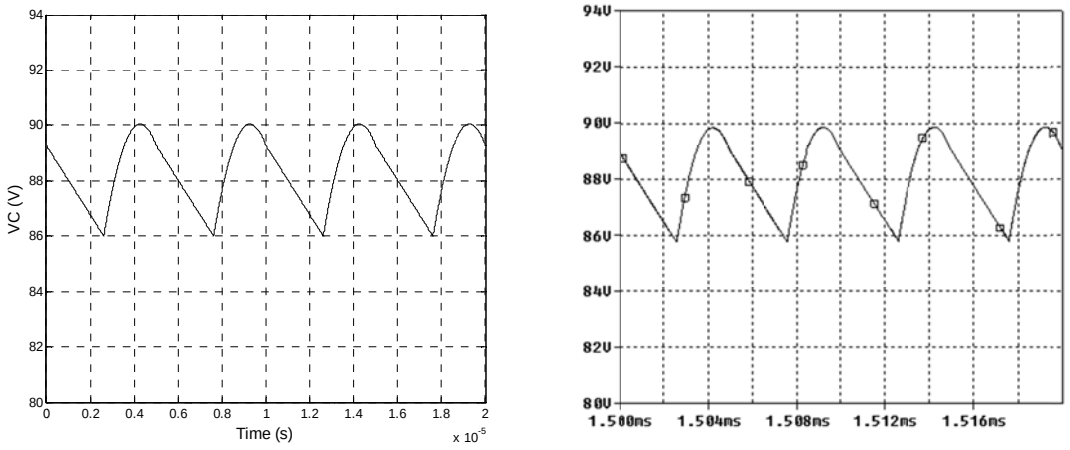
(a) (b)

Figure 5.6 : Boost inductor voltage waveform (a) analytical (b) P-SPICE



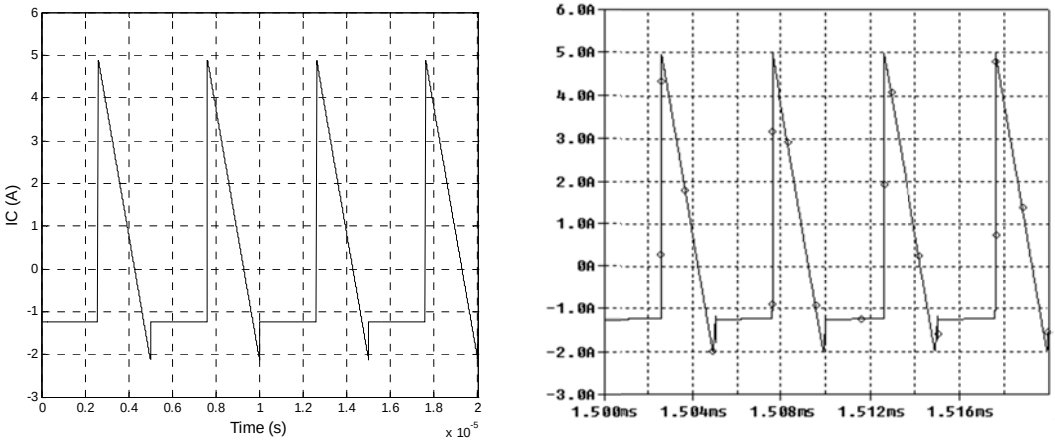
(a) (b)

Figure 5.7 : Boost inductor current waveform (a) analytical (b) P-SPICE



(a) (b)

Figure 5.8 : Boost capacitor ripple voltage waveform (a) analytical (b) P-SPICE



(a) (b)

Figure 5.9 : Boost capacitor ripple current waveform (a) analytical (b) P-SPICE

5.3 Small Signal Modelling of ZVRT Boost Converter

The sampled data modelling technique [91] is used to obtain the small signal model of the converter. One complete switching cycle extending from time t_0 to t_4 is shown in Figure 5.10. The equivalent circuit from time t_0 to t_1 and t_2 to t_3 is shown in Figure 5.2 (a) and (b) respectively. The interval t_1 to t_2 and t_3 to t_4 represents the dead time and is included in the modelling process to improve accuracy. During this interval the body diode of the mosfet conducts the inductor current. The equivalent circuit during the dead time interval is shown in Figure 5.11 (a) and (b).

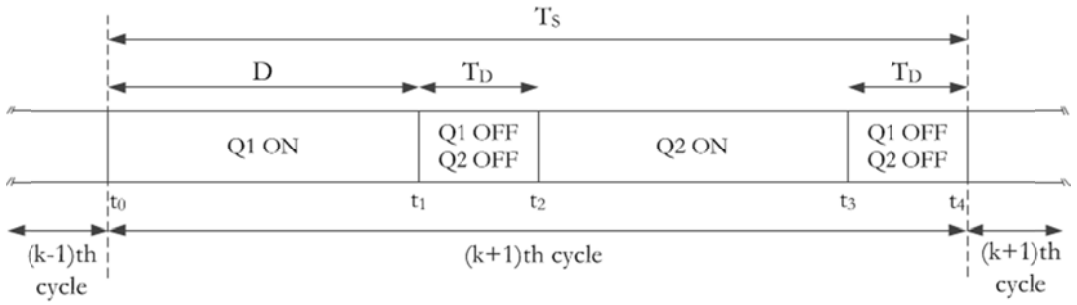


Figure 5.10 : ZVRT boost switching cycle

Using the equivalent circuit, state space equation of the form shown in (5.20) is derived for each of the 4 operating states. $x(t)$ is the state vector consisting of the inductor current $i_L(t)$ and capacitor voltage $v_C(t)$. The output vector $y(t)$ in this case simply consist of the load voltage $v_{out}(t)$.

$$\dot{x}(t) = A_i x(t) + B_i u(t)$$
$$y(t) = C_i x(t) + D_i u(t) \qquad (5.20)$$

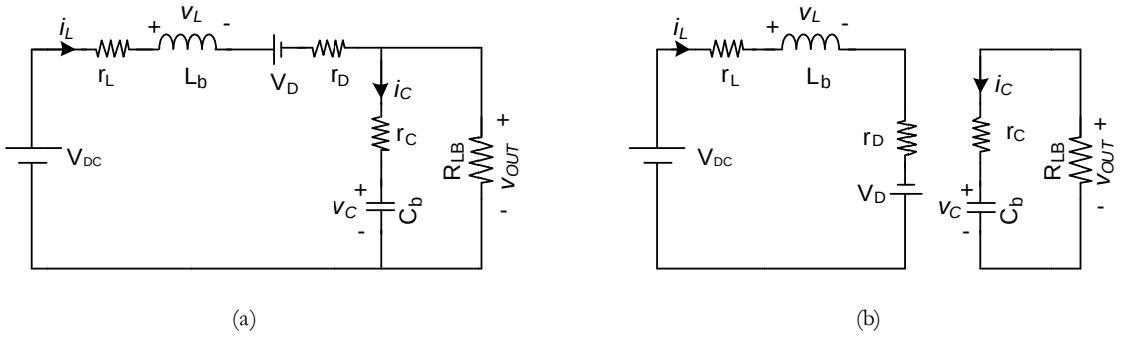


Figure 5.11 : Equivalent circuit during dead time

The matrix $A, B, C \,\&\, D$ for each state of the switching cycle is given in (5.21) to (5.24). The state vector, input vector and output vectors are given in (5.25).

A MATRIX

$$A_1=\begin{pmatrix}\left(-\frac{(r_L+r_{ds})}{L_b}\right) & 0\\ 0 & -\left(\frac{1}{C_b(r_C+R_{LB})}\right)\end{pmatrix};\ A_2=\begin{pmatrix}-\left(\frac{r_L+r_D}{L_b}+\frac{r_C R_{LB}}{L_b(r_C+R_{LB})}\right) & -\left(\frac{R_{LB}}{L_b(r_C+R_{LB})}\right)\\ \left(\frac{R_{LB}}{C_b(r_C+R_{LB})}\right) & -\left(\frac{1}{C_b(r_C+R_{LB})}\right)\end{pmatrix}$$

$$A_3=\begin{pmatrix}-\left(\frac{r_L+r_{ds}}{L_b}+\frac{r_C R_{LB}}{L_b(r_C+R_{LB})}\right) & -\left(\frac{R_{LB}}{L_b(r_C+R_{LB})}\right)\\ \left(\frac{R_{LB}}{C_b(r_C+R_{LB})}\right) & -\left(\frac{1}{C_b(r_C+R_{LB})}\right)\end{pmatrix};\ A_4=\begin{pmatrix}\left(-\frac{(r_L+r_D)}{L_b}\right) & 0\\ 0 & \left(\frac{-1}{C_b(r_C+R_{LB})}\right)\end{pmatrix} \quad (5.21)$$

B MATRIX

$$B_1=\begin{pmatrix}\left(\frac{1}{L_b}\right) & 0\\ 0 & 0\end{pmatrix};\ B_2=\begin{pmatrix}\left(\frac{1}{L_b}\right) & -\left(\frac{1}{L_b}\right)\\ 0 & 0\end{pmatrix};\ B_3=\begin{pmatrix}\left(\frac{1}{L_b}\right) & 0\\ 0 & 0\end{pmatrix};\ B_4=\begin{pmatrix}\left(\frac{1}{L_b}\right) & \left(\frac{1}{L_b}\right)\\ 0 & 0\end{pmatrix} \quad (5.22)$$

C MATRIX

$$C_1=\begin{pmatrix}0 & \left(\frac{R_{LB}}{(r_C+R_{LB})}\right)\end{pmatrix};\quad C_2=\begin{pmatrix}\left(\frac{r_C R_{LB}}{r_C+R_{LB}}\right)\left(\frac{R_{LB}}{r_C+R_{LB}}\right)\end{pmatrix}$$

$$C_3=\begin{pmatrix}\left(\frac{r_C R_{LB}}{r_C+R_{LB}}\right)\left(\frac{R_{LB}}{r_C+R_{LB}}\right)\end{pmatrix};\ C_4=\begin{pmatrix}0 & \left(\frac{R_{LB}}{(r_C+R_{LB})}\right)\end{pmatrix} \quad (5.23)$$

D MATRIX

$$D_1=\begin{pmatrix}0 & 0\end{pmatrix};\quad D_2=\begin{pmatrix}0 & 0\end{pmatrix};\quad D_3=\begin{pmatrix}0 & 0\end{pmatrix};\quad D_4=\begin{pmatrix}0 & 0\end{pmatrix} \quad (5.24)$$

STATE VECTOR, INPUT VECTOR & OUTPUT VECTOR

$$x(t)=\begin{pmatrix}i_L(t)\\ v_C(t)\end{pmatrix};\ u(t)=\begin{pmatrix}V_{DC}\\ V_D\end{pmatrix};\ y(t)=\begin{pmatrix}v_{out}(t)\end{pmatrix} \quad (5.25)$$

Table 5.1 : State space equations for ZVRT boost converter

5.3.1 Sampled Data Modelling Procedure Summary

Although the technique is mathematically complicated, it offers a more accurate model compared to the averaging technique. A brief procedural description of the sampled data modelling technique as related to the analysis of proposed circuit is given below. However interested readers are referred to [91] for a more rigorous treatment of the underlying concepts

Fundamentally, integrating (5.20) it can be shown that the state vector $x(t_n)$, at time t_n can be expressed in terms of $x(t_{n-1})$, the state variable at a previous time t_{n-1}. The resulting equation is given as

$$x(t_n) = \phi_n(t_n - t_{n-1})x(t_{n-1}) + \Delta_n(t_n - t_{n-1}) \tag{5.26}$$

Where $\phi_n(t_n - t_{n-1})$ and $\Delta_n(t_n - t_{n-1})$ are defined as follows

$$\phi_n(t_n - t_{n-1}) = e^{A_n(t_n - t_{n-1})} \tag{5.27}$$

$$\Delta_n(t_n - t_{n-1}) = \int_{t_{n-1}}^{t_n} \phi_n(t_n - \tau)B_n u_k(\tau)d\tau \tag{5.28}$$

Applying (5.26) for each interval in the switching cycle and using the obtained results in the next interval, the state vector at the beginning of the $(k+1)^{th}$ cycle can be expressed in the form shown in (5.29) where F and g are both matrices. In the case of the ZVRT boost converter with 4 transition interval, this can be shown to be equal to (5.30).

$$x_{k+1} = F(p_k, T_k)x_k + g(p_k, T_k) \tag{5.29}$$

$$\begin{aligned} x_{k+1} = &\left[\phi_4(t_4 - t_3)\phi_3(t_3 - t_2)\phi_2(t_2 - t_1)\phi_1(t_1 - t_0)\right]x_k \\ &+ \begin{bmatrix} \phi_4(t_4 - t_3)\phi_3(t_3 - t_2)\phi_2(t_2 - t_1)\Delta_1(t_1 - t_0) \\ \quad + \phi_4(t_4 - t_3)\phi_3(t_3 - t_2)\Delta_2(t_2 - t_1) \\ \quad + \phi_4(t_4 - t_3)\Delta_3(t_3 - t_2) + \Delta_4(t_4 - t_3) \end{bmatrix} \end{aligned} \tag{5.30}$$

In addition to the system matrices, to compute (5.30), it is necessary to know the transition times and the input vector. In the effort to generalize and formally capture these information, it is first necessary to identify all independent control parameters and sources. For this particular case, the independent control parameter vector p_k is given in (5.31) where D is the duty cycle, T_s is the period of the switching cycle, T_d is the dead time, V_{DC} is the input voltage, V_D is the body diode forward voltage and finally R_L is the load impedance.

$$p_k = \begin{pmatrix} D \\ T_s \\ T_d \\ V_{DC} \\ V_D \\ R_{LB} \end{pmatrix} \tag{5.31}$$

The switching interval in the k^{th} cycle is represented in a relative transition time vector T_k as shown in (5.32). In a broader context, the transition time can depend either on external control parameter or be implicitly determined by the system state.

$$T_k = \begin{pmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{pmatrix} \tag{5.32}$$

A set of constraint equations in the form shown in (5.33) is used to relate the transition time to the controlling parameters and the state vector. In this case however all the transition times are determined explicitly by control parameters and the constraint equation are shown in (5.34).

$$C(p_k, T_k)x_k + d(p_k, T_k) = 0 \tag{5.33}$$

$$\begin{aligned} t_1 - p_{k1}p_{k2} &= 0 \\ t_2 - (p_{k1}p_{k2} + p_{k3}) &= 0 \\ t_3 - (p_{k2} - p_{k3}) &= 0 \\ t_4 - p_{k2} &= 0 \end{aligned} \tag{5.34}$$

The computed transition time from (5.34) can be used in (5.30) to compute the state vector at the beginning of the next cycle and this effectively gives the exact large signal description of the circuit. The steady values for x can be found by substituting the steady state p and T matrix into (5.29) until the condition $x_k = x_{k+1}$ is met.

The auxiliary output variable as defined in (5.20) can be expressed in the form shown in (5.35). In this particular case, the output quantity of interest is the average output voltage. The average output voltage is computed by integrating the output equation in (5.20) for each transition and finally dividing by the period of the switching cycle. The matrices H and m are computed by substituting (5.26) for each transition interval.

$$y_k = H(p_k, T_k)x(t_k) + m(p_k, T_k) \tag{5.35}$$

To obtain the dynamic model, small perturbations are introduced to the various system variables and the behaviour of the system is then analysed. The perturbation is represented as the difference between the value at the k^{th} cycle and the expected steady state value and it is shown in (5.36).

$$\begin{aligned} \widetilde{x_k} &= x_k - x \\ \widetilde{p_k} &= p_k - p \\ \widetilde{T_k} &= T_k - T \end{aligned} \tag{5.36}$$

Substituting (5.36) into the large signal model (5.29), (5.33) and (5.35) and using Taylor series linearization techniques the small signal model of the system can be represented by (5.37) and (5.38)

$$\widetilde{x_{k+1}} = F_o \widetilde{x_k} + G_o \widetilde{p_k} \tag{5.37}$$

$$\widetilde{y_k} = H_o \widetilde{x_k} + M_o \widetilde{p_k} \qquad (5.38)$$

Where F_o, G_o, H_o and M_o is given by (5.39) to (5.42)

$$F_o = F - \left[\frac{\partial}{\partial T} Fx_k + g\right]\left[\frac{\partial}{\partial T} Cx_k + d\right]^{-1} C \qquad (5.39)$$

$$G_o = \left[\frac{\partial}{\partial p} Fx_k + g\right] - \left[\frac{\partial}{\partial T} Fx_k + g\right]\left[\frac{\partial}{\partial T} Cx_k + d\right]^{-1}\left[\frac{\partial}{\partial p} Cx_k + d\right] \qquad (5.40)$$

$$H_o = H - \left[\frac{\partial}{\partial T} Hx_k + m\right]\left[\frac{\partial}{\partial T} Cx_k + d\right]^{-1} C \qquad (5.41)$$

$$M_o = \left[\frac{\partial}{\partial p} Hx_k + m\right] - \left[\frac{\partial}{\partial T} Hx_k + m\right]\left[\frac{\partial}{\partial T} Cx_k + d\right]^{-1}\left[\frac{\partial}{\partial p} Cx_k + d\right] \qquad (5.42)$$

The control to output transfer discrete function of the system in the z-domain can then be obtained by taking the Z transform of (5.37) and (5.38) and is given by (5.43).

$$G_{vc}(z) = \frac{Y_k(z)}{P_k(z)} = H_o\left[zI - F_o\right]^{-1} G_o + M_o \qquad (5.43)$$

Mathematica was used to compute the small signal sampled data model matrices and the control and line to output transfer function. Equation (5.44) gives the Z-domain small signal control (duty cycle) to output transfer function. The line to output transfer function is given in (5.45) and the variation of the output voltage to load is given in (5.46) . The steady state operation point is determined using PSPICE simulation as shown in Figure 5.12. $x = \left[-0.8484 \;\; 89.2940\right]^T$, $T = [2.6us \;\; 2.7us \;\; 4.9us \;\; 5.0us]^T$ & $p = [0.52 \;\; 5us \;\; 100ns \;\; 42 \;\; 1.3 \;\; 70]^T$.

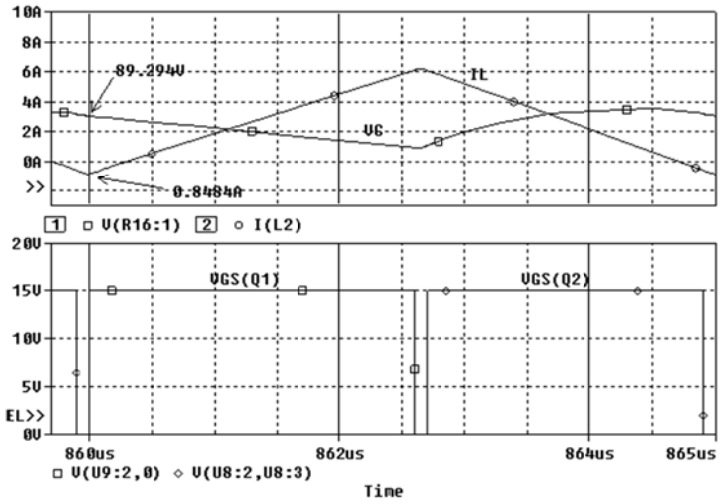


Figure 5.12 : ZVRT Boost steady state PSPICE simulation

$$G_{vd} = \frac{1.69909\ (0.337254 + z)(25.4615 + z)}{(0.906028 - 1.59011z + z^2)} \tag{5.44}$$

$$G_{vg} = \frac{0.121041(0.276516 + z)(3.38349 + z)}{(0.906028 - 1.59011z + z^2)} \tag{5.45}$$

$$G_{vl} = \frac{0.0424615(z - 0.973137)(z + 0.971529)}{(0.906028 - 1.59011z + z^2)} \tag{5.46}$$

The complete system small signal control block diagram is shown in Figure 5.13. The blocks $G_{VD}(s)$, $G_{VG}(s)$ and $G_{VL}(s)$ are continuous time representation of (5.44) to (5.46). The resonant inverter is modelled as a gain, according to (4.59). The feedback network consist of voltage scaling network and peak detector which can be modelled as $\frac{K_s}{sR_fC_f + 1}$ where K_s is determined by the voltage divider configuration used to scale the output voltage to be compatible with the ADC input voltage range. R_f and C_f is selected such that the corner frequency of the peak detector is between one fifth to one third of the HFAC bus frequency. A suitable digital controller can be easily designed using Matlab sisotool (control system toolbox). The design and implementation of digital compensator for systems similar to the one shown in Figure 5.13 have been widely published. Notable example include [92-94], where a step by step design procedure and firmware implementation detail is given.

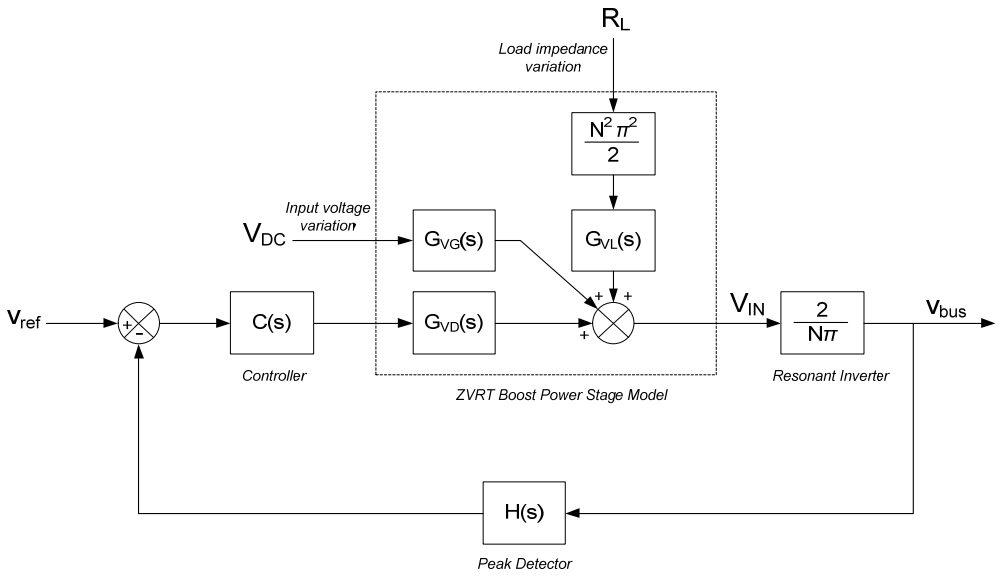


Figure 5.13 : Small signal control block diagram of ZVRT boost converter

5.4 Experimental Setup & Results

The proposed inverter configuration was constructed to verify the analytical prediction. A simplified circuit diagram of the power stage is shown in Figure 5.14. The control is implemented using dsPIC33FJ16GS504 a digital signal controller from Microchip Technology Inc, which is specifically designed for SMPS and power conversion application. The device is capable of 40MIPS operation. In addition the device has high speed 10bits ADC (4Msps) and a high speed PWM module. The photo of the complete inverter and control PCB is shown in Figure 5.15.

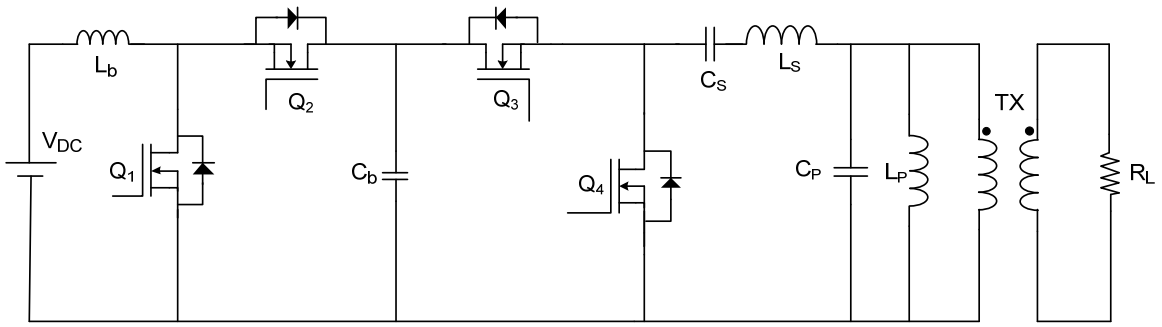


Figure 5.14 : Simplified power stage circuit diagram of HFAC inverter

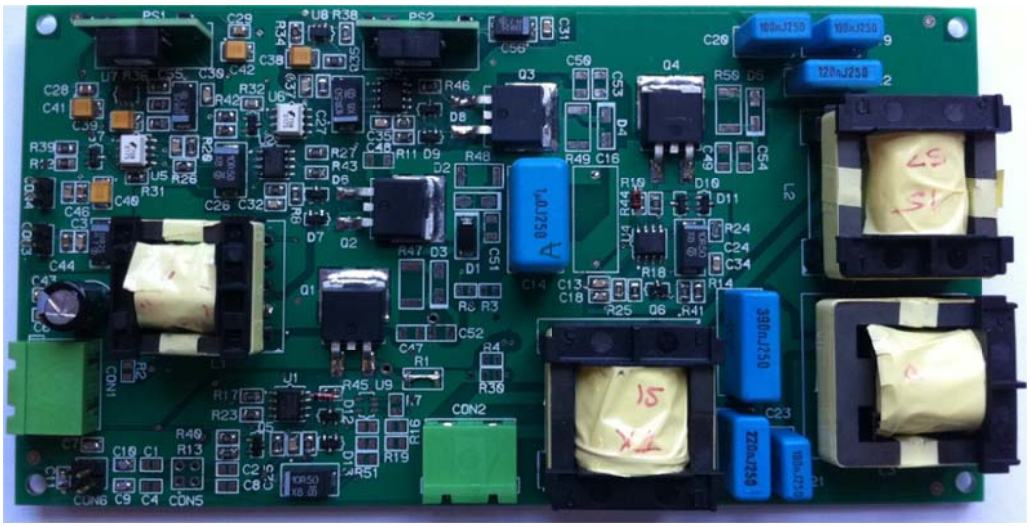


Figure 5.15 : Photo of HFAC resonant inverter PCB

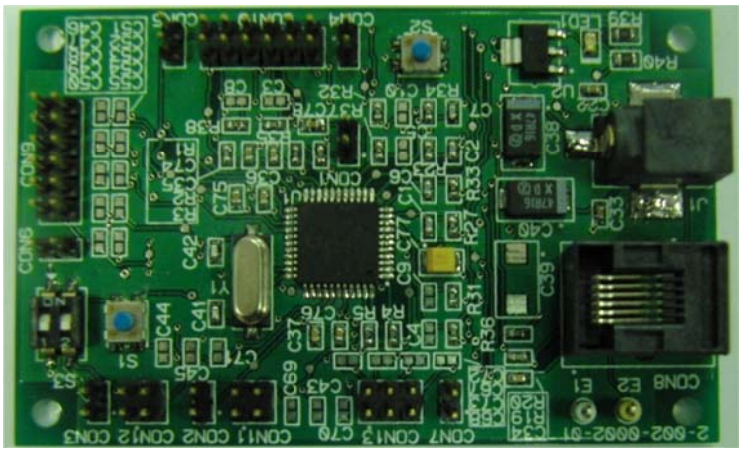


Figure 5.16 : Photo of digital controller PCB

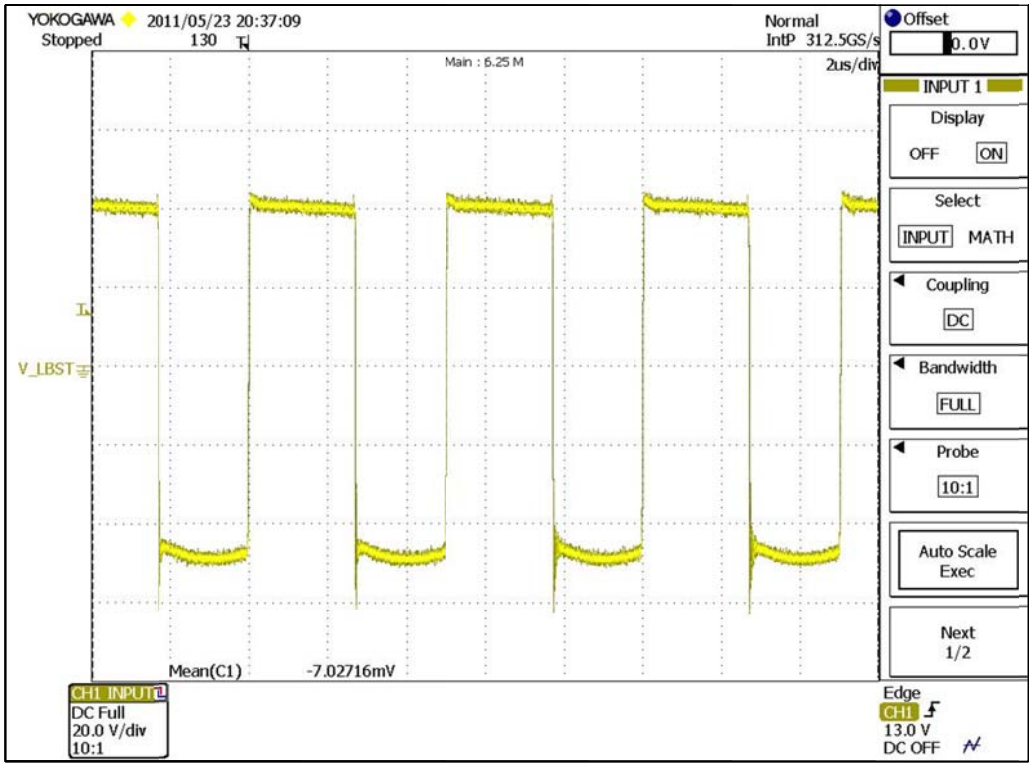
The component values of the physical circuit are based on the optimization results obtain from section 4.6.1. Table 5.2 shows the computed and the actual values of component used in the physical design.

Design Parameter	Computed Value	Actual Measured Value
Boost Inductor L_b	15.38μH	15.85μH
Boost Capacitor C_b	1.0μF	1.0μF
Series Resonant Capacitor C_s	169.03nF	170.1nF
Series Resonant Inductor L_s	59.94μH	60.73μH
Parallel Resonant Capacitor C_p	234.69nF	239.6nF
Parallel Resonant Inductor L_p	35.68μH	34.5μH
Transformer Turns Ratio N	0.3961	0.400
Boost Switching Frequency f_{boost}	200kHz	199.68kHz
Resonant Inverter Operating Frequency f_{bus}	50kHz	49.91kHz

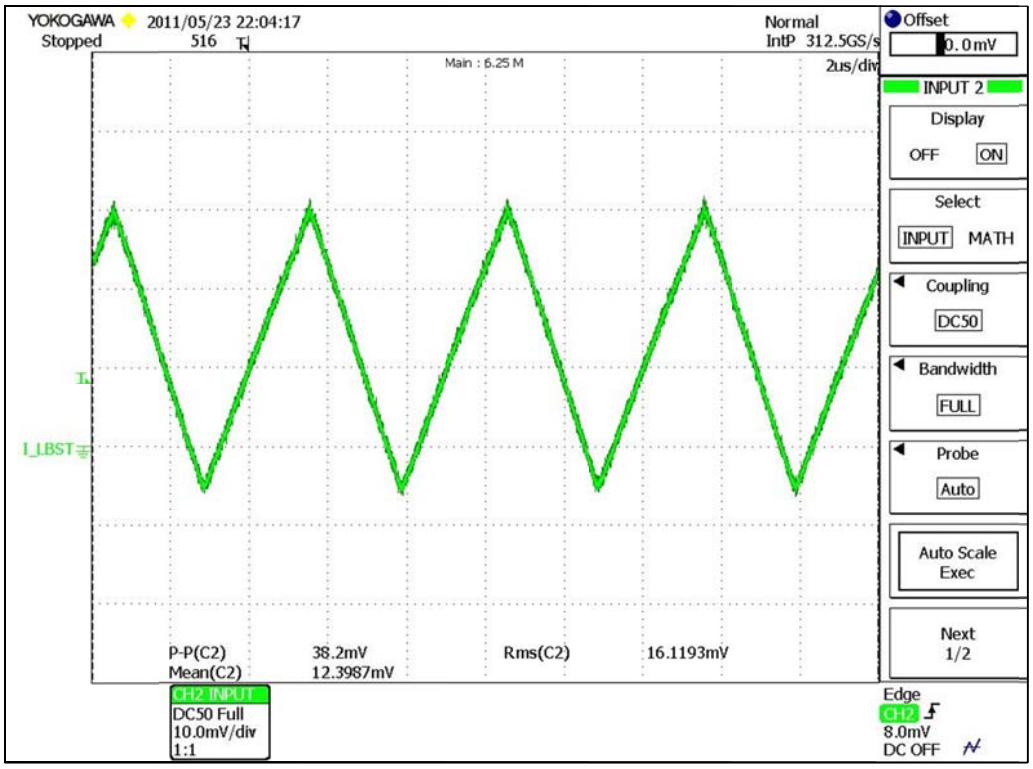
Table 5.2 : Actual design component values

5.4.1 ZVRT Boost Converter – Experimental Measurements

The performance of the front end ZVRT boost converter was experimentally tested to compare it with the analytical model developed in section 5.2. It can be seen that the inductor and capacitor current waveform in Figure 5.17 and Figure 5.18 agree well the analytical and simulation results shown in Figure 5.6 to Figure 5.9.

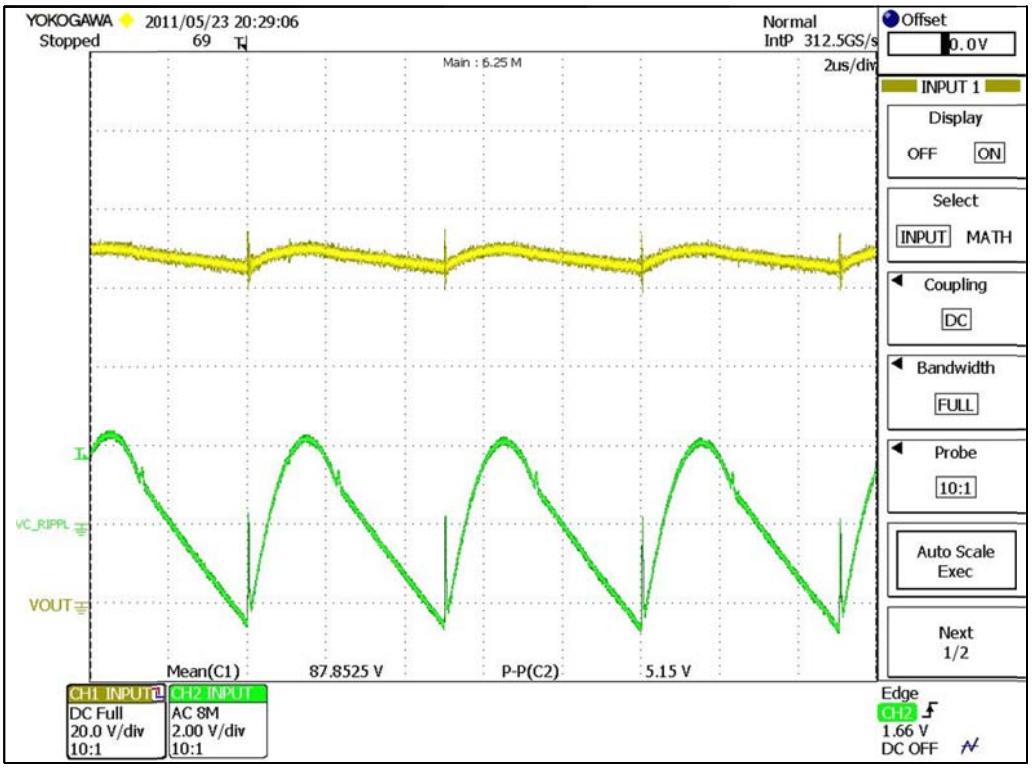


(a) Inductor Voltage (20V / div)

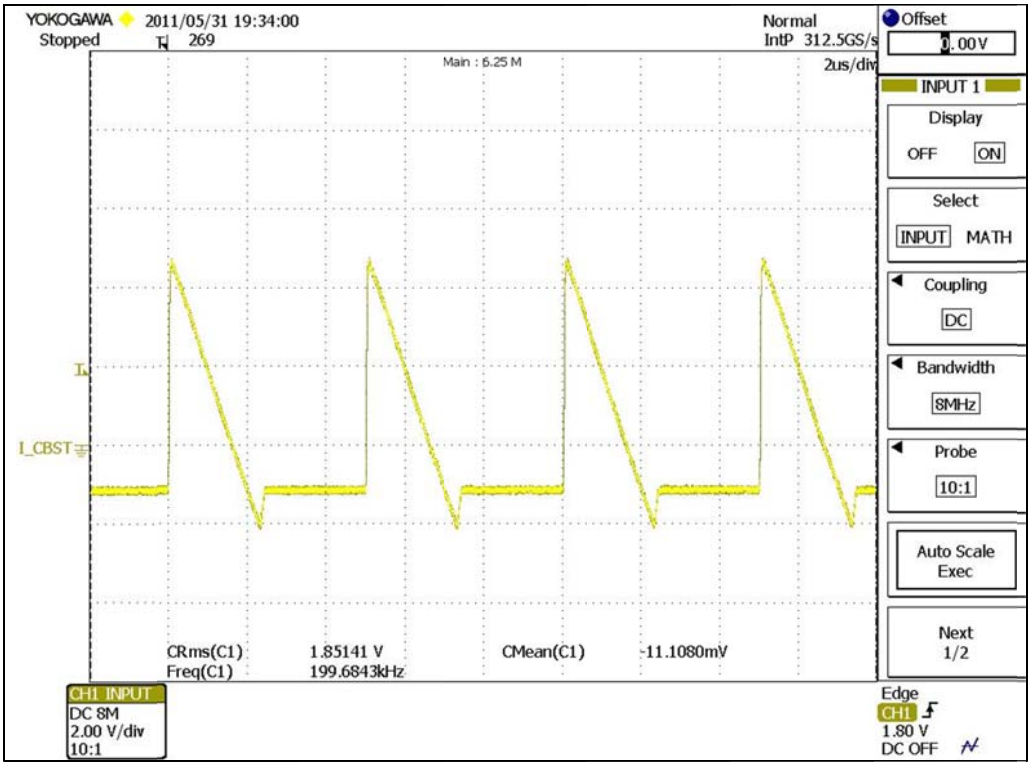


(b) Inductor Current (2A / div)

Figure 5.17 : Boost inductor (a) voltage & (b) current waveform



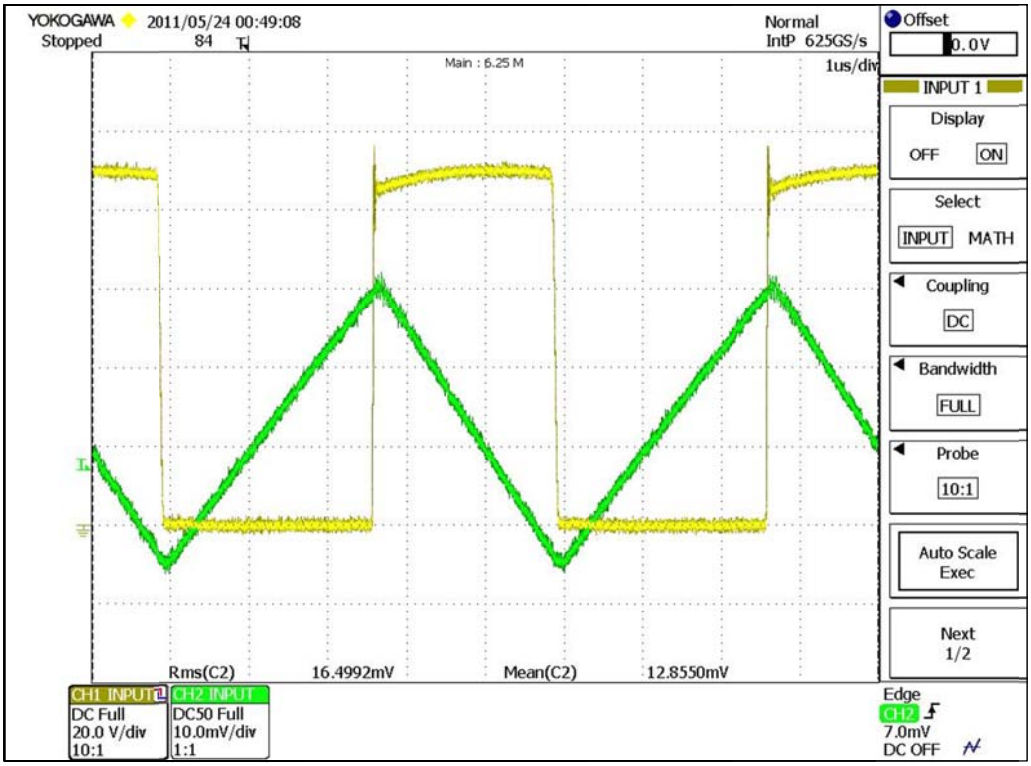
(a) Capacitor Voltage (CH1 :2V/div, CH3 : 20V/div)



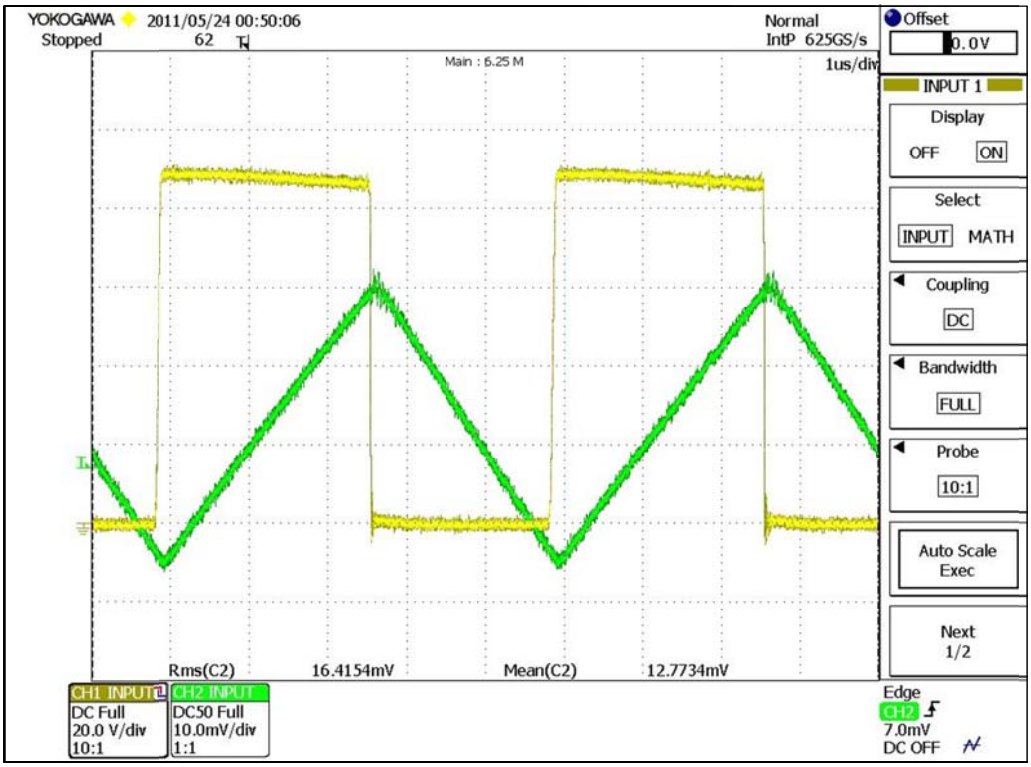
(b) Capacitor Current (2A/div)

Figure 5.18 : Boost capacitor (a) voltage & (b) current waveform

Figure 5.19 shows the mosfet drain to source voltage and the inductor current waveform under 100% loading condition. It can be seen from this capture that both the mosfets Q1 and Q2 are turned ON under ZVS condition. Figure 5.20 shows similar waveform for 50% loading condition. The efficiency vs output curve is given in Figure 5.21. This converter was designed for nominal output power of 100W. The boost inductor value was selected to be approximately 30% lower than minimum inductance predicted by equation (5.19). As such sufficient soft switching headroom is available even under heavier loading condition, up to 160% of the nominal load. Under lighter loading condition, the ratio of the RMS current to the average inductor current increases and therefore the efficiency drops as the output power falls. At 20% loading condition, the efficiency of the converter is approximately 75%.

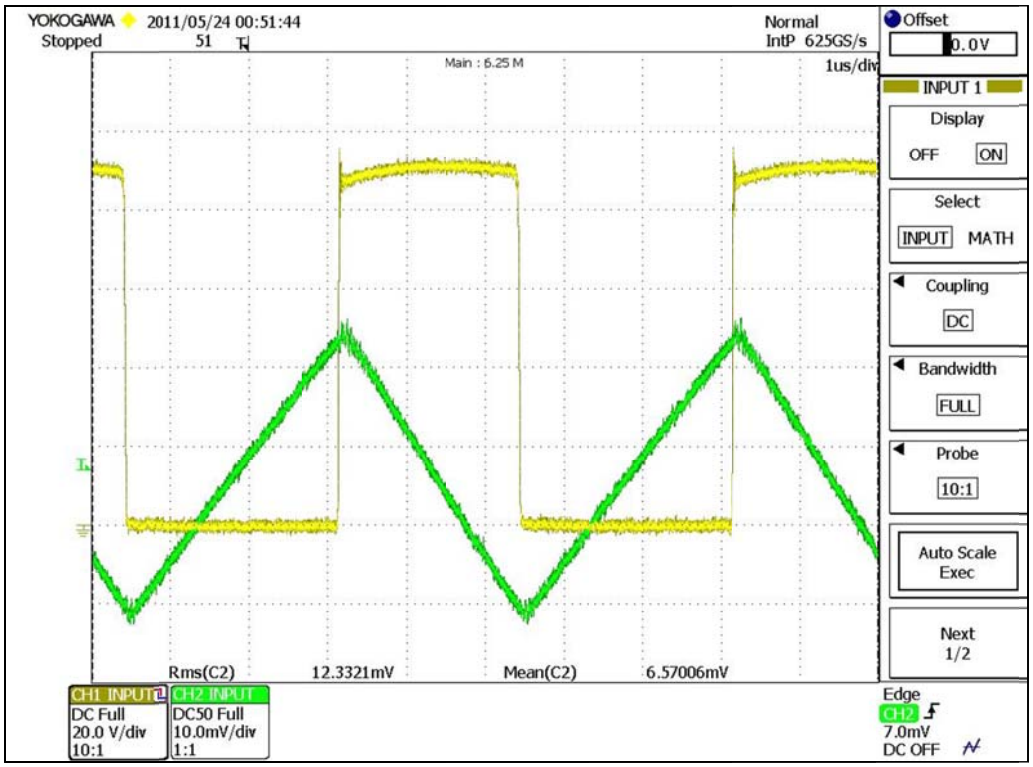


(a) Q1 (CH1 :2A/div, CH3 : 20V/div)

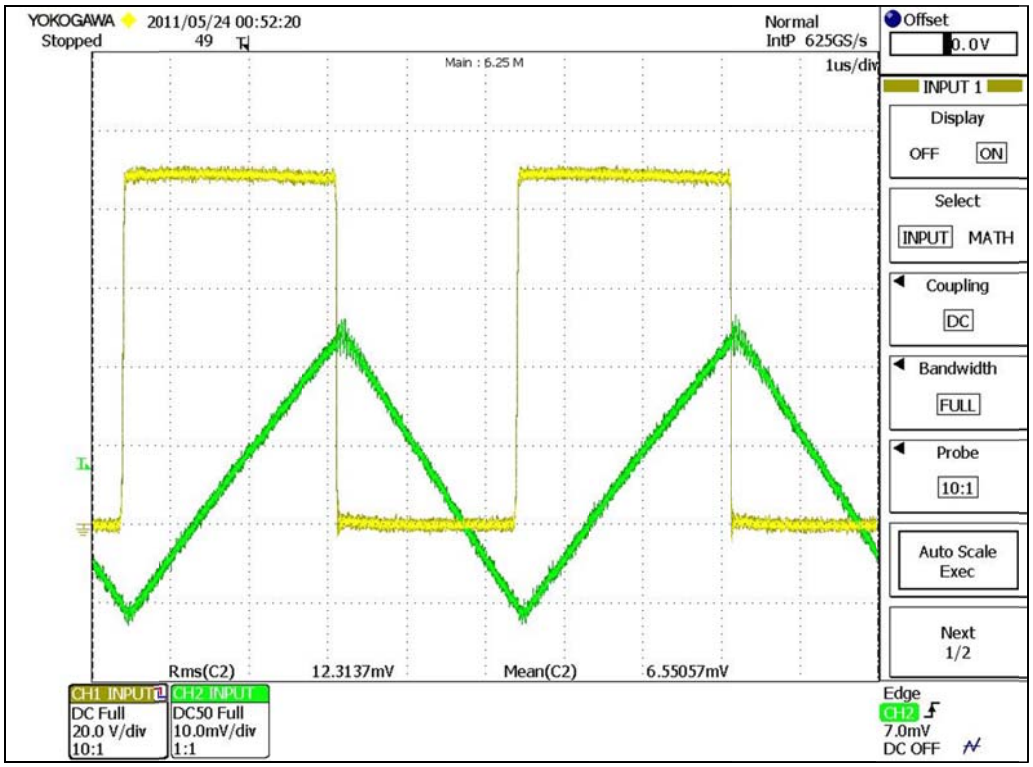


(b) Q2 (CH1 :2A/div, CH3 : 20V/div)

Figure 5.19 : Q1 & Q2 switching waveform (100% load)



(a) Q1 (CH1 :2A/div, CH3 : 20V/div)



(b) Q2 (CH1 :2A/div, CH3 : 20V/div)

Figure 5.20 : Q1 & Q2 switching waveform (50% load)

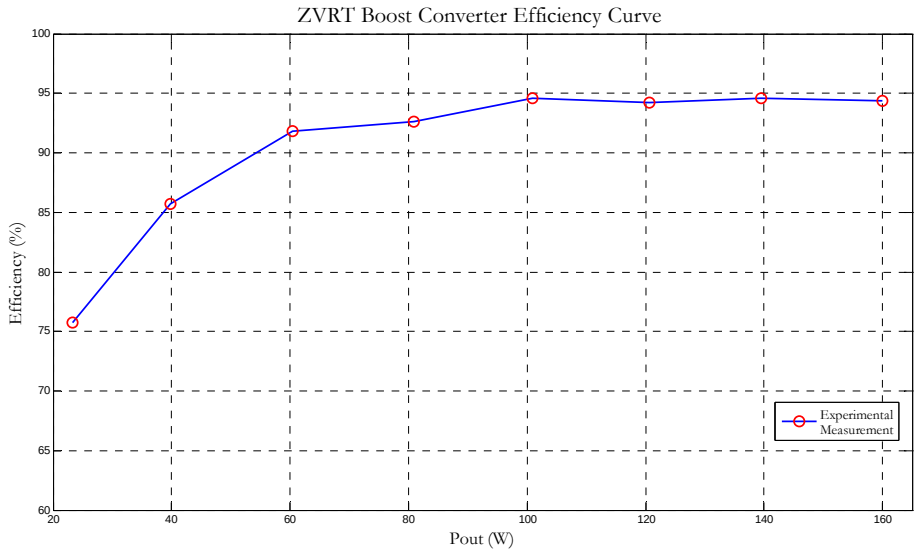
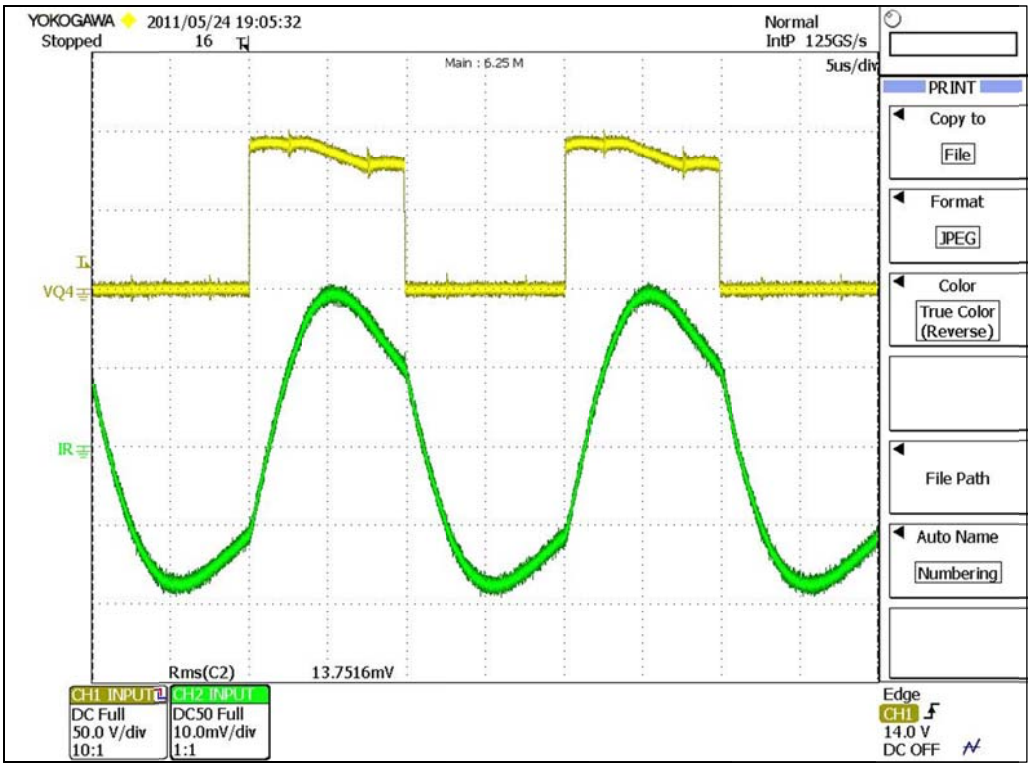


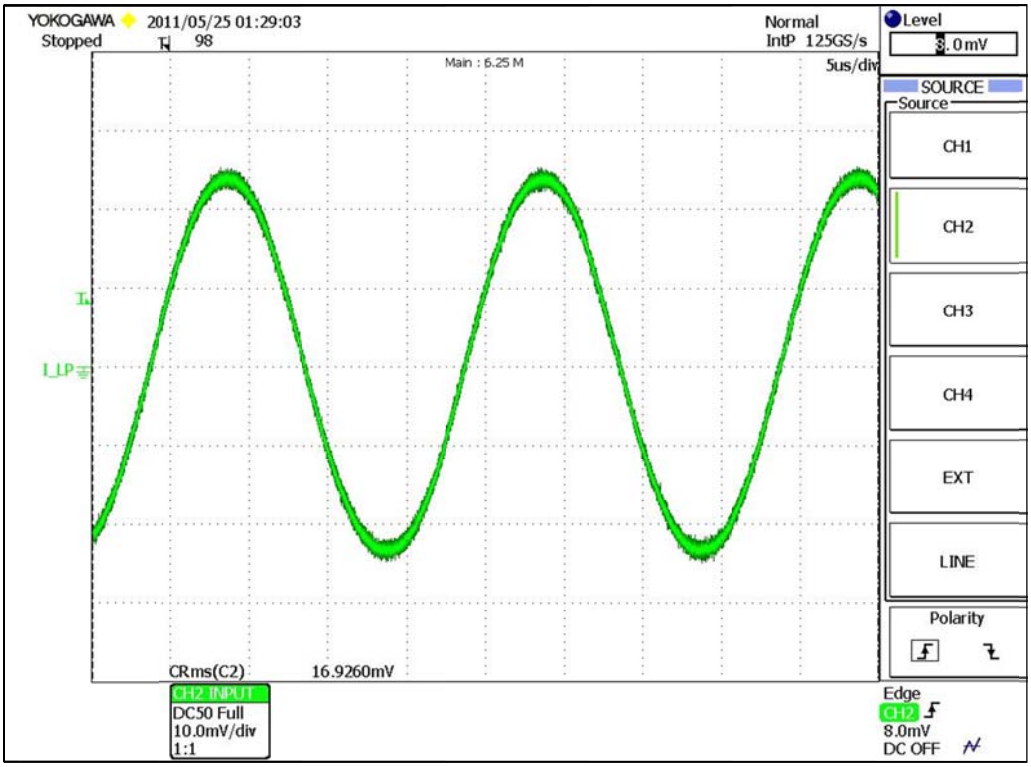
Figure 5.21 : Efficiency vs output power (ZVRT Boost)

5.4.2 Resonant Inverter – Experimental Measurements

Experimental measurement of the resonant inverter constructed based on the optimized component value obtain from section 4.6 is shown below. Figure 5.22 (a) shows the resonant tank input current and voltage waveform. It can be observed that the resonant current waveform matches the analytical and simulation results shown in Figure 4.4 quite well. Further it can be observed that the resonant current lags the tank voltage, indicating that the resonant tank presents an inductive impedance thus enabling ZVS switching of the mosfets. The scope capture of the current through the parallel inductor is shown in Figure 5.22 (b) and is in good agreement with simulation results shown in Figure 4.9.



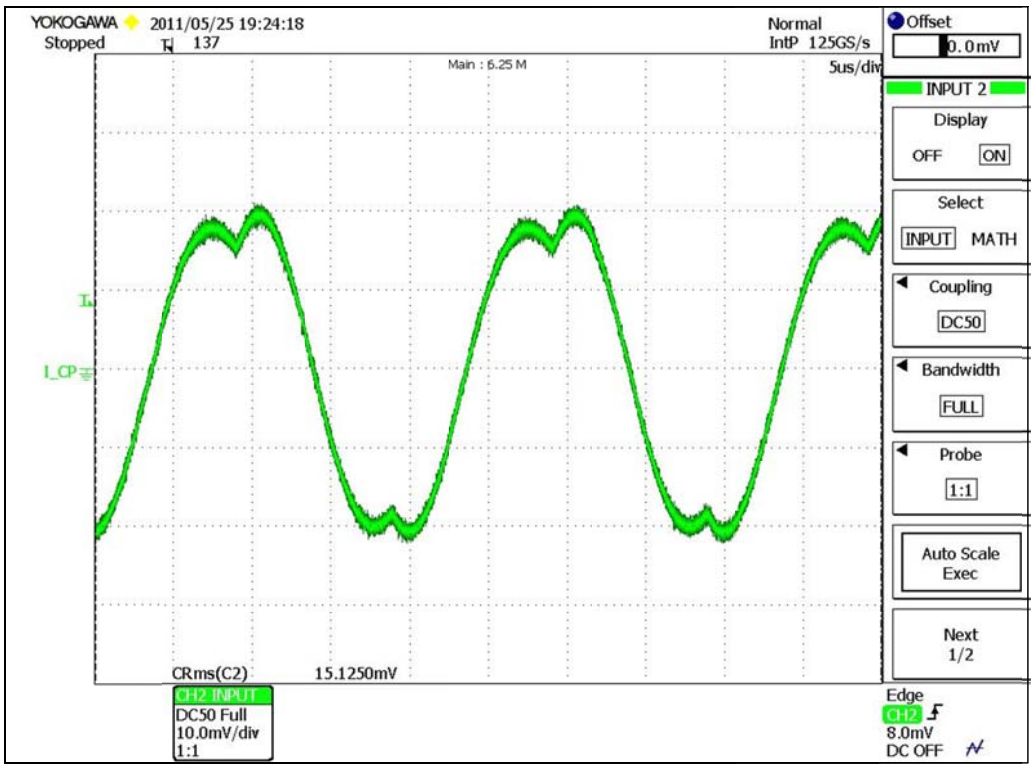
(a) i_r & v_a (CH2 :2A/div, CH1 : 50V/div)



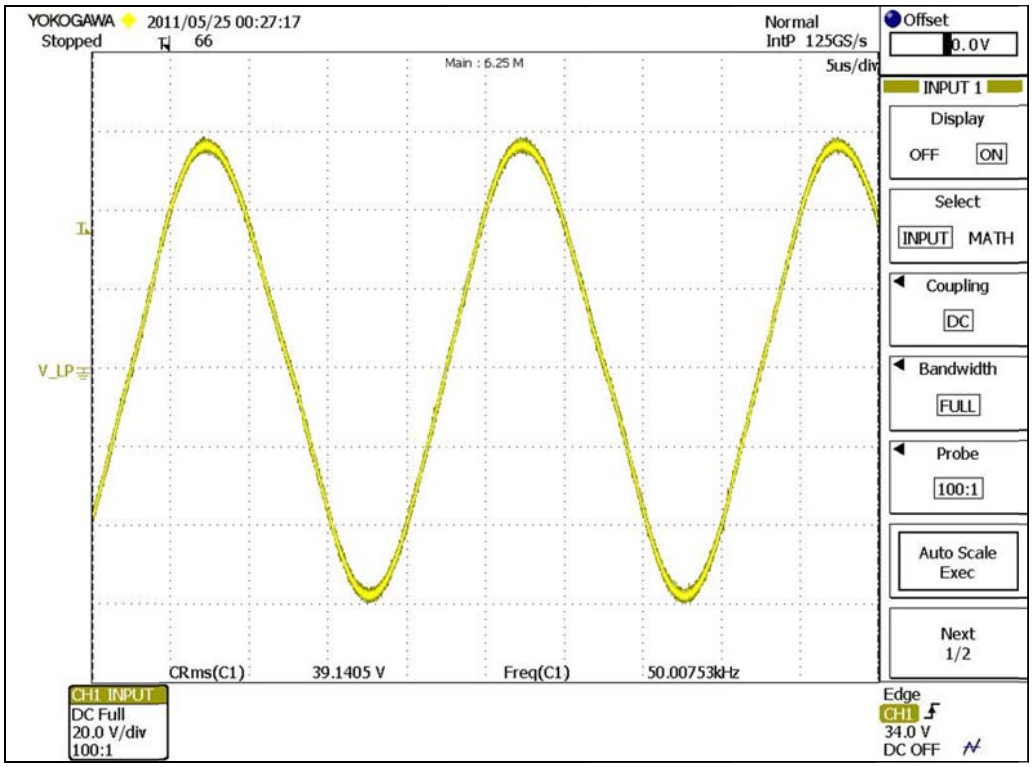
(b) i_{lp} (CH2 :2A/div)

Figure 5.22 : (a) Tank input current & (b) Parallel inductor current

The waveform of the current and voltage across the parallel capacitor is shown in Figure 5.23. The voltage measurement across the series capacitor and inductor is given in Figure 5.24. It can be seen that these measurements agree well with the simulation and analytical prediction presented in section 4.1.4.

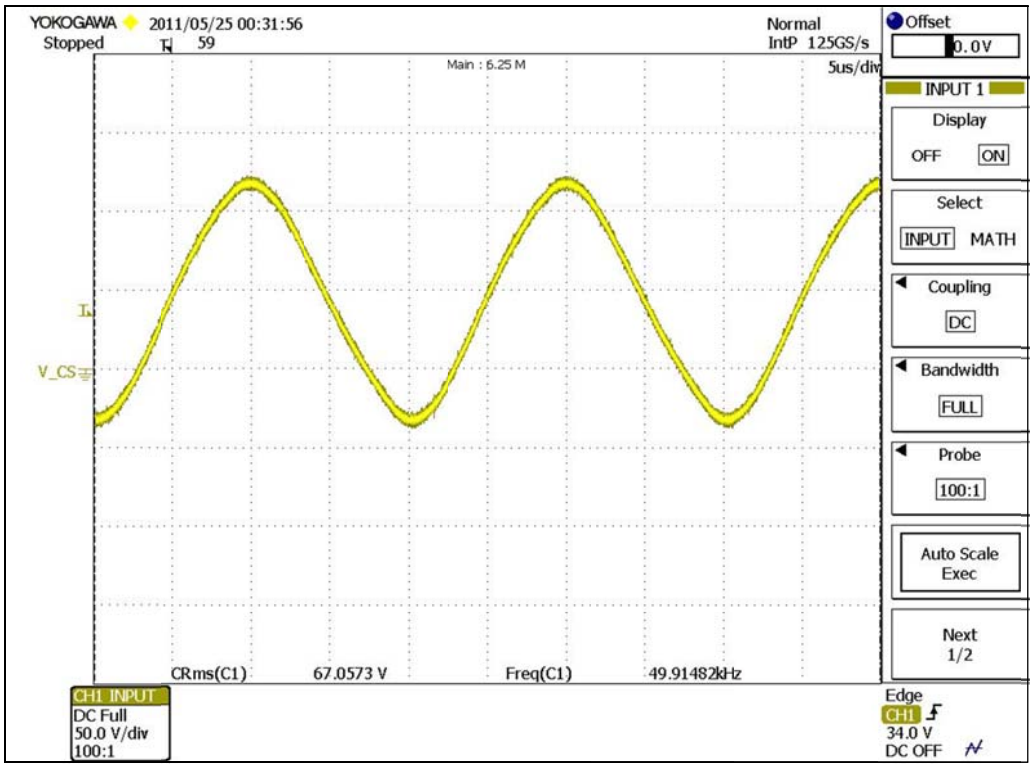


(a) i_{cp} (CH2 :2A/div)

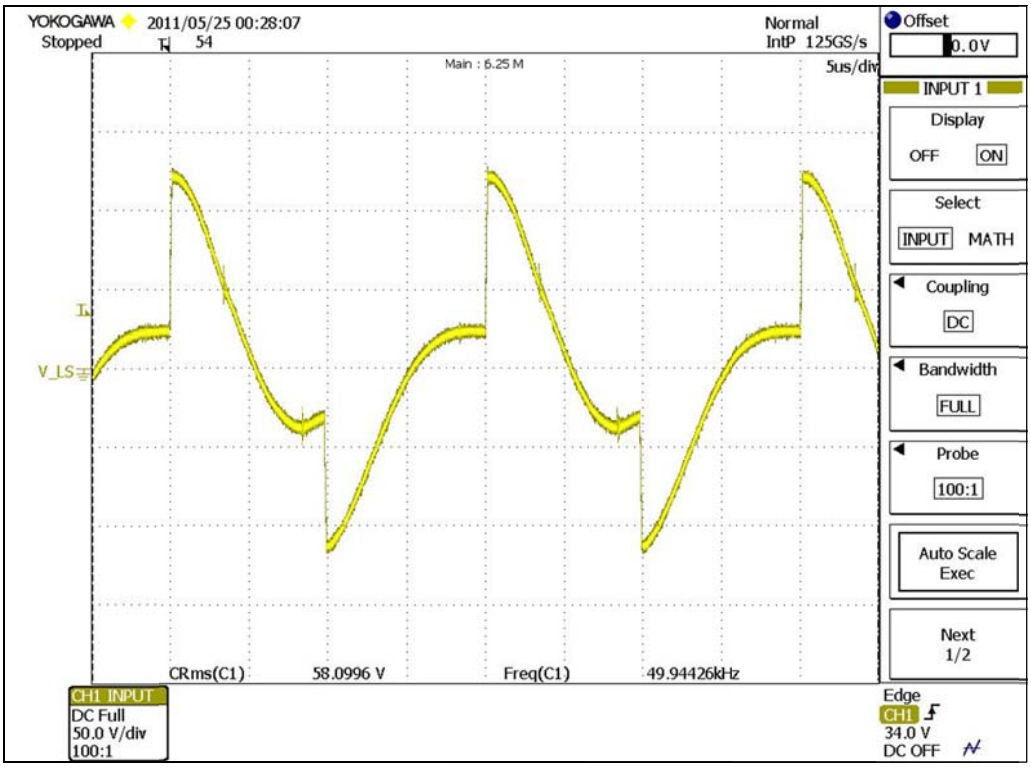


(b) v_{cp} (CH1 :20V/div)

Figure 5.23 : (a) Parallel capacitor current & (b) Parallel capacitor voltage



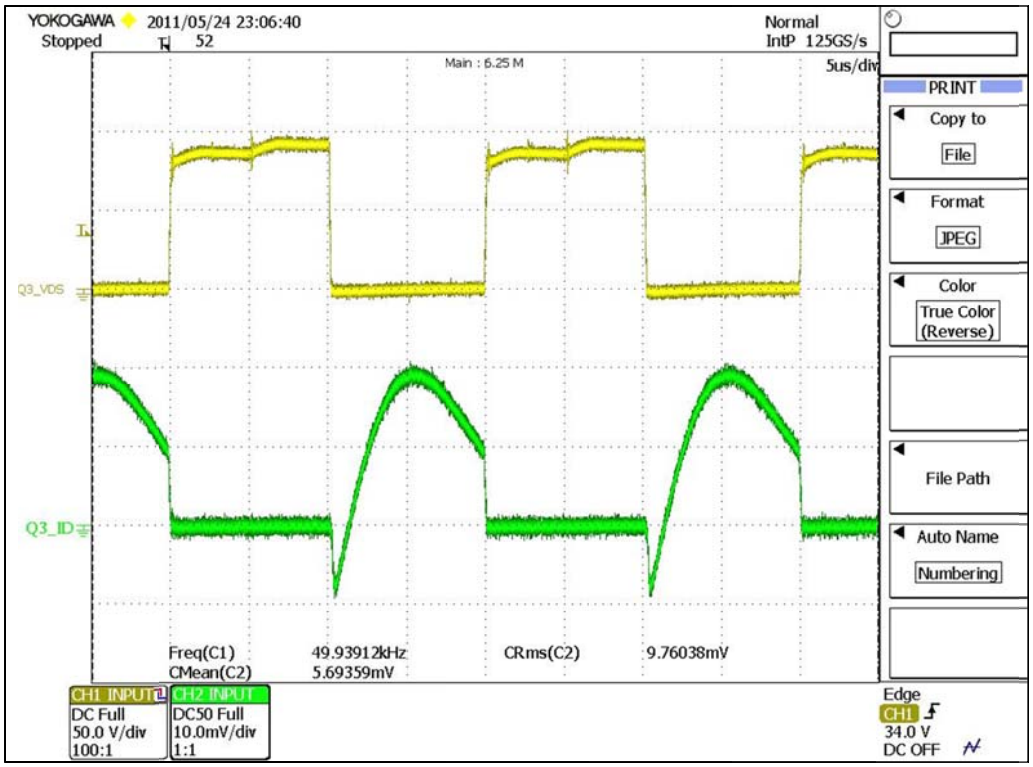
(a) v_{cs} (CH1 :50V/div)



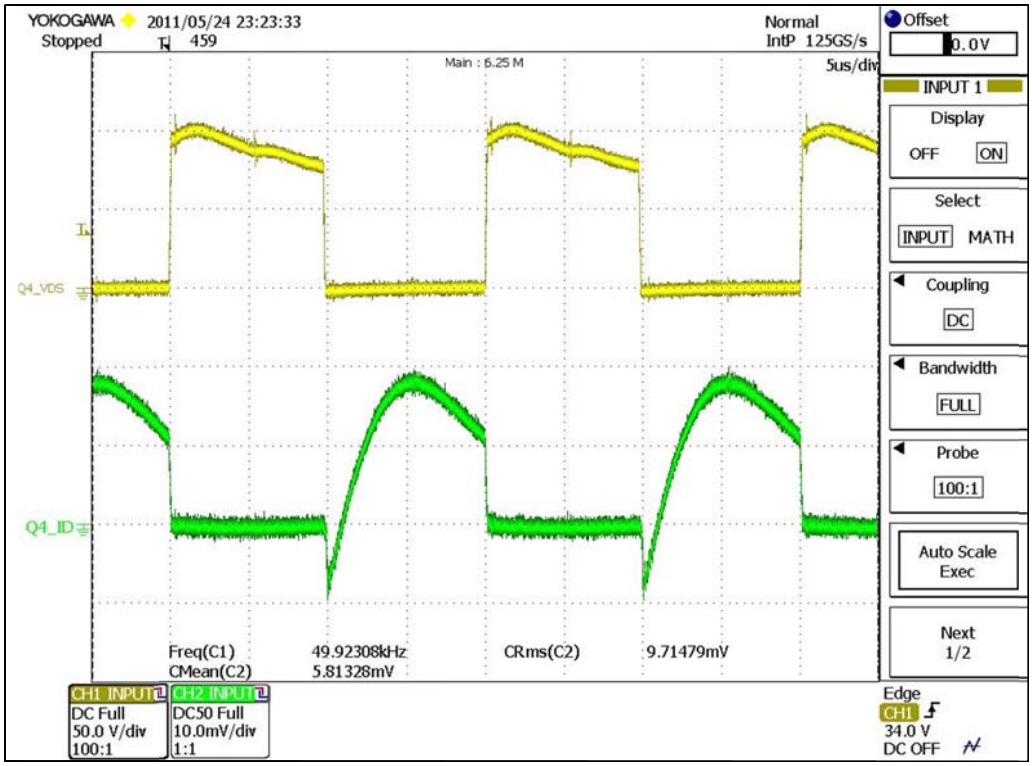
(b) v_{ls} (CH1 :50V/div)

Figure 5.24 : Series capacitor voltage & (b) Series inductor voltage

The mosfet drain to source voltage and the drain current for both Q3 and Q4 is shown in Figure 5.25 (a) and (b) respectively for full load condition. Similar measurement under 50% loading condition is given in Figure 5.26. It can be seen that in both cases, the mosfet switches ON when the body diode is conducting and thus ZVS is achieved. The waveforms match the analytical and simulation results shown in Figure 4.10 and Figure 4.11.

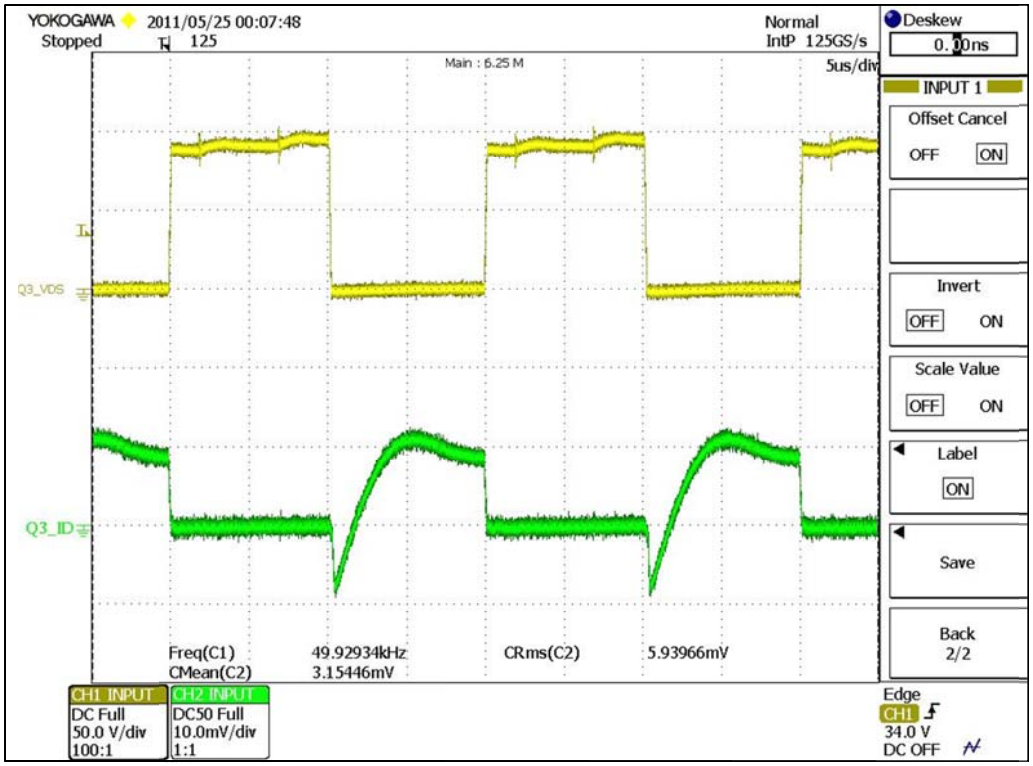


Q3 (CH2 :2A/div, CH1 : 50V/div)

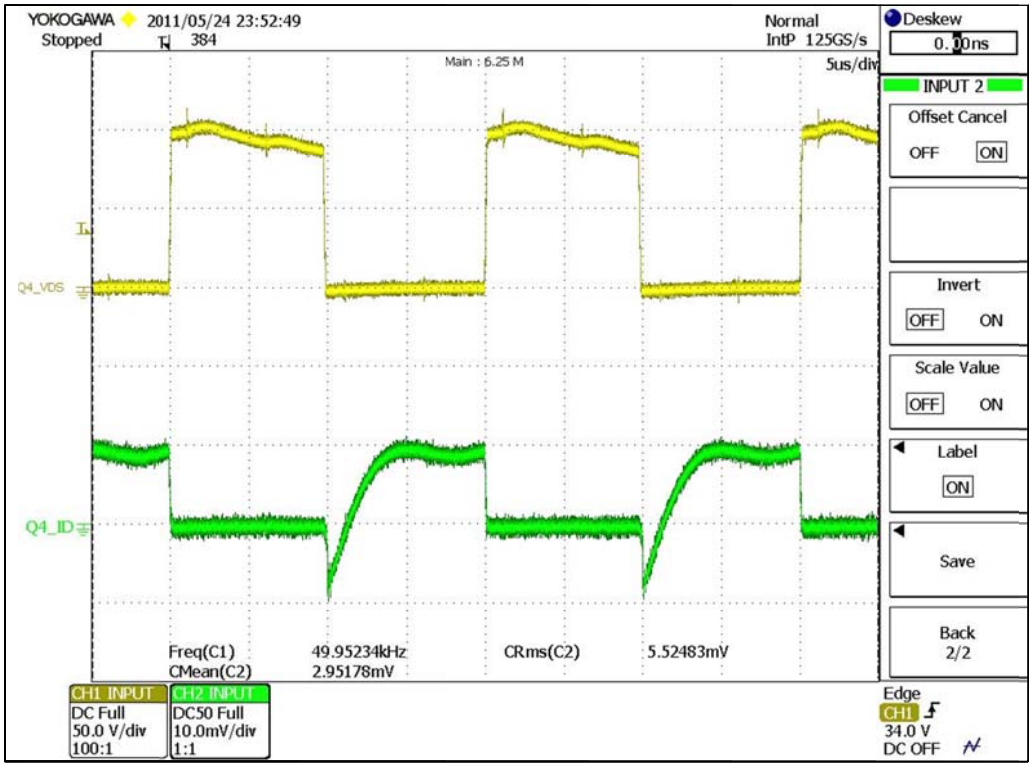


(b) Q4 (CH1 :2A/div, CH3 : 50V/div)

Figure 5.25 : Resonant inverter mosfet switching waveform (100% load)



(a) Q3 (CH2 :2A/div, CH1 : 50V/div)



(b) Q4 (CH1 :2A/div, CH3 : 50V/div)

Figure 5.26 : Resonant inverter mosfet switching waveform (50% load)

The computed and measured performance parameters are shown in Table 5.3. It can be observed that the simplified analysis used in the optimization process yields results that are very close to the actual experimental measurements.

Performance Parameter	**Computed Value**	**Measured Value**
Tank Input Resonant Current (i_r)	2.60 A_{RMS}	2.748 A_{RMS}
Parallel Inductor Current (i_{lp})	3.53 A_{RMS}	3.39 A_{RMS}
Parallel Capacitor Current (i_{cp})	2.92 A_{RMS}	3.01 A_{RMS}
Series Capacitor Voltage (v_{cs})	48.92 V_{RMS}	49.69 V_{RMS}
Parallel Capacitor Voltage (v_{cp})	39.61 V_{RMS}	39.32 V_{RMS}
Efficiency (η)	97.15%	96.26%
Transformer Turns Ratio	0.397	0.400
Total Harmonic Distortion (THD)	3.69%	-

Table 5.3 : Comparison between calculated and measured resonant inverter performance

The phase angle control of the second stage is shown in Figure 5.27. The yellow trace (CH1) represents the reference waveform to the DSP, the green trace (CH2) the input voltage to the resonant tank and the pink trace (CH3) is the bus voltage waveform. As discussed in section 3.2.7, the PWM signal can be easily synchronized with an external reference using a digital signal processor. This is achieved by programming the PWM frequency to be slightly lower than the desired bus frequency and clearing the PWM frequency counter at every rising edge of the phase reference signal. It can be seen from Figure 5.27 that the phase angle of the bus voltage is in sync with the reference voltage, with a small fixed delay, which is independent of loading and input voltage variations.

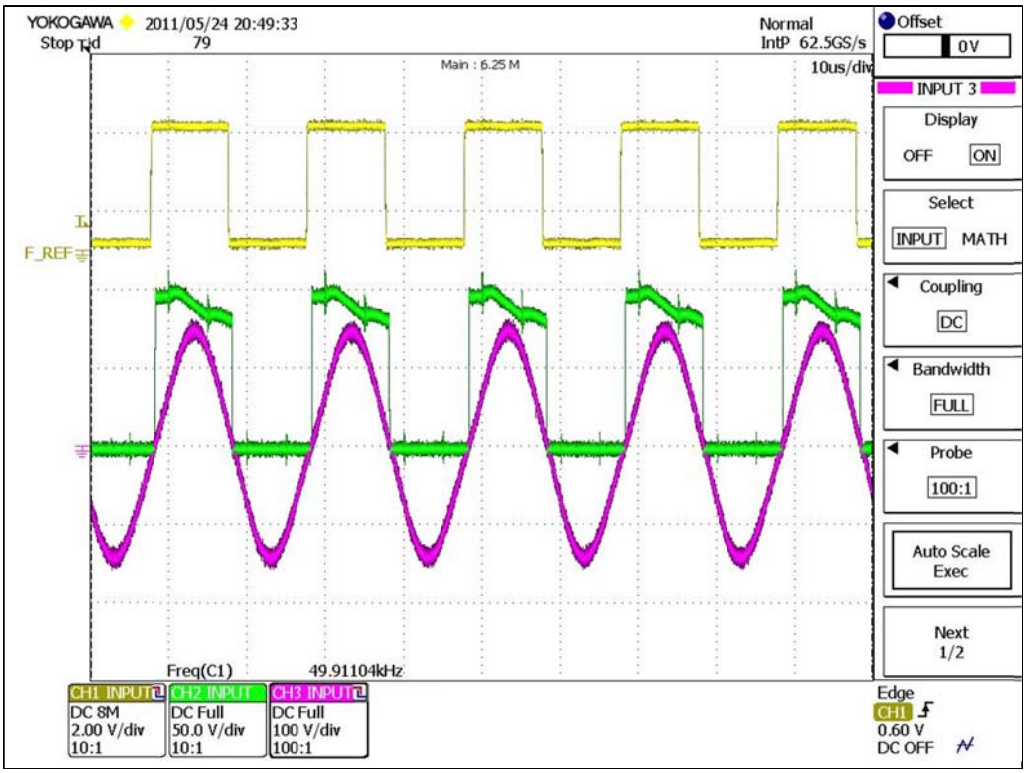


Figure 5.27 : Phase angle of HFAC bus voltage relative to reference waveforrm
(Pink : HFAC bus voltage, Green : Tank input voltage (v_a), Yellow : Phase reference signal)

5.5 Concluding Remarks

In this chapter, mathematical modelling of the ZVRT boost converter was presented and based on this analysis the complete system control block diagram was generated. It was shown that for magnitude control, the second stage resonant inverter can be modelled simply as a gain and therefore does not increase the control complexity of the ZVRT boost converter. Phase angle synchronization can be achieved by ensuring the phase of the resonant inverter PWM signal is in phase with the desired reference phase signal. This can be achieved easily using a digital signal processor. The proposed MSI is therefore suitable for parallel operation due to the decoupled phase and magnitude control. Good correlation between experimental measurements and the predictions of the mathematical model were observed.

CHAPTER 6

POINT OF LOAD POWER CONVERTER

*"The whole of science is nothing more than a refinement of everyday thinking" – **Albert Einstein, 1879-1955.***

In high frequency AC distributed power architecture, the VRM, known also as the 'point of use power converter', is an important part of the system. The VRM has two main objectives. First, it serves to convert the bus power of a particular voltage and frequency to the form that is required by the load. It can be regarded as an intermediate power interface unit between the load and the HFAC power bus. Secondly, it 'decouples' the load from the HFAC bus. This allows the system to distribute power optimally from the transmission point of view without being constrained by load requirements. It also offers the flexibility for the load to be designed to accept input power that is optimal for the operation of the load. In this chapter, the existing VRM designs and topologies proposed in literature are investigated. Presented in chronological order, each topology is analysed, and the advantages and limitations are discussed. Following this, the integral cycle converter is identified as an attractive option with opportunity for further research. Finally the mathematical modelling of the integral cycle converter is undertaken and it is shown that power factor of the converter can be improved by optimal selection of the switching sequence.

6.1 Review of Existing Topology

The VRM topology shown in Figure 6.1 was first proposed by NASA in 1983 to be used in space application [15]. This is the first documented implementation of local regulation module for high frequency power distribution system. A low frequency output waveform was synthesized from the HFAC source by controlling the switching sequence of the full bridge inverter. To provide meaningful regulation however, it is important to ensure that the synthesized output frequency is much smaller than the HFAC bus frequency. This VRM has the capability to generate a DC or an AC output voltage.

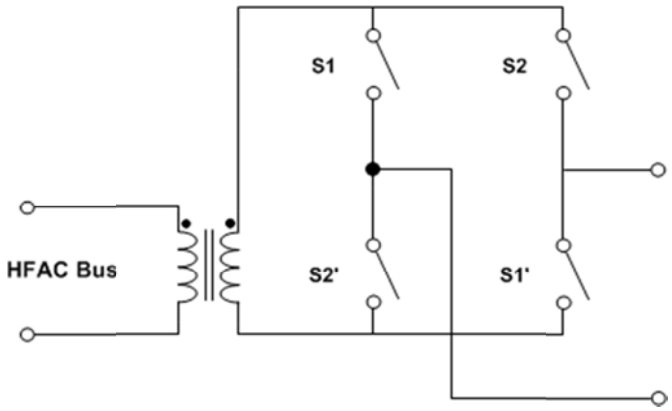


Figure 6.1 : First VRM design for space application (extracted from [15])

Then in 1988, Sood, Lipo & Hansen in [95] proposed a VRM similar to the one described above with some added enhancement. The proposed VRM was a non-isolated design which interfaces directly to the HFAC bus without a transformer. A LC tank circuit tuned to the bus frequency was connected in parallel to the full bridge switching network. The LC tank offers a low impedance path to currents at frequencies other than the bus frequency and stops it from being fed back to the source.

Area comparison pulsed density modulation was proposed as a suitable control method. In this control scheme all switching is performed at voltage zero crossing, thus reducing switching losses. This design has AC and DC output capability and the output voltage can be controlled discretely. This technique is commonly known as integral cycle control. This design offers better harmonic current suppression and therefore has lower total harmonic distortion as compared to the previous design. In the same paper, two other

VRM variants based on the same idea was presented. These are generally half bridge variant of the original design.

In 1989, the VRM topology in Figure 6.2 was proposed in [36] to power entertainment units in aircrafts over a current fed HFAC bus. A Shunt regulator was used in the secondary DC side (after the rectifier) in parallel to the load to regulate the output DC voltage. The shunt regulator draws sufficient regulation current (I_{SHUNT}) to keep the rectifier output current (I_{ROC}) constant regardless of variation in the load current (I_{LOAD}). The use of a shunt regulator in this design leads to low efficiency due to the lossy nature of such regulators. In this paper, efficiency analysis was not addressed. This design is only suitable for very simple loads, and it is believed that the focus of this design is principally to exploit the contactless operation of HFAC.

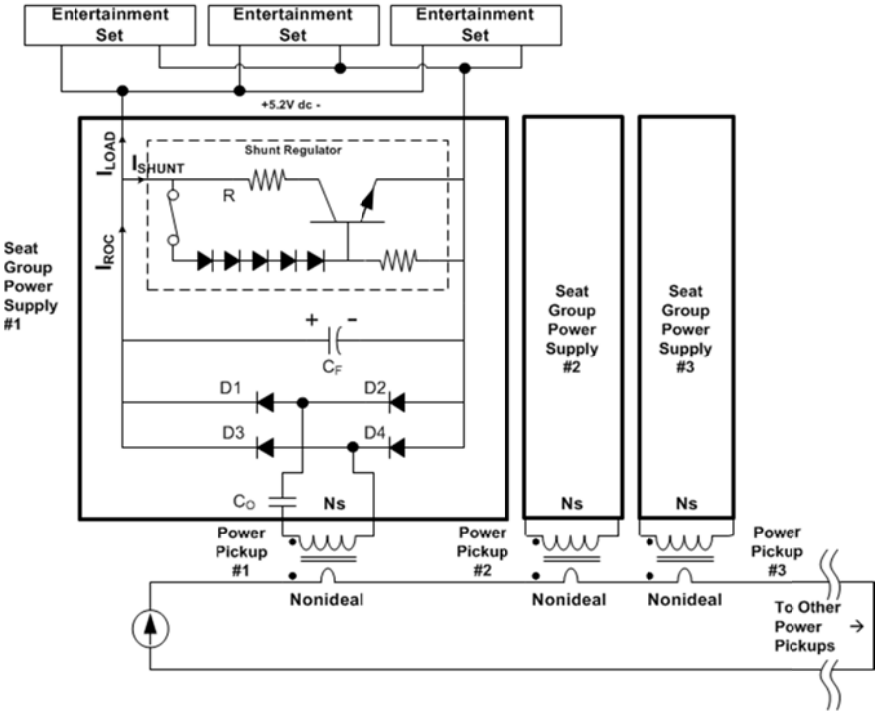


Figure 6.2 : VRM for current fed HFAC system in aircraft application (extracted from [36])

Tsai & Lee [55] in 1990 proposed 3 versions of VRM. The first design is a DC output type and it consists of a centre tapped HFAC transformer, controlled rectifier and a LC low-pass filter as shown in Figure 6.3. The output voltage magnitude is regulated by controlling the firing angle of the rectifier switches (T1 & T2) with respect to the HFAC

bus voltage zero crossing. This design is expected to have poor input power factor, large current harmonics and high EMI. Regulating the output voltage by phase angle control (hard switching) is generally inefficient.

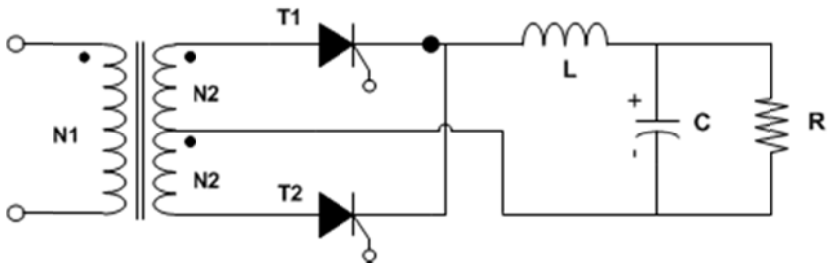


Figure 6.3 : DC VRM for space application (extracted from [55])

The second VRM design proposed by Tsai & Lee was capable of generating AC output. This design is shown in Figure 6.4. Fundamentally it consists of a full bridge switching network followed by a LC low pass filter. It interfaces with the HFAC bus via a high frequency transformer and converters the HFAC input to a regulated low frequency AC output voltage. The conversion is achieved by implementing pulse density modulation, where the output voltage is constructed using integral half cycle of the HFAC input waveform. In essence, this topology is similar to the designs proposed in [15, 95].

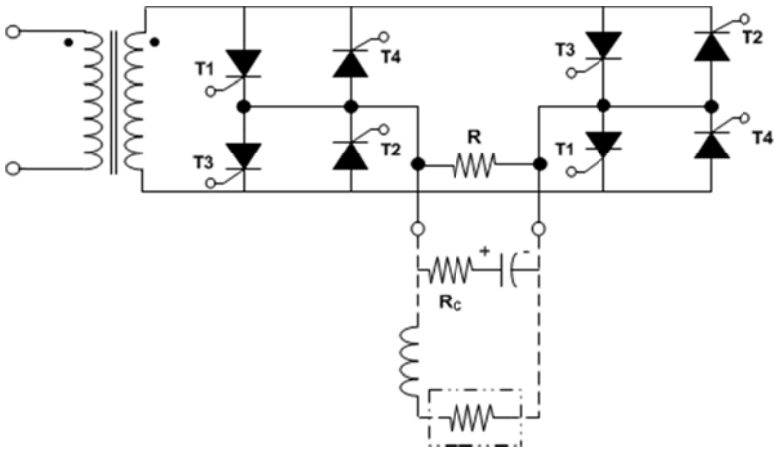


Figure 6.4 : AC VRM for space application (extracted from [55])

The third variant is a bidirectional VRM topology; it is shown in Figure 6.5. It is based upon a Mapham converter with a switch in series with the capacitor. The circuit can operate both in forward and reverse direction. The power flow direction depends on the switching orientation.

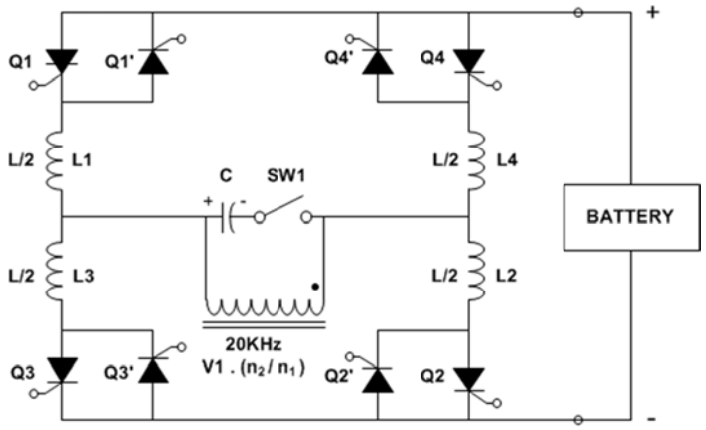


Figure 6.5 : Bidirectional VRM topology (extracted from [55])

In forward mode operation the converter takes the HFAC bus as the input and converters it to a DC output to power the load. In the forward mode Q1 to Q4 remains OFF and the firing angle of Q1' to Q4' is controlled to regulate the output. The switch SW1 is also turned OFF. In the forward mode, the circuit operation is similar to the topology shown in Figure 6.4. In the reverse mode operation, Q1'-Q4' are continuously gated and the power from the battery (at the load terminal) acts as a DC input source to the converter. The switch SW1 is also turned ON, and the Q1-Q4 is controlled to generate a HFAC output. This circuit now operates as a Mapham inverter. As this design employs phase angle control, the switches are not soft switched; therefore the overall efficiency is low.

In 1993 Jain, Tanju et.al in [96] proposed 3 versions of DC VRM. The three types are called Type 1-A, Type1-B and Type1-C. Each of this topology is based on the generic configuration shown in Figure 6.6. The resonant network however is different for each type. The control parameter for all cases is the phase angle of the current controller. Each variant has a unique, voltage conversion ratio, input current THD and power factor vs phase angle characteristics.

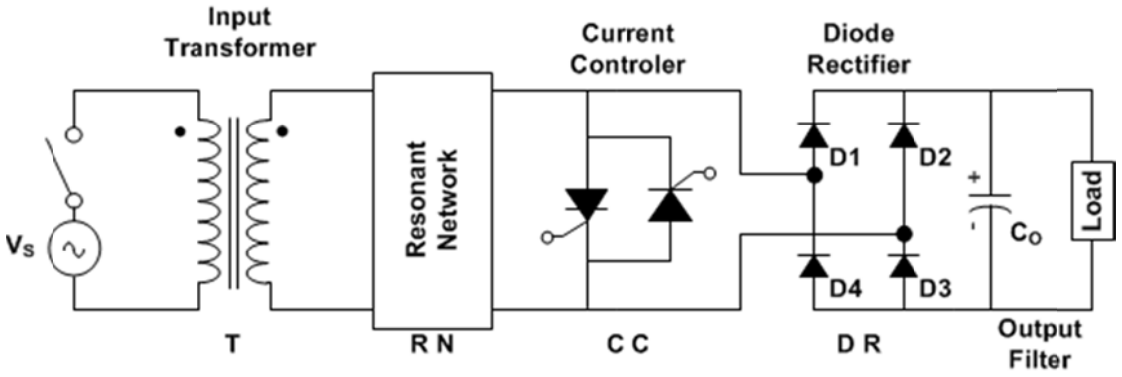


Figure 6.6 : Generic DC VRM circuit configuration (extracted from [96])

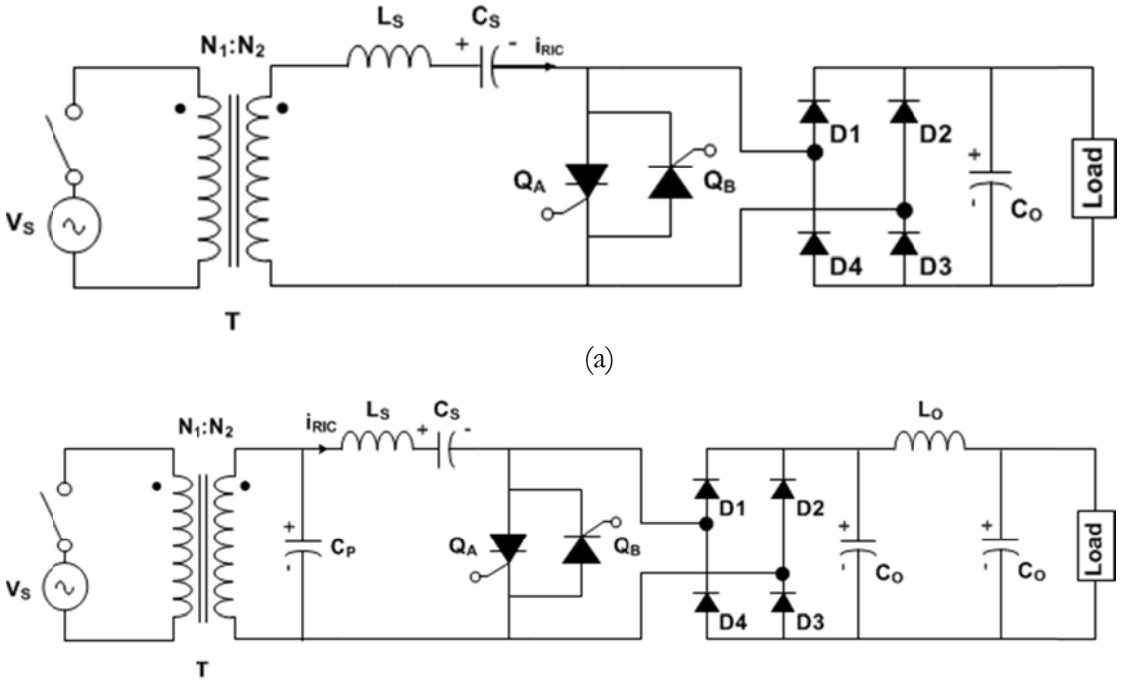
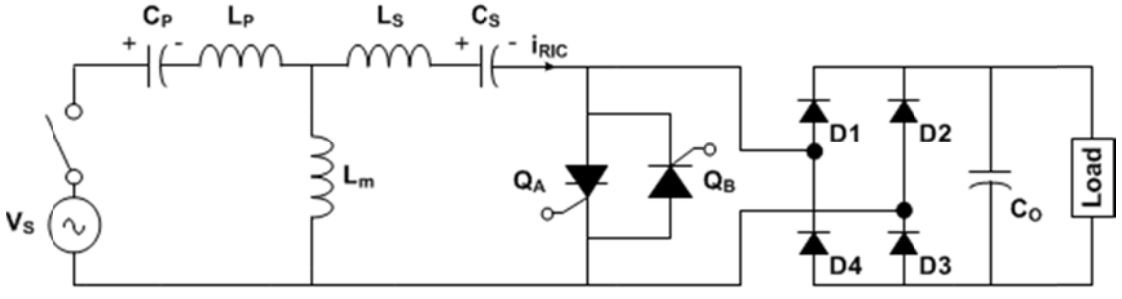
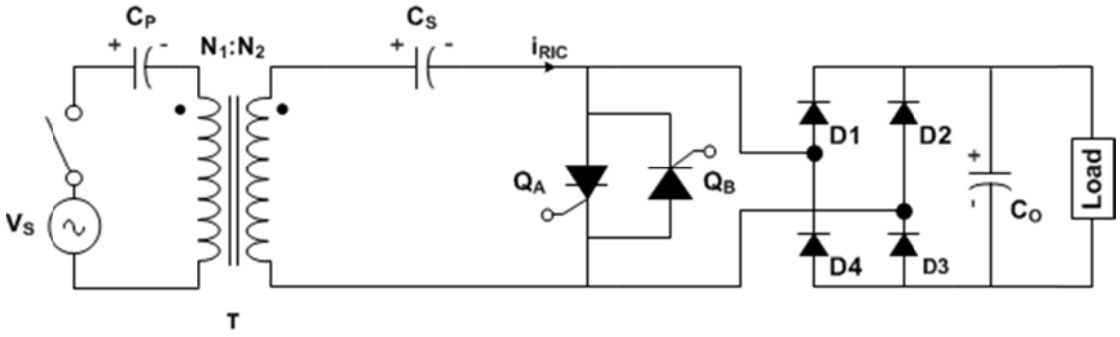


Figure 6.7 : DC VRM - (a) Type 1-A (b) Type 1-B (extracted from [96])



(a)



(b)

Figure 6.8 : DC VRM - (a) Type 1-C (b) Type 1-C simplified (extracted from [96])

The resonant network of type1-A design is a series LC network as shown in Figure 6.7 (a). The circuit starts up with the current i_{RIC} charging the output capacitor C_o, via $D1$ and $D3$, during the positive cycle. The capacitor is kept charging until Q_A is turned ON (at $\omega t = \alpha$) at which time the capacitor charging is stopped and the current now flow through Q_A until the current goes to zero. When Q_A is ON, the energy from the input is not delivered to the load but stored in the resonant network. The operation of the circuit is similar during the negative cycle, but with Q_B controlled and with diodes $D2$ and $D4$ conducting when power is delivered to the load. In this converter, the output voltage control is provided by controlling the firing angle α of the current controller.

Although this topology is claimed to have close to unity power factor and low THD input current, it is important to note that these are function of the firing angle α. Therefore it is not possible to independently control the output voltage without affecting the THD and power factor. Another limitation with this design is that the output voltage control is limited and cannot be controlled from zero to the rated value. On the other hand, this topology allows for greater output voltage than the input (boost operation). Finally the problems associated with phase angle control such as low efficiency and high switching stress on the switching device remains.

The Type1-B configuration is shown in Figure 6.7 (b). This design has different characteristic namely the output voltage is proportional to the firing angle and the PF is less sensitive to variation in the firing angle. The power factor is generally higher than

Type1-A design and its fairly independent of the firing angle. Therefore it is possible to control the output voltage without the expense of decreased power factor. The output voltage can be control from zero right up to the rated value. It was shown that the THD is under approximately 5% for the entire range of firing angle.

The third configuration, the Type1-C is shown in Figure 6.8 (a). This configuration has a more elaborate resonant network, comprising of C_p, C_s, L_p, L_s and L_m. Although at first, the resonant circuit appears complex, the 3 inductors can be integrated as part of the output transformer and therefore only 2 capacitors are required in the physical implementation. The inductors L_p and L_s is represented by the leakage inductance and L_m by the magnetizing inductance of the transformer. The circuit implementation of this topology is shown in Figure 6.8 (b). The characteristic curves of this design are similar to the Type1-B configuration described above.

Drobnik in [24] proposed a simple uncontrolled DC VRM to be used in telecommunication network as a local convertor for a HFAC power distribution bus. The design is shown in Figure 6.9. The only difference between the proposed design and regular rectifier circuit is the presence of the series LC resonant tank at the primary of the transformer. The purpose of the resonant network is for power factor improvement. The output voltage of this design however is not controllable and it is fixed at design time by the transformer winding ratio. While the series LC resonant network helps improve the power factor, the performance is load dependent. Therefore for fixed load this scheme could be tuned to provide acceptable power factor. A similar design has also been proposed by Jain, Cooper, et al [26] to be used in hybrid fibre/coax multimedia distribution networks.

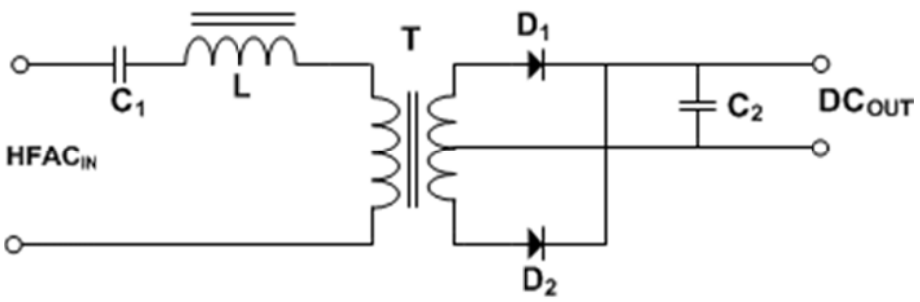


Figure 6.9 : Uncontrolled rectifier VRM (extracted from [24])

In 1996, Watson, Chen et al [28], suggested an improvement to the uncontrolled VRM presented in [24] by proposing a controllable inductor to replace the existing inductor in the original design. The new design is shown in Figure 6.10.

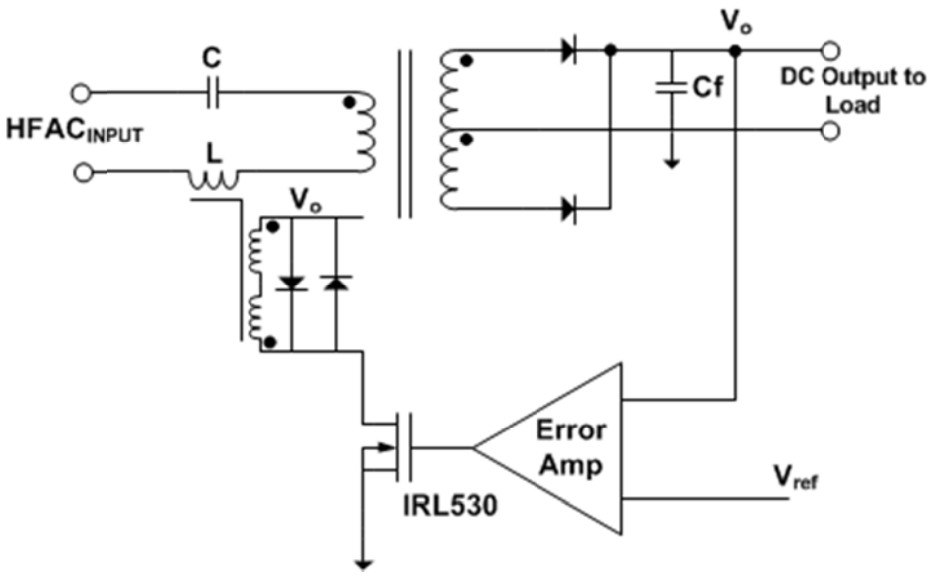


Figure 6.10 : Variable inductor controlled VRM (extracted from [28])

The output voltage is regulated by varying the impedance of the resonant network and this is achieved by varying the value of the resonant inductor. A current controlled inductor was used in this design where the inductance of the main coil is altered by changing the DC current through a control coil. The current through the control coil is regulated using an error amplifier that drives a mosfet connected in series with the control coil. The mosfet is driven in proportion to the error voltage thus the ON resistance (r_{ds}) of the mosfet is altered accordingly (linear operation region) to maintain the desired bias current. This simple control loop regulates the output voltage.

In 1997, Jain, Tanju et al [97] proposed a VRM based on a doubly tuned series-parallel resonant circuit as shown in Figure 6.11. The resonant circuit comprising of series and parallel tuned branches are tuned to the AC input voltage frequency (in this case 20kHz). The series resonant network (L_s and C_s) provides a low impedance path to the fundamental frequency of i_{RIC}, and high impedance to the harmonic frequencies of i_{RIC}. On the other hand, the parallel resonant network (L_p and C_p) offers low impedance

path to the harmonics of i_{RIC}. This helps to shape the current drawn from the bus by reducing the harmonic distortion.

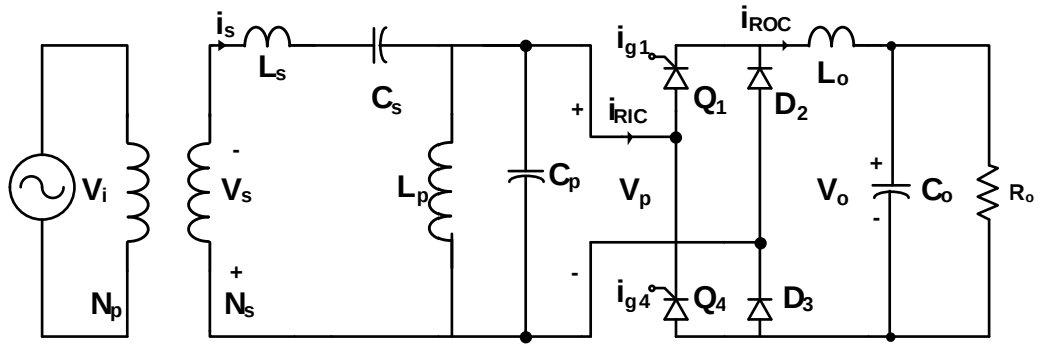


Figure 6.11 : DC VRM with LCLC resonant network (extracted from [97])

Two controlled rectifier, Q_1 and Q_4 are used to control the output voltage by using symmetrical phase control angle techniques that generates fundamental AC current that is in phase with the input voltage. The characteristic curve of the topology above is shown in Figure 6.12.

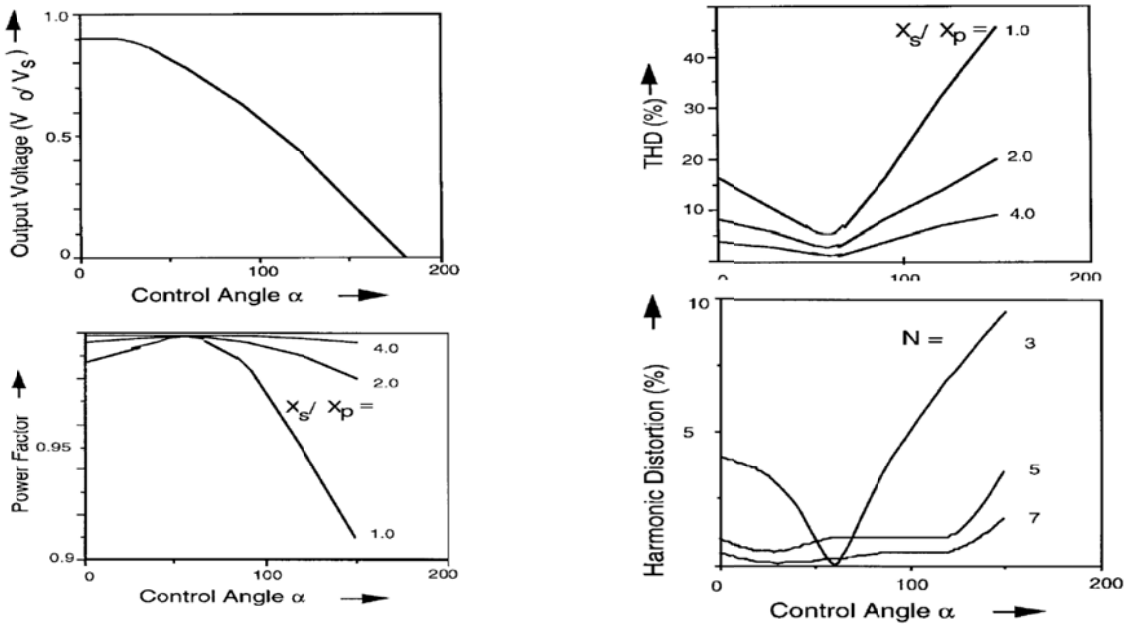


Figure 6.12 : Characteristic curve of LCLC resonant VRM (extracted from [97])

It can be seen that the output voltage is a function of α, and it can be controlled from a maximum value of 90% of the RMS value of the input voltage, to a minimum value of zero. From the THD curve, it appears that the lowest harmonic distortion occur at a

phase angle of about 60°. This coincides with the 3rd harmonic being close to zero at this point, which has the largest contribution to the THD. The THD is also lower for higher values of X_s/X_p ratio. The power factor curve also indicate close to unity power factor for α = 60°, and generally better for higher values of X_s/X_p. Therefore, based on the curves above, the recommended values for X_s/X_p and control angle is 4 and 60° respectively. It can be observed that for these values, the THD is very low and the power factor is close to unity. This design being based on phase angle control naturally has low efficiency and higher switching stresses. However the strength of this circuit lies in the good power factor and low THD for a wide range of α provided the resonant component values are carefully selected. Within this range, the output voltage can be controlled without having undesirable effects on the power factor.

Drobnik, Huang et al [29] in 1999, proposed a VRM as shown in Figure 6.13. This circuit is based very closely on an earlier design proposed by the same authors [24]. The resonant circuit at the primary consist of 2 capacitors in series with an inductor. Typically the value of the capacitor C_r is larger than C_{ac}. The series combination of C_r and C_{ac}, together form the resonant capacitor. In addition a bidirectional switch (composed of 2 inverse series connected FET) is connected across C_{ac}. In effect, the switch allows for C_{ac} to be a part of the resonant network or be shorted out. When the AC switch is completely turned OFF, the resonant network consists of the series combination of C_r & C_{ac} and inductor L_r. When the AC switch is turned ON, the resonant network consists of only C_r and L_r. Therefore the AC switch can be viewed as adjusting the average value of the series resonant capacitor. The control of the AC switch relative to the HFAC voltage has the effect of varying the voltage across to the transformer primary. This topology allows for output voltage control by varying the resonant frequency of the series resonant circuit

The AC bi-directional switch can be zero voltage switched, which reduces switching losses and subsequent allows for high frequency switching. During the turn-OFF transition, the current is shunted through the capacitor, and thus voltage rise across the switch is limited. The switch is turned ON during the positive half cycle of the AC voltage, when the capacitor voltage is driven towards zero; that is when it has fully

discharged. (V_{DS} = 0). At the secondary side, to achieve rectification, synchronous rectifiers are used for better efficiency. A similar design was later proposed again in [31, 33, 98]. In [33] a novel PWM control technique was proposed and it was shown that as long as the turn ON delay of the switch is set to be large enough, zero voltage switching can be achieved under wide load condition. In [98] an attempt to implement phase shift control was reported. Comparison between the PWM and phase shift control were drawn and it was concluded that the converter's performance in terms of power factor, total harmonic distortion, voltage stress of the switches and ZVS range are very similar. However under PWM control, the overall efficiency of the converter is higher compared to the phase shift control.

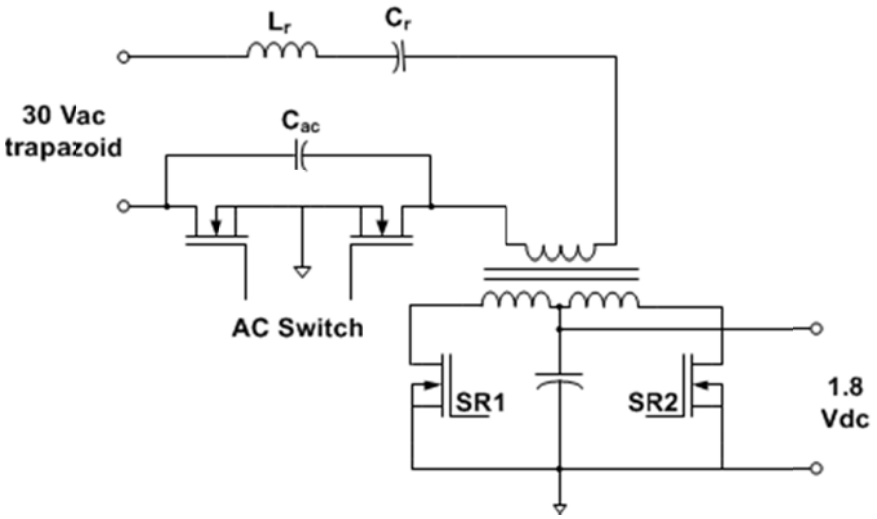


Figure 6.13 : Variable capacitor controlled VRM (extracted from [29])

In 2000, Luo, Gu et al in [2] proposed a VRM design for a square wave HFAC bus as shown in Figure 6.14. The design relies on a magnetic-amplifier to perform output voltage regulation. Post regulation using mag-amp is a fairly common method used on secondary taps of transformer with multiple output power rails. The mag–amp consists of a coil of wire wound on a core which has a relatively square B-H curve. This allows the core to operate in either unsaturated or saturated mode. In unsaturated mode, the core causes the coil to appear as a large inductor, capable of maintain a voltage difference across its terminal with limited current flow. In the saturated mode, the core saturates and the coil impedance drops. The coil now appears as a short circuit, allowing current to flow with negligible voltage drop across it.

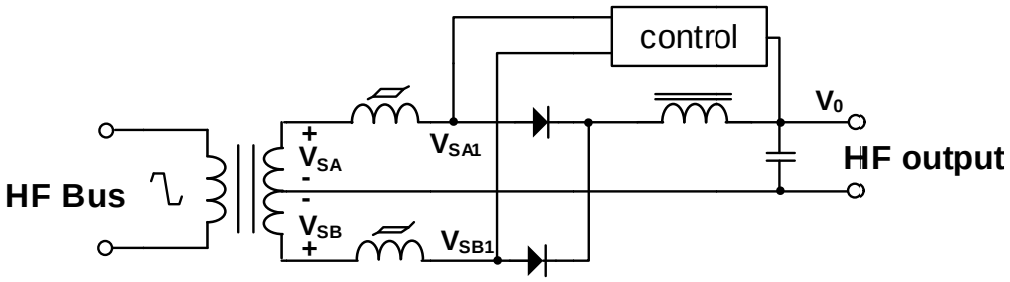


Figure 6.14 : VRM design with MAG-AMP (extracted from [2])

The control circuit samples the output voltage and injects a corresponding negative DC bias (with OR-ing diodes not shown) at V_{SA1} & V_{SB1} as shown in Figure 6.14. The injected DC source controls the core reset volt-sec during the negative cycle of the output. During the positive cycle, the voltage at the output of the coil (V_{SA1} & V_{SB1}) is delayed (remains at zero volts) for a duration t such that the positive volt-sec product balances the reset volt-sec during the negative cycle. After this duration, the coil saturates and $|V_{SA}|$ or $|V_{SB}|$ appears at the output terminal (V_o) for the rest of the positive cycle. The timing diagram for the operation of the mag-amp is shown in Figure 6.15.

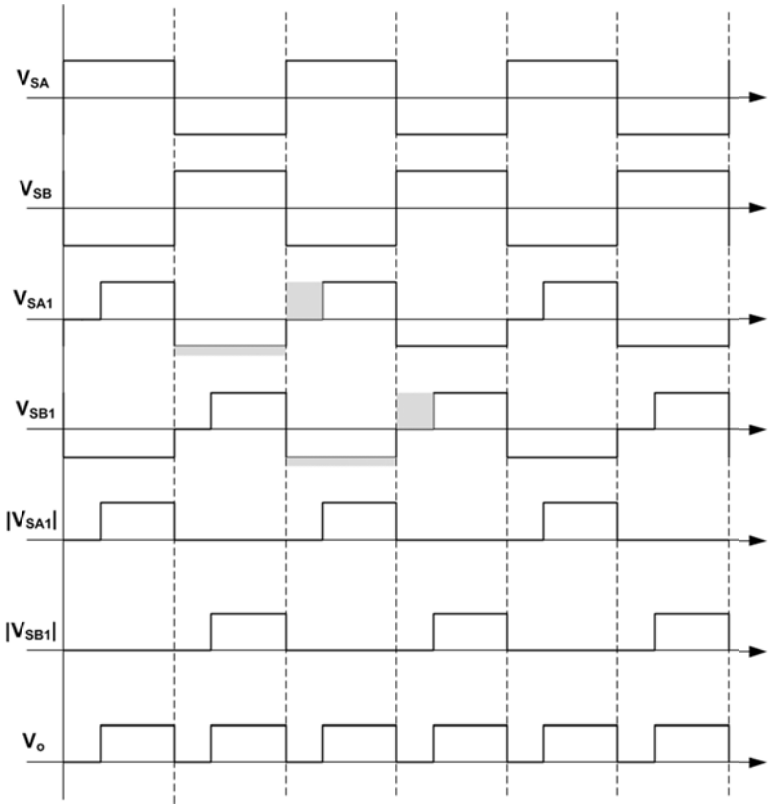


Figure 6.15 : Magnetic amplifier (Mag-Amp) timing diagram

6.2 Observation & Summary

Based on the discussion of the existing VRMs in the previous section, an attempt is made to logically classify available designs and identify the main challenges. In a HFAC VRM it is important to ensure that the current drawn from the bus has low distortion and is in phase with the bus voltage. Active power factor correction techniques often employed in low frequency application is not suitable for HFAC application. In active PFC circuits, the switching frequency needs to be in range of approximately 500 times higher than the bus frequency to be viable [96]. Therefore in HFAC application, the switching frequency will need to be prohibitively high to offer acceptable power factor improvement.

Passive power factor correction techniques utilizing tuned resonant input filters are the only available option for HFAC VRM application to date. Passive PFC techniques are not very appealing for low frequency application (50/60Hz) mainly due to the large size of the filter components. However for HFAC application, depending on the bus frequency, the size of the filter components can be very small and thus can be an attractive option. Freeland in his PhD dissertation [99] offers an extensive treatment on the subject of input current shaping of rectifiers using passive filters. Although his work was focused on low frequency mains application (50/60Hz), all the theoretical concepts are directly applicable for HFAC implementation. In a more related work, Vorperian et al in [100] have demonstrated the viability of using passive power factor correction technique in a HFAC VRM operating at a bus frequency of 20kHz.

In the simplest form the DC VRM can be represented by the block diagram shown in Figure 6.16. The resonant filters can take various form such as series resonant circuit [24, 26, 28, 33, 96], parallel resonant circuit [31, 96] or series parallel resonant circuit [97]. As discussed previously each of these configurations have unique characteristics in terms of THD, power factor, voltage conversion ratio and load sensitivity.

VRMs can be broadly classified as controlled and uncontrolled types. The uncontrolled types are in the form shown in Figure 6.16, where the output voltage is fixed at design time by selecting a suitable transformer turns ratio. In this type of VRMs, the output voltage cannot be dynamically controlled and are normally suitable only for the simplest loads. In some designs, post regulators are sometimes used to provide improved voltage

regulation. An example of uncontrolled VRM with a series regulator, shunt regulator and mag-amp based regulation are given in [37], [36] and [2] respectively.

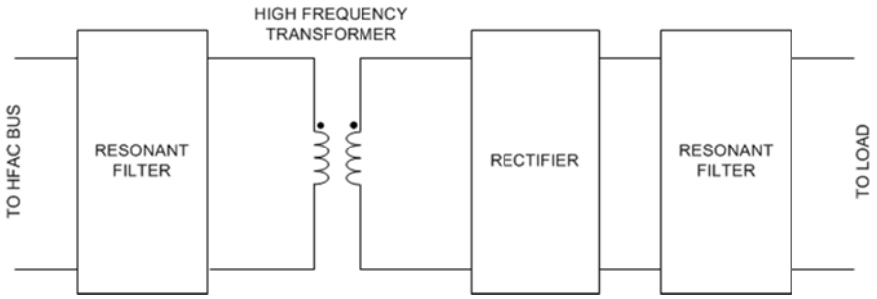


Figure 6.16 : Uncontrolled HFAC VRM with PFC

Controlled VRMs have provisions for active control of the output voltage. The control is normally attained using one of the 3 methods described below. The first technique is by phase angle control of the bridge rectifier. Normally a SCR or thyristor is used in place of diodes in the rectifier circuit and by controlling the firing angle; the average output voltage is controlled. Examples of this method are given in [55, 97]. The second technique involves using a current controller to shunt the current into the bridge rectifier. The current controller circuit consists of a bidirectional switch connected at the input of the rectifier stage. An example of this implementation is given in [96]. The main drawback of both the first and second technique proposed above is that the switches are hard switched and thus can be inefficient at high frequencies.

The third technique involves the control of the resonant frequency of the resonant input filter used for power factor correction. As the resonant frequency varies, the impedance of the resonant element changes and accordingly the voltage across the input of the rectifier circuit changes. The resonant frequency of the tuned filter is normally controlled by varying either the effective capacitance or the effective inductance of the circuit. Examples of this implementation are given in [29, 31, 33] and [28] respectively. This method offers the possibility of soft switching but the control of the output voltage is not independent of the power factor and THD.

Finally, another class of controllable VRM capable of generating both DC and low frequency AC output has been proposed in [15, 55, 95, 101]. Fundamentally these types of converters are variants of either half bridge or full bridge implementation of integral

cycle converters. Modelling and analysis of this converter has been presented in [102, 103]. The basic idea involves synthesizing a required output waveform using the HFAC sinusoids as a building block. The classification of all existing VRM is shown graphically in Figure 6.17.

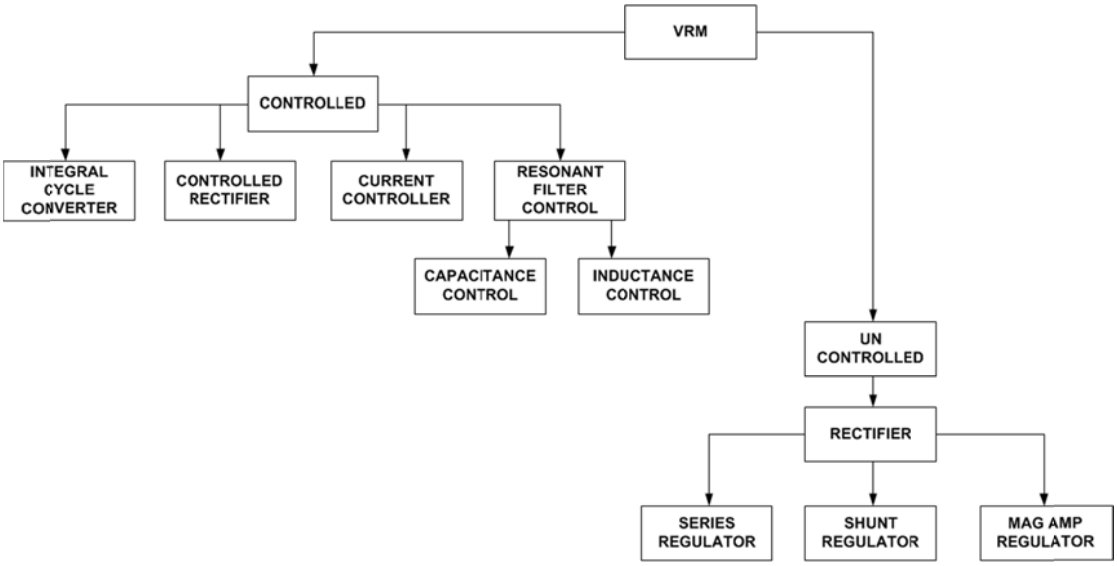


Figure 6.17 : VRM classification

6.3 Further Investigation

The research on HFAC VRM has been predominantly focused on DC output types and most of resonant rectification techniques employed in low frequency application can be adapted for HFAC application. The integral cycle converter based design however is unique to HFAC application. Although they have been proposed in the past as shown in the literature survey in section 6.1 there are some aspects of this converter that warrants further investigation. Primarily, it is interesting to understand the relationship between the harmonics composition of a synthesized output to the switching sequence.

To date, no mathematical model describing this relationship has been published. The aim of pursuing this path is to identify if there are preferred switching arrangement that may produce a desired harmonics spectrum while still meeting output voltage requirements. In other words, it can be shown that for a given average output voltage requirement; there are numerous ways the output can be synthesized. Each synthesized output has a

different harmonic spectrum. Understanding how best to select the switching arrangement is the goal of this study.

In the next section the analysis and design of the integral cycle converter to be used as a local point of load converter in a high frequency distributed power system is presented. In particular, a model for the ICC is developed to investigate the degree of distortion of the input current drawn from the bus, and to study the synthesized output voltage as a function of switching sequence. An intuitive method to estimate the effect of a given switching sequence on a particular harmonic component is proposed, and its application to the improvement of the power factor of an ICC is demonstrated.

6.4 Modelling of Integral Cycle Converter

As discussed in the previous section, the basic idea behind the ICC lies in synthesizing a low frequency AC or a DC output using a half cycle unit of the HFAC sinusoid as building blocks. An example of this process is illustrated in Figure 6.18. The output can be constructed with reasonable accuracy provided the frequency of the bus is at least higher than the required output by a factor of 20 [104].

Using this technique, the switching of the semiconductor switches in the converter is always limited at the voltage zero crossing and therefore the switching losses of the converter is reduced. In addition, the ability of the converter to synthesize low frequency AC as well as DC offers further advantage over soft switching resonant rectifiers that are only capable of generating a DC output. The switching network in a typical integral cycle converter consists of an arrangement of bidirectional switches that either allows a half wave unit of the high frequency sinusoid to pass through to the load or to be blocked from being presented to the load. There are typically two types of switching configurations, the half bridge and the full bridge. The differences between the two are discussed below. A low pass filter is used to extract the low frequency envelope of the synthesized signal and suppress the high frequency harmonics before it is presented to the load.

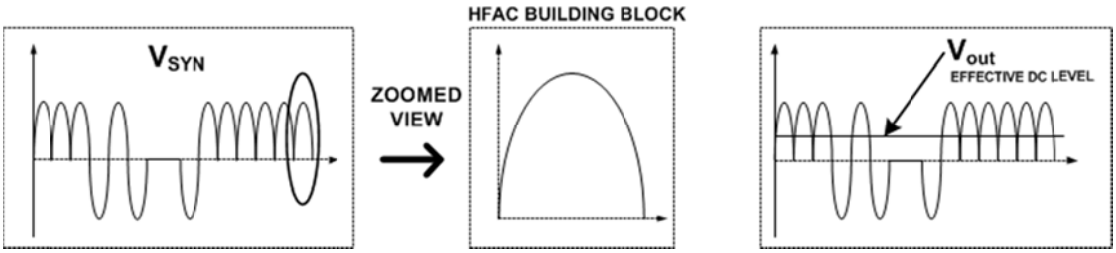


Figure 6.18 : Synthesis of DC voltage from HFAC bus voltage

6.4.1 Full Bridge Switching Stage

The full bridge switching network is similar to a H-bridge configuration consisting of 4 bidirectional switches. Each bidirectional switch consists of an inverse series connection of 2 mosfets. Thus a total of 8 mosfets are required to realize this configuration. These switches are turned ON or OFF at the zero crossing instants of the input bus voltage. At any given time it is possible to impress a positive or negative half wave sinusoid across the load by turning ON the corresponding leg of the full bridge. A zero voltage (absence of sinusoid) can be achieved by either turning ON both the top legs or both the bottom legs. Therefore this configuration allows for 3 state synthesis. The simplified circuit of the power stage is shown in Figure 6.19.

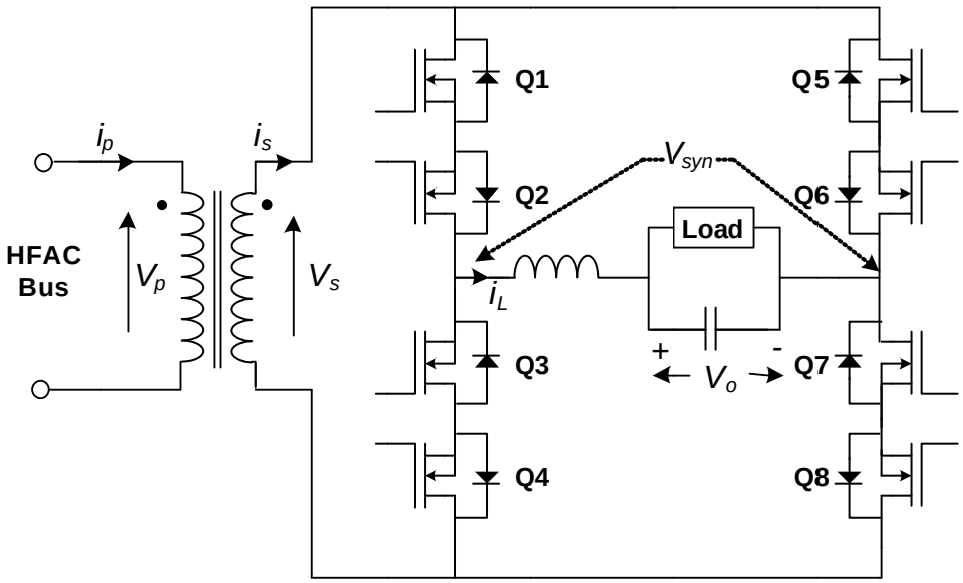


Figure 6.19 : Full bridge integral cycle converter

6.4.2 Half Bridge Switching Stage

The half bridge switching network shown in Figure 6.20 consists of 2 bidirectional switches and a center tapped transformer. Similar to the full bridge implementation, the bidirectional switches are realized using 2 mosfet connected in inverse series fashion. This configuration allows for either a positive or negative half wave sinusoid to be impressed across the load. It is not possible to impress zero voltage as this would require that both the top and bottom bidirectional switches be turned OFF simultaneously. This would disrupt the inductor commutation current path and mosfet damage could occur. The switching strategy for this configuration is discussed in details in [105]. In summary this configuration allows for 2 state synthesis.

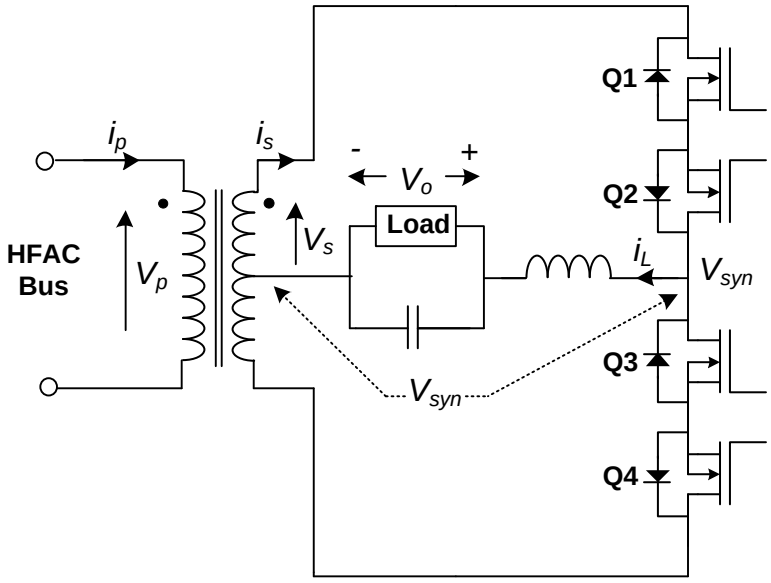
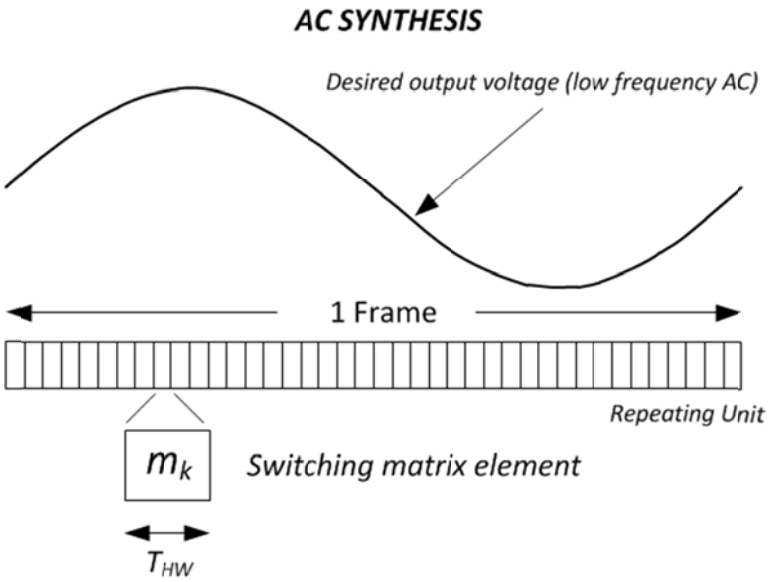


Figure 6.20 : Half bridge integral cycle converter

6.4.3 Output Voltage Synthesis

To mathematically model various aspect of the ICC with respect to the synthesis sequence, the switching sequence information is captured in the form a matrix called the switching matrix. The elements of the switching matrix can hold 3 possible values, a 1: representing a positive half wave sinusoid, a -1: representing a negative sinusoid and 0 representing a 0V output (absence of pulse). The switching sequence can be represented

as a $1 \times N_{FR}$ matrix as $[m_1, m_2 \ldots\ldots\ldots\ldots m_n]$. The variable N_{FR} denotes the total number of elements in the matrix and it called the frame length. It represents the number of sinusoids that are used to construct the output voltage. Therefore the length of the frame in time is equivalent to the duration of a half wave high frequency pulse multiplied by N_{FR}. For LFAC synthesis, the frame length and thus N_{FR} is constrained by the frequency of the desired output voltage. For a DC output voltage, there is some freedom in the selection of frame length. However it is important to keep in mind that the selection of N_{FR} dictates the maximum resolution of output voltage control.



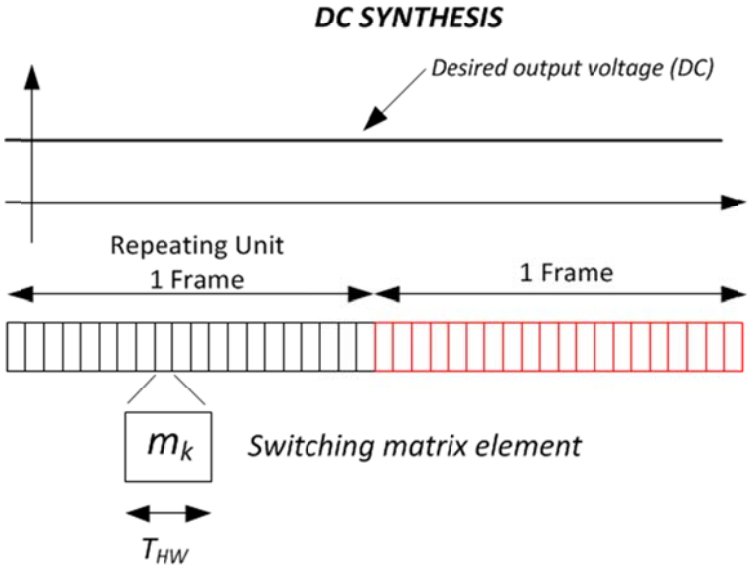


Figure 6.21 : AC & DC synthesis representation

For a given switching sequence, an expression of the synthesized voltage $V_{syn}(t)$ is given as follows.

$$V_{syn}(t) = \begin{cases} V_{s\_peak} m_1 \sin(2\pi f_{bus} t) & : 0 \le t < \dfrac{1}{2 f_{bus}} \\ -V_{s\_peak} m_2 \sin(2\pi f_{bus} t) & : \dfrac{1}{2 f_{bus}} \le t < \dfrac{1}{f_{bus}} \\ \vdots & \\ -V_{s\_peak} m_n (-1)^n \sin(2\pi f_{bus} t) & : \dfrac{(n-1)}{2 f_{bus}} \le t < \dfrac{n}{2 f_{bus}} \end{cases} \quad (6.1)$$

where

V_{s_peak} is the peak transformer secondary voltage,

n is the row index on the switching matrix,

m_n is the nth element of the switching matrix, and

f_{bus} is the frequency of the high frequency bus.

From (6.1) the average output voltage (after the low pass filter) can be calculated using (6.2). Note that the average output voltage is dependent only on the sum of the element in the switching matrix and not on the orientation of the elements within the matrix.

$$V_o = \frac{2V_{s\_peak}}{N_{FR}\pi} \sum_{n=1}^{N_{FR}} m_n \quad (6.2)$$

To determine the harmonic composition of a particular switching sequence, it is desirable to express the synthesized output voltage $V_{syn}(t)$ in the form shown in (6.3).

$$\begin{aligned} V_{syn}(t) = V_0 &+ V_1 Sin(\omega t + \phi_1) + V_2 Sin(2\omega t + \phi_2) + V_3 Sin(3\omega t + \phi_3) \\ &+ V_4 Sin(4\omega t + \phi_4) \ldots\ldots\ldots + V_x Sin(n\omega t + \phi_x) \end{aligned} \quad (6.3)$$

In (6.3), ω represents the angular frequency of the synthesized output, dictated by the frame length N_{FR} and is calculated using (6.4). It can be inferred from this equation $(N_{FR}/2)$ th harmonics of V_{syn} is equal to the bus frequency (f_{bus}).

$$\omega = \frac{4 f_{bus} \pi}{N_{FR}} \tag{6.4}$$

The DC component, V_0 in (6.3) is given in (6.2). To calculate the harmonic amplitude, the Fourier series coefficients, a_x and b_x are calculated and given in (6.5) to (6.7). For the case where $x = N_{FR}/2$, $a_x = 0$ and b_x is given by (6.5)

$$b_x = \left(\frac{V_m}{N_{FR}} \right) [m_1 - m_2 + m_3 - m_4 + m_5 - m_6 .....] \tag{6.5}$$

For the case where $x \neq N_{FR}/2$

$$a_x = J \begin{bmatrix} m_1 + (m_1 + m_2)\cos(\pi A) + (m_2 + m_3)\cos(2\pi A) + \ldots \\ \ldots + (m_{N_{FR}-1} + m_{N_{FR}})\cos((N_{FR} - 1)\pi A) + m_N \cos(N_{FR}\pi A) \end{bmatrix} \tag{6.6}$$

$$b_x = J \begin{bmatrix} (m_1 + m_2)\sin(\pi A) + (m_2 + m_3)\sin(2\pi A) + \ldots \\ \ldots (m_{N_{FR}-1} + m_{N_{FR}})\sin((N_{FR} - 1)\pi A) + m_{N_{FR}} \sin(N_{FR}\pi A) \end{bmatrix} \tag{6.7}$$

Where $A = \frac{2x}{N_{FR}}$ & $J = \left(\frac{V_{s\_peak}}{N_{FR}\pi} \right) \left(\frac{2}{1 - A^2} \right)$

The amplitude V_x and phase angle φ_x of the x_{th} harmonic can be calculated in the usual way using the coefficient a_x & b_x.

6.4.4 Harmonic Spectrum

From (6.2) it can be seen that the DC component of a synthesized waveform depends on the peak voltage of the sinusoid V_{s_peak}, the frame length represented by N_{FR} and the sum of all the elements is the switching matrix. In practice, the values of V_{s_peak} and N_{FR} are decided at design time. At run time, the DC voltage is regulated by manipulating the switching matrix element. It is obvious that the exact position of the 1, 0 and -1 in the switching matrix does not affect the DC output voltage. However based on equations

(6.5) to (6.7) it can be observed that the harmonic amplitude does depend on the distribution of the 1,0 and -1 in the switching matrix. This implies that for a required DC output voltage, there are a finite number of ways the voltage can be synthesized with each switching pattern having different harmonic spectrum.

Equations (6.5) to (6.7) allows the harmonic content to be calculated analytically. Therefore it is possible to compute the best switching sequence that would give the lowest amplitude for a particular harmonic, for a given DC output requirement and frame length. Although it is relatively easy to write an algorithm to accomplish such a requirement, fundamentally the process in which this is done involves working out the harmonic amplitude for all the permutations of the switching matrix and selecting one that meets the desired criteria. Whilst this can be computed relatively quickly by a computer for reasonable frame length, it does not provide any insights on how the elements of the switching matrix affect a particular harmonic amplitude. As such it is only useful for applications with fixed voltage requirements, where the optimal switching pattern is computed at design time. However for dynamic loads that require constant regulation, the harmonic spectrum needs to be computed online each time the output voltage needs to be changed. This is often not feasible and thus another simpler and real-time implementable method is needed.

For the case where the harmonic frequency x to be suppressed is equal $N_{FR}/2$, equation (6.5) dictates that its best to group similar polarity pulses consequently in pairs such that their summation cancels out and do not contribute to increase in harmonic amplitude. For the case where x is not equal to $N_{FR}/2$, the effect that a particular switching has on the harmonic amplitude is not immediately obvious. To best understand this, it is useful to graphically represent the discrete values of $\cos(n\pi A)$ vs n. This gives a representation of the magnitude contributed by a_x. Similarly a plot of $\sin(n\pi A)$ vs n gives an indication of the magnitude contribution of b_x.

Suppose in this design it is desired that the 2nd harmonic be kept as low as possible. To determine the switching restriction in this case, the $\cos(n\pi A)$ and $\sin(n\pi A)$ terms corresponding to the magnitude of a_x and b_x is plotted as shown in Figure 6.22 & Figure 6.23. From these figures, it can be observed that switching elements must be selected

such that the matrix elements should be altered in pairs [1,11] [2,12,] [3,13] [4,14] [5,15] [16,26] [17,27] [18,28] [19,29] [20,30] [21,31] [22,32] [23,33] [24,34] [25,35] [26,36] [27,37] [28,38] [29,39] [30,40]. As the peak magnitude of the $\cos(n\pi A)$ element is given as $[m_n + m_{n+1}]$. Therefore for the first pair in the sequence [1,11] it is necessary to ensure that $m_1 + m_2$ equals $m_{11} + m_{12}$. In this manner, any changes cancel out each other and do not contribute to the increase in harmonic amplitude.

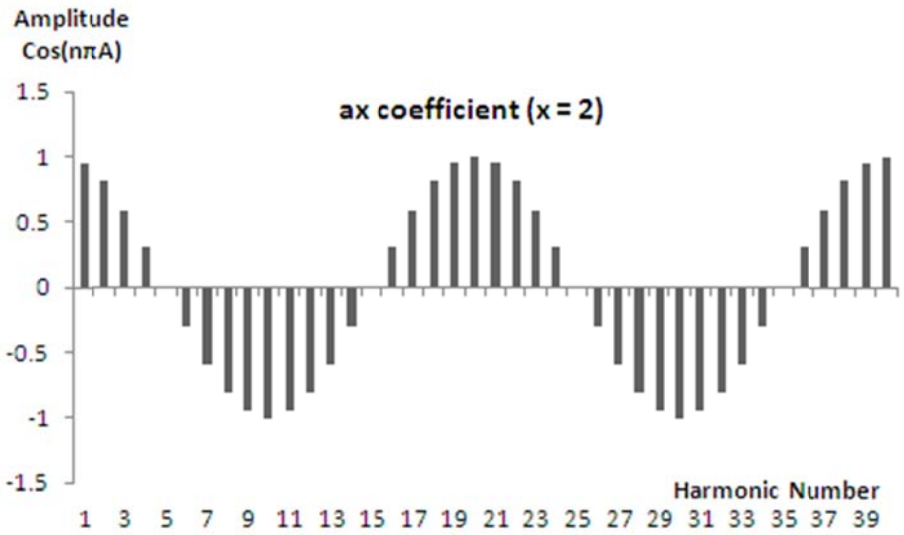


Figure 6.22 : Discrete plot of cos(nπA) vs n for x = 2

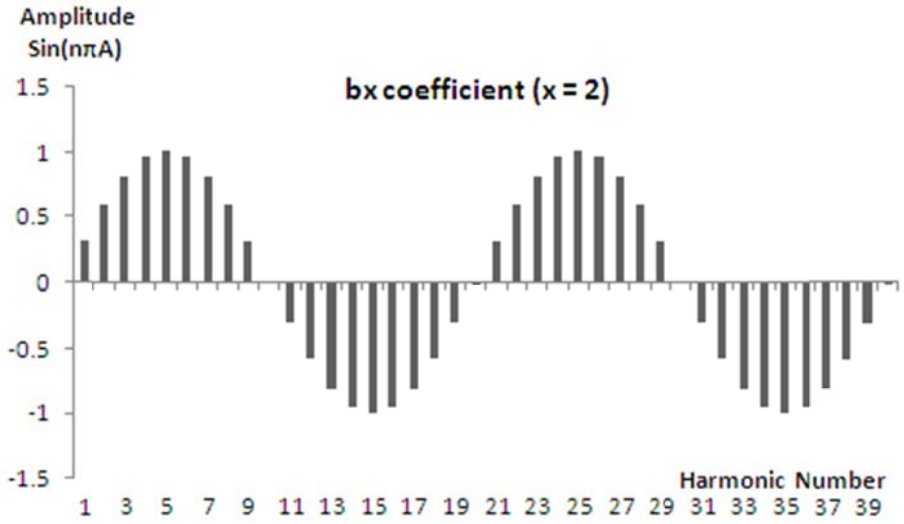


Figure 6.23 : Discrete plot of sin(nπA) vs n for x = 2

With this insight, it is now possible to implement the control using simple rule base algorithm instead of calculating the harmonics spectrum using (6.5) to (6.7) , which is computationally intensive. The rule based algorithm can be easily implemented in real time. However it is important to note that in cases where it is necessary to ensure the amplitude of two different harmonics be simultaneously low, the flexibility on the control may be reduced. In some cases, it may not be mutually exclusive. Therefore in such cases the selection of N_{FR} needs to be reconsidered to achieve the best possible results

6.4.5 Modelling Input Power Factor

Firstly the required peak voltage at the transformer secondary is determined by finding V_{s_peak} that satisfies (6.8).

$$\left(\frac{2V_{s\_peak}}{\pi}\right) > V_0 \tag{6.8}$$

Using the calculated V_{s_peak} value, the transformer turns ratio can be calculated such that $\left(n_p/n_s\right) < \left(V_{bus\_peak}/V_{s\_peak}\right)$ is satisfied. The turns ratio is then rounded to an integer value. With this selection the maximum and minimum synthesizable DC output voltage is recalculated. The selection of frame length N_{FR} depends on the minimum resolution of output voltage that is required. A large value for N_{FR} allows for finer control of the output voltage but also reduces the fundamental frequency. This can lead to difficulties in filtering out the undesired harmonic component. Once N_{FR} is determined, the fundamental harmonic of the frame can be calculated using (6.4). The LC filter should therefore be designed to have a cutoff frequency of approximately 10 times less than the frame frequency to sufficiently reject the high frequency harmonics. If the inductor L_f is selected to be sufficiently large, the current through it can be considered to be constant and its value can be calculated using (6.9)

$$I_L = \left[\frac{2V_{s\_peak}}{N_{FR}\pi}\sum_{n=1}^{N_{FR}} m_n\right]\left[\frac{1}{R_L}\right] \tag{6.9}$$

The transformer primary current is given by (6.10)

$$i_p(t)=\begin{cases}+I_L\dfrac{n_s}{n_p}m_1-i_{p\_DC} & :\ 0\le t<\dfrac{1}{2f_{bus}}\\ -I_L\dfrac{n_s}{n_p}m_2-i_{p\_DC} & :\ \dfrac{1}{2f_{bus}}\le t<\dfrac{1}{f_{bus}}\\ \vdots & \\ +I_L\dfrac{n_s}{n_p}(-m_n)(-1)^n-i_{p\_DC} & :\ \dfrac{(n-1)}{2f_{bus}}\le t<\dfrac{n}{2f_{bus}}\end{cases} \tag{6.10}$$

Where $i_{p\_DC}=\dfrac{I_L}{N_{FR}}\dfrac{n_s}{n_p}\sum_{n=1}^{N}(-m_n)(-1)^n$

To represent the primary transformer current in the frequency domain, the Fourier coefficients can be calculated using (6.11) to (6.12).

$$a_x=K\left[\begin{array}{l}\left(m_1+m_2\right)sin\left(\pi A\right)-\left(m_2+m_3\right)sin\left(2\pi A\right)+\ldots\\ \ldots\left(m_{N_{FR}-1}+m_N\right)sin\left((N_{FR}-1)\pi A\right)-m_{N_{FR}}sin\left(N_{FR}\pi A\right)\end{array}\right] \tag{6.11}$$

$$b_x=K\left[\begin{array}{l}m_1-\left(m_1+m_2\right)cos\left(\pi A\right)+\left(m_2+m_3\right)cos\left(2\pi A\right)-\ldots\\ \ldots-\left(m_{N_{FR}-1}+m_N\right)cos\left((N_{FR}-1)\pi A\right)+m_{N_{FR}}cos\left(N_{FR}\pi A\right)\end{array}\right] \tag{6.12}$$

where $K=\left(\dfrac{1}{\pi x}\right)\left(\dfrac{n_sV_0}{n_pR}\right)$

The RMS value of the primary current can be expressed by (6.13).

$$i_{p\_RMS}=\frac{I_L}{N_{FR}}\frac{n_s}{n_p}\sqrt{N_{FR}\sum_{n=1}^{N_{FR}}(m_n)^2-\left[\sum_{n=1}^{N_{FR}}m_n(-1)^n\right]^2} \tag{6.13}$$

As the bus voltage is a pure sinusoid with frequency f_{bus} only the harmonic component of the current with the same frequency as the bus frequency delivers power to the load.

The harmonic number of the current with frequency f_{bus} is $N_{FR}/2$. The peak amplitude of this harmonic is given in (6.14) and the corresponding phase shift is calculated to be equal to zero.

$$i_{p\_peak(f=f_{bus})} = \frac{4}{N_{FR}\pi}\left(\frac{n_s}{n_p}\right)\left(\frac{V_0}{R_L}\right)\left(\sum_{n=1}^{N_{FR}} m_n\right) \tag{6.14}$$

The average power of the primary side of the transformer can be computed using (6.15)

$$P_{avg} = \frac{4V_{s\_peak}{}^2}{\pi^2 N_{FR}^2 R_L}\left[\sum_{n=1}^{N_{FR}} m_n\right]^2 \tag{6.15}$$

Using (6.13) and (6.15), he power factor can be computed to yield the expression in term of the switching matrix element as in (6.16)

$$PF = \frac{\frac{2\sqrt{2}}{\pi}\sum_{n=1}^{N_{FR}} m_n}{\sqrt{N_{FR}\sum_{n=1}^{N_{FR}} m_n{}^2 - \left[\sum_{n=1}^{N_{FR}} m_n(-1)^n\right]^2}} \tag{6.16}$$

For the half bridge switching network where only -1 and 1 are allowed in the switching matrix, further simplification can be made to (6.16). The first term in the denominator can be simplified as shown in (6.17) for the HBICC. It can be seen that this terms of the equation is determined simply by the frame length and changing this would change the resolution of synthesis.

$$N_{FR}\sum_{n=1}^{N_{FR}} m_n{}^2 = N_{FR}^2 \tag{6.17}$$

The numerator term of (6.16), is simply dictated by the required output DC voltage. Manipulating this term would change output voltage as predicted by (6.2). To yield maximum power factor, the second term in the denominator must be as large as possible. This term will always be less than N_{FR}^2 and the exact value will depend on the orientation of the 1's and -1's in the switching matrix.

It becomes immediately obvious that if similar polarity pulses are aligned next to each other, they cancel out. The pulse sequence in Figure 6.24 shows this condition. This is generally not desirable as it minimizes the value of the second term in the denominator. The maximum value for this term is attained when opposite polarity pulses are present consecutively as shown in Figure 6.25. The value of this term for both optimized and the worst case orientation is given by (6.18) and (6.19) respectively.

$$\left[\sum_{n=1}^{N_{FR}} m_n(-1)^n\right]^2 = \left[N_{FR} - \sum_{n=1}^{N_{FR}} m_n\right]^2 \tag{6.18}$$

$$\left[\sum_{n=1}^{N_{FR}} m_n(-1)^n\right]^2 = 0 \tag{6.19}$$

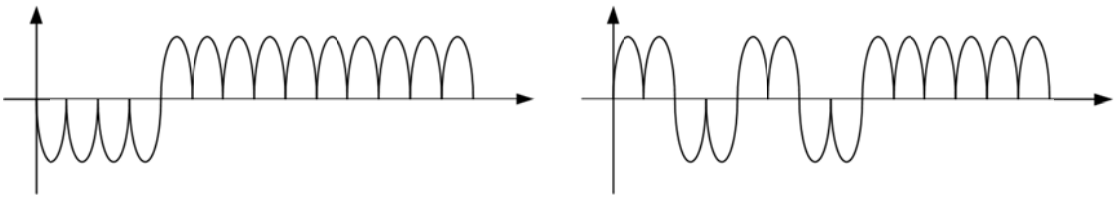


Figure 6.24 : Switching sequence with low power factor

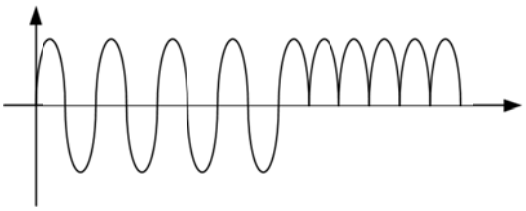


Figure 6.25 : Switching sequence with maximum power factor

With optimized orientation, the maximum attainable power factor is given in (6.20). Conversely the worst case power factor is given by (6.21). For both arrangements, the maximum attainable power factor is limited by $2\sqrt{2}/\pi$ and this is achieved only when V_0 is at the maximum possible value of $2V_{s\_peak}/\pi$. The power factor can be poor for low V_0 value and thus may draw distorted current form the bus when operating in this condition. The plot of the power factor vs output voltage for both the condition is shown in Figure 6.26.

$$PF = \sqrt{\frac{8V_0}{\pi\left[4V_{s\_peak} - V_0\pi\right]}} \tag{6.20}$$

$$PF = \sqrt{2}\,V_0 / V_{s\_peak} \tag{6.21}$$

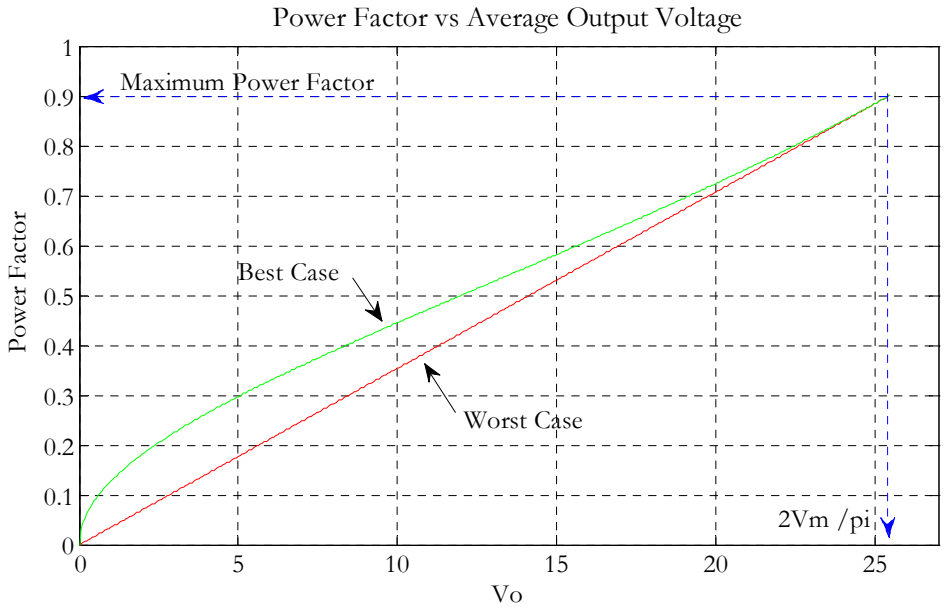


Figure 6.26 : Power factor vs DC output voltage

6.4.6 Improving Power Factor

As discussed in section 6.2 resonant input filters are often used to shape the input current. In general some variant of a band pass filter is used to filter out the harmonics of the primary current from reaching the source. By means of an example, it is shown in this section how the appropriate selection of the pulse orientation helps to relax the constraint imposed on the input filter design.

The harmonics spectrum of the transformer primary current waveform near the vicinity of the bus frequency is shown in Figure 6.27. The harmonic number $N_{FR}/2$ corresponds to the bus voltage frequency. To offer best performance, it is therefore necessary to ensure that the harmonics closest to the bus frequency $(N_{FR}/2)-1$ and $(N_{FR}/2)+1$ are eliminated or are sufficiently attenuated.

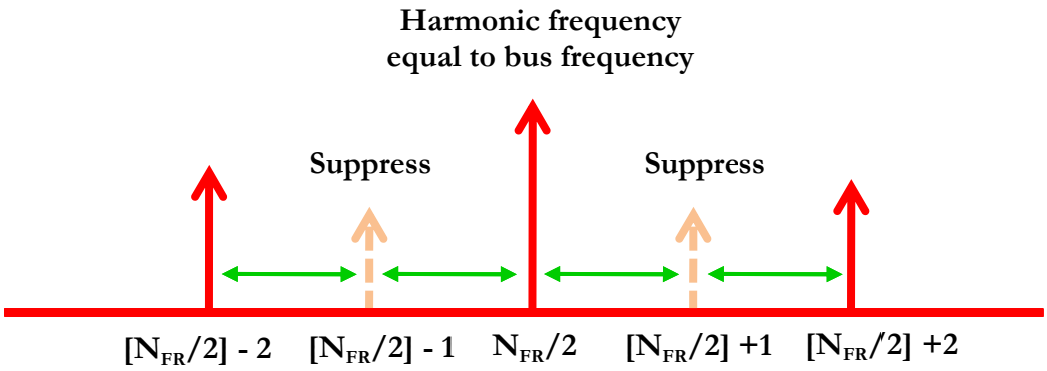


Figure 6.27 : Harmonic spectrum of transformer primary current

For the case where the frame length is 40 ($N_{FR} = 40$), the 20th harmonics is equal to the bus frequency and therefore the harmonics to be eliminated is the 19th and the 21st. The $\cos(n\pi A)$ and $\sin(n\pi A)$ terms vs n are plotted for x = 19 and x = 21 in Figure 6.28.

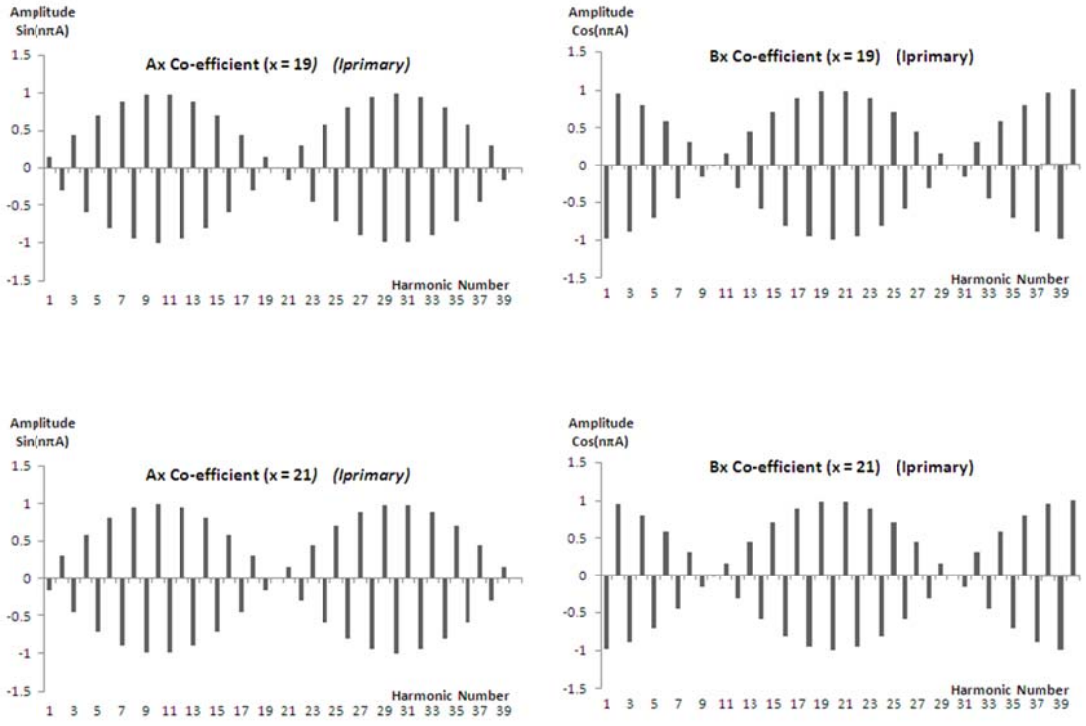


Figure 6.28 : Plot of cos(nπA) & sin(nπA) for x =19 & 21

From this plot, it can be observed that the k_{th} and $(k+20)_{th}$ component are the corresponding pair that have equal but opposite magnitude. So the pulse orientation shall be selected such that the element $(m_k + m_{k+1})$ is equal to $(m_{k+20} + m_{k+21})$ to ensure that the 19th and 21st harmonics are eliminated. Figure 6.29 and Figure 6.30 show an optimal

and worst case switching orientation respectively. Both of this sequence has the same DC output voltage. The first sequence is designed to eliminate the 19th and 21st harmonic to improve the power factor. And the 2nd sequence is deliberately selected such that both the 19th and 21st harmonics are enhanced. Pspice simulation of the synthesized waveform for both the switching sequence is shown in Figure 6.31 & Figure 6.32.

m_1	m_2	m_3	m_4	m_5	m_6	m_7	m_8	m_9	m_{10}
-1	1	-1	1	-1	1	-1	1	1	1
m_{11}	m_{12}	m_{13}	m_{14}	m_{15}	m_{16}	m_{17}	m_{18}	m_{19}	m_{20}
1	1	1	1	1	1	1	1	1	1
m_{21}	m_{22}	m_{23}	m_{24}	m_{25}	m_{26}	m_{27}	m_{28}	m_{29}	m_{30}
-1	1	-1	1	-1	1	-1	1	1	1
m_{31}	m_{32}	m_{33}	m_{34}	m_{35}	m_{36}	m_{37}	m_{38}	m_{39}	m_{40}
1	1	1	1	1	1	1	1	1	1

Figure 6.29 : Optimal switching sequence

m_1	m_2	m_3	m_4	m_5	m_6	m_7	m_8	m_9	m_{10}
1	1	1	1	1	1	1	1	1	1
m_{11}	m_{12}	m_{13}	m_{14}	m_{15}	m_{16}	m_{17}	m_{18}	m_{19}	m_{20}
1	1	1	1	1	1	1	1	1	1
m_{21}	m_{22}	m_{23}	m_{24}	m_{25}	m_{26}	m_{27}	m_{28}	m_{29}	m_{30}
-1	-1	-1	-1	-1	-1	-1	-1	1	1
m_{31}	m_{32}	m_{33}	m_{34}	m_{35}	m_{36}	m_{37}	m_{38}	m_{39}	m_{40}
1	1	1	1	1	1	1	1	1	1

Figure 6.30 : Worst Case switching sequence

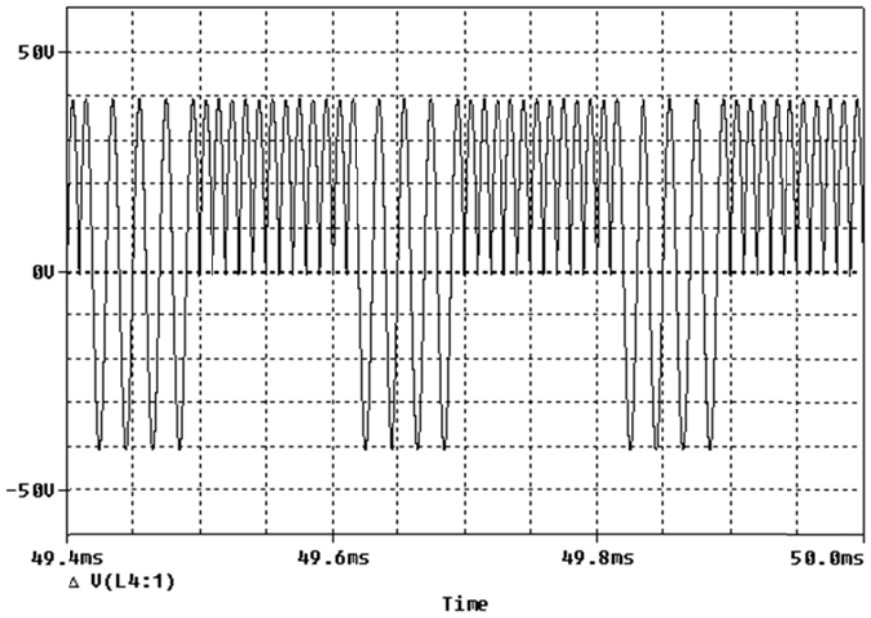


Figure 6.31 : Vsyn - Optimal switching sequence

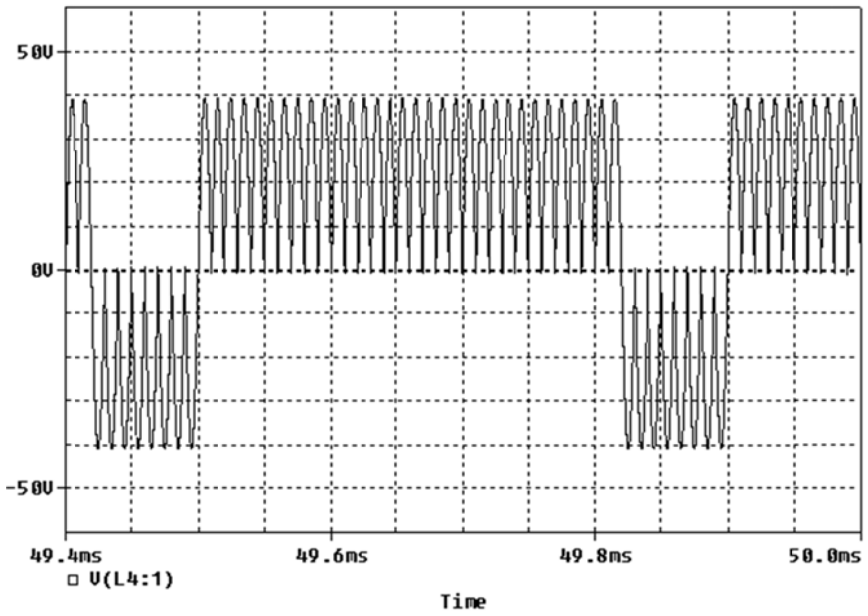
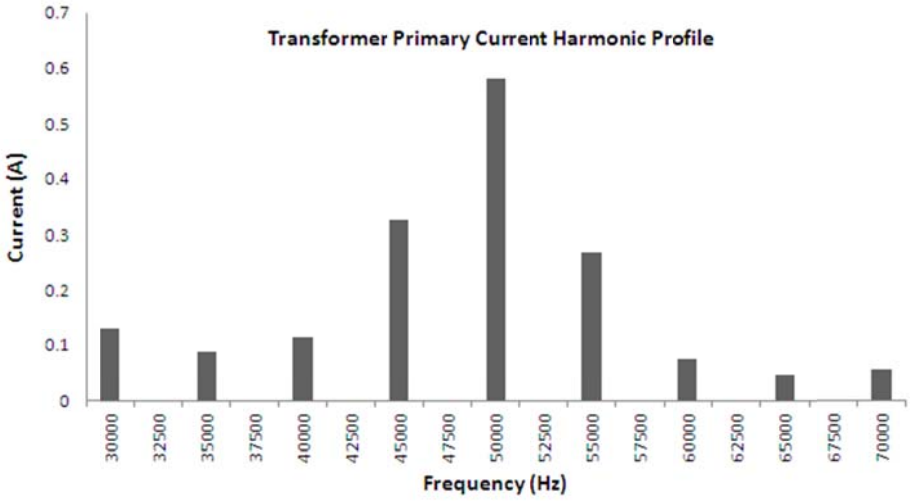


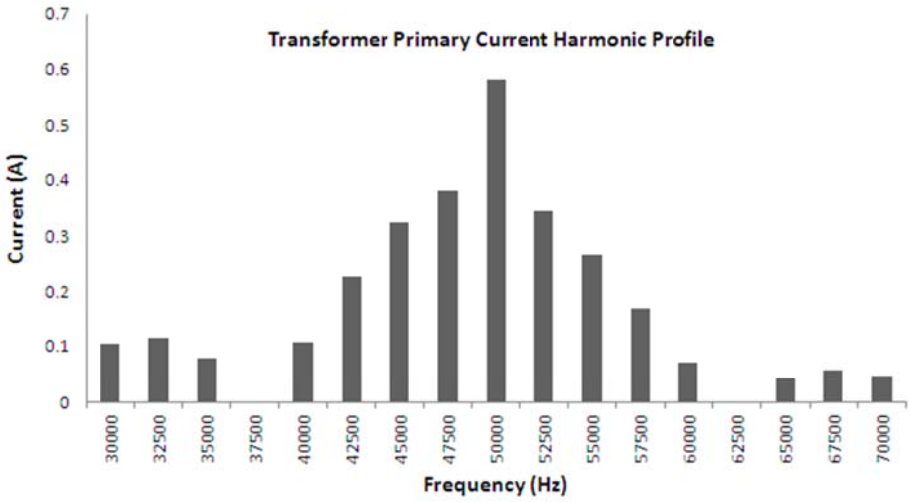
Figure 6.32 : Vsyn - Worst case switching sequence

The harmonic spectrum of the primary current for the optimal and worst orientation calculated using the analytical model presented above is shown in Figure 6.33 (a) and (b) respectively. A PSPICE simulation result of the transformer primary current waveform and harmonic spectrum is shown in Figure 6.34 & Figure 6.35 for both cases. It can be seen that the orientation of the sinusoids in the synthesized output voltage has important

harmonics implications. Selecting an optimal sequence helps to improve current distortion and relaxes the constraint on the design of the input resonant filter.

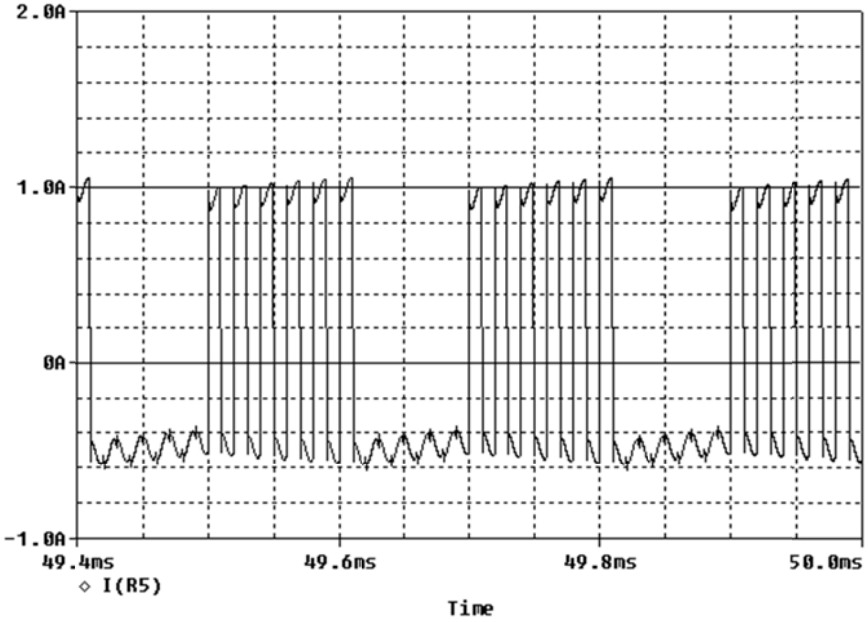


(a) Optimal

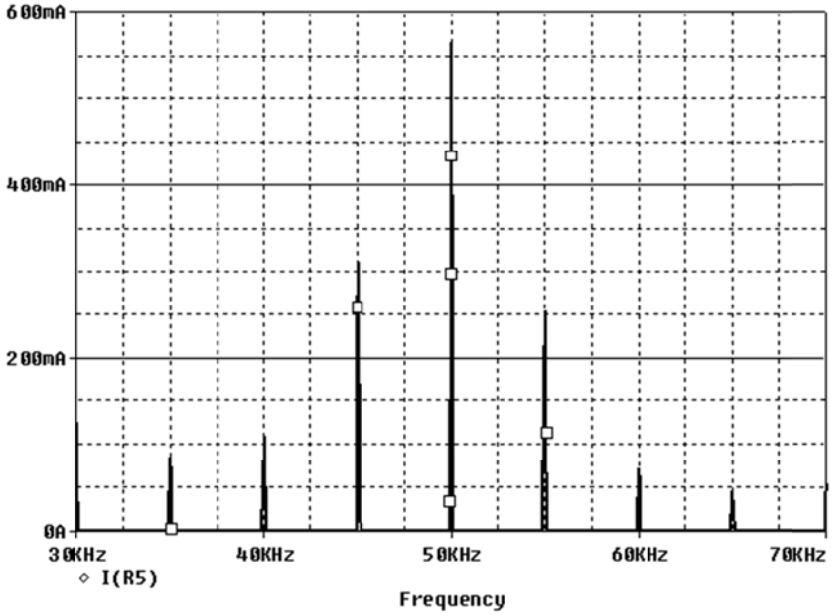


(b) Worst case

Figure 6.33 : Harmonic spectrum of transformer primary current – (analytical model)

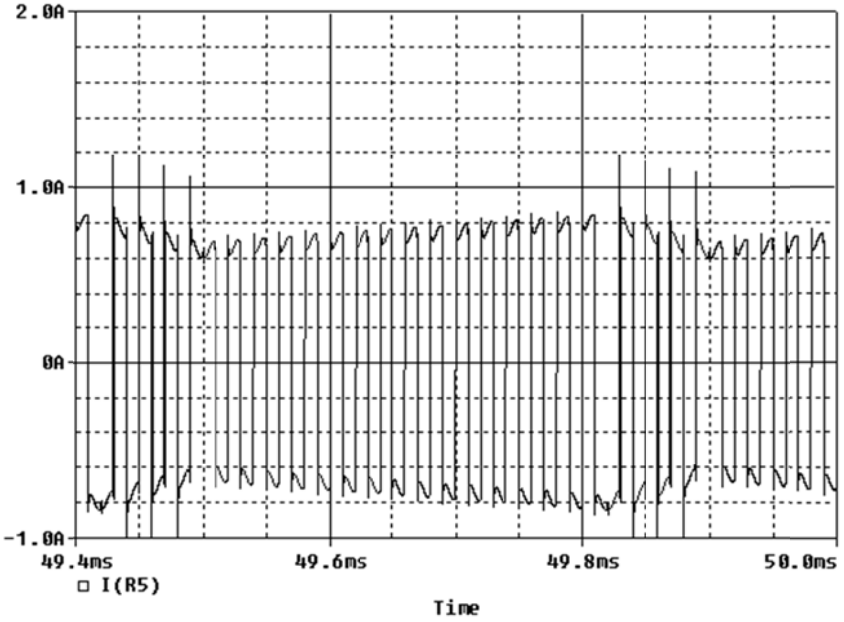


(a) Time domain waveform

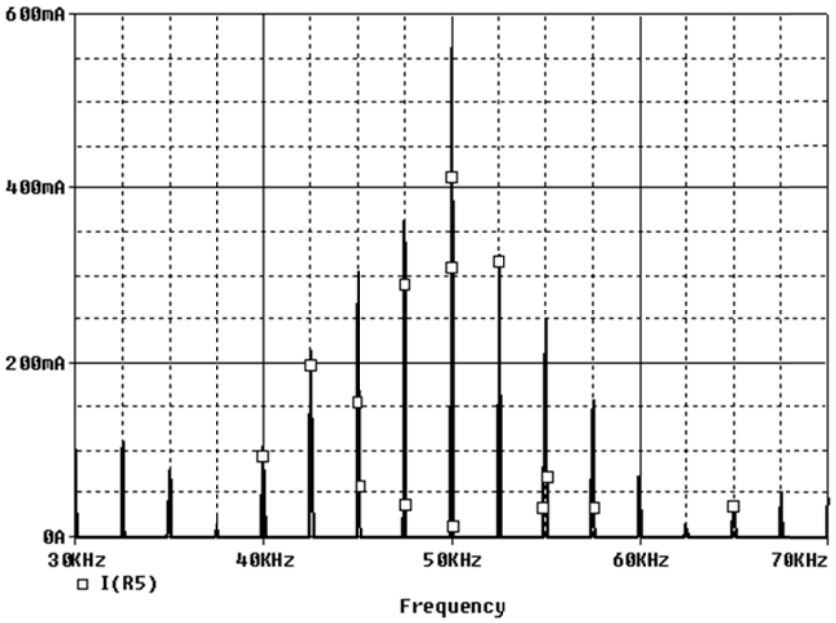


(b) Harmonic spectrum

Figure 6.34 : Transformer primary current – (optimal sequence)



(a) Time domain waveform



(b) Harmonic spectrum

Figure 6.35 : Transformer primary current – (worst case sequence)

6.5 Concluding Remarks

In this chapter, a thorough appraisal of VRM topologies proposed in literature was undertaken and the advantages and disadvantages of each topology were addressed. Existing designs were then logically classified and it was recognized that most designs were derived variants of resonant rectifier topologies. The ICC on the other hand was unique to HFAC DPS and was identified as an attractive contender for further investigation. In this chapter, a complete mathematical model relating the pulse switching orientation to the resulting harmonic composition was developed. It was shown that selecting a proper orientation can reduce distortion in the input current and help to relax the constraints imposed on the design of the input filter

CHAPTER 7

DATA OVER HFAC DPS

"The important thing in science is not so much to obtain new facts as to discover new ways of thinking about them" – ***Sir William Bragg, 1862-1942.***

The primary requirement for intelligent management of a distributed power system lies in the ability to control power flow based on real time information about the state of the system. The key enabling feature to realize this requirement is the creation of a communication framework that allows the various sources and loads in the system to communicate seamlessly with each other. This chapter explores the means by which this can be achieved effectively and efficiently, without the need for installation of additional physical communication channels. This approach has the advantage of being compatible with existing HFAC DPS whereby communication capabilities can be retrofitted with minimal effort as the need arises. The development of the required hardware and communication protocol forms the main part of this work with strong emphasis on circuit level implementation. As a proof of concept, a data modem capable of bidirectional communication over the HFAC bus was built and the communication capability was experimentally demonstrated over a current fed HFAC system.

7.1 Overview

In this chapter the means to enable communication in a HFAC DPS is investigated. Using separate communication channel offer a convenient means to enable communication between the various subsystems, however in most cases the requirement for additional dedicated wiring is not always desirable. Wireless communication technology such as Zigbee, can be used in these cases but this often involves high cost. A third alternative is to explore communication over the existing HFAC power line by overlaying communication signals over the HFAC bus voltage. This dispenses the need for additional wiring. Although communication over traditional 50/60Hz power line has been around for a long while, no attempts of its implementation on HFAC DPS have been reported in literature. There are many complete one chip silicon solutions for traditional power line communication that comprise the physical and data link layers [106-109]. These solutions cannot however be used directly for data over HFAC implementation. As such this chapter is focused on the design of a custom HFAC power line modem to demonstrate the possibility of overlaying communication signal over the HFAC power bus. Attaining the ability to communicate over the HFAC bus presents interesting possibilities for intelligent management and monitoring of the power system.

7.2 Fundamental Requirements

The fundamental requirement for the data modem is illustrated in Figure 7.1. The basic function of the modem is to enable bidirectional communication capability over the HFAC bus. In the transmit mode, the modem is required to process the raw digital command and convert it to a suitable form to be injected into the HFAC bus. In the receiving mode, the modem extracts the communication signal from the bus and processes it to reconstruct the digital message that was originally transmitted. This must be achieved without interruption to the power flow of the HFAC DPS.

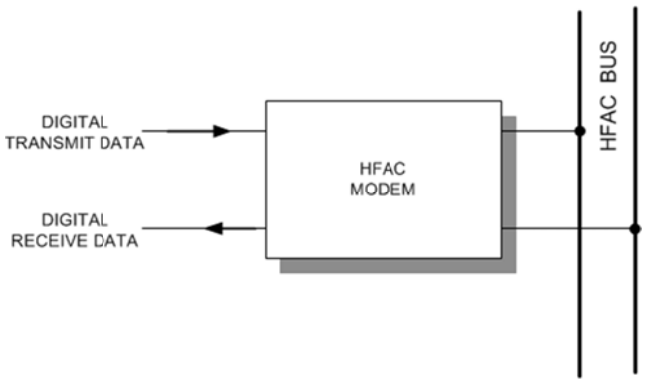


Figure 7.1 : Fundamental requirement of HFAC data modem

In a typical HFAC network, it is anticipated that there would be many subsystems all communicating with each other over the same HFAC bus. It is therefore possible that data collision could occur if two or more modems are simultaneously transmitting. This would lead to data corruption or failed transmission. It is therefore necessary that some form of bus arbitration mechanism is implemented to ensure that collisions are avoided and detected if they do happen.

As the communication is required mainly for telemetry purposes, the required data bitrate is relatively low. A data rate of less than 1kbps is sufficient for most application. Another desirable feature is for the modem to be compatible with both voltage and current fed HFAC system. Before proceeding to the detailed design of the modem, two important design considerations need to be first addressed. The first is related to the choice of data encoding technique and next the choice of modulation scheme. These are covered in the following sections.

7.2.1 Data Encoding

As the data is transmitted over the existing power bus which consists of only two conductors, the data would need to be asynchronously transmitted. The microcontroller naturally generates the transmit data in NRZ format. Without an accompanying clock signal, the detection of NRZ encoded data at the receiving end can be challenging especially when long strings of '1s' or '0s' are transmitted. Any drift in the clock generator at the receiving end could cause a bit slip and corrupt the received data. Figure

7.2 shows an example of such a case. In summary NRZ is not self-clocking and the clock frequency component is not present in the NRZ spectrum.

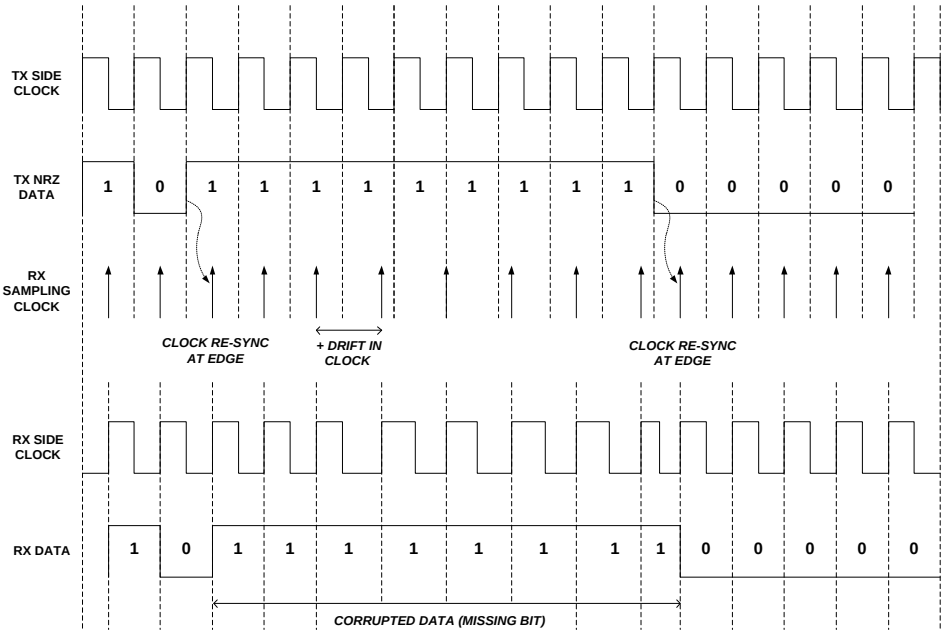


Figure 7.2 : NRZ data transmission & recovery

One way to overcome this problem would be use the HFAC bus voltage frequency as a synchronizing clock. At the transmit side, the NRZ data is generated in synch with the 50kHz HFAC bus voltage/current. At the receiving end, the clock signal can be derived from the bus voltage using a simple comparator circuit which can then be used to retime the received NRZ data. This solution can eliminate the bit slip problem even if deviation in the bus frequency exists.

This seemingly simple solution has some limitations. Firstly the transmission bit rate is dependent on the bus voltage frequency. The absolute maximum achievable bit rate is equal to 1 bit per period of the bus voltage. Lower bit rates (integer ratios of bus frequency) are possible but require additional circuitry. Next, the synchronization of the transmit data with the bus frequency would naturally require that data transmission begin at the zero crossing point of the bus voltage. This greatly increases the probability of data collision in a system with many communication nodes.

An alternate solution is to Manchester encode the NRZ data stream. In a Manchester encoded data a logic '1' is represented by a high to low transition and logic '0' by a low to high transition. These transitions occur at the midpoint of the data bit frame. Therefore there will be a guaranteed transition at the middle of every bit period regardless of the bit pattern of the digital stream being encoded. This method indirectly embeds the clock rate information within the transmitted data and therefore is self-clocking. This has great benefit in the clock recovery process at the receiving end. Using Manchester encoding, the data bit rate is not constrained by the bus voltage frequency and the data transmission need not be aligned with the zero crossing points of the bus voltage.

7.2.2 Digital Modulation

In order to be able to physically transmit the digital data over the power line, it would first need to be modulated. For low speed power line communication, frequency shift keying (FSK) or ON-OFF keying (OOK) it often the preferred choice. The primary advantage of using OOK is in its simple implementation. OOK can be easily generated using a cmos astable multivibrator. Detection and demodulation is also simple and be performed using a rectifier and peak detector circuit. OOK implementation for regular 50/60Hz power line communication is given in [110] and the proposed OOK circuit can also be used for HFAC implementation. The main disadvantage of OOK is that it is not compatible with multiple bus access systems. This is due to the inability to distinguish between 'no transmission' and logic zero transmission.

The modulation and demodulation circuitry of FSK is more complex that the OOK implementation. On the other hand it is compatible with multiple bus access system as a carrier signal is present during the transmission of both logic '1' and '0'. Therefore is it possible to identify if the bus is idle before a node decides to transmit information. Having identified a suitable encoding and modulation scheme, the detailed design of the hardware and software aspects of the modem can now be explored.

7.3 Modem Design

A complete block diagram of a proposed HFAC data modem is shown in Figure 7.3. At one end, the modem has a serial interface link to communicate with external systems. At the line end a coupling circuit is used to interface to the HFAC bus. In this section the circuit level implementation of the modem is discussed.

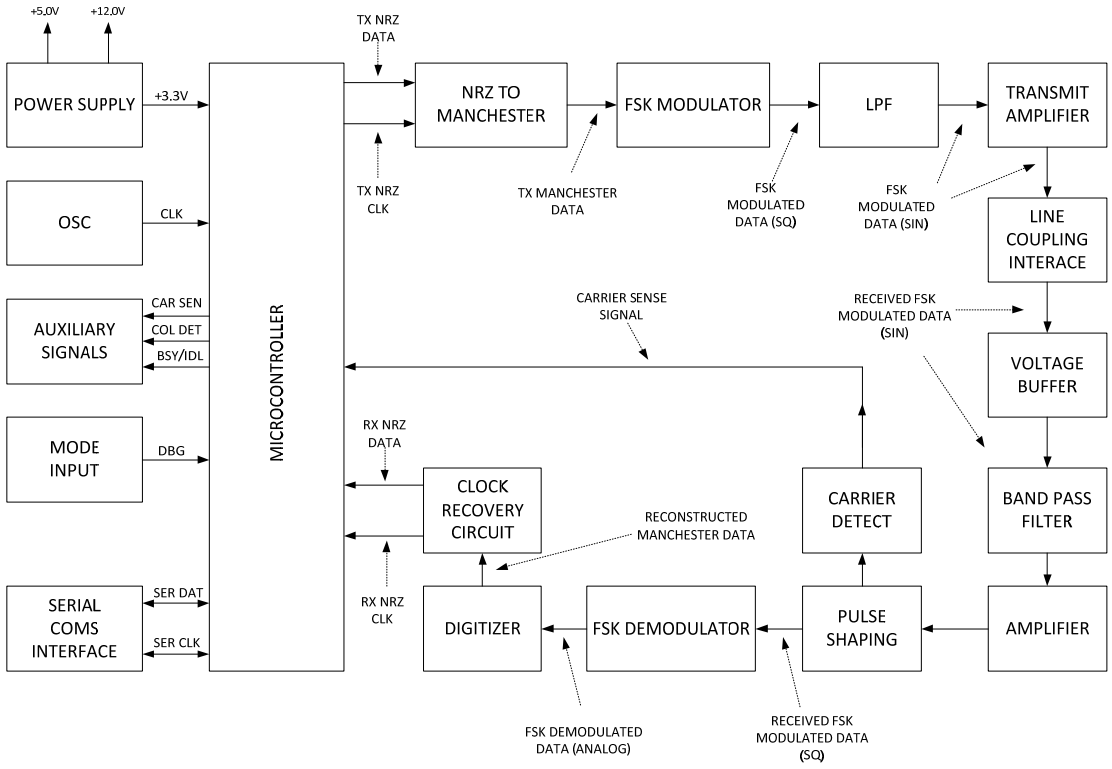


Figure 7.3 : Block diagram of HFAC data modem

7.3.1 NRZ to Manchester Encoding

The microcontroller generates the data to be transmitted in NRZ format and outputs two signals, NRZ_DATA and NRZ_CLK. In this design, the firmware supported bitrate of the NRZ data stream is shown in Table 7.1. The maximum bitrate is limited by the processor speed, software load and programming efficiency. The NRZ data is converted into Manchester code by using a XNOR logic gate with NRZ_DATA and NRZ_CLK as inputs. PSPICE simulation of the generation of Manchester code is shown in Figure 7.4. It can be verified from this figure that the Manchester encoded data always has transition in the middle of the bit period as described previously in section 7.2.1. It is important to

ensure that the generation of the NRZ_DATA and NRZ_CLK signals is implemented in a single instruction by the microcontroller. This requires that both these pins are assigned to the same port in the MCU. Individually setting NRZ_DATA and NRZ_CLK pin would introduce glitches in the Manchester data due to finite instruction execution time.

Supported Bit Rate	NRZ Clock Period
156250 bps	6.4 μs
78125 bps	12.8 μs
39062.5 bps	25.6 μs
19531.25 bps	51.2 μs
9765.625 bps	102.4 μs
4882.8125 bps	204.8 μs
2441.40625 bps	409.6 μs

Table 7.1 : Supported NRZ data stream bit rate

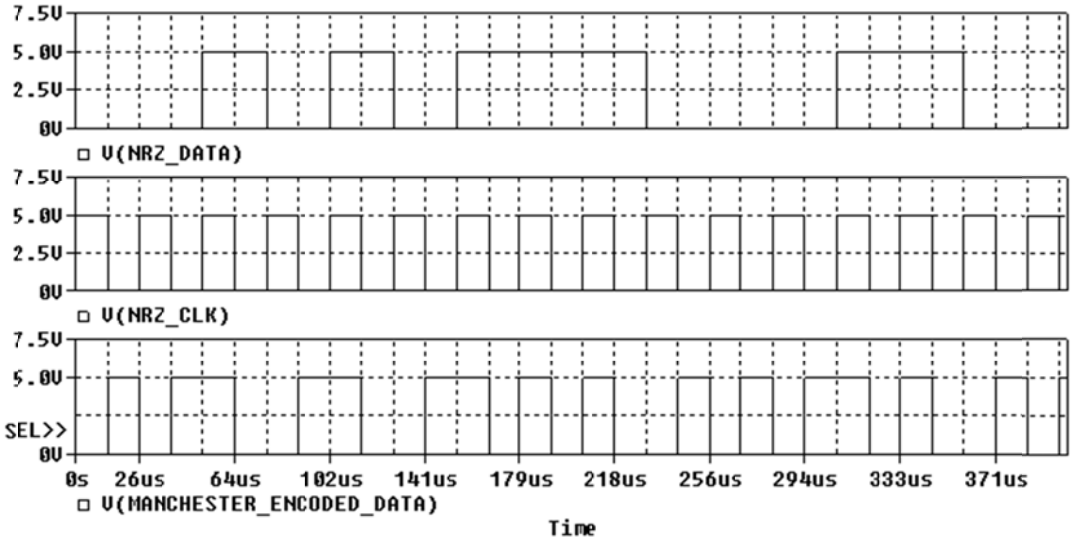


Figure 7.4 : NRZ to Manchester encoding (XNOR operation)

7.3.2 Frequency Shift Keying Modulator

As discussed in section 7.2.2, FSK modulation will be used in this design. The carrier frequency shall be selected such that the ratio between the carrier and the bus voltage frequency is as high as possible. The greater the ratio, the more relaxed the requirement for the coupling circuit becomes. In addition using high carrier frequency reduces the susceptibility of interference form the bus voltage. On the other hand, using too high a

frequency imposes constraint on the selection of opamps and power amplifier in the signal processing chain. High gain bandwidth opamps would be required and these can often be expensive.

On balance, a logic 1 and logic 0 carrier frequency of 12.5MHz & 10.5MHz was selected. FSK modulation can be implemented using any voltage controlled oscillator (VCO) with a suitable frequency range. In this case CD74HC7046A integrated circuit from Texas Instrument was used. This IC is in fact a complete PLL circuit, however in this implementation; the phase comparator and feedback loop were disabled. Effectively only the VCO section of the IC was used. This IC was selected due to the excellent VCO frequency linearity and at the time of design it was surprisingly cheaper than an equivalent VCO only IC. A simplified circuit level implementation is shown in Figure 7.5.

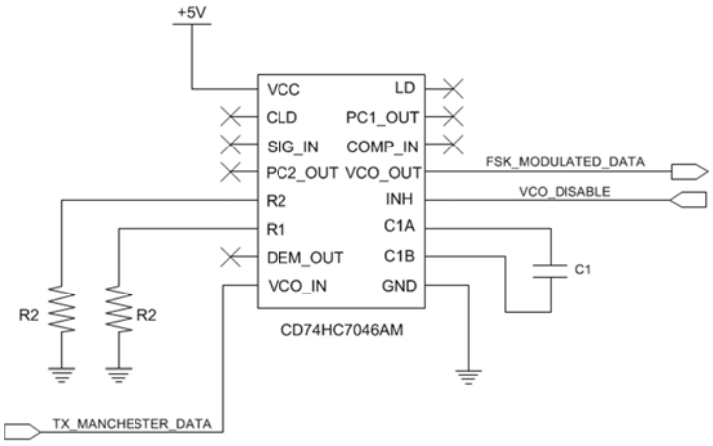


Figure 7.5 : FSK Modulator circuit implementation

The typical VCO frequency characteristic curve is shown in Figure 7.6. The values of R1, R2 and C1 should be selected in manner that shapes the VCO frequency curve to suit the input voltage range. At Vmin of 0V (logic 0 input) the value of fmin should be equal to 10.5MHz and at Vmax of 5V, fmax should be equal to 12.5MHz. The frequency range is determined by the values of R1 and C1 and the frequency offset is determined by the value of R2 [111]. In general for a given value of C1, the frequency range and offset frequency is inversely related to R1 and R2 respectively. In practice, for a desired offset frequency the value of R2 and C1 is first selected based on Figure 7.7 (a), then the value of R1 is determined from Figure 7.7 (b) for the desired frequency range.

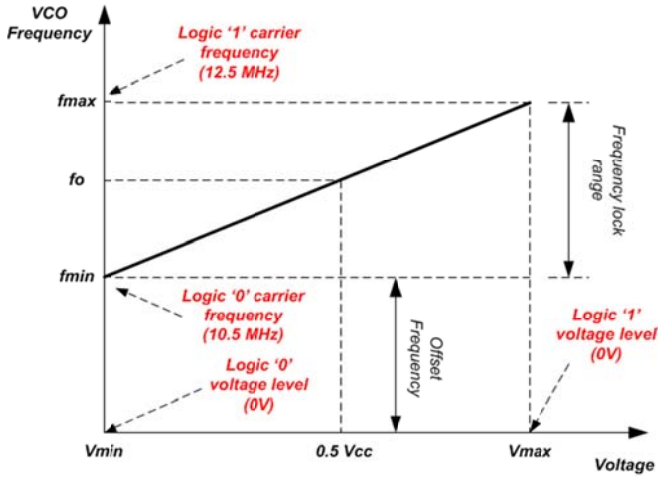
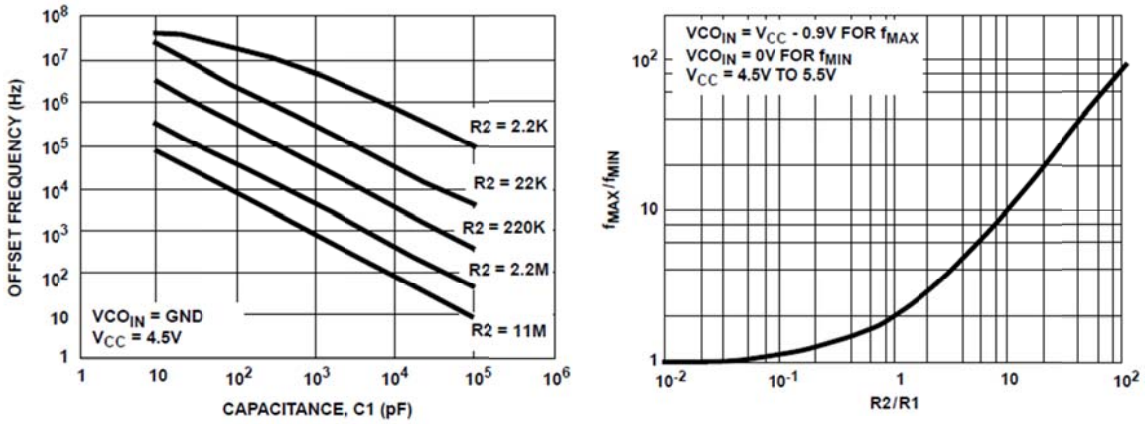


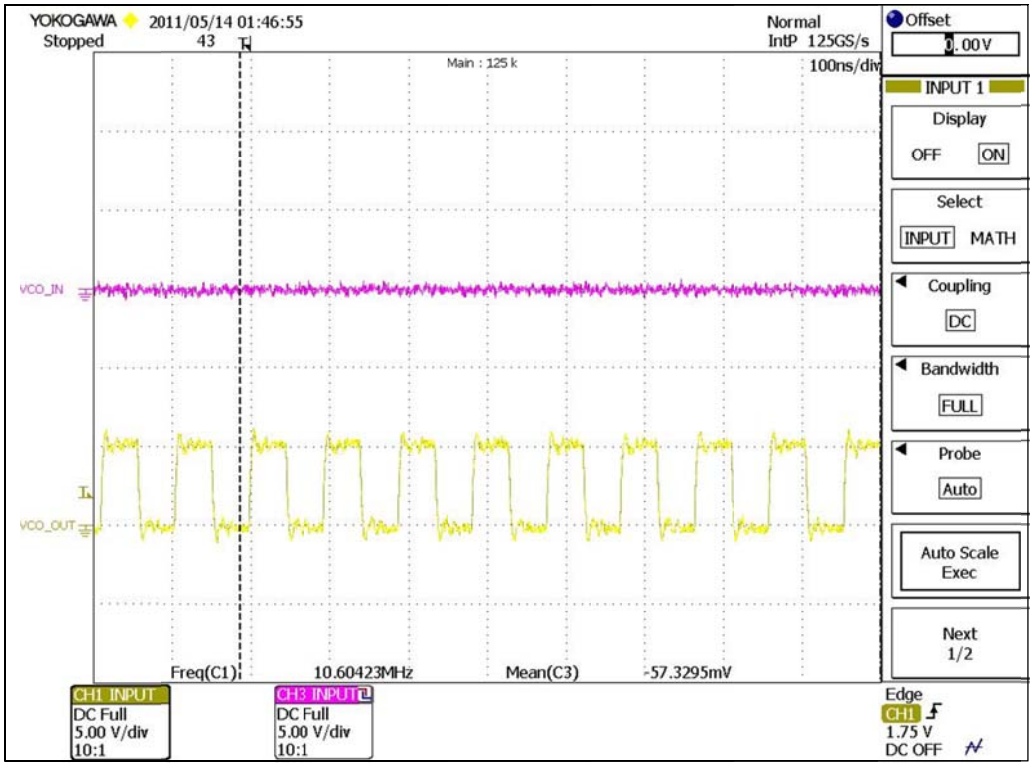
Figure 7.6 : VCO frequency characteristic curve



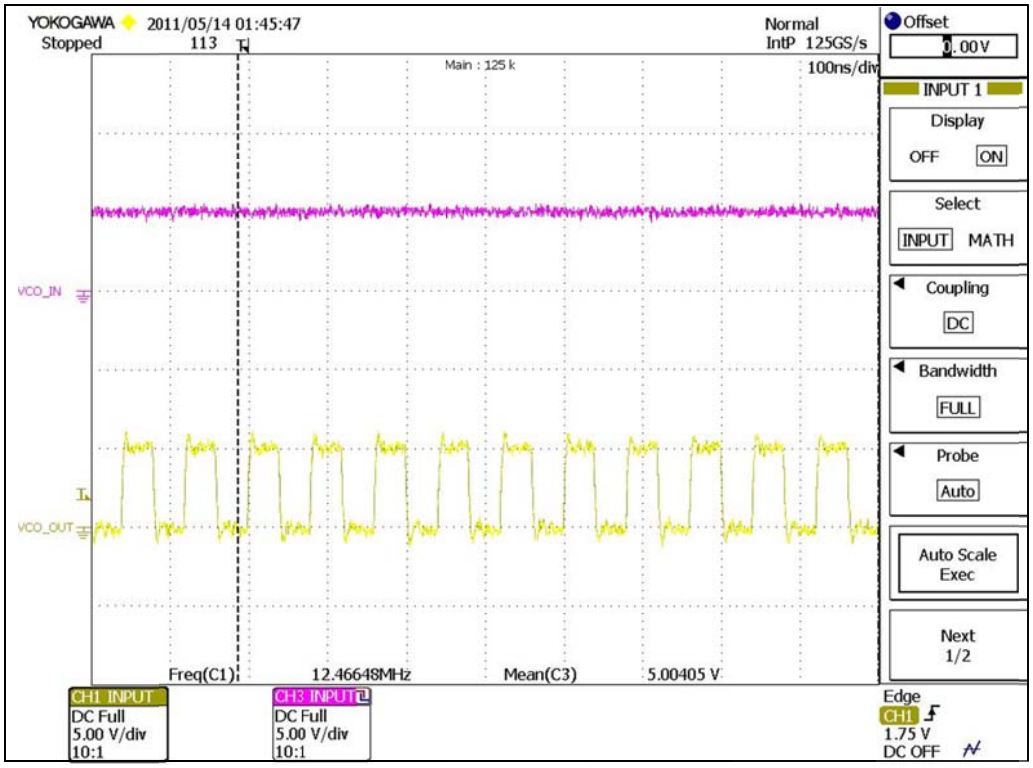
(a) (b)

Figure 7.7 : Performance curve - CD74HC7046A (extracted from [111])

In this design, the following values were used : R1 = 47kΩ, R2 = 10kΩ and C1 = 56pF. These measured VCO frequency for 0V and 5V input is shown in Figure 7.8 (a) & (b) respectively. From the figure, it can be seen that for logic 0 input, fmin was measured to be 10.60423MHz and for logic 1, fmax is equal to 12.46646MHz.



(a) Logic 0 input



(b) Logic 1 input

Figure 7.8 : VCO frequency measurement

7.3.3 Transmit Low Pass Filter

The FSK modulated signal from the VCO is a square wave with 50% duty cycle. A low pass filter is used to filter out all the high order harmonics and to generate a sinusoidal FSK modulated signal. The main requirement of the filter is a steep roll off rate to ensure the 3rd harmonic is sufficiently suppressed. In addition a small gain variation at 10.5MHz and 12.5MHz is desired to ensure uniform amplitude of both the carrier frequency. To meet this requirement, a 6th order Butterworth low pass filter (T-configuration) was used. The PSPICE frequency response simulation of the filter is shown in Figure 7.9(a). The frequency spectrum of the filtered output shown in Figure 7.9(b) confirms that both the design requirements stated above are sufficiently met.

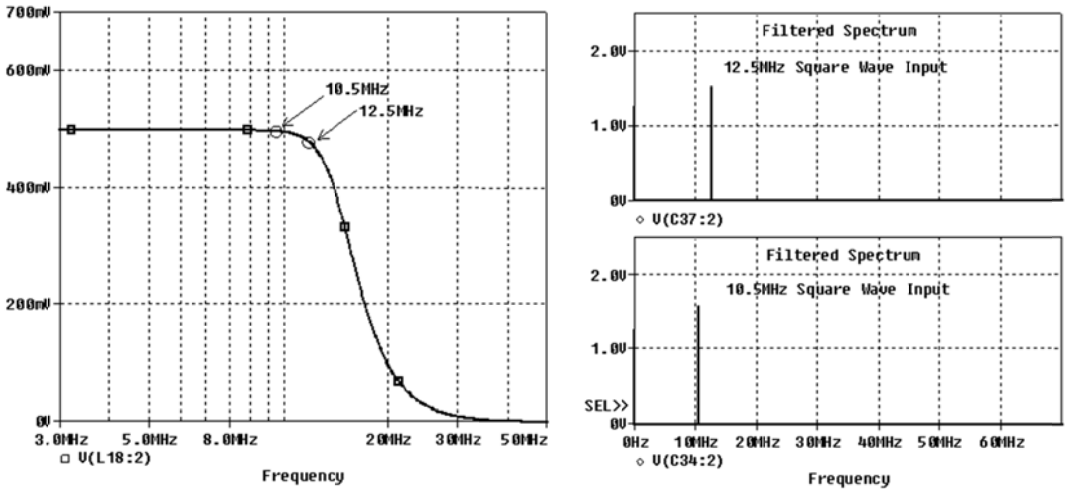


Figure 7.9 : Transmit low pass filter frequency response

7.3.4 Transmit Amplifier

The modulated FSK data will first need to be sufficiently amplified before it is injected onto the HFAC bus. A single stage inverting opamp with a class B push pull output stage is proposed. The impedance of the HFAC bus is often varying depending on the loading condition and under low impedance condition it can significantly load the transmit amplifier. The output stage is therefore necessary, to increase the current drive capability of the inverting amplifier.

The input to the inverting amplifier is AC coupled using C1. The gain of the amplifier is determined by the ratio of the feedback resistor to the input resistor and is given as $(-R_2 / R_1)$. The opamp used in this design has a gain bandwidth rating of 83MHz. Therefore the maximum gain that can be attained in this design is approximately equal to 6.5. The input impedance of the opamp is equal to R1 and it should be selected to be sufficiently large to ensure the preceding transmit filter is not excessively loaded. However from a noise immunity point of view, the small value of R1 and R2 is often preferred. In this design R1 value of 1kΩ is proposed.

For this application, the cross over distortion which is often associated with the push pull configuration is not a critical concern. Simple measures to alleviate this problem can however be taken such as (i) using D1 and D2 to compensate for the transistor V_{BE} drop and (ii) tapping the opamp feedback signal at the push pull output stage.

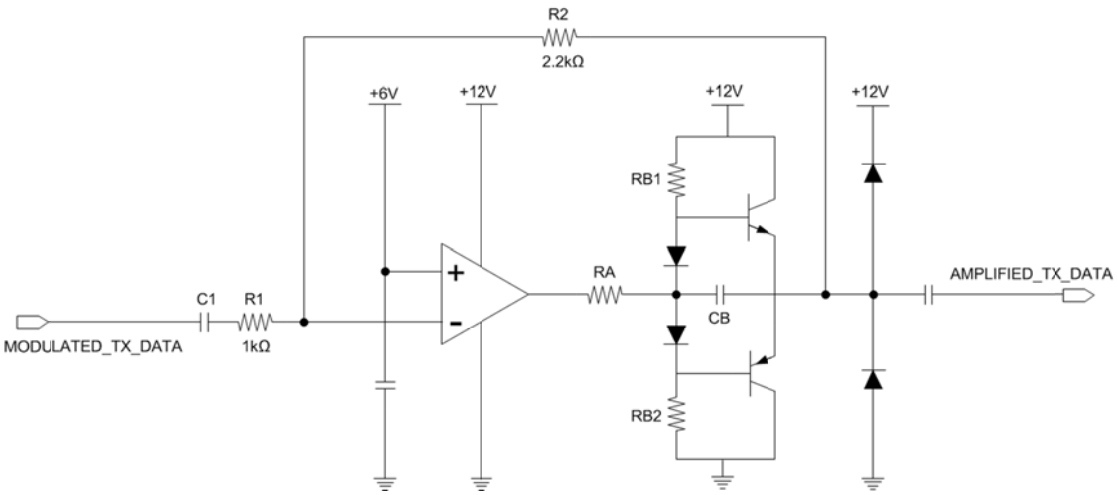


Figure 7.10 : Transmit amplifier circuit implementation

7.3.5 Coupling Circuit

In principal the coupling circuit consists of a tuned LC high pass filter that presents a low impedance path to the carrier frequency and at the same time blocks the bus power frequency. The design requirement for the coupling circuit will be discussed in depth in section 7.4.

7.3.6 Receive Band Pass Filter

While the coupling circuit filters out the carrier signal from the bus, further signal processing is required to ensure the received signal can be successfully decoded. Coupling circuit components, are required to be rated to handle the bus voltage levels and therefore are often bulky, expensive and can be difficult to find in a wide range of values at low tolerances. Therefore a second stage filtering process with a narrower pass band is used to filter out the high order harmonics of the bus voltage/ current frequency that may be present in the communication signal.

Directly cascading the receive band pass filter to the coupling circuit can pose some problems. In doing so the input impedance of the receiver section will be determined directly by the input impedance of the band pass filter. This is not desirable as the modem input impedance requirement for the current fed and voltage fed system is different. Therefore a non-inverting voltage buffer amplifier is used as an interface between the coupling and filter circuit. This allows the input impedance of the modem to be determined using a resistor at the input terminal of the amplifier. A common filter configuration can then be used for both the current fed and voltage fed systems. A 3rd order Butterworth band pass filter (PI configuration) was used in this design. The PSPICE frequency response simulation of the filter is shown in Figure 7.11.

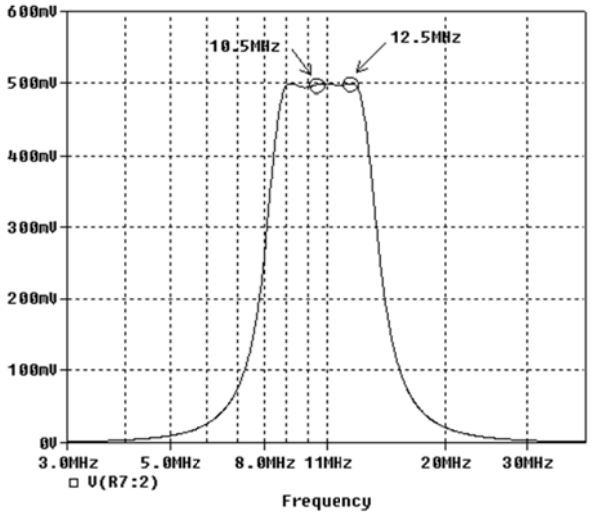


Figure 7.11 : Receive band pass filter frequency response

7.3.7 Receive amplifier

In general the received signal amplitude is quite low, and it can vary broadly depending on the impedance of loads connected to the bus. In this application it is only crucial that the frequency information of the signal is preserved. Actual signal wave shape is not important. Therefore the strategy employed in this design is to use an amplifier with sufficient gain such that at the lowest expected input amplitude, the signal is adequately amplified. With this approach, if the input signal is considerably larger than the minimum value, the high gain amplification could cause signal clipping. This is not a concern as the frequency of the signal remains unchanged even under these conditions.

The receive amplifier was implemented using a CMOS inverter operating in linear mode. This topology offers high gain at very low cost and eliminates that need for opamps with high gain bandwidth requirement. In this design a HEF4069UBT unbuffered CMOS inverter operating at supply voltage of 12V was used. This IC has 6 set of inverters, and 3 were used to form a there stage cascaded amplifier. The gain measurement of a single stage inverter is shown in Figure 7.12. CH1 (yellow trace) is the input signal to the amplifier and has a peak to peak value of 180mV. The amplified output, CH2 (pink trace) has a magnitude of 1.5Vpp. A gain of approximately 8.3 times was achieved. The frequency of the both the signals are equal.

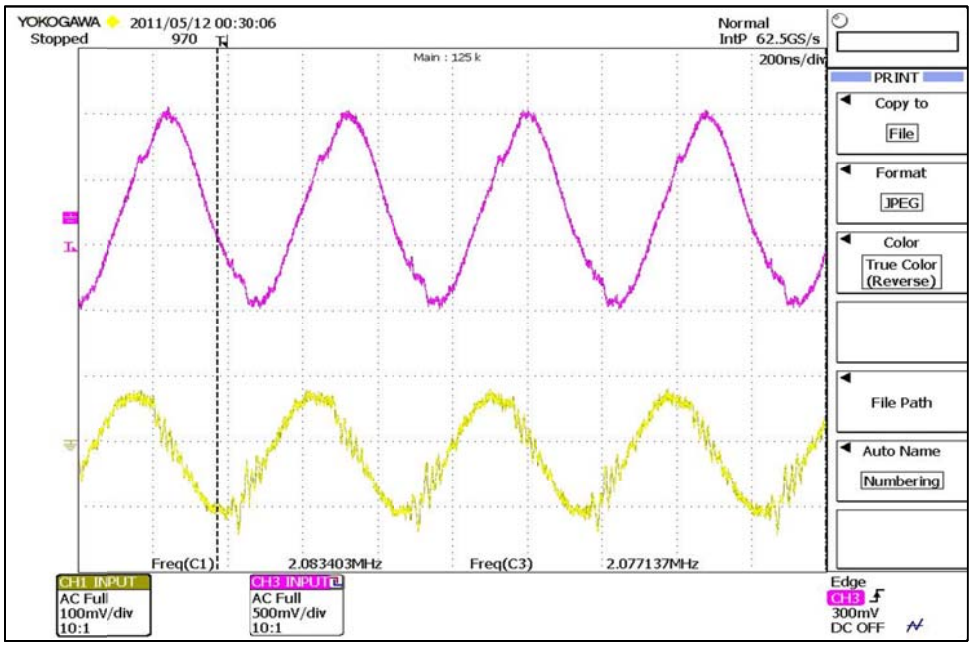
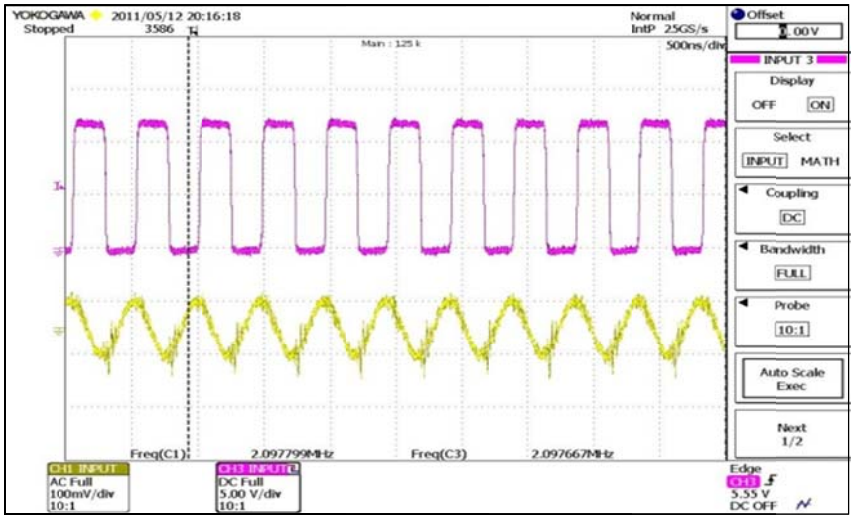


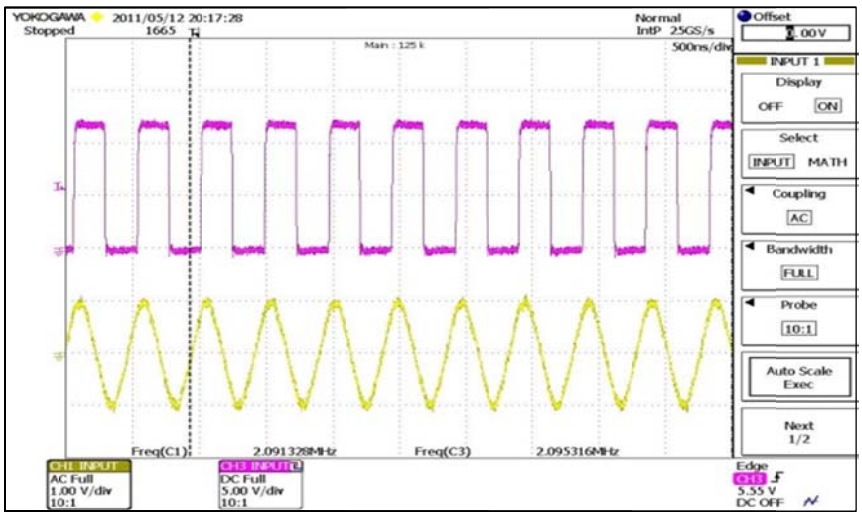
Figure 7.12 : Waveform of single stage linear amplifier

7.3.8 Pulse Shaping

As discussed in the previous section, the waveform of the amplified signal depends on the amplitude of the input signal. To ensure consistent and accurate decoding irrespective of the amplitude of the input signal, it is necessary to shape the amplified pulse to a square wave. This can be easily done by feeding the output of the amplifier through a logic inverter. The spare gate in the HEF4069UBT IC is ideal for this purpose. Figure 7.13 shows the reshaped waveform and the input signal to the amplifier stage. In Figure 7.13 (a) the amplitude of the input voltage is approximately 100mVpp and in Figure 7.13 (b) the amplitude is 2Vpp. Note that in both cases, the reshaped square wave is identical, the frequency matches the original input signal and the duty cycle is 50%.



(a) 100mVpp input signal

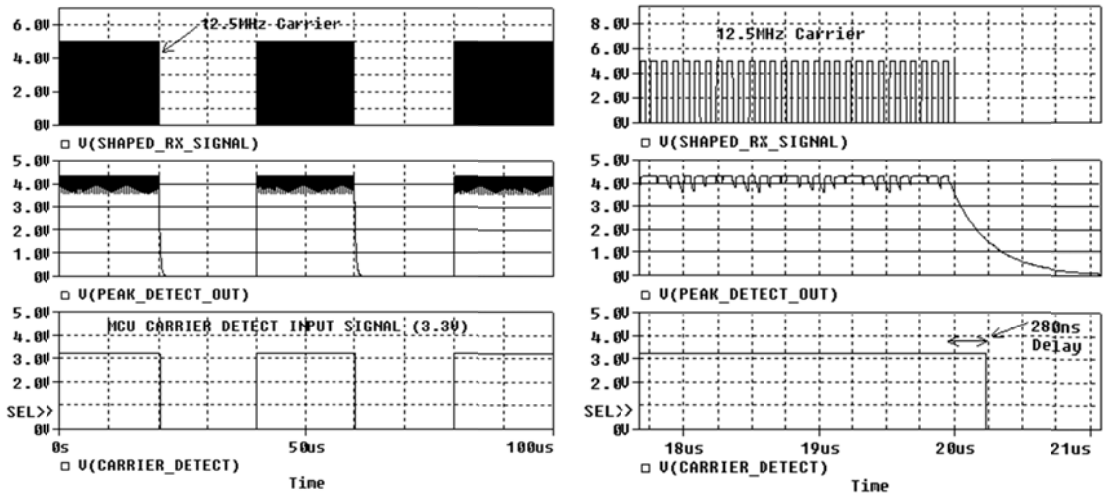


(b) 2Vpp input signal

Figure 7.13 : Shaped linear amplifier output

7.3.9 Carrier Detect

The main purpose of the carrier detection circuitry is to identify if the bus is in the idle state or if it is currently busy with ongoing communication. The presence or absence of a square wave from the pulse shaping circuitry can be used to determine if the bus is idle. The carrier detection circuitry is designed to output a logic high to the microcontroller to indicate a 'busy' state and logic 0 for 'idle' condition. This can be implemented using a simple envelop detection circuitry and non-inverting Schmitt trigger or comparator circuit. The time constant of the envelop detector should be approximately 3 to 4 times the period of the carrier frequency. In this design a 1kΩ resistor and 270pF capacitor was used. Figure 7.14 shows a PSPICE simulation of the operation of the carrier detection circuitry.



(a) Carrier detection simulation (b) Zoomed view

Figure 7.14 : PSPICE simulation of carrier detect circuitry

7.3.10 FSK Demodulation

The output of the pulse shaper is demodulated using a PLL. The PLL locks to the frequency of the input signal and generates an output voltage proportional to the frequency of the input signal. In the ideal case, the frequency profile of the PLL should be designed to match the transmit VCO frequency profile. However temperature drift at the transmit side could cause the frequency output of the VCO to increase beyond the designed value. The PLL should therefore be designed with a narrower profile to ensure

robust detection as shown in Figure 7.15. In general a larger offset frequency and a reduced range is necessary and therefore a large R2 value and a smaller R1 value is expected. The values of R1, R2 and C1 can be selected using the design curve in Figure 7.7. In this design CD74HC7046A PLL IC from Texas Instrument was used. The IC has two types of phase detectors, an XOR phase comparator and positive edge triggered phase and frequency detector (PFD). The PFD was experimentally found to offer better performance over the XOR. In this design the PFD phase detector and passive lead lag low pass loop filter was used. Figure 7.16 (a) & (b) shows the scope capture of the demodulated output voltage for 10.5MHz and 12.5MHz input frequency respectively. For 10.5MHz input, the demodulated voltage was measured to be 0.879V and for 12.5MHz a voltage level of 3.412V was recorded.

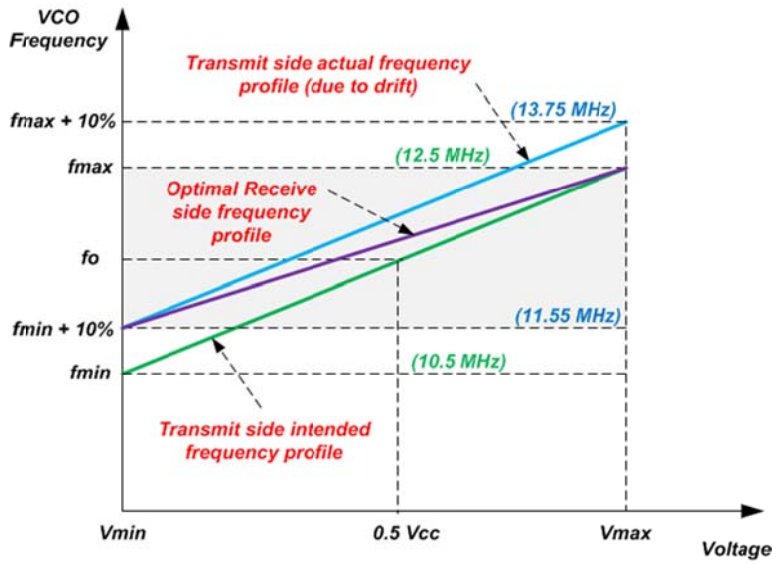
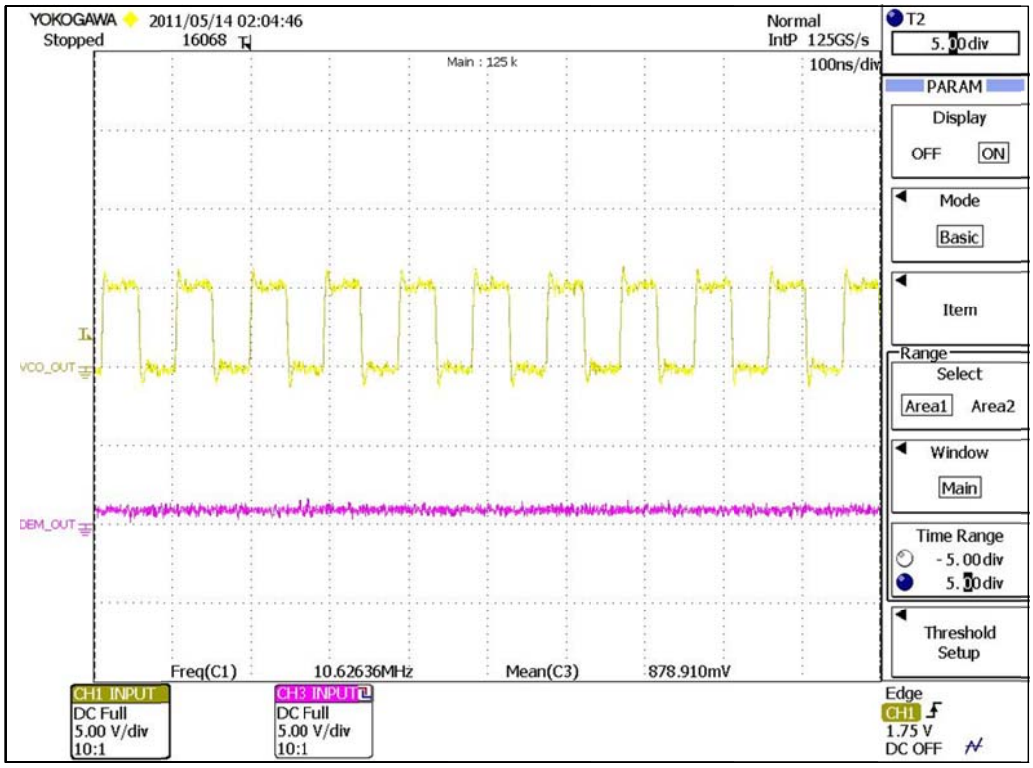
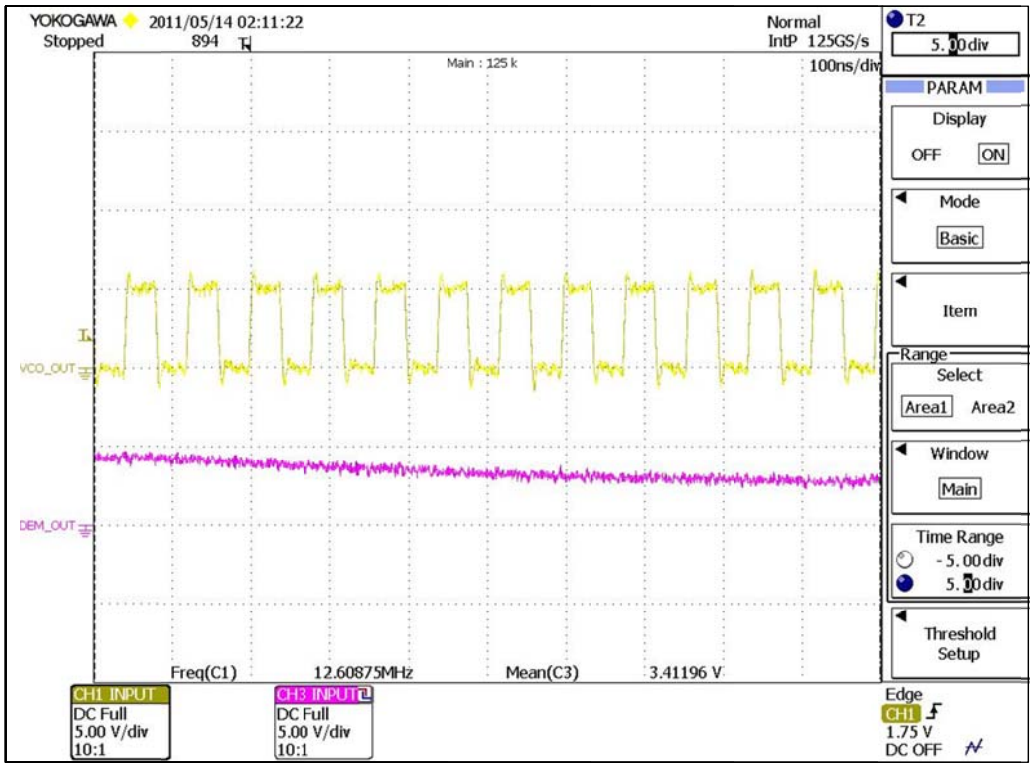


Figure 7.15 : PLL frequency profile



(a) 10.5MHz input



(b) 12.5MHz input

Figure 7.16 : FSK demodulation waveform

7.3.11 Digitizer

The demodulated signal is an analog voltage between 0V to 5V proportional to the input frequency. In order to digitally decode the received data, the demodulated signal will need to be digitized to crisp logic levels. This is implemented using a voltage comparator circuit with hysteresis. The output of the comparator is effectively the transmitted Manchester encoded data stream.

7.3.12 Clock Recovery Circuit

Before the received Manchester encoded data can be decoded, it is first necessary to extract the synchronizing clock information from the Manchester data stream. With the clock signal available, the retimed NRZ equivalent data and clock signal can be generated and sent to the MCU for further processing.

The proposed clock recovery circuit to perform this function is shown in Figure 7.19. As described in section 7.2.1, the Manchester encoded signal has a transition in the middle of every clock period. A logic '1' is represented by a high to low transition and vice versa. Therefore, latching the Manchester data stream just prior to the midpoint of the clock signal results in the NRZ representation of the data. The timing diagram in Figure 7.17 shows how this can be achieved using a shifted clock signal which is 90° out of phase with the original clock used to encoded the Manchester data.

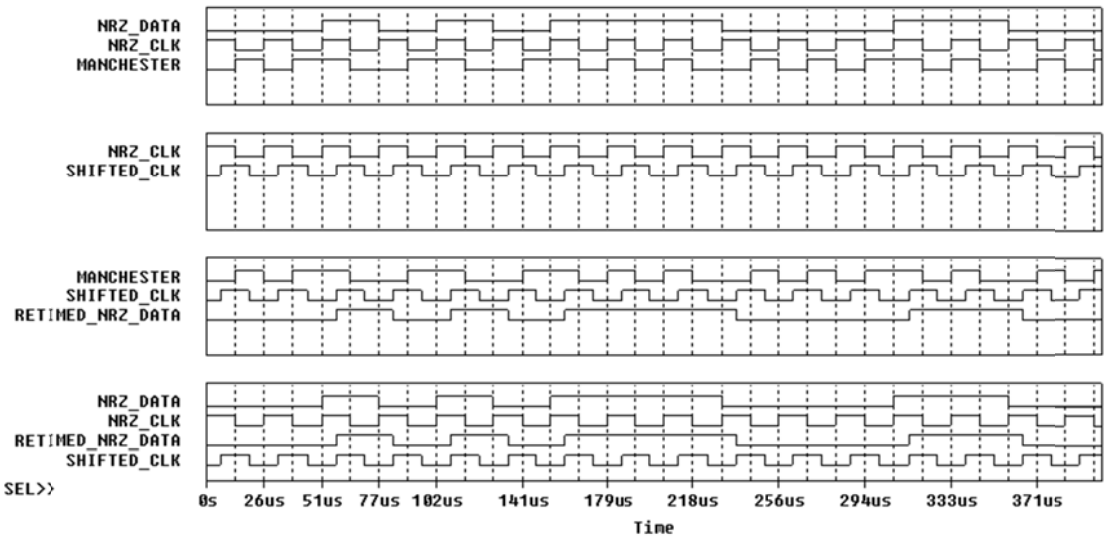


Figure 7.17 : Transmit and receive NRZ data & clock signals

The problem now lies in generating the shifted clock signal. This is performed by the circuit enclosed in the dotted section of Figure 7.19. Fundamentally a high frequency clock (16 times transmit NRZ clock) and a binary counter operating as a frequency divider is used derive the phase shifted clock signal. The binary counter is synchronized at every edge of the Manchester incoming data stream and therefore any deviations in the high frequency clock are corrected at every transition. The timing diagram in Figure 7.18 shows the operation of this circuitry.

There are however some limitations with this technique. Although the Q0 output of the binary counter (SHIFTED_CLK) toggles at the right frequency, the state of the Q0 output can either be a logic 1 or 0 at the start of data stream. In other worlds the recovered clock can either lead or lag the transmit clock by 90°. In both condition, the sampling point of the incoming Manchester bit stream differs and can produce different results. Additional synchronization circuitry to reset U2 appropriately can be fairly complicated. This problem can be solved reasonable easily in software by exploiting the fact that the Manchester encoded data sampled at either + 90° or -90° relative to the transmit clock will result in either the correct NRZ data or the inverse of the transmit data as shown in Figure 7.20. The preamble detection routine in software can be used to identify if the received data is inverted.

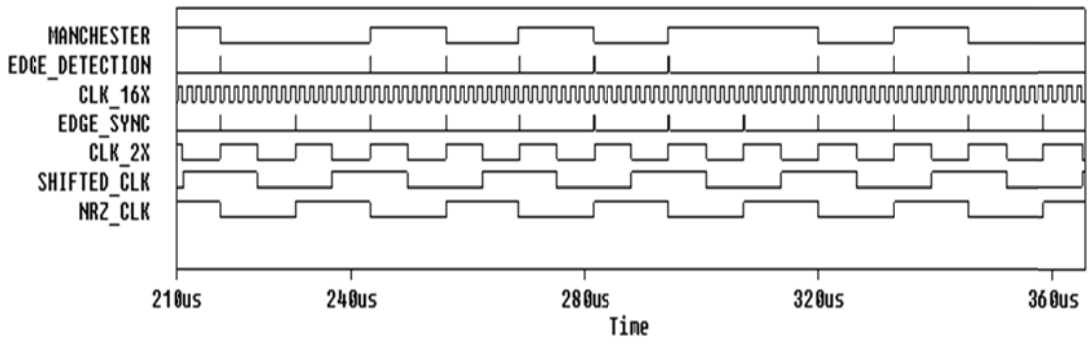


Figure 7.18 : Timing diagram of clock recovery circuit

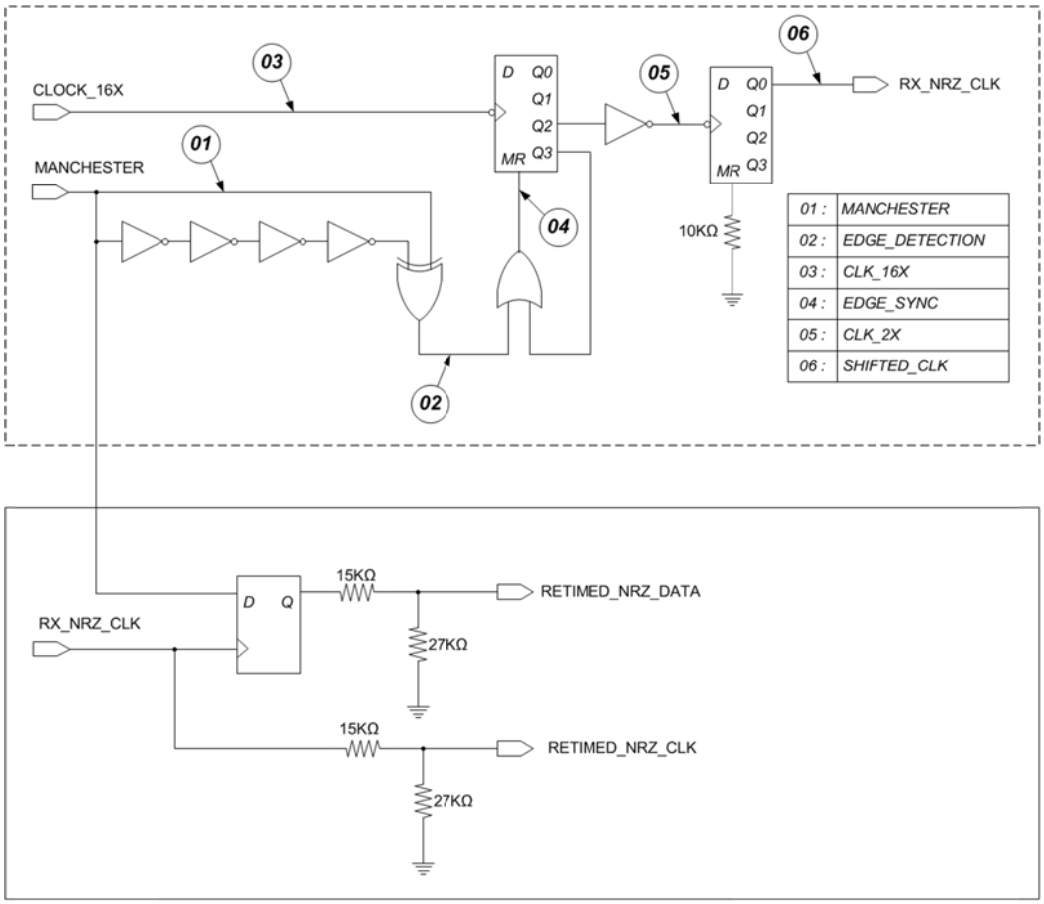
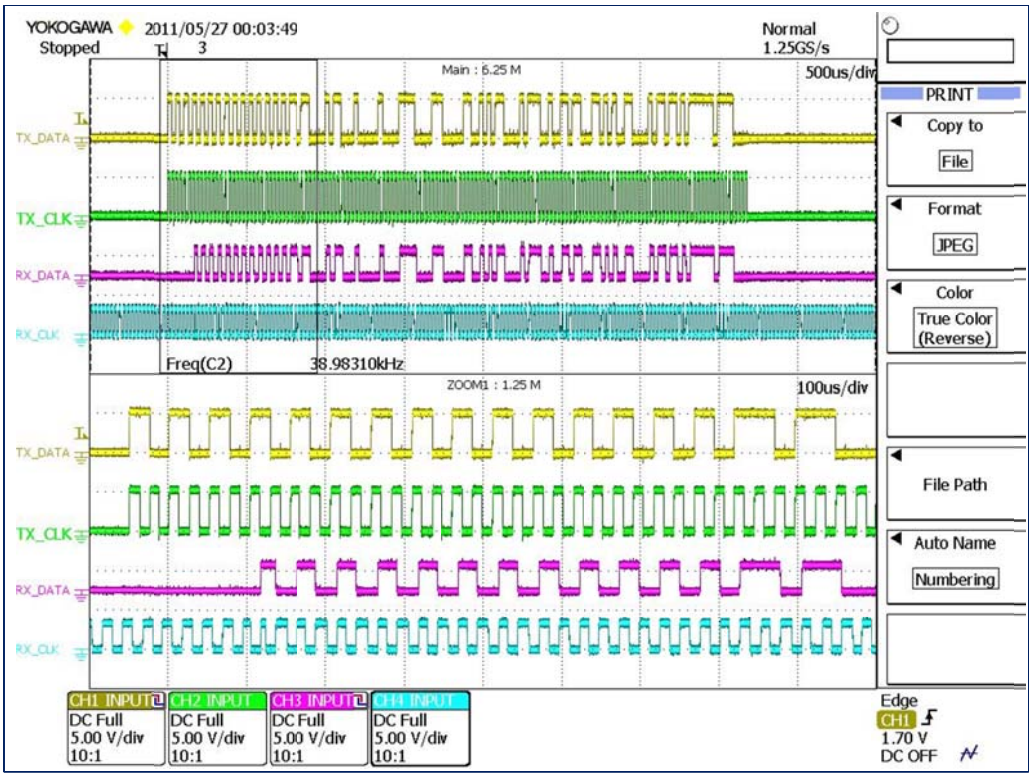
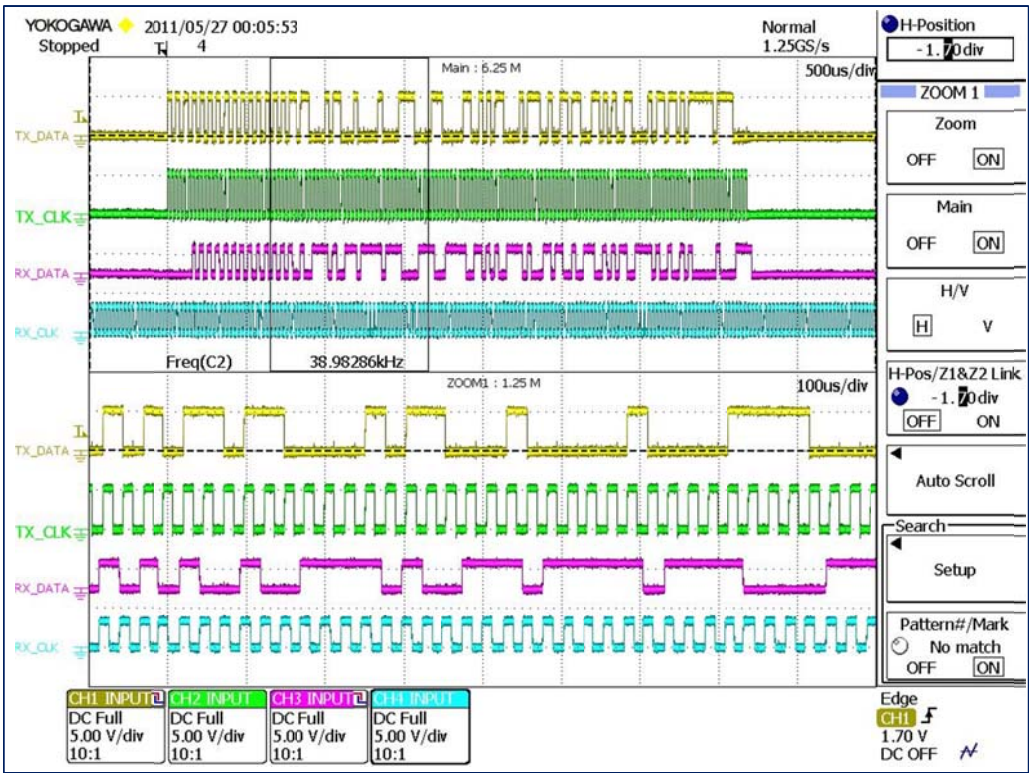


Figure 7.19 : Simplified clock recovery circuit



(a) Non inverted RX NRZ data



(b) Inverted RX NRZ data

Figure 7.20 : Retimed received NRZ data waveform

7.4 Coupling circuit

In a voltage fed system, the modems are effectively connected in parallel to the HFAC bus. Figure 7.21 shows a simplified equivalent circuit for a number of modem connected to a HFAC bus. In this case it is assumed that no loads are present in the system. The modems are represented as a voltage source with series impedance Z_{MODEM}. The HFAC inverter that generates the bus voltage is modelled as a Thevenin equivalent circuit. We now assume that the Modem 1 in the system is transmitting information over the bus. All other modems are assumed to be in receive mode. The red dotted lines represent the current flow due to Modem 1. For maximum communication efficiency, the follows conditions are necessary

(i) The impedance of the modem in transmit mode (Z_{MODEM} 1) should be as small as possible at the carrier frequency.

(ii) The impedance of the modem in receive modem (Z_{MODEM} 2 to Z_{MODEM} N) should be reasonably high at the carrier frequency to avoid loading the transmitter excessively.

(iii) The impedance of the HFAC inverter ($Z_{INVERTER}$) should be very high at the carrier frequency

(iv) The impedance of the modem both in transmit and receive mode should be very high at the bus voltage frequency

(v) The impedance of $Z_{INVERTER}$ should be very small at the bus voltage frequency for efficient power transfer.

The function of the coupling circuitry is to realize requirements (i), (ii) & (iv). Requirement (v) is a natural design requirement for any power source and therefore is assumed to be true in all cases. Requirement (iii) is also normally true if the carrier frequency is considerably higher than the bus voltage frequency. To ensure that this requirement is always met, a tuned band rejection filter can be added in series with the voltage source.

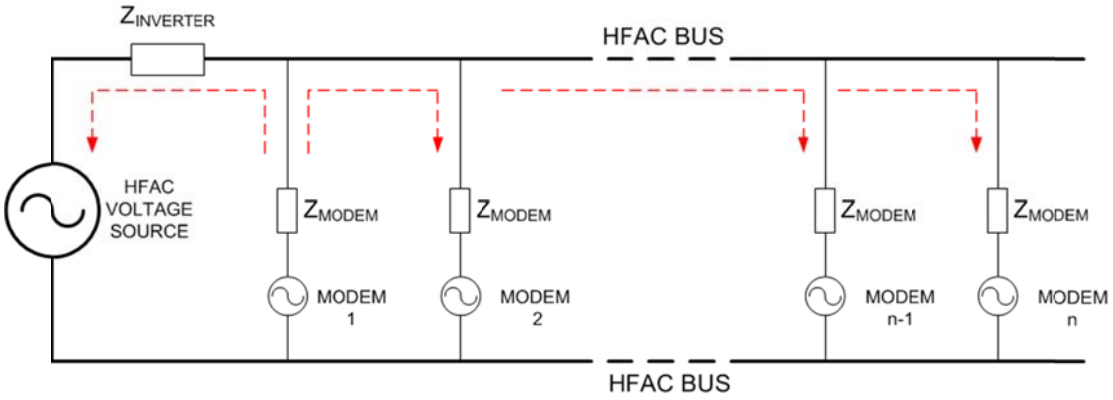


Figure 7.21 : Multiple modems on voltage fed HFAC bus

7.4.1 Design of Coupling Circuit.

Fundamentally the modem can be represented as shown in Figure 7.22, where TA and RA represent the transmit and receive amplifier circuits. The transmit amplifier by design has negligible output impedance and the receive amplifier has very high input impedance. Therefore the effective input impedance of the receiver circuit is equal to the value of R_{IN}. The coupling circuit is shown in the figure as an equivalent 2 port network.

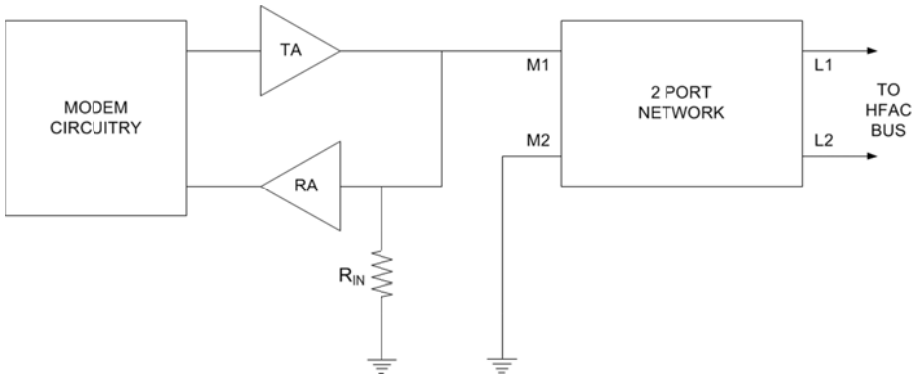


Figure 7.22 : Simplified representation of modem line interface stage – Voltage fed system

To meet requirement (i), the input impedance of the network seen from terminal M1 and M2 should be very small at the carrier frequency. Requirement (ii) & (iv) calls for the impedance seen from terminal L1 and L2 be equal to the value of R_{IN} at the carrier frequency and at the bus voltage frequency the impedance should be very high. An impedance network with a high pass or band pass characteristics would meet these requirements.

In this design a band pass configuration consisting of a tuned series and parallel resonant circuit was used. An isolation transformer was also used to provide electrical isolation between the HFAC bus and the modem circuitry. The leakage inductance and magnetizing inductance of the transformer also influences the performance of the circuit and in this design it was intentionally used to form part of the coupling circuit. The coupling circuit is shown in Figure 7.23. In selecting the coupling transformer, it is important to ensure the operating frequency range is compatible with the carrier frequency. In this design, T60403-K4031-X008 coupling transformer from Vacuum Schmelze was used. This transformer is rated for operation from 1 to 30MHz. The leakage and magnetizing inductance (line side) was measure to be 620nH and 1.458mH respectively. The series capacitor Cs value of 330pF was selected to be in resonant with the L_{LEAK}. At the modem side, a parallel resonant circuit is used. The value of Lp should be selected to be much smaller than the magnetizing inductance. In this design Lp and Cp values of 22nH and 10nF was used. The simulated frequency response of the proposed coupling circuit is shown in Figure 7.24. It can be observed that the bus voltage frequency, (50kHz) is well attenuated. The frequency response curve shows almost no sensitivity to changes in the value of R_{IN}.

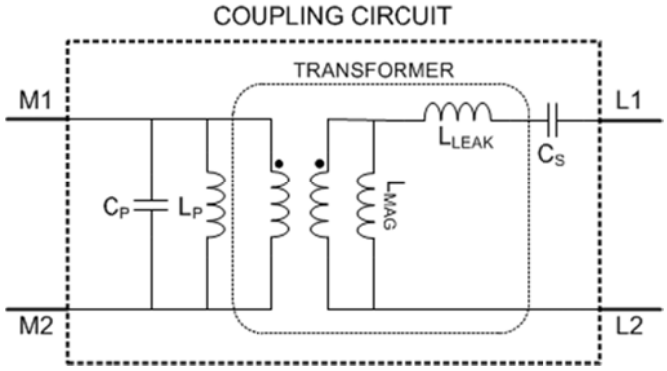


Figure 7.23 : Modem coupling circuit for voltage fed system

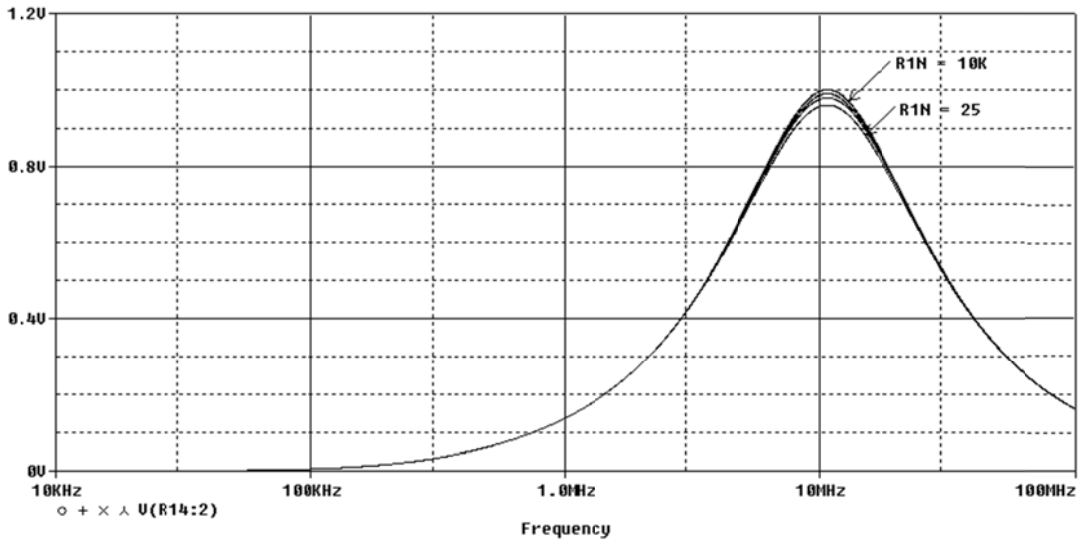


Figure 7.24 : Frequency response simulation of coupling circuit - voltage fed system

7.4.2 Coupling Circuit for Current Fed Systems

In a current fed system, the modems are effectively connected in series to the HFAC current loop. Figure 7.25 shows a simplified equivalent circuit for a number of modem connected to a HFAC current loop. In this case it is assumed that no loads are present in the system. The inverter generates a HFAC sinusoidal constant current output. To ensure that the impedance of the inverter ($Z_{INVERTER}$) does not attenuate the communication signal, a tuned band pass filter can be added in parallel with $Z_{INVERTER}$ to offer an alternate low resistance path for the communication signal.

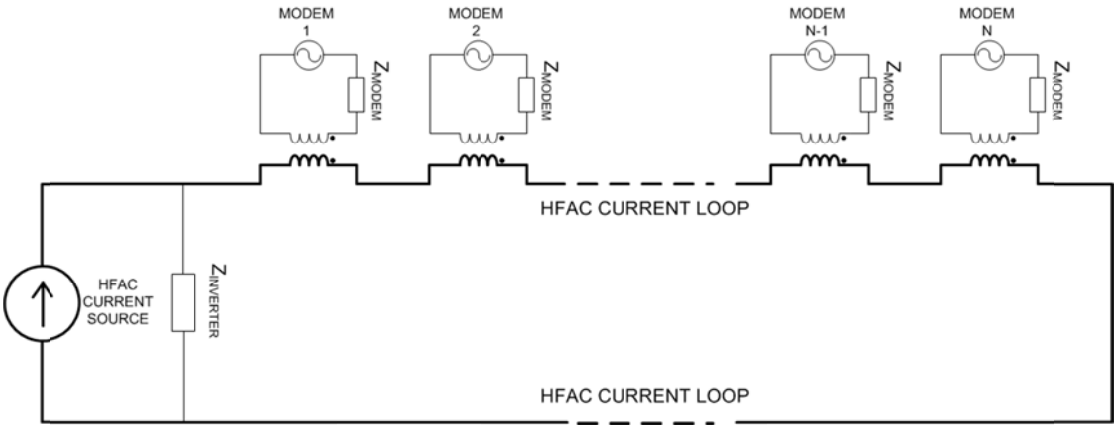


Figure 7.25 : Multiple modems on current fed HFAC bus

The simplified equivalent modem circuit is shown in Figure 7.26. The requirement of the coupling circuit is described as follows.

(i) The impedance seen by the HFAC bus current flowing from L1 to L2 should be exceedingly small.

(ii) The HFAC bus current must be prevented from flowing through R_{IN}, therefore the impedance network should offer an alternate parallel bypass path.

(iii) The input impedance of the network seen from terminal M1 and M2 at the carrier frequency should be equal to the impedance seen outward form terminal L1 & L2.

(iv) The impedance seen by the carrier frequency current flowing from L1 to L2 should be equal to R_{IN}.

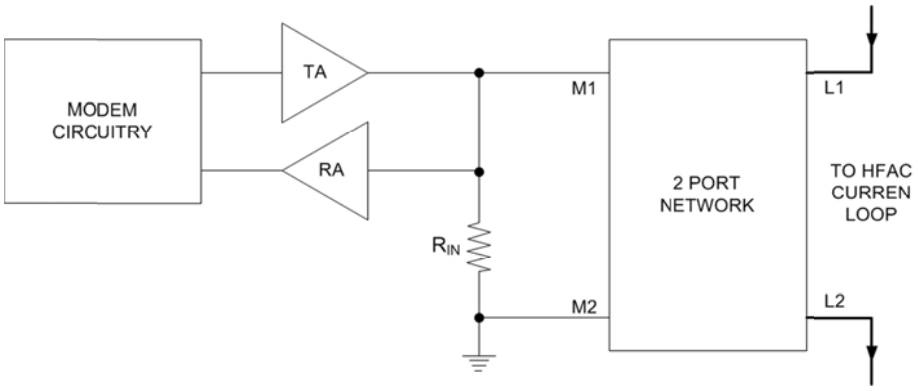


Figure 7.26 : Simplified representation of modem line interface stage – Current fed system

The constraints stated above can be achieved by using a coupling circuit of the form shown in Figure 7.27. Note that this coupling circuit is similar to the one in Figure 7.23 for the voltage fed design. The only difference lies in the orientation of the series and parallel branch. However this difference in orientation is crucial for proper operation of the circuit. Both the series and parallel branch is tuned to the carrier frequency. The parallel branch offers a low impedance path for the bus current.

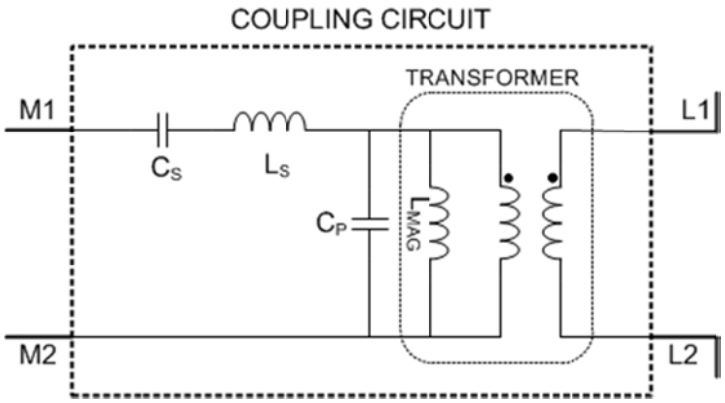


Figure 7.27 : Modem coupling circuit for current fed system

7.4.3 Data Communication Challenges in Current Fed Systems

Consider a system with multiple modems as shown in Figure 7.25 with the coupling circuit as proposed in Figure 7.27. Assuming the resonant elements are tightly tuned, the input impedance of the modem at the carrier frequency is simply equal to the value of R_{IN}. The impedance seen by the transmitting modem in a system with N_m modem can be represented as in Figure 7.28. If the transmit amplifier output voltage is V_{mdm}, then the voltage across each receiving node is equal to $V_{mdm}/(N_m - 1)$. Therefore even under ideal conditions with no line and load impedance, amplitude of the received signal falls as the number of modems increases. In the voltage fed design, under similar ideal conditions, the amplitude of the received signal remains constant regardless of the number of modem in the system (provided the transmit amplifier has sufficient current drive capability).

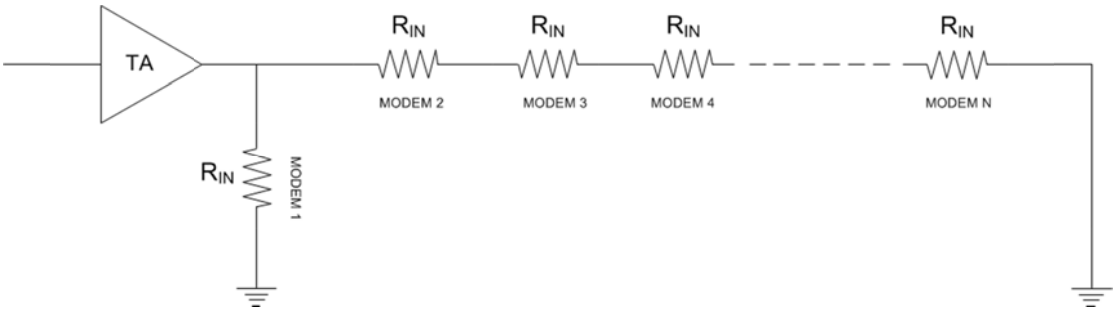


Figure 7.28 : Transmit mode equivalent impedance model

Next consider a similar system but with two modems simultaneous transmitting. This condition is represented in Figure 7.29. At the input node of modem 1, a signal of amplitude V_{mdm} due to self-transmission will be present. In addition, another voltage component due to the simultaneous transmission of modem N will appear across the input node of modem 1. The amplitude of this component will be $V_{mdm}/(N_m - 1)$. Therefore the signal seen at the input of both modems will consist of the sum of both the self-transmission component and the simultaneous transmission by the neighbouring modem. If the number of modems in the system is large, the amplitude of the voltage due to the transmission of the neighbouring modem will be small and may be totally overwhelmed by the self-transmission component. This may potentially impair the collision detection capability.

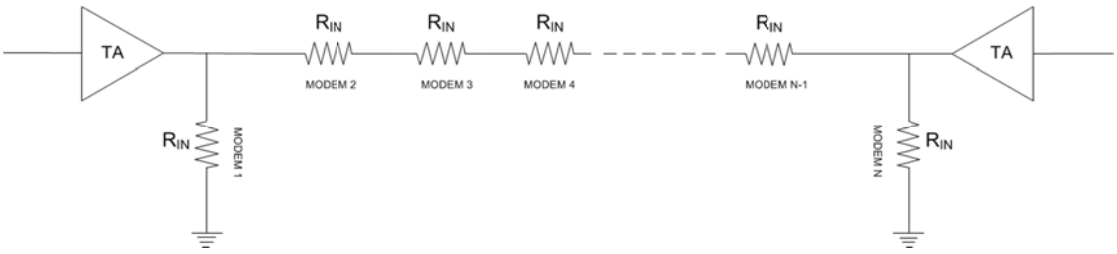


Figure 7.29 : Multiple transmit mode equivalent impedance model

Any load connected to the loop increase the total resistance and further aggravates these problems. Therefore a tuned band pass bypass filter should always be used across all loads to offer an alternate low resistance path for the communication signals.

7.4.4 Analytical Modelling of Coupling Circuit for Current Fed Systems

In transmit mode, the equivalent circuit of the modem and the coupling circuit is shown in Figure 7.30 where R_{IN} is the input impedance of the modem and the R_T is the sum of the impedance of the remaining modems in the system and is given by (7.1).

$$R_T = (N_m - 1)R_{IN} \tag{7.1}$$

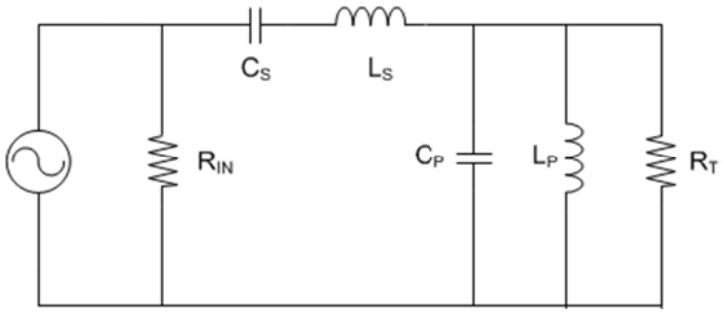


Figure 7.30 : Coupling circuit equivalent circuit - transmit mode

The quality factor and the resonant frequency of the series and parallel branch are defined as

$$Q_{sm} = \frac{\sqrt{L_s}}{R_{IN}\sqrt{C_s}} \tag{7.2}$$

$$Q_{pm} = \frac{R_{IN}\sqrt{C_p}}{\sqrt{L_p}} \tag{7.3}$$

$$\omega_{sm} = \frac{1}{\sqrt{L_s C_s}} \tag{7.4}$$

$$\omega_{pm} = \frac{1}{\sqrt{L_p C_p}} \tag{7.5}$$

Both the series and parallel branches are tuned to the same frequency. The tuning ratio is defined as the ratio of the drive frequency to the resonant frequency and is given as.

$$k = \frac{\omega_o}{\omega_{sm}} = \frac{\omega_o}{\omega_{pm}} \tag{7.6}$$

Using the definition (7.2) to (7.6), the magnitude of the voltage transfer function $H(s)$ can be expressed as (7.7).

$$\left|H(s)\right| = \frac{k^2(N_m - 1)}{\sqrt{(k^3 - k)^2 Q_{sm}^2 + \left[k^2 - (k^2 - 1)^2 Q_{sm} Q_{pm}\right]^2 \left[N_m - 1\right]^2}} \tag{7.7}$$

In receive mode, the modem is driven by a current source and can be represented as in Figure 7.31. The transfer function of the voltage across R_{IN} to the current is given as (7.8).

$$\left|P(s)\right| = \frac{k^2}{\sqrt{(k^3 - k)^2 Q_{pm}^2 + \left[k^2 - (k^2 - 1)^2 Q_{sm} Q_{pm}\right]^2}} \tag{7.8}$$

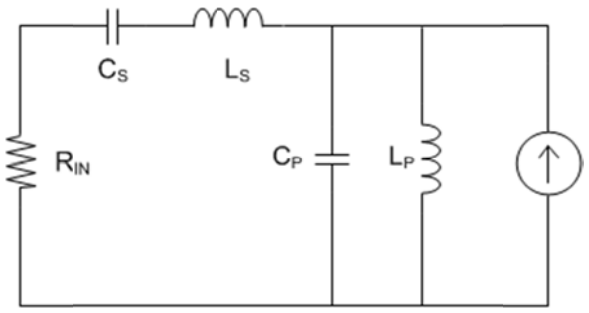


Figure 7.31 : Coupling circuit equivalent circuit - receive mode

Equations (7.7) and (7.8) can be used to identify the constraints imposed on the selection the coupling circuit element. At this stage it is interesting to note that the magnitude of $P(s)$ is independent of N while the magnitude of $H(s)$ is not. The output of the modem is well controlled and predictable. However in receive mode, the content of the current source is less predictable. It represents the sum of the communication current, the bus current and any noise that may have been pickup up by the bus. Therefore the coupling circuit will be designed with the desired response of $P(s)$ taking precedence over $H(s)$.

The first constrain is defined to limit the magnitude of $P(s)$ below a certain frequency to be smaller than a prescribed value ε. This is to ensure that the HFAC bus current is

sufficiently attenuated. This can be mathematically represented by (7.9). It is recommended that k_0 be selected to represent at least the 10th harmonic of the bus current. Substituting $k_0 = 0.045$ into (7.9) & (7.8), the first constraint imposed on the coupling circuit is derived and is given in (7.10).

$$\left|P(s)\right|_{k \le k_0} < \varepsilon \tag{7.9}$$

$$\sqrt{\frac{1}{491.829\,Q_{pm}^2 + (1 - 491.829\,Q_{pm}Q_{sm})^2}} \le \varepsilon \tag{7.10}$$

The plot of the magnitude of $H(s)$ for various values of Q_{sm} is shown in Figure 7.32. It can be seen that the magnitude plot appears to have a peak for some values of Q_{sm}. The frequency at which this peaking occurs and the magnitude of the peaks depends on the values of Q_{sm}, Q_{pm} and N_m. Figure 7.33 shows how the magnitude of $H(s)$ varies as the number of modem in the system changes for fixed values of Q_{sm} & Q_{pm}. It can be observed from the figure that the frequency at which the peak occurs remains fairly constant but the peak amplitude increases rapidly with N.

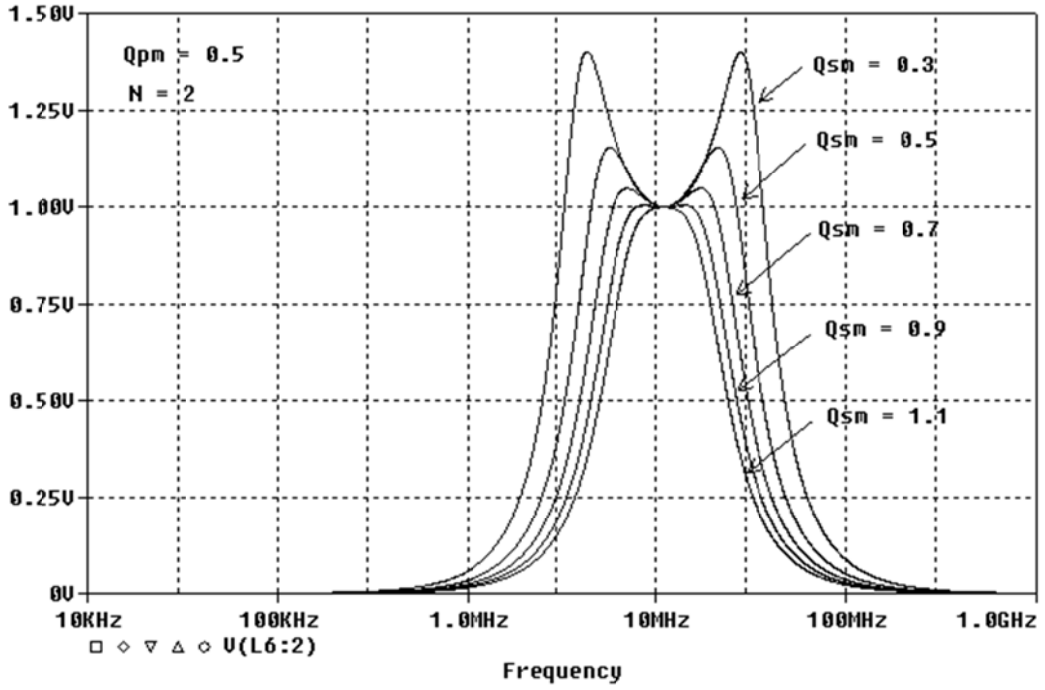


Figure 7.32 : Frequency response of H(s) for various Qsm values

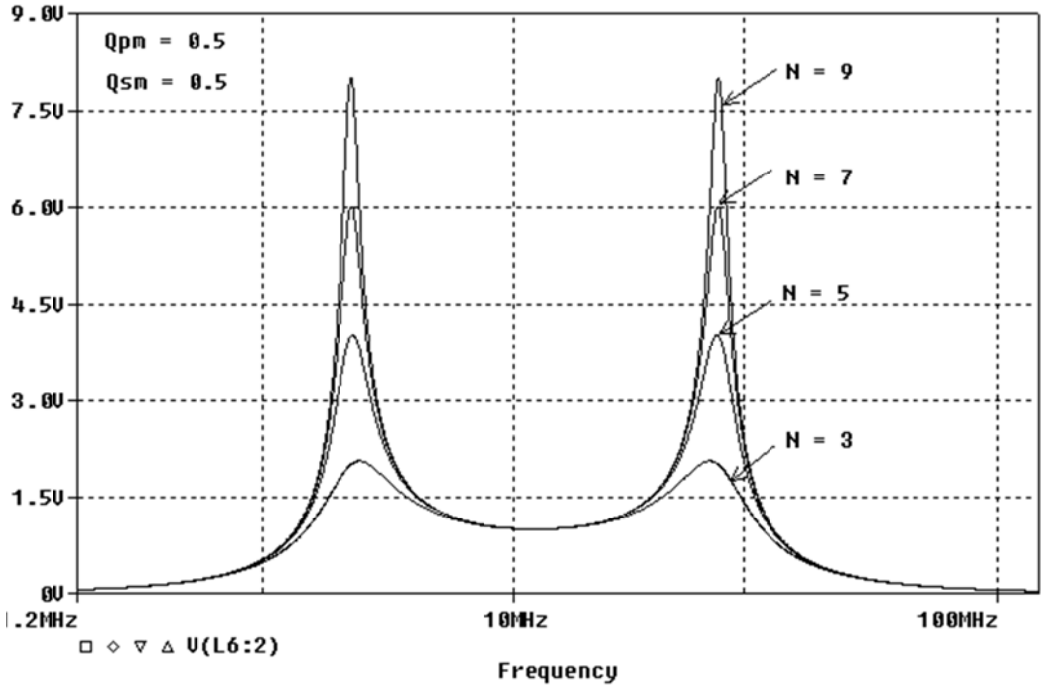


Figure 7.33 : Frequency response of H(s) for various number of moderns

Taking the derivate of (7.7) with respect to k and equating it to zero, the value of k at which the peaking occurs can be calculated. This is given in (7.11).

$$k_p = \sqrt{\frac{\left(J_A + J_B\right) \pm \sqrt{\left(J_A + J_B\right)^2 - J_B^2}}{J_B}} \tag{7.11}$$

Where

$$\begin{aligned} J_A &= 2(N_m - 1)^2 Q_{pm} - Q_{sm} \\ J_B &= 4(N_m - 1)^2 Q_{pm}^2 Q_{sm} \end{aligned} \tag{7.12}$$

The magnitude of the peaks can be found by substituting (7.11) into (7.7). It can be further shown from (7.11) that the peaks in $|H(s)|$ start to appear when condition (7.13) is met. Similar peaking behaviour can be observed in the magnitude of $|P(s)|$, when condition (7.14) is met.

$$Q_{sm} < 2(N_m - 1)^2 Q_{pm} \tag{7.13}$$

$$Q_{sm} > \frac{Q_{pm}}{2} \tag{7.14}$$

The relationship between the frequencies at which the peaking occurs to the number of modem in the system has interesting properties. This plot is shown in Figure 7.34 for various values of Q_{sm} & Q_{pm}. It can be seen that for values of N_m greater than about 4, the value of k_p remains constant. However the magnitude of the peak does increase as more modems are present in the system. A good approximation for k_p can be found by letting $N_m \to \infty$ in (7.11) and solving the resulting equation yields a simple relation between k_p and the quality factors (7.15).

$$Q_{pm} Q_{sm} \approx \frac{k_p^2}{(k_p^2 - 1)^2} \tag{7.15}$$

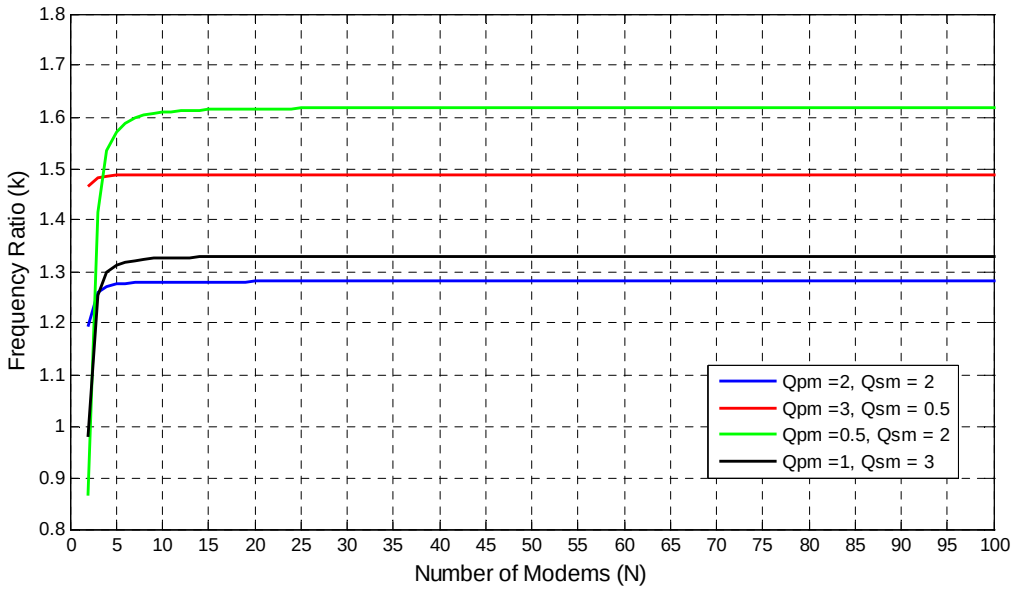


Figure 7.34 : Peaking frequency ratio vs number of modems

As can be seen from Figure 7.33 the magnitude of the peak grows very rapidly with the increase of the number of modems in the system. Therefore it is important to ensure that the output of the transmit amplifier does not have any harmonic frequency component at

these frequencies. Although it was shown that the transmit low pass filter in Figure 7.9 has excellent characteristics, it is preferable to ensure that the peaking effects occurs at even harmonics of the carrier frequency. The reason for this is that the output of the transmit VCO is a symmetrical square wave and does not contain even harmonics.

In summary, equation (7.10) and (7.15) and (7.14) can be used as a guide to select ideal values for the coupling circuit. Table 3.1 shows a set of computed value for the first 6 even harmonics. Firstly for each even harmonic component the product of $Q_{sm}Q_{pm}$ is computed using (7.15). Then the minimum value of Q_{pm} is determined using (7.10) for a desired ε value. In this case ε value of 0.05 was used. It is proposed that a headroom of at least 20% is added to the computed Q_{pm} value and further this must be check to ensure compliance with (7.14). Once the value of Q_{pm} is finalized, then Q_{sm} can be determined using (7.15), and the physical values of the coupling circuit can then be determined. In general it is desired that the coupling circuit be designed to ensure the peaking of $H(s)$ occurs at the 2nd harmonics. This would give then best performance, however in some cases this may impose high constraints on the values of the components required for the coupling circuit.

The first row in the Table 7.2 gives the values of coupling circuit elements that ensure the peak response of $H(s)$ occurs at the second harmonic. These values are proposed for this design. The simulated response of $H(s)$ and $P(s)$ for $L_s = 560nH$, $C_s = 390pF$ $L_p = 1uH$ & $C_p = 180pF$ is shown in Figure 7.35 & Figure 7.36 respectively. It can be seen that the simulation matches the expected response based on the approximate modelling.

kp	Qpm x Qsm	Min Qpm	Qpm +10%	Qsm	Ls	Cs	Lp	Cp
2	0.444	0.943	1.131	0.393	5.68E-07	3.68E-10	1.28E-06	1.64E-10
4	0.071	0.377	0.453	0.157	2.27E-07	9.21E-10	3.20E-06	6.55E-11
6	0.029	0.670	0.804	0.037	5.29E-08	3.96E-09	1.80E-06	1.16E-10
8	0.016	0.850	1.020	0.016	2.29E-08	9.15E-09	1.42E-06	1.48E-10
10	0.010	0.890	1.068	0.010	1.38E-08	1.51E-08	1.35E-06	1.55E-10
12	0.007	0.900	1.080	0.007	9.43E-09	2.22E-08	1.34E-06	1.56E-10
Remarks : Rin = 100Ω, ε = 0.05								

Table 7.2 : Calculation of coupling circuit element values

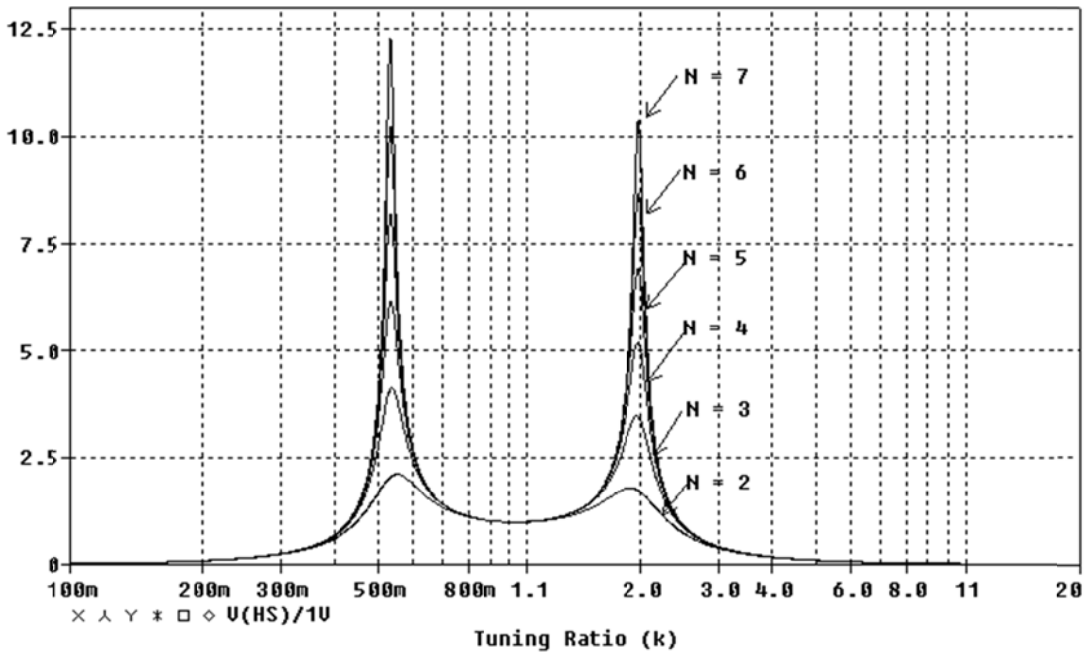


Figure 7.35 : Frequency response of H(s) for final coupling circuit design

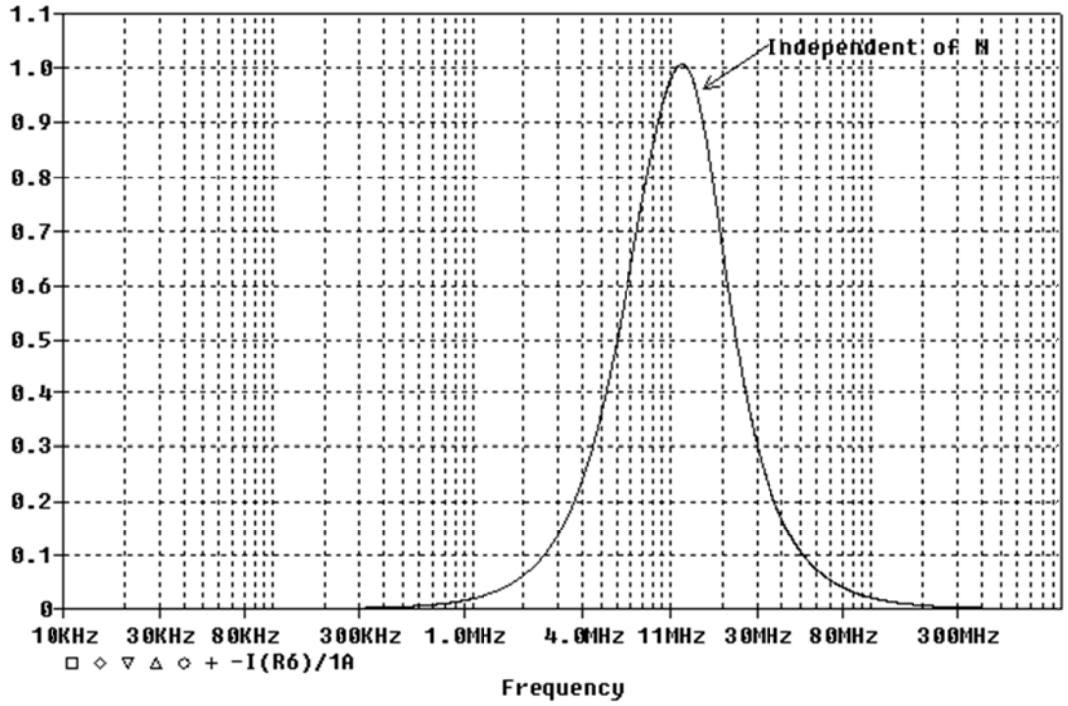


Figure 7.36 : Frequency response of P(s) for final coupling circuit design

7.4.5 Coupling Transformer Design

In the physical circuit, L_p is the value of the magnetizing inductance of the coupling transformer (referred to the modem side). The transformer is custom made, using a suitable high frequency ferrite core. In this design a toroidal core from Micrometal (Mix 6) suitable for operation up to 30MHz was used. The transformer winding configuration is shown in Figure 7.37. This configuration is particularly proposed for improved common mode noise immunity. As the current loop can extend long distances (depending on spatial distribution of the loads in the system) it is susceptible to noise. With the proposed winding configuration, common mode noise induces equal and opposite magnetic field in the ferrite core that effectively cancel and therefore is not reflected to the secondary.

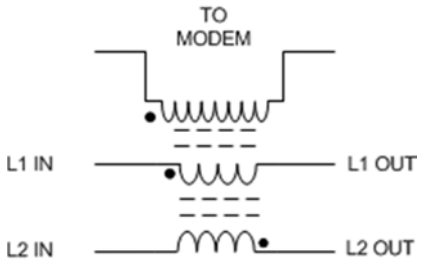


Figure 7.37 : Coupling transformer winding configuration

7.5 Realistic Power Line Attenuation Model

In the previous section, it was assumed that the HFAC power line was ideal with zero line impedance. Further the impedance of loads that may be connected to the bus was not accounted for. A realistic power line attenuation model for the voltage fed system is given in Figure 7.38. This model is similar to the model used for regular power line communication as proposed in [112].

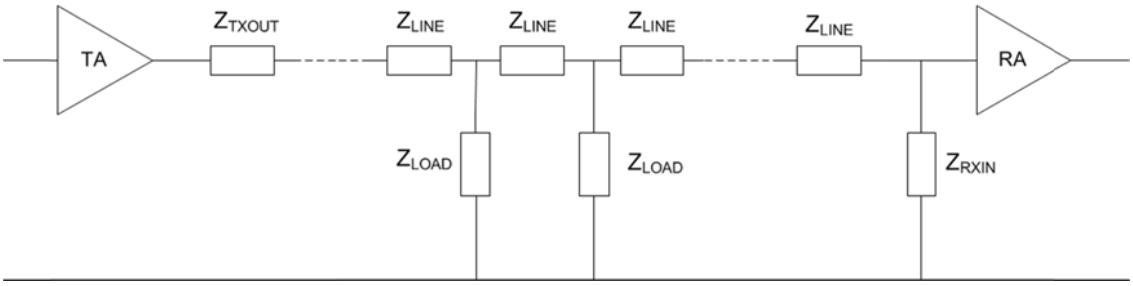


Figure 7.38 : Attenuation model - voltage fed HFAC bus

If the load impedance is small at the carrier frequency, a large portion of the signal will flow into Z_{LOAD} and the amplitude of the signal at the receiver (across Z_{RXIN}) will be severely attenuated. Therefore it is necessary to ensure that the point of load power converter that are used to interface the load to the bus have high impedance at the carrier frequency. Further as the input impedance of the receiver Z_{RXIN} forms a voltage divider network with the line impedance Z_{LINE}, Z_{RXIN} should be designed to be high for minimum signal attenuation. In a system with many modems, the input impedance of the modems are effectively in parallel and this reduces the total system impedance, thus further loading the transmit amplifier. Finally the output impedance of the transmitter Z_{TXOUT} should be small to reduce signal attenuation.

The attenuation model of the current fed system is shown in Figure 7.39. In this case, all the load, line and modem input impedances are connected in series. A carrier frequency bypass stub consisting of a tuned series LC circuit will need to be connected across the all the loads in the system. In addition the input impedance of the modem will need to be sufficiently small to ensure the communication signal is not severely attenuated. Further when many modems are connected to the system, the total system impedance increases.

Therefore Z_{RXIN} should be selected such that the amplitude of the signal at the receiver is sufficiently high when the maximum number of modems are present in the system

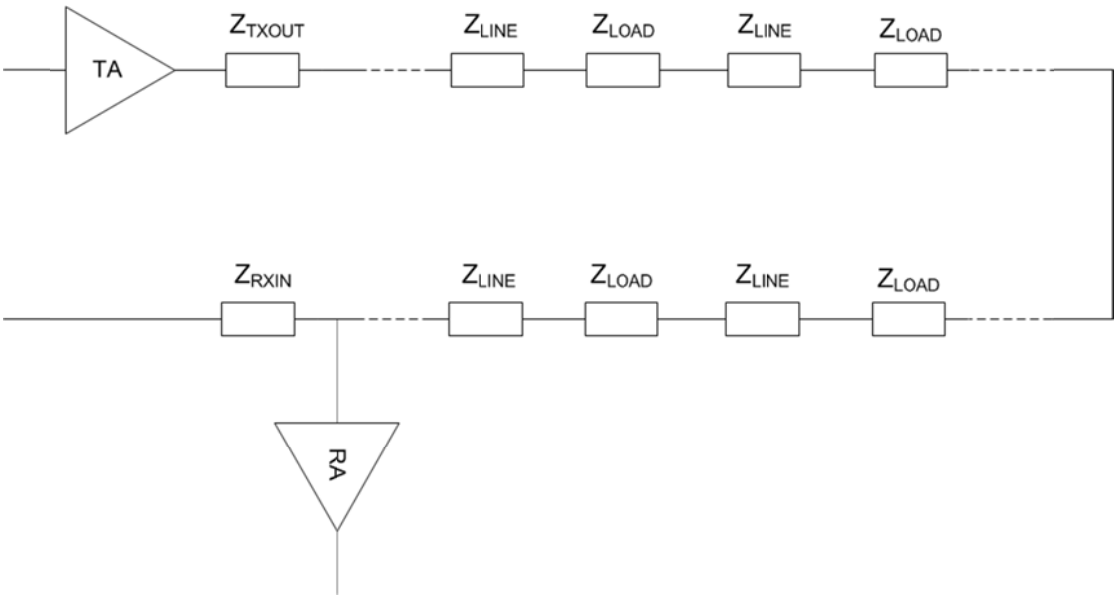


Figure 7.39 : Attenuation model - current fed HFAC bus

7.6 Frame Format

The raw data needs to be properly formatted before it can be transmitted. A frame or data packet is constructed by appending other relevant information to the raw data such as addressing information, error detection and synchronization features. The proposed frame format for this application is shown in Figure 7.40. This format is a simplified implementation derived from the frame structure of the Ethernet protocol (IEEE 802.3).

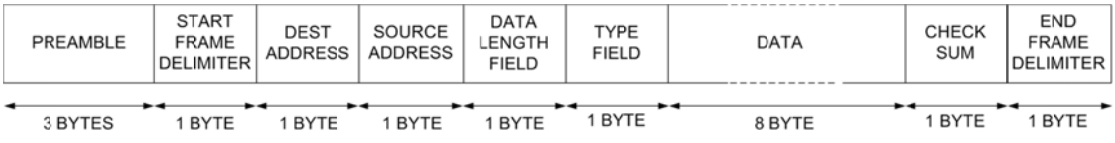


Figure 7.40 : Data frame format

The total frame length is 18 bytes. The first 3 bytes is the preamble, defined as 0xAA. These bytes consist of alternating 1s and 0s and is used to enable the PLL to lock to the received signal. This is followed by a start frame delimiter (SFD) which is 1 byte in length and is defined as 0xAB. The SFD is used to indicate the start of the frame. Next a 1 byte

destination address (DA) and source address (SA) is used for packet routing & addressing. A total of 256 modems (unique addresses) are theoretical supported. The data length field (DLF) is used to indicate the number of bytes of payload data present. The data type field (DTF) is used to indicate the type of frame; this could be used to distinguish control frames from data frames if necessary. Next eight bytes of actual raw data is sent followed by an eight bit checksum (CS) information. The checksum of the frame is calculated by taking the XOR of all the bytes in the frame up to the last data byte. Finally an end frame delimiter (EFD) is used to indicate the end of the current frame. The EFD is defined as 0xF0.

7.7 Bus Access Mechanism

It is necessary to implement a suitable bus access mechanism to enable multiple modems to exist and communicate harmoniously over a common HFAC bus. In this design, carrier sense multiple access with collision detection (CSMA/CD) was implemented. Before a node attempts to transmit information over the HFAC bus, the medium is first checked to ensure it is idle. This is done by reading the carrier sense signal. If the medium is not idle, then the modem waits until it becomes available. When the bus is idle, the modem starts to transmit the frame.

It is possible that two or more modems start transmitting at the same instant. Therefore as the modems are transmitting, it is programmed to monitor its own transmission to ensure no data collision has occurred. Collision detection is implemented by comparing the received information with the transmitted frame. If a mismatch is detected, it is assumed that a data collision has occurred. The received information is discarded and the frame transmission is aborted immediately. Then the transmitter send a jam single to ensure all nodes in the system are made aware of the collision. The jam signal consists of a string of alternating 1's and 0's with a length of 4 bytes. After the end of jam signal transmission, all modems wishing to transmit will wait for a random period of time before attempting a retransmission. The backoff time is typical chosen to be small compared to the frame duration.

However if there are many modems in the system and high communication traffic is likely, then the probability of collision will be higher under these conditions. Therefore

the backoff time will need to be determined relative to the number of detected collision. These types of techniques are implemented widely in Ethernet applications and can be adapted to HFAC PLC if necessary with minor software modification.

7.8 MCU Implementation

In this design, a dsPIC33FJ16GS502 microcontroller from Microchip Inc. operating at 40MIPS was used. Figure 7.41 shows the allocation of the control function and the special features of the MCU used for the implementation.

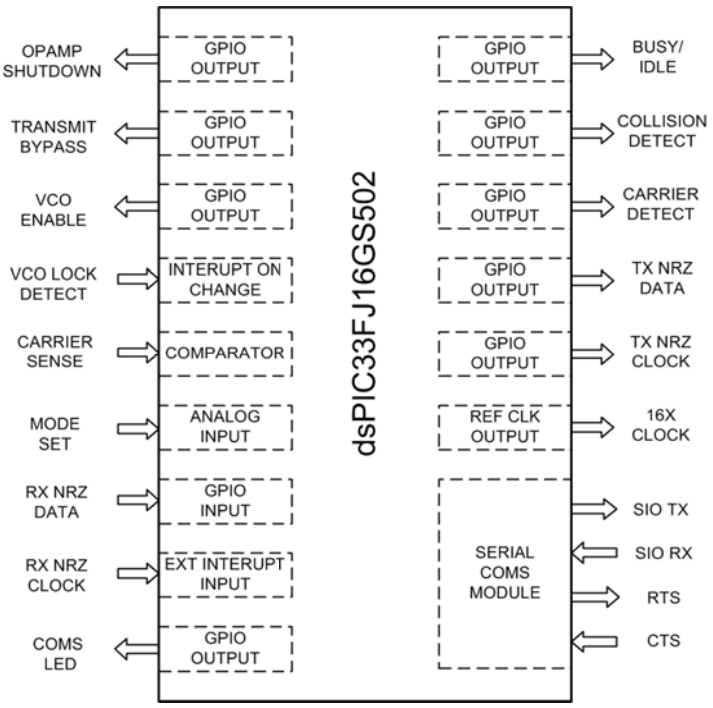


Figure 7.41 : MCU function assignment

In addition to the feature shown in Figure 7.41, two 16 bit timers were used. One timer is required for general purpose timing and another required for the NRZ transmit clock generation. The interface between the modem and the external host is defined by 3 auxiliary signal (BUSY/IDLE, COLLISSION DETECT & CARRIER DETECT) and the serial communication link. The auxiliary signals are used to inform the external system the current state of the modem. These signals are not normally required by the host in normal operating mode. The transmit information is received from the external system via the serial link which is then used to construct the transmit frame. In a similar

manner, when information is received from the bus, the MCU strips out the unnecessary information from the received frame and send the raw received data to the external system.

7.9 Experimental Setup & Results

The HFAC data modem design is shown in Figure 7.42. The description of the block are as follows : (A) power supply block (B) NRZ to Manchester converter, (C) FSK modulator, (D) Transmit LPF (E) Transmit amplifier (F) Coupling circuit (G) Receive BPF (H) Pulse shaping circuitry (I) Receive amplifier (J) FSK Demodulator (K) Clock recovery (L) Microcontroller circuitry.

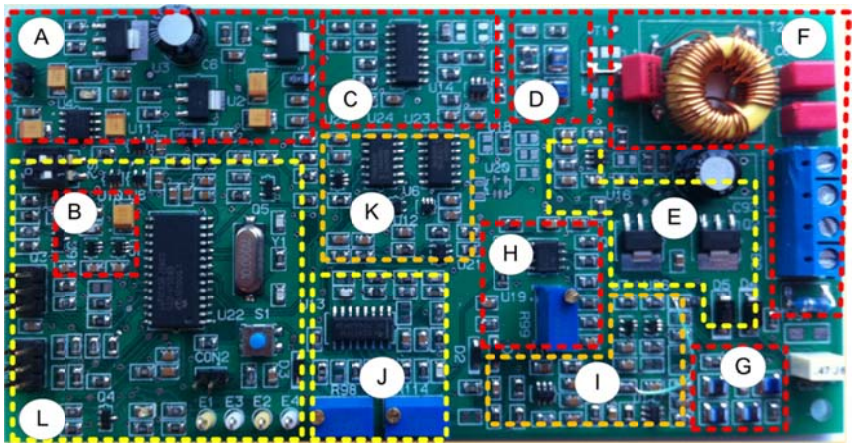


Figure 7.42 : Physical mounted PCB - HFAC modem

The experimental setup to test the capability of the system is shown in Figure 7.43 & Figure 7.44. A constant current HFAC inverter was used establish a loop current of 1.35A RMS at 50kHz. A 12W LED load was connected to the loop via a DC VRM. Two modems were connected within the loop and data was transmitted over the HFAC current bus. Two bypass stubs consisting of a series LC circuit tuned to the carrier frequency was used across the inverter and VRM to provide a low impedance path to the communication signal.

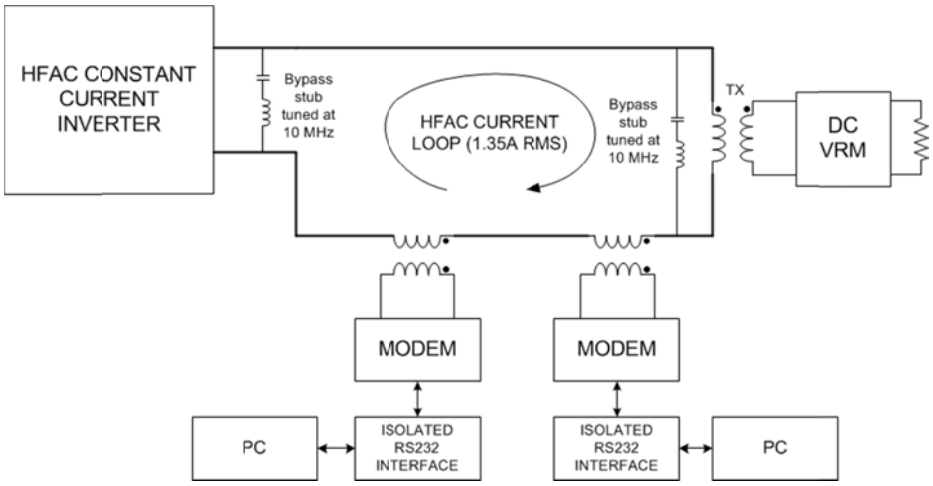
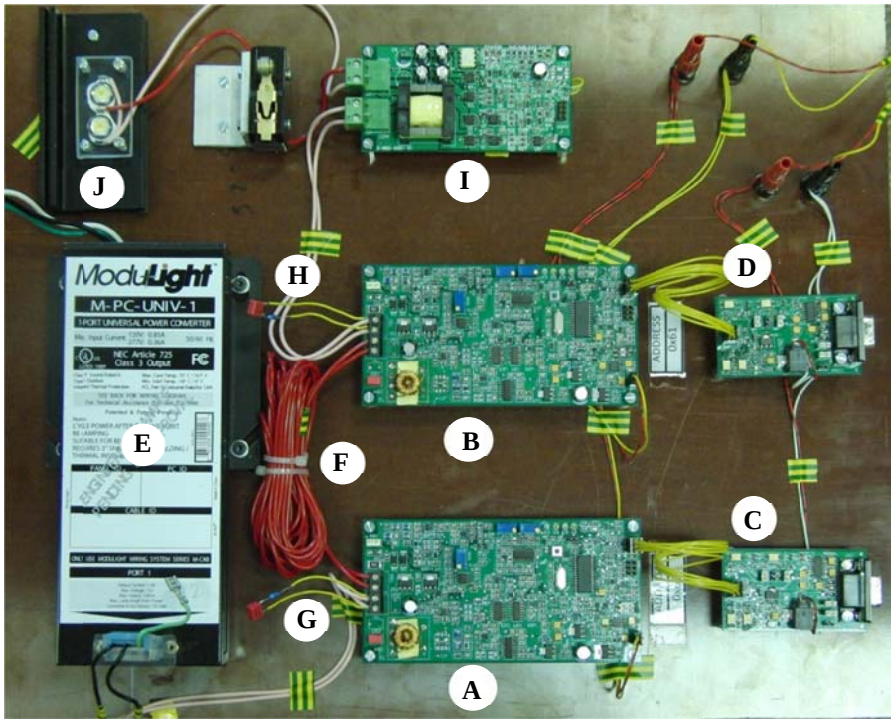


Figure 7.43 : Experimental setup of communication over HFAC current fed bus



(A & B) : Modem, (C & D) : RS-232 Interface, (E) : HFAC inverter,
(F) : Transmission cable, (G & H) : Tuned bypass stub, (I) : VRM, (J) : Load

Figure 7.44 : Photo of HFAC modem experimental setup

The intended transmit frame data and the MCU generated NRZ transmit data is shown in Figure 7.45 and Figure 7.46 (a) to (e) respectively. The raw transmit information was received from an external host (a PC in this experiment) and based on this information the transmit frame was constructed. It can be seen that the generated data matches the intended transmit frame exactly. The NRZ clock frequency is approximately 38.983 kHz, and one bit of data transmitted at every clock period.

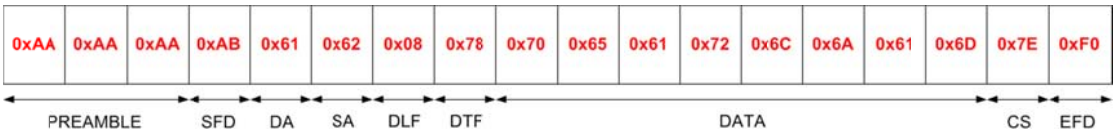
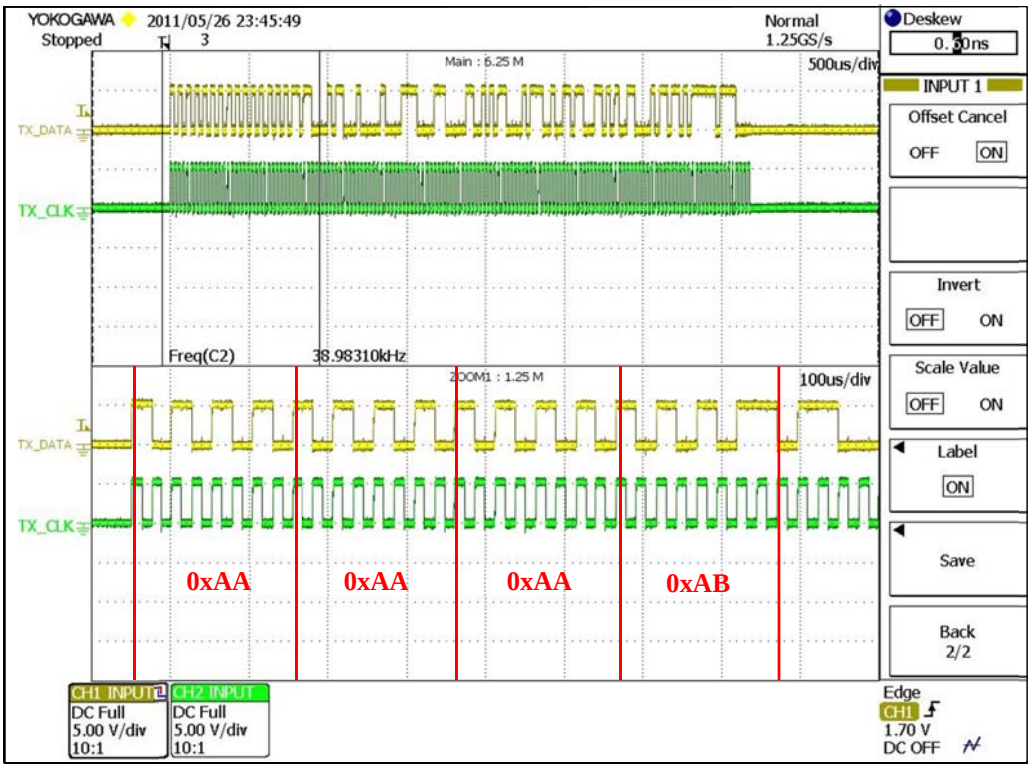
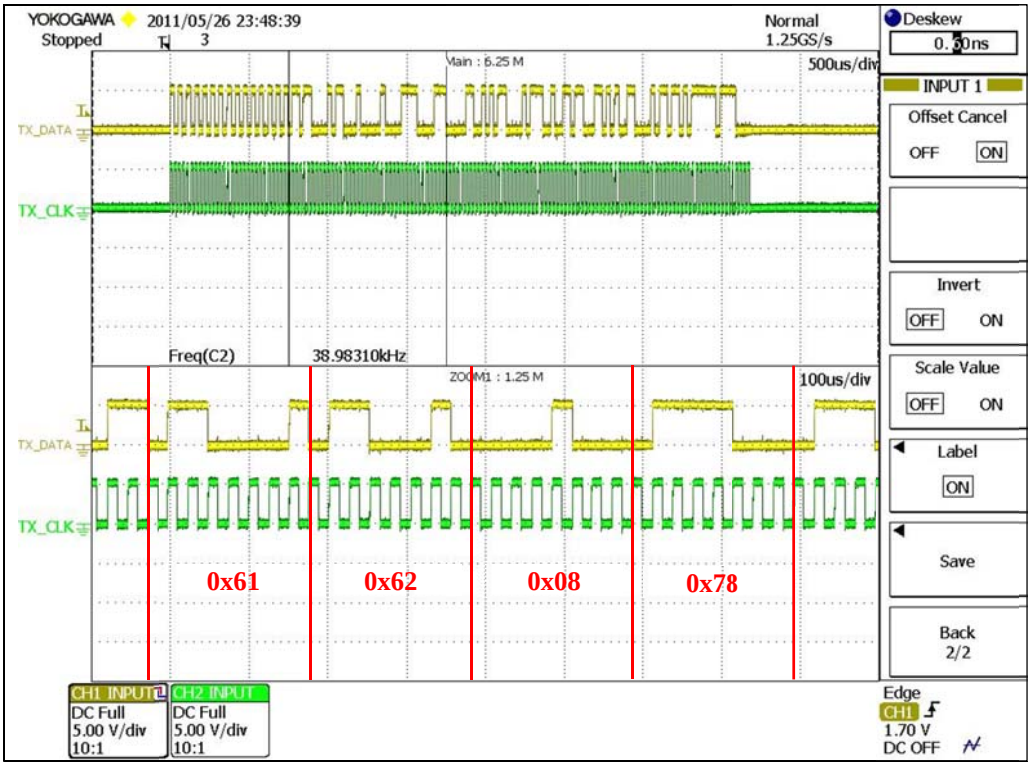


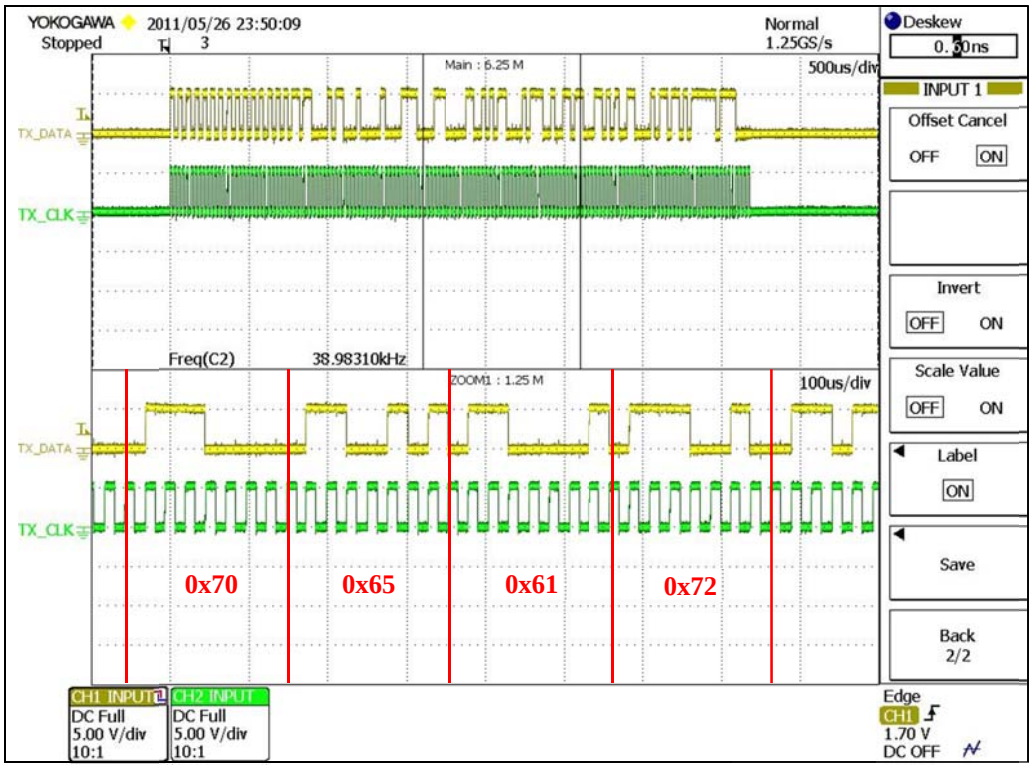
Figure 7.45 : Transmit frame data



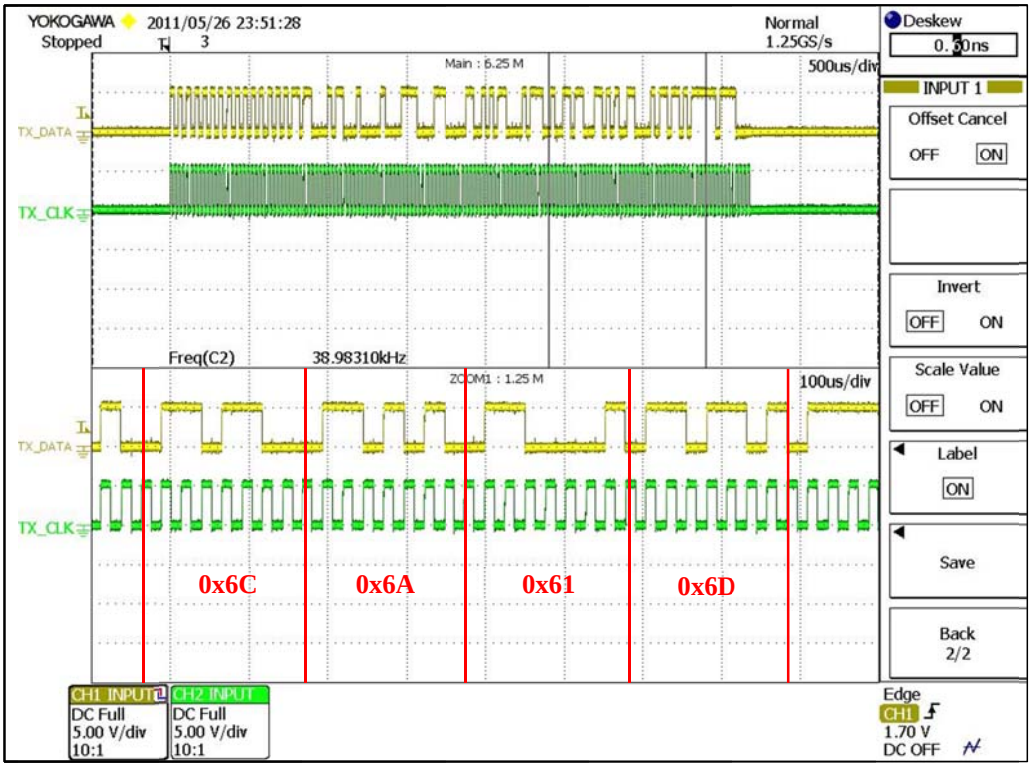
(a)



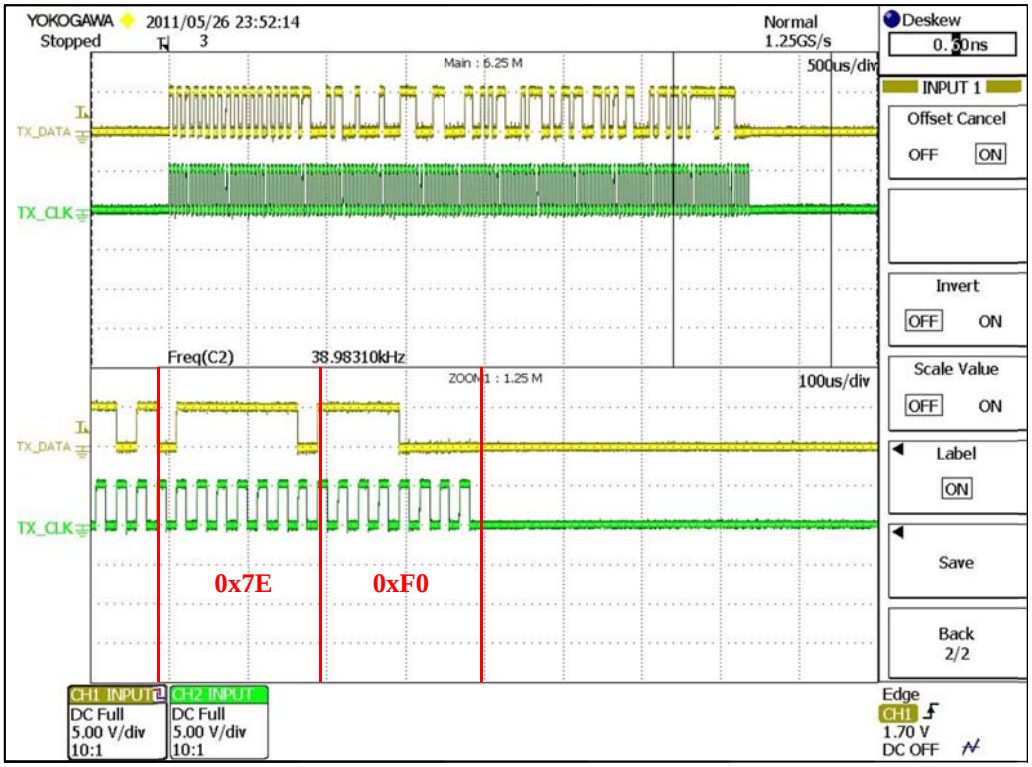
(b)


YOKOGAWA
2011/05/26 23:50:09
Stopped
Normal
1.25GS/s
Main : 6.25 M
500us/div
TX_DATA
TX_CLK
Freq(C2)
38.98310kHz
ZOOM1 : 1.25 M
100us/div
0x70
0x65
0x61
0x72
Deskew
0.00ns
INPUT 1
Offset Cancel
OFF ON
Invert
OFF ON
Scale Value
OFF ON
Label
ON
Save
Back
2/2
CH1 INPUT
DC Full
5.00 V/div
10:1
CH2 INPUT
DC Full
5.00 V/div
10:1
Edge
CH1
1.70 V
DC OFF

(c)


YOKOGAWA
2011/05/26 23:51:28
Stopped
Normal
1.25GS/s
Main : 6.25 M
500us/div
TX_DATA
TX_CLK
Freq(C2)
38.98310kHz
ZOOM1 : 1.25 M
100us/div
0x6C
0x6A
0x61
0x6D
Deskew
0.00ns
INPUT 1
Offset Cancel
OFF ON
Invert
OFF ON
Scale Value
OFF ON
Label
ON
Save
Back
2/2
CH1 INPUT
DC Full
5.00 V/div
10:1
CH2 INPUT
DC Full
5.00 V/div
10:1
Edge
CH1
1.70 V
DC OFF

(d)



(e)

Figure 7.46 : Actual transmit frame data waveform capture

To simulate a system with many modems, a series resistor was added to the transmit path to limit the transmit current to under 10mA. This is representative of a system with approximately twelve modems with input impedance of 100Ω each. In addition, amplitude imbalance in the logic 0 and logic 1 carrier frequencies were simulated by tuning the low pass filter just under 10MHz. Therefore a larger attenuation at logic 1 carrier frequency (12.5MHz) is observed.

In Figure 7.47 the transmitted data and the loop current waveform with the bus power turned OFF is shown. The yellow trace (CH1) represents the transmit NRZ data and the pink trace (CH3) represents the Manchester encoded transmit data. The green trace (CH2) is the loop current waveform, captured at 10mA/Div. The reconstructed received signal at the receiver modem (output of the pulse shaping block) is represented by the blue trace (CH4). It can be observed that the amplitude of the logic 0 carrier is approximately 10mA and the logic 1 carrier amplitude is approximately one third of the logic 0 carrier amplitude. It is important to note that although the loop current waveform resembles an amplitude modulated signal, it is in fact a FSK modulated signal with the logic 1 carrier deliberately attenuated. This is done to model non idealities in the filter

frequency response and the attenuation of the signal due to inductance of the HFAC bus which could result in the logic 1 carrier frequency (12.5MHz) to be attenuated by a greater degree. The zoomed view of Figure 7.47 shows that the signal at the receiving end is successfully reconstructed despite the amplitude difference in the logic 1 and logic 0 signals. This can be verified by examining Figure 7.48 and Figure 7.49.

Using the same setup, the communication features were tested with the bus power turned ON (1.35A RMS at 50kHz). Figure 7.50 shows the waveform of the transmitted information captured at the source modem (CH1) and the received waveform captured at the destination modem (CH3). It can be seen that the information was successfully transmitted over a powered HFAC bus. The bus current is represented by the green trace (CH2), captured at 1A/Div. It can be seen that the bus RMS current is 1.31A with a frequency of 50.24 kHz. A stable and consistent bitrate of 38kbps was achieved.

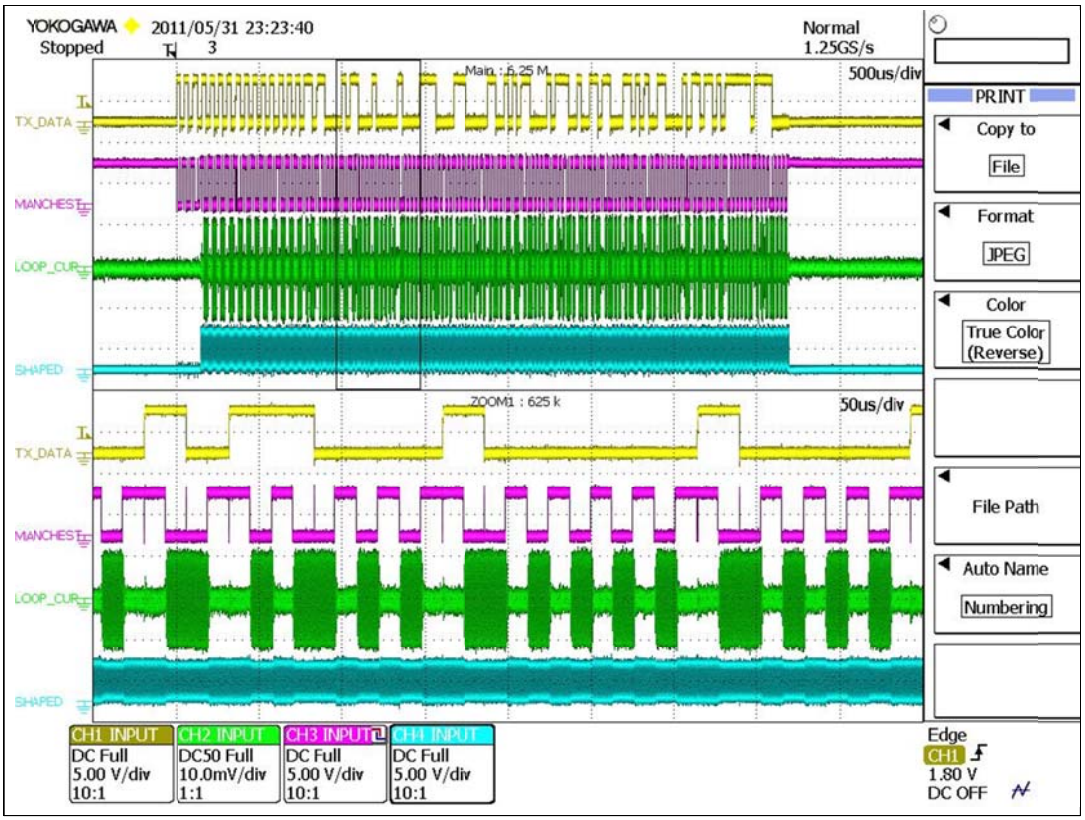


Figure 7.47 : Communication signal loop current waveform

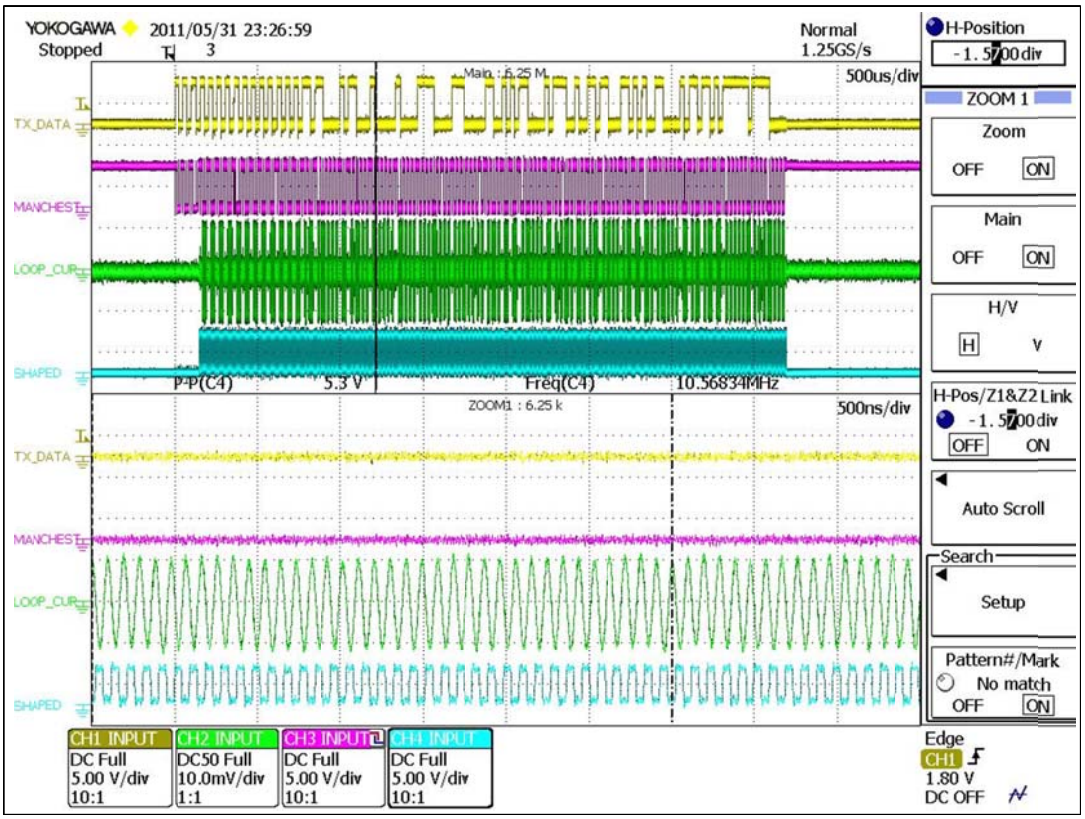


Figure 7.48 : Reconstructed signal at receiver - logic 0

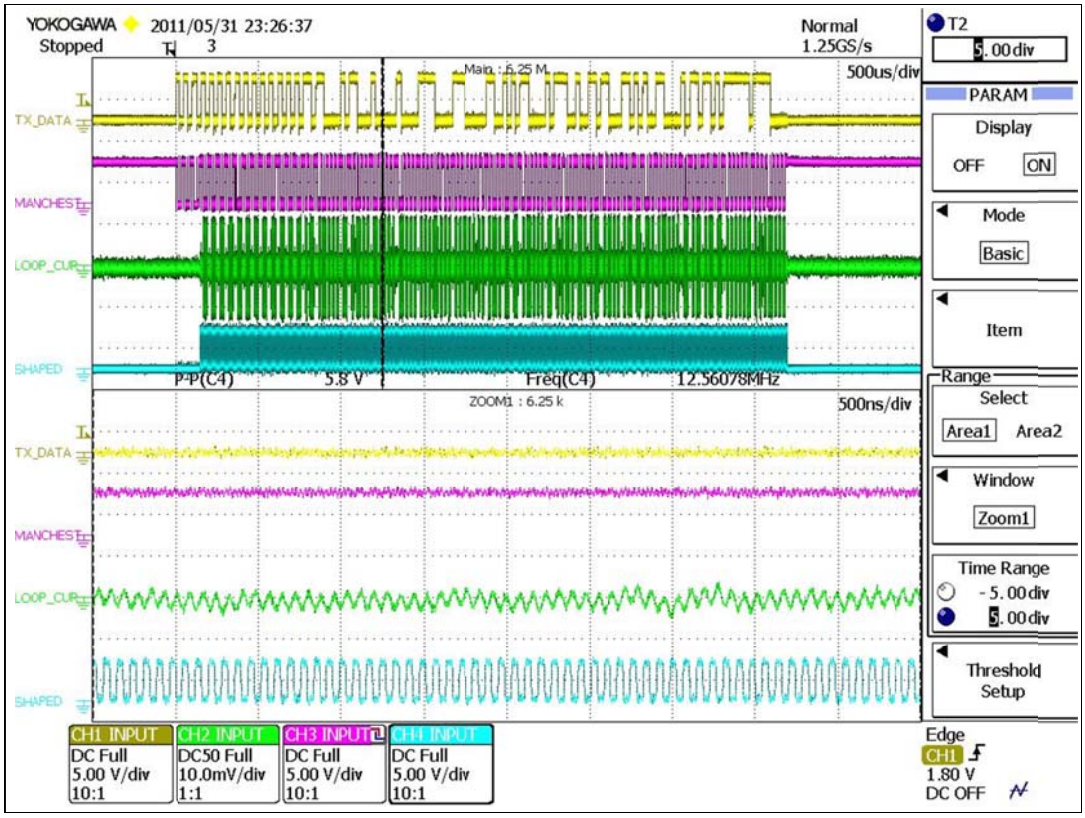


Figure 7.49 : Reconstructed signal at receiver - logic 1

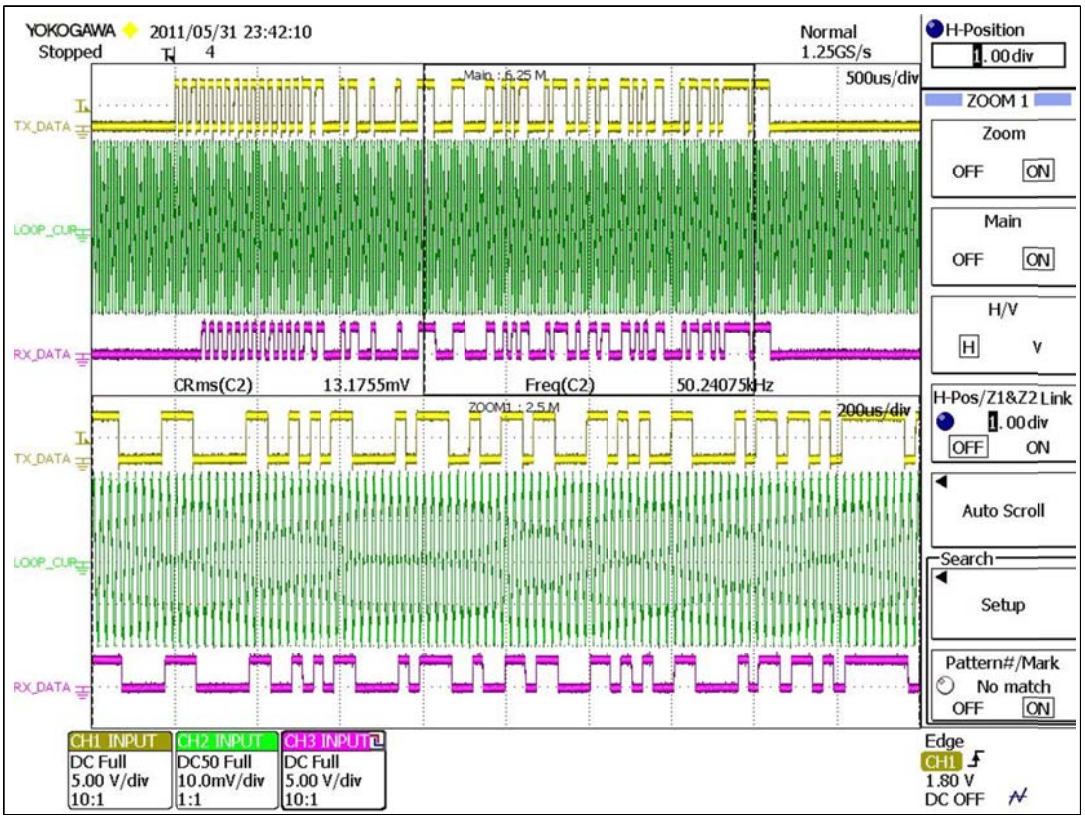


Figure 7.50 : Transmitted and received NRZ data over HFAC bus

7.10 Concluding Remarks

In this chapter, communication over a HFAC constant current bus has been demonstrated. A data modem capable of implementing bidirectional communication at a data rate of 38kbps over the HFAC power bus was proposed. Carrier sense multi access with collision detection (CSMA-CD) bus arbitration scheme was implemented to enable multiple node addressable bidirectional communication. Enabling communication over the HFAC network has vast potential that can be exploited in implementing intelligent power management scheme in a multiple inverter and multiple load HFAC network.

CHAPTER 8

DISCUSSIONS & CONCLUSION

"It is not the possession of truth, but the success which attends the seeking after it, that enriches the seeker and brings happiness to him" – ***Max Planck, 1858-1948.***

This chapter concludes the dissertation. It begins with a discussion on the possibility of converting the HFAC DPS to an intelligent power network. It is shown how the work presented in the previous chapters come together to form the main building blocks that are required to introduce intelligence to the HFAC DPS. Potential advantages and application examples are presented. The main findings of the proceeding chapters are assembled and an overall conclusion to the research is presented. It is shown that the main aims and objectives set out in the initial stage of this project have been successfully achieved. Aspects of this work that require further research to address limitations and potentially interesting areas not within the original scope of this project that warrants further investigation is suggested.

8.1 Discussions

To date most research in the area on HFAC is focused on the power processing and delivery aspects. To this end, various novel power conversion topologies and control schemes have been proposed with the aim of improving the overall efficiency of the HFAC DPS. As part of this work, a different approach to the research is presented. Rather than viewing the HFAC DPS as merely a power delivery system, the possibility of converting it into a more intelligent architecture is investigated. An intelligent power delivery system could offer interesting possibilities such as (i) better utilization of the various power processing structures in the system (ii) capturing performance statistics of the system (iii) metering power consumption and duty cycle of individual loads (iv) intelligent scheduling of non-critical loads (v) health monitoring and fault reporting and (vi) intelligent anticipatory control implementation.

Applying intelligent management techniques, at any given instant the power flow could be effectively coordinated to ensure load demand is optimally met in the most efficient manner. In a system with many dynamic loads with varying power demand and operating duty cycle, having real time information of the instantaneous power demand of the bus could offer a significant opportunity for improving overall system performance. Based on demand, optimal power routing strategies from the numerous front end power converters could be determined on a real time basis. This would help enhance system efficiency beyond what is possible by only increasing operational efficiency of individual power converters.

In some applications, often more than one type of power source is present with each source possibly having different power trajectory. Additionally, the availability and capacity of power sources could be a function of time. This is true for most renewable sources. For other types of sources such as mains power, cost is normally a function of time, where off peak consumption is often less costly. This information could be incorporated in the power arbitration strategy to better manage and utilize energy resources or instead could be used to implement load scheduling. Non critical, low priority loads could be powered only when the capacity exists or when economically viable.

The potential for intelligent management in HFAC DPS is vast. Most of the key smart grid features could potentially be implemented in a HFAC environment. The primary requirement to enable intelligent management in a HFAC distributed power system is the ability to communicate and control. The various power sources, power converters and loads in the system need to be able to communicate with one another seamlessly. Having this ability would allow every subsystem to identify itself and communicate power demand and other necessary information to the system controller. The system controller can then decide the proper course of action based on the current state of the bus and issue relevant commands to various front end HFAC inverters in the systems demanding a particular action.

The front end inverters in the system need the ability to control the power flow in response to the state of the system. Therefore the inverters require the capability to turn ON and OFF depending on demand. As there may be many power converters in the system, the inverter must be capable of parallel operation to avoid circulating current. Additionally, the ability for the inverter to dynamically vary its internal control loop parameters based on anticipated changes in the system offers the possibility for improved transient performance. For example if the system is expected to see sudden heavy loading, the reference input to the controller could be increased to avoid large voltage dip. It is apparent that some form of digital function in the HFAC inverter is necessary to process the received information and respond accordingly. It is possible that a digital supervisory circuit be added to work in tandem with the existing analog control loop of the inverter. A more desirable solution would be to implement the entire control loop digitally.

In chapter 3, a digitally controlled multi stage HFAC inverter capable of independent control of phase angle and voltage magnitude is presented. This design has parallel operation capability and is ideal as a front end HFAC inverter in an intelligent HFAC DPS. In chapter 5, the proposed HFAC power line data modem has been demonstrated to enable robust bidirectional communication over the HFAC bus. This satisfies the communication requirement in the implementation of intelligent HFAC DPS. The system controller can be implemented using a simple microcontroller coupled with a modem for communication. The controller shall be programmed to perform high level power management functions based on the information about the loads and power

converters in the system. In complex systems, this function can be performed by a computer. Conversely in simpler systems, the role of the system controller could be delegated to any power converter in the system.

The block diagram of the traditional HFAC inverter module is shown in Figure 8.1 (a). It can be seen that it consists of only a power block and an analog control loop. The block diagram of an intelligent HFAC inverter is shown in Figure 8.1 (b). This inverter consists of a power stage, a digital control loop, a set of contactors and a communication module (HFAC data modem). A similar block diagram for the POL converter is shown for both the traditional and intelligent version in Figure 8.2 (a) and (b) respectively. It can be seen that the power and control stage of both variants are the same. In the intelligent version, a MCU is required to interface with the modem and control the contactors. This MCU is not involved in the control of the power stage of the POL and therefore any low performance MCU would be sufficient.

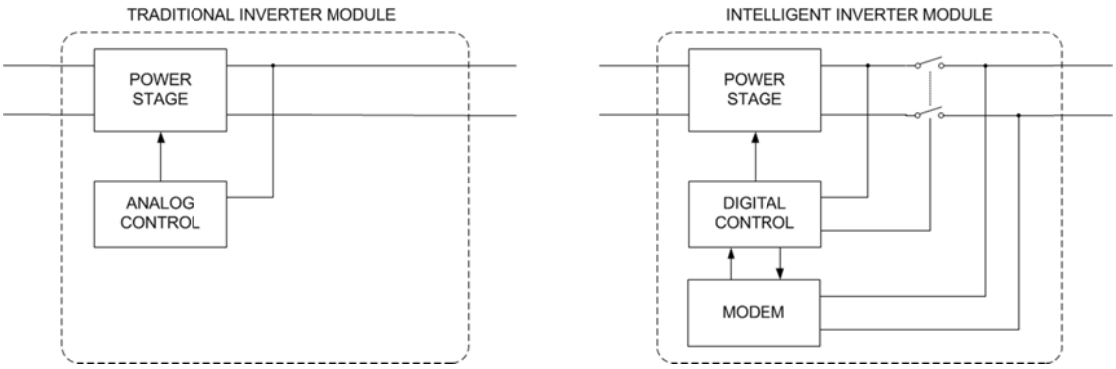


Figure 8.1 : HFAC inverter module (a) traditional (b) intelligent

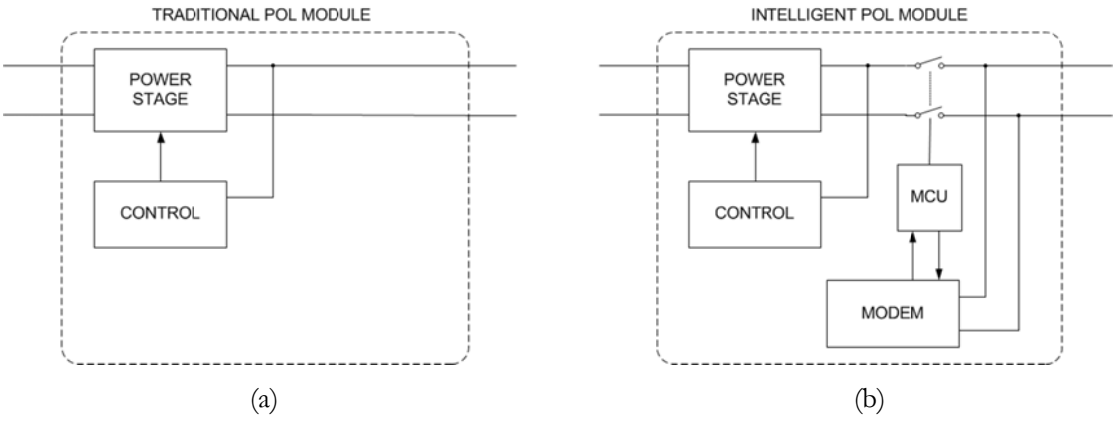


Figure 8.2 : POL converter module (a) traditional (b) intelligent

With all the 'enabling technologies' available, an intelligent HFAC DPS can be realized. Power management algorithms and strategies are normally custom designed for a particular application and are out of the scope of this research. However some implementation examples are discussed below to demonstrate the advantages of introducing intelligence to the HFAC DPS.

In [77], it is shown that by paralleling power supply, the efficiency curve of the resulting combination may extend the 'high efficiency' operation range. It is well known that in power converters the efficiency curve is fairly constant from full load to reasonably light loads. As the load falls further, the efficiency starts to drop. A hypothetical representation of the efficiency curve is shown in Figure 8.3. It is assumed that the converter has constant 'high efficiency' from 20% to 100%. Below 20%, the efficiency falls linearly with a steep slope. While practical converters exhibit a more gradual curve, nevertheless the hypothetical representation is useful to illustrate the advantages attained in efficiency range in paralleled converters as described in [77].

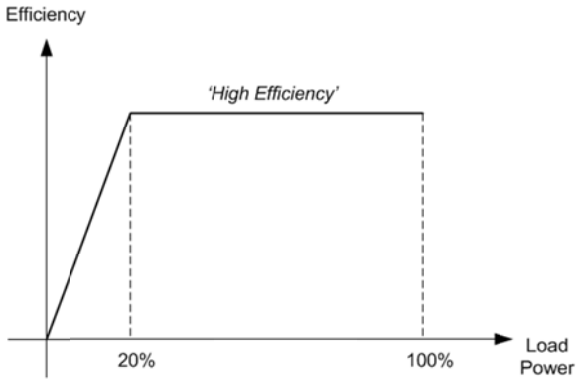


Figure 8.3 : Inverter hypothetical efficiency curve

Consider a system with two HFAC power converters operating in parallel and powering a common bus as shown in Figure 8.4. Both converters, P1 and P2 are rated at 500W each, and have a 'high efficiency' range from 20% to 100% load (100W to 500W). The combined system has a total power output capacity of 1000W and has a 'high efficiency' operating range from 100W right up to full load at 1000W. In this configuration, the theoretical 'high efficiency' range extends from 10% to 100%. To achieve this, when the load is less than 100W, only one converter is turned ON. Beyond 100W, both P1 and P2 are turned ON and the load current is shared between the two converters.

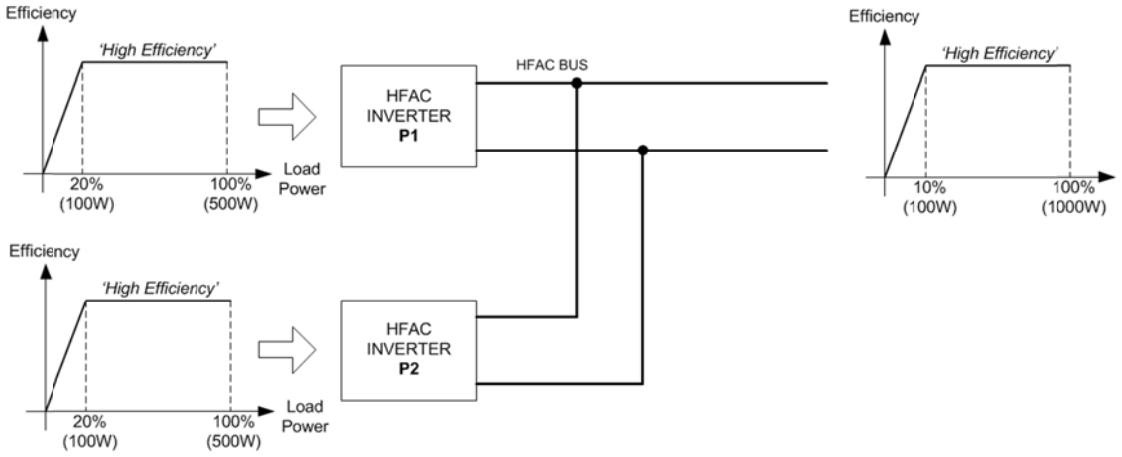


Figure 8.4 : Hypothetical efficiency curve - parallel inverter combination

In an intelligent HFAC DPS, with the efficiency curve of the various inverters and power rating of all loads in the system known, the system power management controller can identify the most efficient way of powering the bus by deciding which inverter to turn ON and which to be kept OFF. When new loads are added to the bus, it can be programmed to inform the system controller of its average power rating. Therefore the power management controller is constantly kept up to date on the actual loading of the system. This form of automatic control to ensure optimal operation of the power system is not possible on traditional HFAC DPS.

Connecting or disconnecting large loads can cause the bus voltage to temporarily fluctuate. Therefore before the load contactors are engaged (or disengaged), the HFAC inverter can be made aware of the situation. This offers the opportunity for the inverters to proactively respond to the event by varying its internal control parameters and potentially reducing the undesired transients. In the scenario where many loads are simultaneously connected or disconnected from the bus, the effects can be similar to the case discussed above. However in this case, there are other possible techniques that can be applied. The system controller can sequentially activate (or deactivate) each load with a small time lapse such that the bus voltage is allowed to stabilize.

In this section, several examples have been provided to demonstrate the potential efficiency enhancement and reduction of transient effects that can be attained in an intelligent HFAC DPS that is difficult or impossible to achieve in a traditional HFAC system.

8.2 Conclusion

This work presents a fresh perspective to the HFAC distributed power systems. Traditional views of looking at the HFAC DPS merely as a passive power distribution architecture is challenged. The main 'enabling technologies' required to realize an intelligent HFAC DPS were identified and developed. It is demonstrated that the communication over the HFAC bus without the need for additional communication channel can be achieved. A data modem that enables bidirectional multi node communication over the HFAC bus was designed, built and experimentally tested. Bus arbitration was implemented using CSMA-CD, and various features of Ethernet communication protocol were emulated were applicable and necessary.

The modem allows easy integration, and is capable of communicating with any host device with a simple serial communication interface. All communication functions are done transparently to the host. The modem has the capability to work with both voltage and current fed HFAC systems with only minor variation required in the coupling circuit. The modem was experimentally demonstrated to work reliability under simulated non ideal conditions. The hardware and software design aspects of the HFAC data modem is documented in great detail in this work.

Digital control implementation in the front end HFAC inverter is desirable in an intelligent HFAC DPS. This was demonstrated to be viable for low and medium frequency applications. Additionally, optimal design techniques were developed as part of this research to guide the design of the HFAC inverter. In the domain of point of load converter, power factor improvement techniques were presented for an integral cycle converter.

Some interesting findings were uncovered in the course of this research. These cover the following three areas (i) Front end inverter (ii) Integral cycle converter and (iii) Communications module. Based on the work carried out in the current study, the following conclusions can be drawn:

8.2.1 HFAC Inverter

- In a HFAC MSI, the selection of the operating parameters of the front end DC-DC converter have been shown to have important efficiency and design implications on the second stage resonant inverter. Current designs view the front end DC-DC stage as merely as a means for independent amplitude control. In this work, the output voltage of the front end DC-DC converter is treated as a design variable and is selected based on efficiency and design constraint.

- It was shown that using sinusoidal approximation to simplify the mathematical model, the calculated RMS currents and voltages in the resonant inverter can be determined with high accuracy (> 98%) for the values of k_p between 1.1 to 1.5 and Q_s and Q_p between 1 to 5. Within this prescribed range, the simplified model is a good approximation to the more complex model presented in section 4.1.3.

- A design objective and physical constraint driven optimization technique was proposed to determine ideal design parameters. With the simplified inverter model, the computation effort is significantly reduced. Mathematical models to estimate losses in physical component due to parasitic resistance were incorporated in the model. The predicted results show good correlation with experimental measurements.

- It was demonstrated that independent phase angle and amplitude control of the HFAC MSI can be implemented using a digital controller for low and medium frequency HFAC implementation. It was also shown that the HFAC MSI controller is no more complex than a digital controller for regular buck or boost converter hence it can be implemented without the need for very high end digital signal processors.

8.2.2 Integral Cycle Converter

- In a HFAC integral cycle converter it was shown that there are numerous ways to synthesis an output voltage for a given DC level. Mathematical model to establish the relationship between the synthesis sequence and the harmonic spectrum were developed. Using this model it was shown that each synthesis pattern has a unique input current harmonic spectrum.

- An intuitive method to describe the relationship between the elements of the switching matrix and harmonic composition was presented. Using this technique, it was demonstrated that manipulating the harmonic amplitude at a given frequency can be implemented using simple rule based techniques. This eliminates the necessity to compute the harmonic spectrum online every time the output voltage is increased or decreased.

- It was demonstrated that by using optimized switching patterns, the attainable power factor for a given frame length and average output voltage is higher compared to any other switching patterns. The difference in power factor is greater at lower output voltages.

- Selective harmonic elimination in the input current to suppress the frequency components nearest to the bus frequency reduces distortion and helps to relax the constraints imposed on the design of the input filter.

8.2.3 Communication

- Using the HFAC bus voltage frequency as the synchronizing clock for data transmission increases the probability of data collision due to the requirement for the transmission to be synchronized with the zero crossing point. It was shown that using Manchester encoding and a suitable clock recovery circuit, data transmission can be made independent of the bus voltage.

- As opposed to the voltage fed HFAC DPS, the collision detection capability degrades as the number of modems in the current fed HFAC DPS increases. It was shown that a combination of a high gain amplifier and pulse shaper helps eliminate this problem. Experimental measurements have shown that the output of the pulse shaper is indistinguishable for input of 100mVpp and 2Vpp.

- It was shown that the response of the modem coupling circuit in a current fed HFAC loop is not independent of the number of modem N_m, in the system. As Nm increases, the voltage transfer function $H(s)$, exhibits two peaks of high amplitude. The amplitude of the peak is proportional to Nm and the frequency at which the peaks occur has been shown to be fairly independent of N_m. Coupling circuit design guides have been proposed to reduce the effect of the sensitivity of $H(s)$ to variation in N_m.

- The differential coupling techniques proposed for the HFAC data modem in a current fed HFAC DPS increases immunity against common mode noise.

8.3 Future Work

In the investigation of the HFAC inverter, it has been demonstrated that the phase angle of the second stage resonant inverter can be synchronized with a reference signal. However there will be a small fixed phase difference due to the delay in the response of gate driver IC and variation in the resonant element due to tolerances. Further work can be done to eliminate this error. Among the possible solution would be to program the DSP to generate the synchronizing signal based on provided reference. With this technique, differences in the phase can be measured and the synchronizing signal could be advanced or delayed as necessary.

In a HFAC DPS there may be many inverters operating in parallel. Each of these inverters may have varying power capacity and efficiency curve. As such, it is possible that under some conditions, it would be beneficial to share the current unequally. Under these types of scenarios, implementing weighted current sharing among the many HFAC front end inverters is desirable. This can potentially offer a wider spectrum of power

routing strategy that may offer further efficiency improvement opportunities. Investigation into digital control techniques incorporating weighted current sharing is an interesting area that warrants further research.

In high frequency HFAC application, where full digital control techniques are not viable, the possibility of incorporating digital supervisory features to work with the existing analog control loop of the power stage in the front end HFAC inverter could be investigated. Successful implementation of this strategy would allow most of the intelligent management features to be realized. Combination of analog and digital control techniques could also be exploited in low and medium frequency application where the implementation of full digital control does not offer sufficient control bandwidth.

The model used in the optimization process for the design of the resonant inverter could be further refined. In the current model, one of the objective functions is the capacitor voltage. The actual RMS voltage a capacitor can tolerate at a given operating frequency and temperature however is dependent on the value of the capacitance and the physical size. Therefore defining the maximum operating voltage could be restrictive as lower capacitor value can normally tolerate a higher voltage for a given size. Accounting for this fact could result in a more accurate model. Additionally, estimation for resonant inductor core loss and other losses as described in [113] could be incorporated in the model.

One of the interesting features of a HFAC DPS is the possibility of implementing contactless power transfer. Further research in this area to design an efficient coupling transformer that enables high efficiency power transfer is needed. However implementation of contactless power in an intelligent HFAC DPS could pose some concerns to the communication aspects. In inductive power transfer implementations, the coupling transformer has high leakage inductance due to the poor coupling between the primary and the secondary coils. The leakage inductance could severely attenuate the high frequency communication signal. This problem needs to be further investigated.

To quantify the efficiency benefits offered by intelligent management of the HFAC DPS, a complete smart power network consisting of numerous front end inverters and loads could be developed and efficiency experimentally determined for various operating

conditions. This could provide the most convincing demonstration of the benefits of an intelligent HFAC DPS.

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APPENDICES

APPENDIX A

Distribution Losses Comparison for Sinusoidal & Square Wave HFAC

Consider a sinusoidal and square wave HFAC inverter, both powering a fixed resistive load of R ohms and delivering a fixed power of P_{load} , as shown in Fig A1.

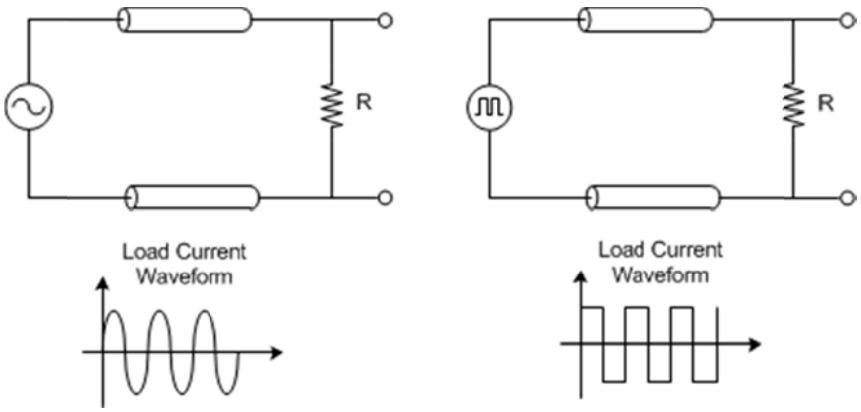


Figure A1 : Sine and square bus waveform

The RMS current delivered to the load for both cases is given in (A.1). Using Fourier analysis, the square wave bus current can be decomposed to the constituting harmonic component as given by (A.2). (Symmetric waveform is assumed)

$$I_{rms} = \sqrt{\frac{P_{laod}}{R}} \tag{A.1}$$

$$I_{sq}(t) = \sum_{n=1,3,5...}^{\infty} \frac{4I_{rms}}{\pi n} \sin(2n\pi f_o t) \tag{A.2}$$

The total distribution resistance is a sum of the static DC resistance and the frequency dependent AC resistance. The AC resistance is a frequency dependent component and due to skin effect it increases proportionally to the square root of the current frequency f [114]. Therefore the distribution resistance can be expressed as (A.3), where α and β are constants that are dependent only on the geometrical structure and material of the distribution cable.

$$R_{dist} = \alpha\sqrt{f} + \beta \tag{A.3}$$

The total distribution loss in a sinusoidal HFAC system can be computed using (A.1) & (A.3) and is given as

$$P_{loss\_\sin} = I_{rms}^2\left[\alpha\sqrt{f}\right] + I_{rms}^2\beta \tag{A.4}$$

For the square wave case, each harmonic component of the current contributes to the total distribution loss. However the effective resistance seen by the current increases with frequency. The total distribution power loss can be calculated using (A.2) and (A.3) and is given by (A.5)

$$P_{loss\_square} = \sum_{n=1,3,5..}^{\infty}\left(\frac{4I_{rms}}{n\pi\sqrt{2}}\right)^2\left(\alpha\sqrt{nf_o} + \beta\right) \tag{A.5}$$

Equation (A.5) can be simplified to (A.6). It can be seen that the distribution losses due to skin effect is about 36% greater in the square wave HFAC bus system for the same load power. As expected the losses due to the static dc resistance is same for both bus waveform.

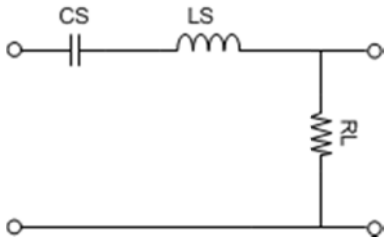
$$P_{loss\_square} = (1.3689)I_{rms}^2\left[\alpha\sqrt{f_o}\right] + I_{rms}^2\beta \tag{A.6}$$

APPENDIX B

PSPICE Simulation – Resonant Tank Response

Series Resonant Tank	
Figure	**Description**
Figure B1	SRC - Voltage gain (V_{out}/V_{in}) vs tuning factor (f_s / f_r)
Figure B2	SRC - Resonant tank current (I_r) vs tuning factor (f_s / f_r)
Figure B3	SRC - Phase angle of tank input impedance ($\angle Z_{in}$) vs tuning factor (f_s / f_r)

Circuit :



Notes :

1. Q_s is defined as $\omega_s L_s / R_L$
2. $\omega_s = 1/\sqrt{L_s C_s}$

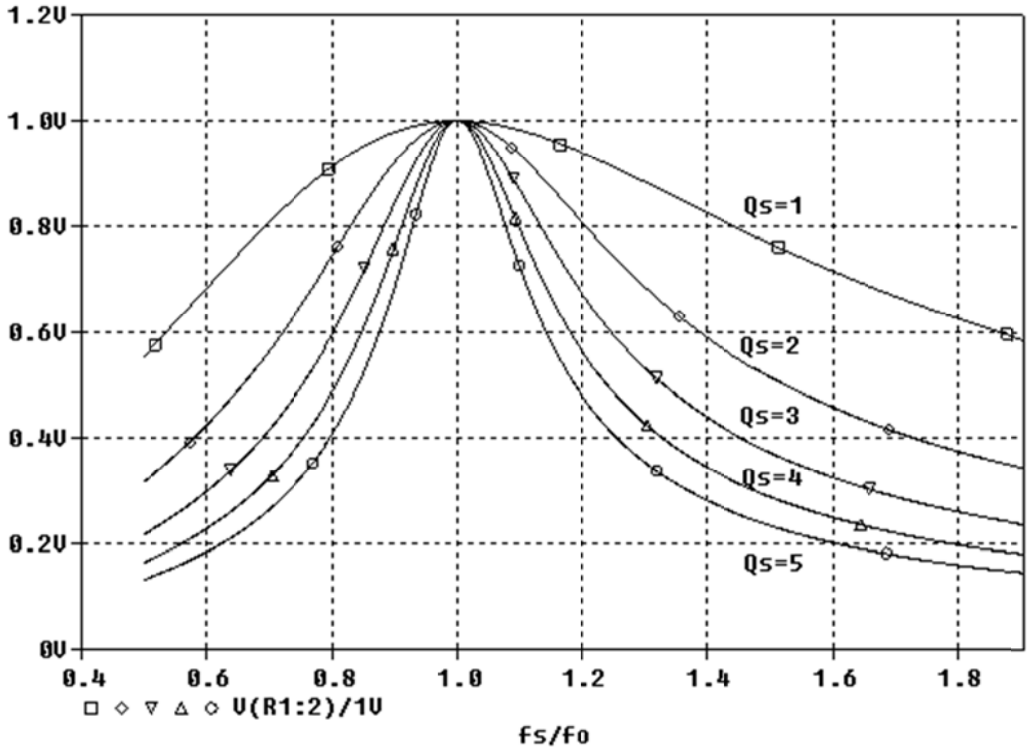


Figure B1 : SRC - Voltage gain vs tuning factor

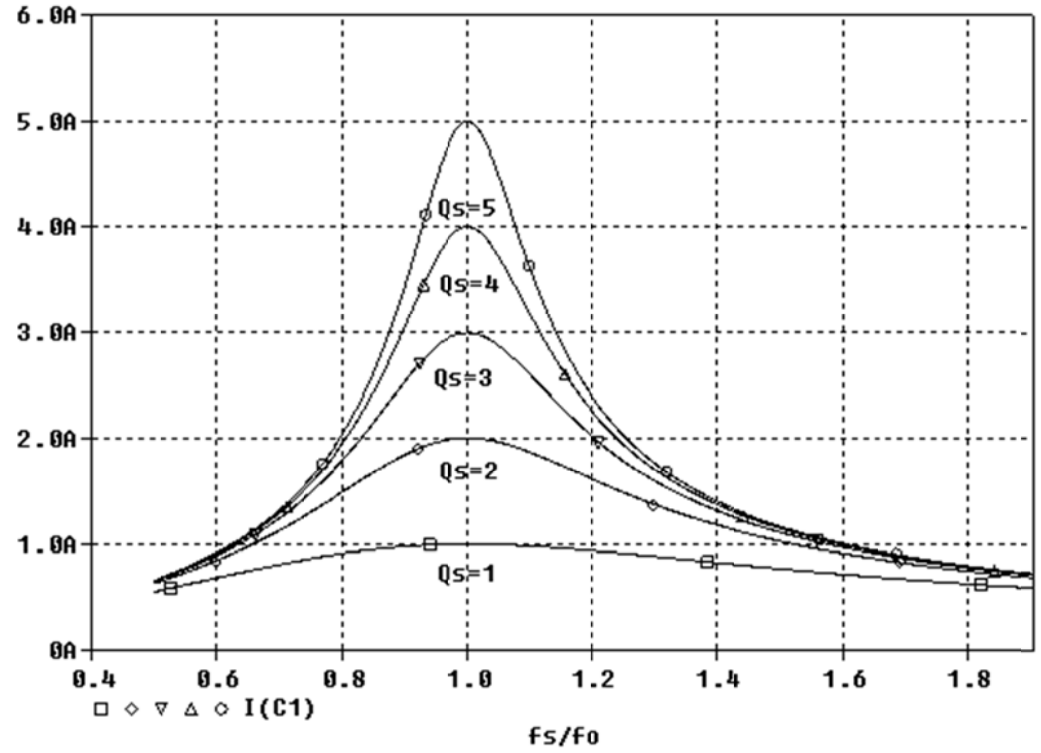


Figure B2 : SRC - Resonant tank current vs tuning factor

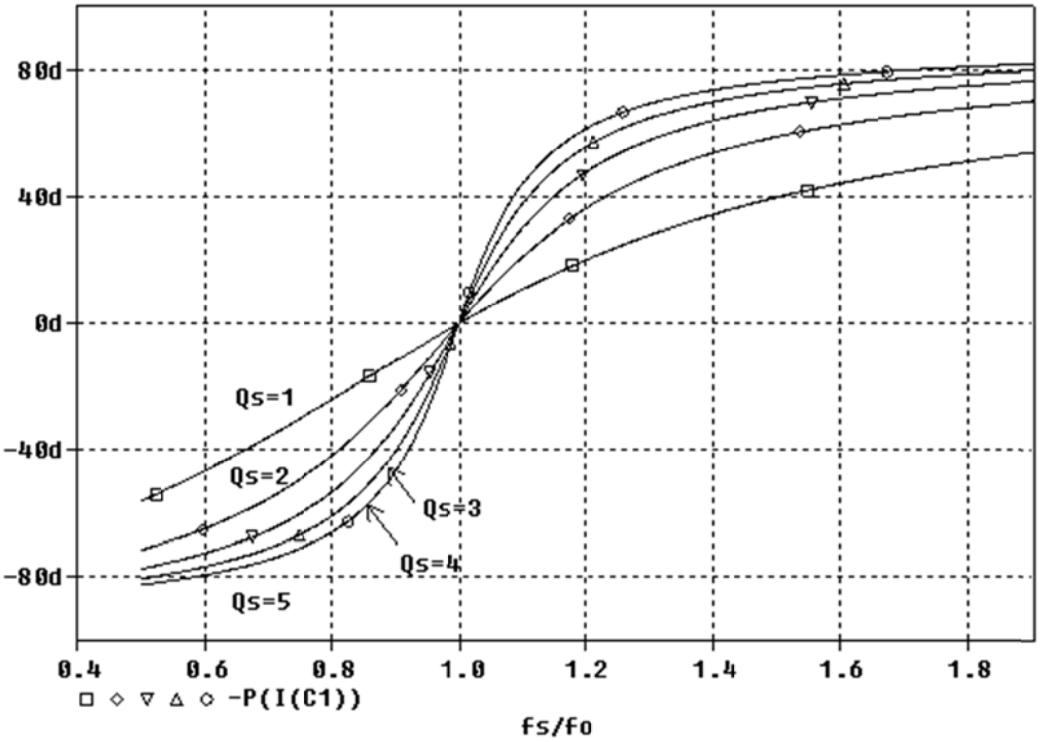
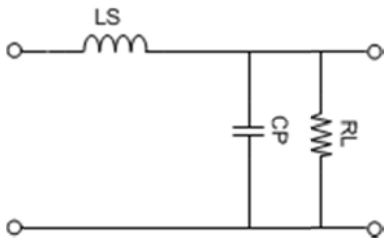


Figure B3 : SRC - Phase angle of tank input impedance vs tuning factor

Parallel Resonant Tank	
Figure	**Description**
Figure B4	PRC - Voltage gain (V_{out}/V_{in}) vs tuning factor (f_s / f_r)
Figure B5	PRC - Resonant tank current (I_r) vs tuning factor (f_s / f_r)
Figure B6	PRC - Phase angle of tank input impedance ($\angle Z_{in}$) vs tuning factor (f_s / f_r)

Circuit :



Notes :

1. Q_p is defined as $R_L/\omega_s L_s$
2. $\omega_p = 1/\sqrt{L_s C_p}$

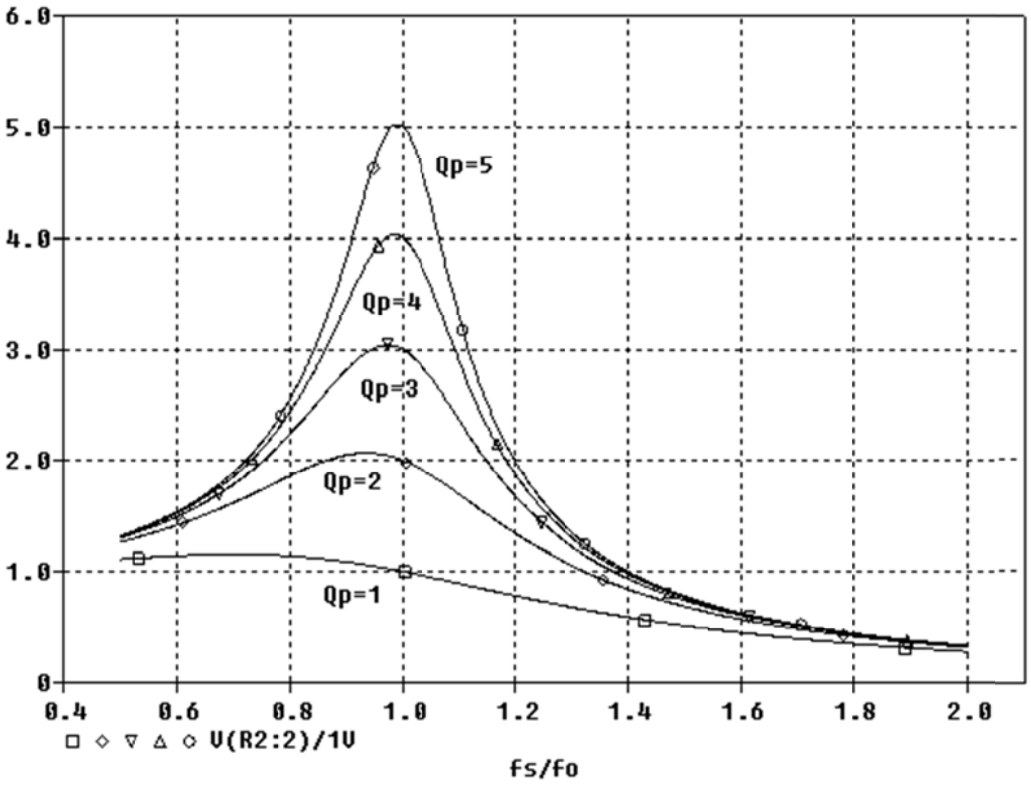


Figure B4 : PRC - Voltage gain (V_{out}/V_{in}) vs tuning factor (f_s / f_r)

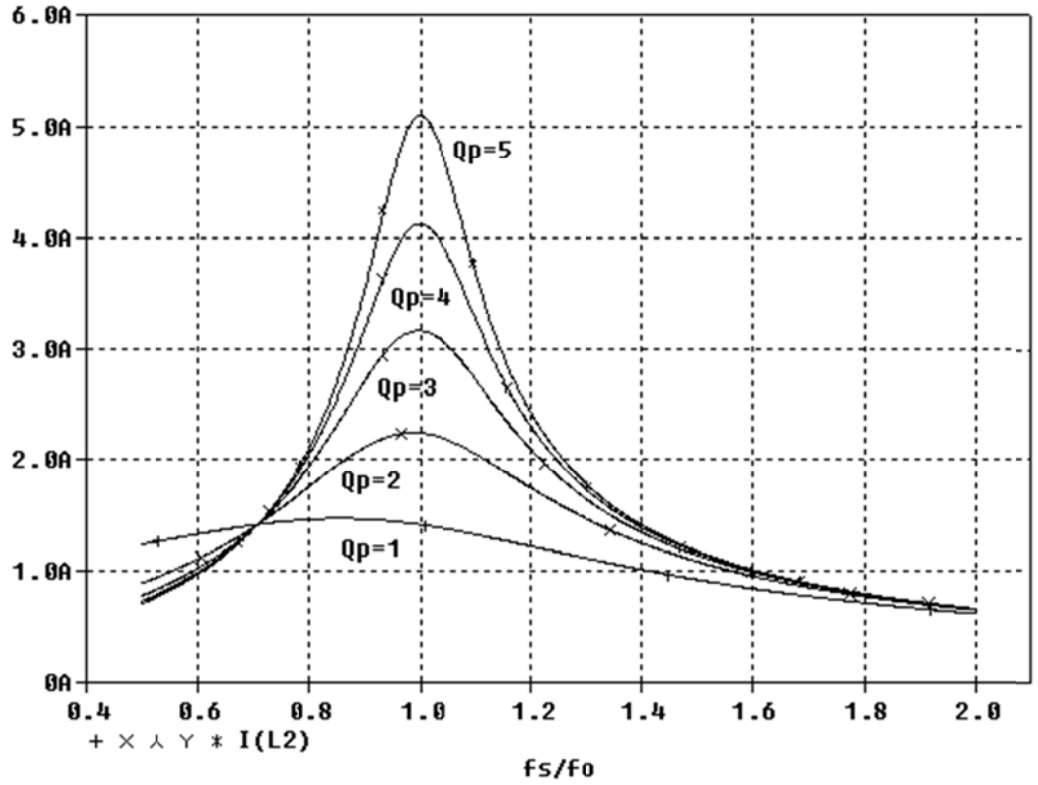


Figure B5 : PRC - Resonant tank current (I_r) vs tuning factor (f_s / f_r)

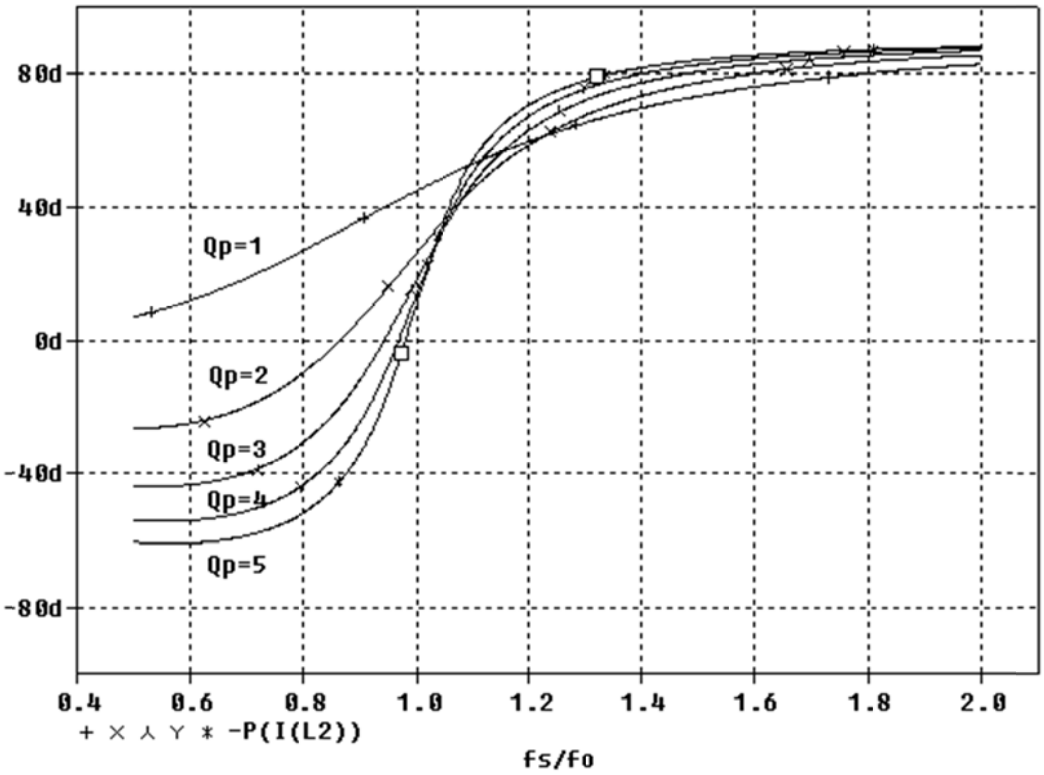
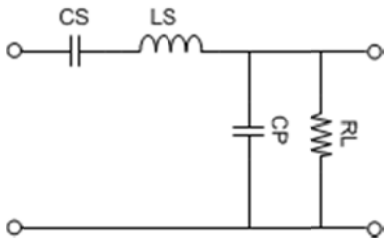


Figure B6 : PRC - Phase angle of tank input impedance ($\angle Z_{in}$) vs tuning factor (f_s / f_r)

LCC Resonant Tank	
Figure	**Description**
Figure B7	LCC - Voltage gain (V_{out}/V_{in}) vs tuning factor (f_s / f_r)
Figure B8	LCC - Resonant tank current (I_r) vs tuning factor (f_s / f_r)
Figure B9	LCC - Phase angle of tank input impedance ($\angle Z_{in}$) vs tuning factor (f_s / f_r)

Circuit :



Notes :

1. Q_s is defined as $\omega_s L_s / R_L$
2. $\omega_s = 1/\sqrt{L_s C_s}$
3. $C_s / C_p = 1$

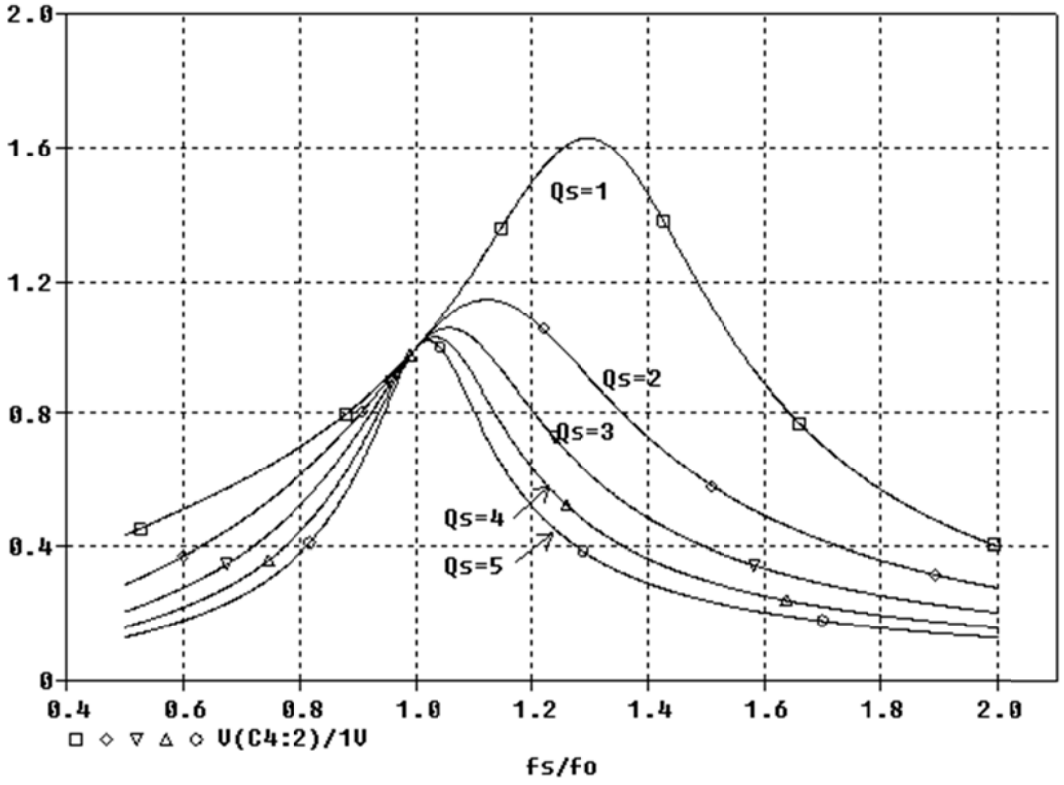


Figure B7 : LCC - Voltage gain (V_{out}/V_{in}) vs tuning factor (f_s / f_r)

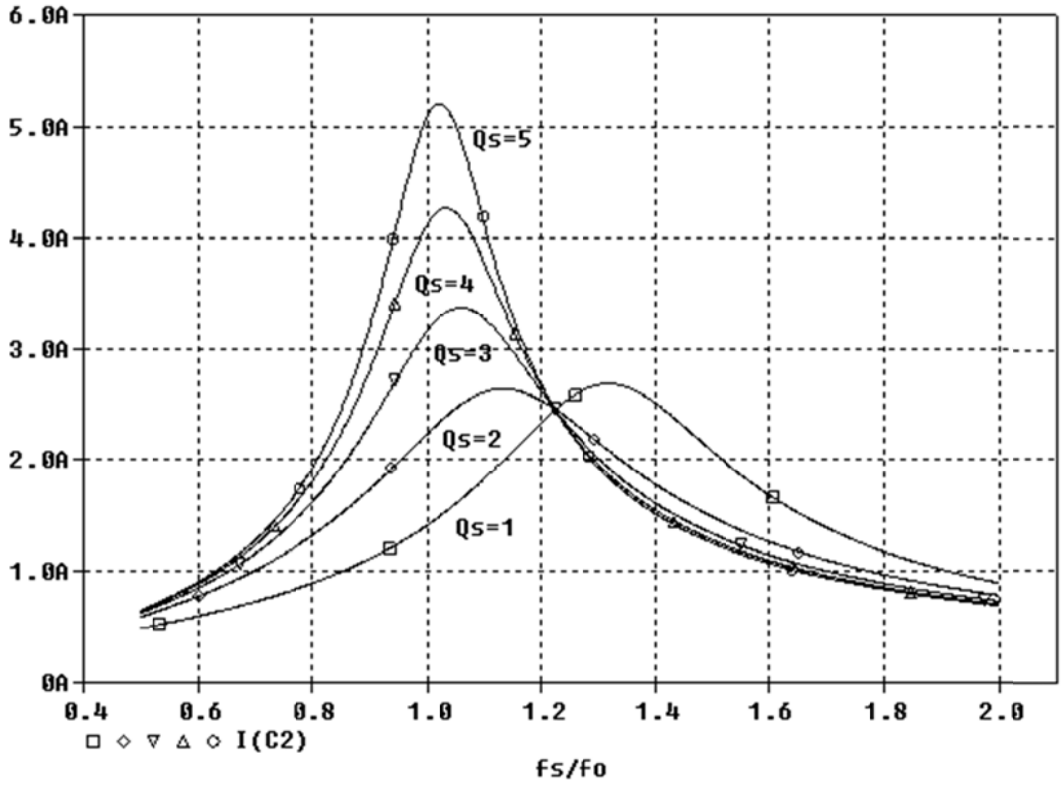


Figure B8 : LCC - Resonant tank current (I_r) vs tuning factor (f_s / f_r)

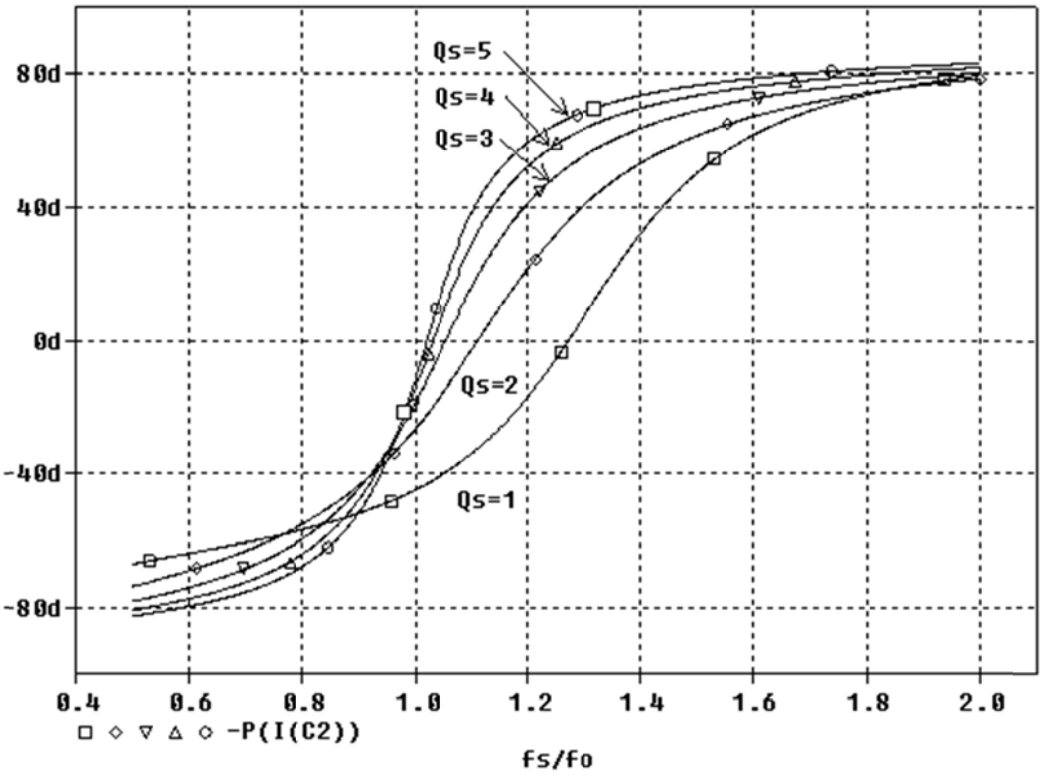
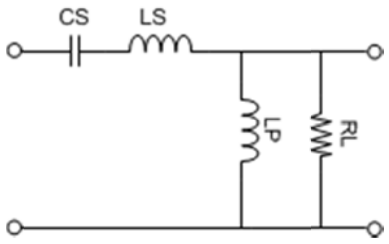


Figure B9 : LCC - Phase angle of tank input impedance ($\angle Z_{in}$) vs tuning factor (f_s / f_r)

LLC Resonant Tank	
Figure	**Description**
Figure B10	LLC - Voltage gain (V_{out}/V_{in}) vs tuning factor (f_s / f_r)
Figure B11	LLC - Resonant tank current (I_r) vs tuning factor (f_s / f_r)
Figure B12	LLC - Phase angle of tank input impedance ($\angle Z_{in}$) vs tuning factor (f_s / f_r)

Circuit :



Notes :

1. Q_s is defined as $\omega_s L_s / R_L$
2. $\omega_s = 1/\sqrt{L_s C_s}$
3. $L_s / L_p = 1$

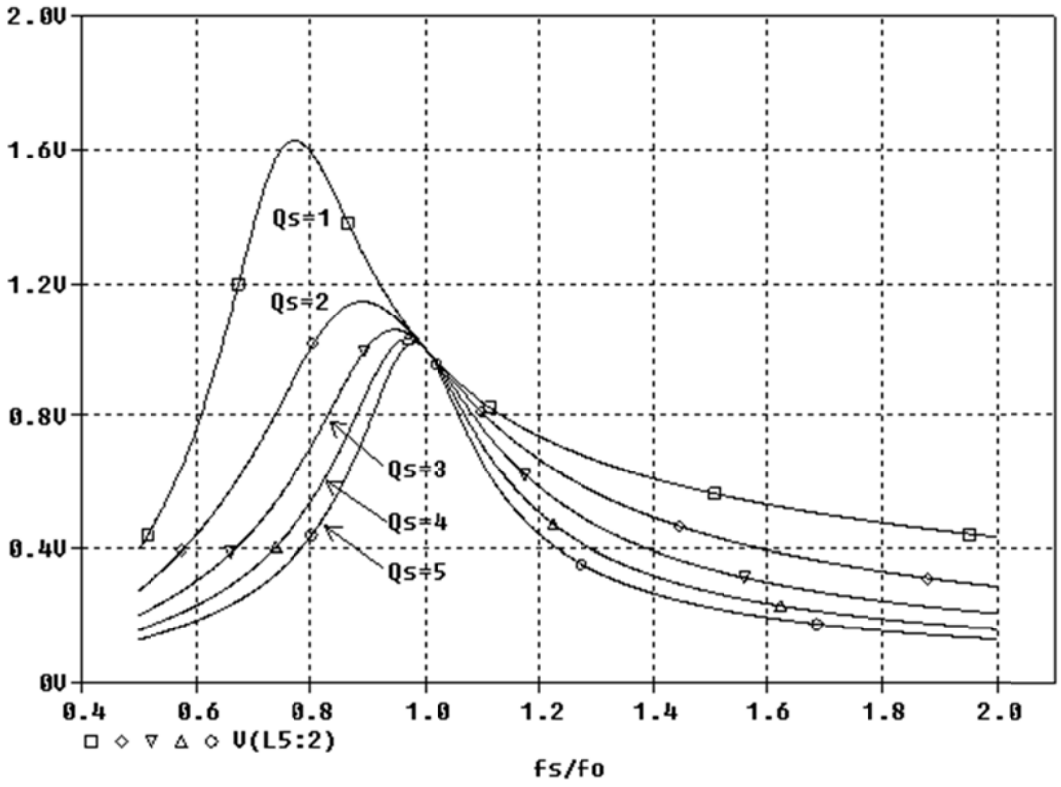


Figure B10 : LLC - Voltage gain (V_{out}/V_{in}) vs tuning factor (f_s / f_r)

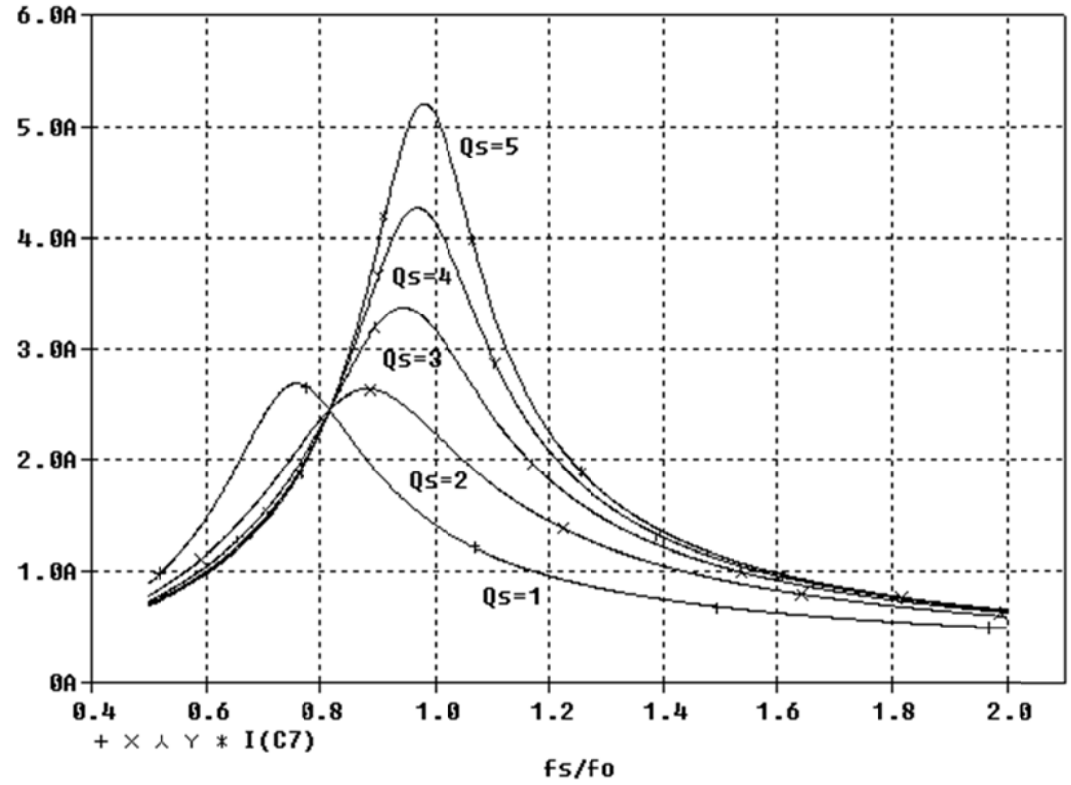


Figure B11 : LLC - Resonant tank current (I_r) vs tuning factor (f_s / f_r)

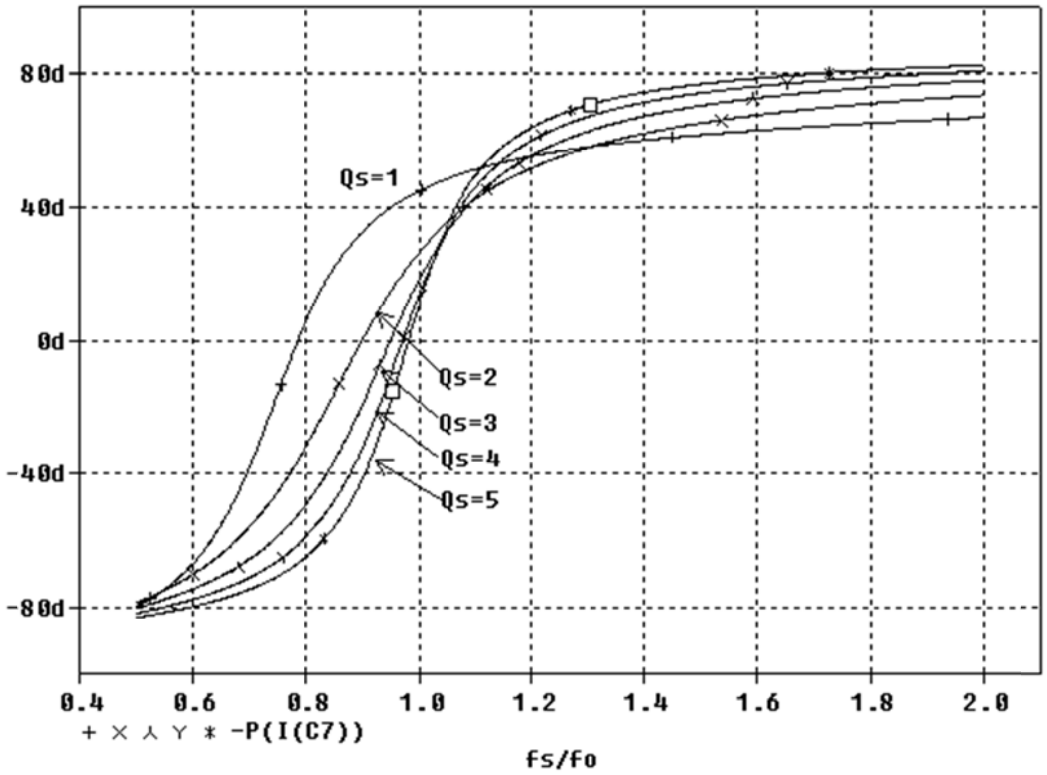
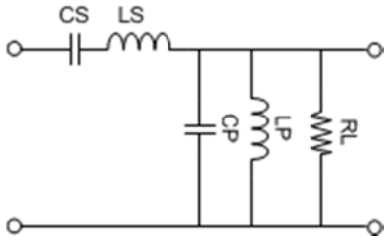


Figure B12 : LLC - Phase angle of tank input impedance ($\angle Z_{in}$) vs tuning factor (f_s / f_r)

LCLC Resonant Tank	
Figure	**Description**
Figure B13	LCLC - Voltage gain (V_{out}/V_{in}) vs tuning factor (f_s / f_r)
Figure B14	LCLC - Resonant tank current (I_r) vs tuning factor (f_s / f_r)
Figure B15	LCLC - Phase angle of tank input impedance ($\angle Z_{in}$) vs tuning factor (f_s / f_r)

Circuit :



Notes :

1. Q_s is defined as $\omega_s L_s / R_L$
2. Q_p is defined as $R_L / \omega_s L_s$
3. $\omega_s = 1/\sqrt{L_s C_s}$
4. $\omega_p = 1/\sqrt{L_p C_p}$
5. The circuit is simulated with Q_p varied from 1 to 5. The value of Q_s is made equal to $1/Q_p$

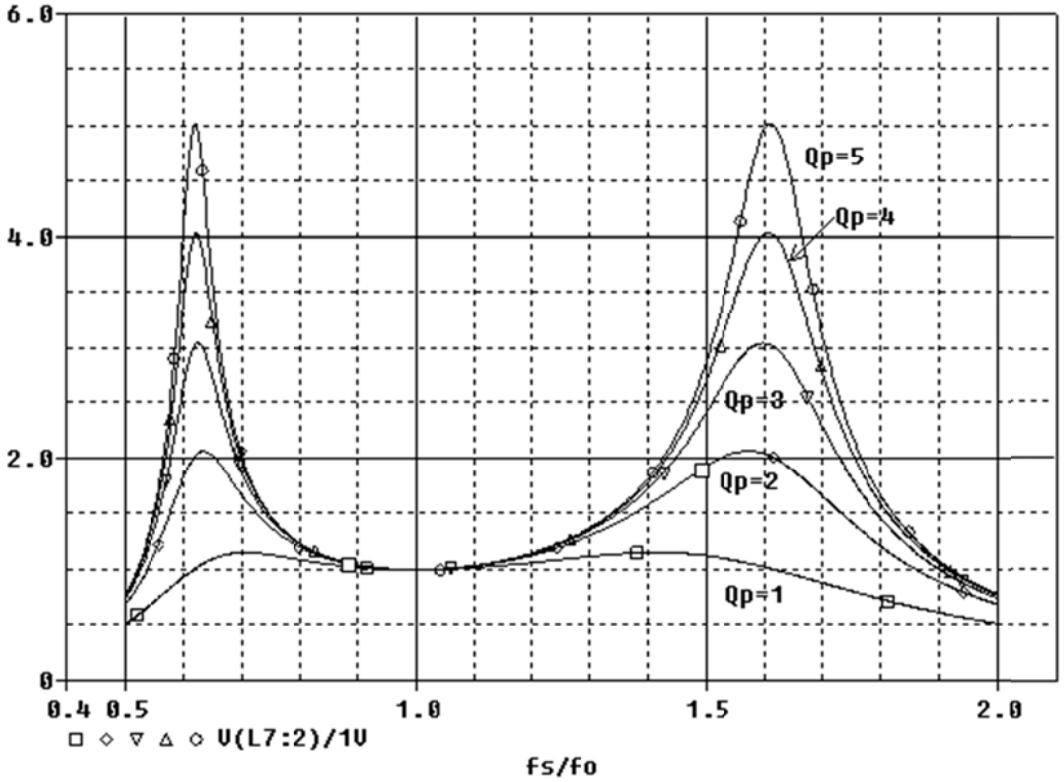


Figure B13 : LCLC - Voltage gain (V_{out}/V_{in}) vs tuning factor (f_s / f_r)

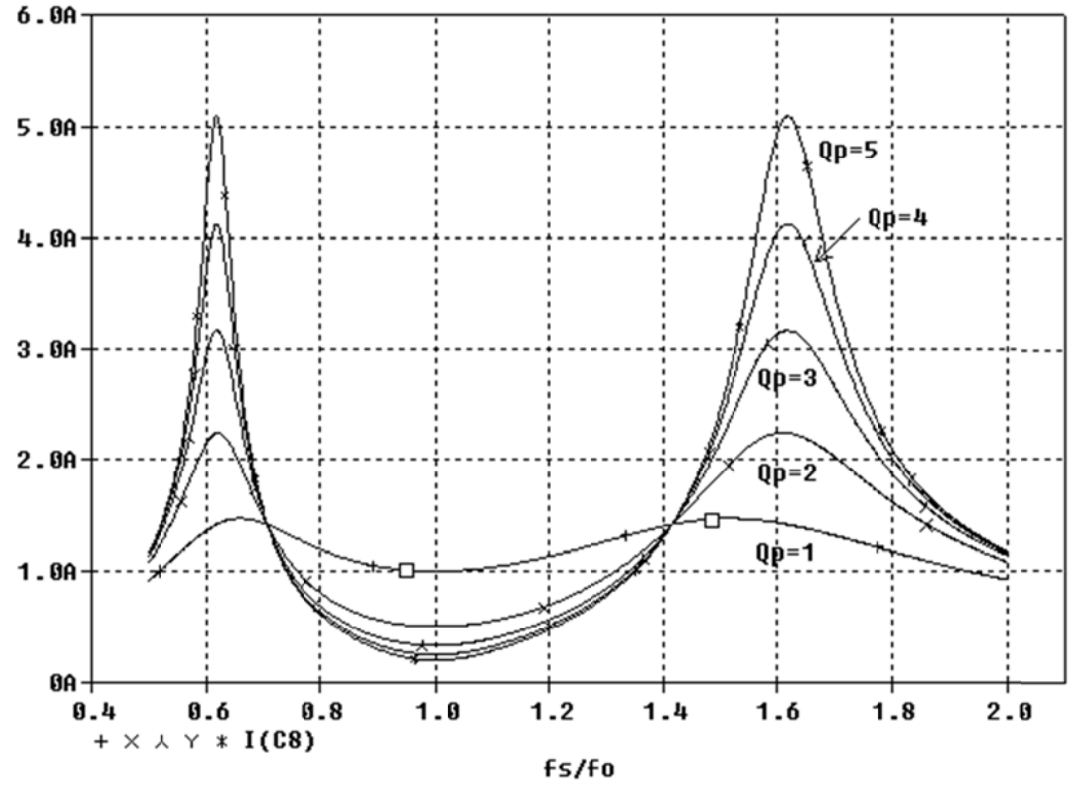


Figure B14 : LCLC - Resonant tank current (I_r) vs tuning factor (f_s / f_r)

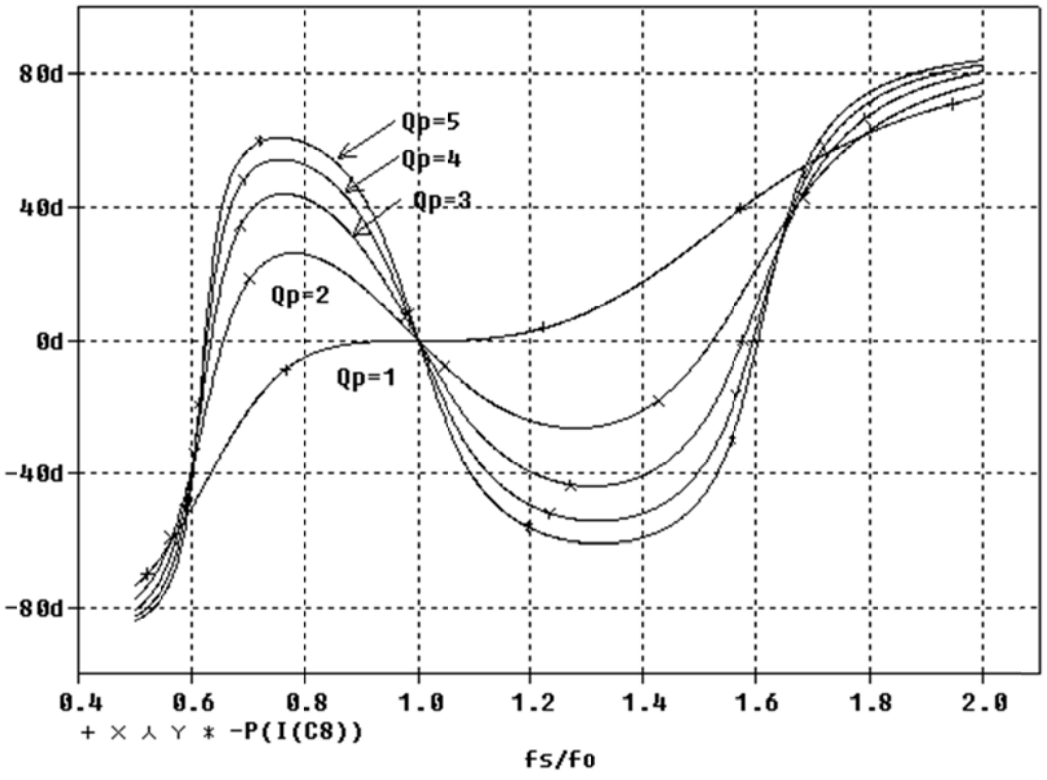


Figure B15 : LCLC - Phase angle of tank input impedance ($\angle Z_{in}$) vs tuning factor (f_s / f_r)